
2.4 GHz High-Linearity, High-Efficiency Power Amplifier

Features

- High Gain:
 - Typically 37 dB gain across 2.4–2.5 GHz over temperature -20°C to +85°C
- High linear output power:
 - >30 dBm P1dB
 - Please refer to [“Absolute Maximum Stress Ratings” on page 5](#)
 - Meets 802.11g OFDM spectrum mask requirement up to 28 dBm
 - Typically 25 dBm with <3% EVM, 802.11g, 54 Mbps
 - Typically 24 dBm with <2.5% EVM, 802.11n, MCS7-HT20, 50% duty cycle
 - Typically 24 dBm with <1.75% EVM, MCS9-HT40, 50% duty cycle
 - Meets 802.11b ACPR requirement up to 28 dBm
- High-speed power-up/down
 - Turn on/off time (10%-90%) <100 ns
- 10:1 VSWR survivability (unconditionally stable up to 28 dBm)
- On-chip power detection
 - >20 dB dynamic range
 - VSWR- and temperature-insensitive
- Simple input/output matching
- Packages available
 - 16-contact UQFN (3mm x 3mm)
 - Pin-to-pin compatible with SST12CP11
- All non-Pb (lead-free) devices are RoHS compliant

Applications

- WLAN (IEEE 802.11b/g/n)
- WLAN 256 QAM
- AP router
- WiMax (IEEE 802.16e)
- Home RF
- Cordless phones
- 2.4 GHz ISM wireless equipment

1.0 PRODUCT DESCRIPTION

SST12CP11C is a high-power and high-gain power amplifier (PA) based on the highly-reliable InGaP/GaAs HBT technology.

This PA can be easily configured for high-power applications with high power-added efficiency while operating over the 2.4-2.5 GHz frequency band. It typically provides 37 dB gain with 25% power-added efficiency @ $P_{OUT} = 28$ dBm for 802.11g.

SST12CP11C has excellent linearity, typically 25 dBm at 3% EVM with 54 Mbps 802.11g operation while meeting 802.11g spectrum mask at 28 dBm. SST12CP11C also has a single-ended power detector which lowers the users' cost for power control.

The power amplifier IC also features easy board-level usage along with high-speed power-up/-down control.

SST12CP11C is offered in 16-contact UQFN package. See [Figure 3-1](#) for pin assignments and [Table 4-1](#) for pin descriptions.

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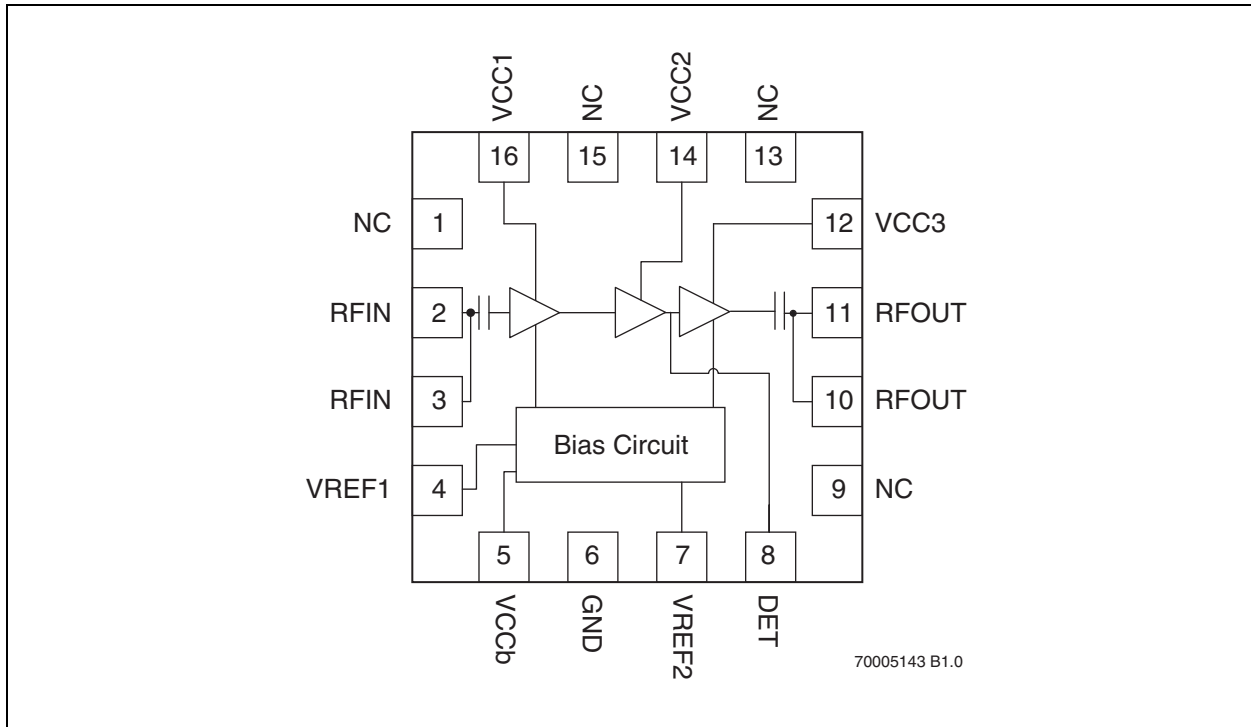
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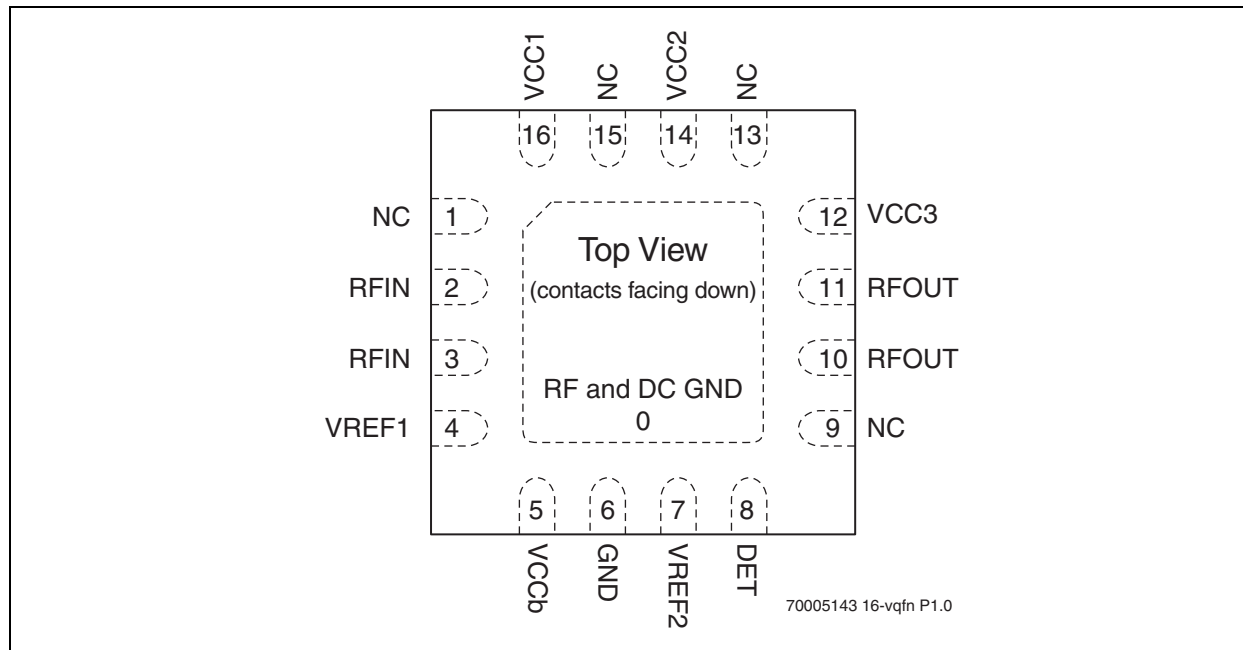
2.0 FUNCTIONAL BLOCKS

FIGURE 2-1: FUNCTIONAL BLOCK DIAGRAM



3.0 PIN ASSIGNMENTS

FIGURE 3-1: PIN ASSIGNMENTS FOR 16-CONTACT UQFN



4.0 PIN DESCRIPTIONS

TABLE 4-1: PIN DESCRIPTION

Symbol	Pin No.	Pin Name	Type ¹	Function
GND	0	Ground		The center pad should be connected to RF ground with several low inductance, low resistance vias.
NC	1	No Connection		Unconnected pins.
RFIN	2		I	RF input, DC decoupled
RFIN	3		I	RF input, DC decoupled
VREF1	4	Power Supply	PWR	1 st stage, idle-current control
VCCb	5	Power Supply	PWR	Supply voltage for bias circuit
GND	6	Ground		
VREF2	7	Power supply	PWR	2 nd and 3 rd stage, idle-current control
DET	8		O	On-chip power detector
NC	9	No Connection		Unconnected pins.
RFOUT	10		O	RF output
RFOUT	11		O	RF output
VCC3	12	Power Supply	PWR	Power supply, 3rd stage
NC	13	No Connection		Unconnected pins.
VCC2	14	Power Supply	PWR	Power supply, 2nd stage
NC	15	No Connection		Unconnected pins.
VCC1	16	Power Supply	PWR	Power supply, 1st stage

1. I=Input, O=Output

5.0 ELECTRICAL SPECIFICATIONS

The DC and RF specifications for the power amplifier are specified below. Refer to [Table 5-2](#) for the DC voltage and current specifications.

Absolute Maximum Stress Ratings (Applied conditions greater than those listed under “Absolute Maximum Stress Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions or conditions greater than those defined in the operational sections of this data sheet is not implied. Exposure to absolute maximum stress rating conditions may affect device reliability.)

Input power to pin 2 and 3 (P_{IN})	-3 dBm
Supply voltage at pins 5,12,14 and 16 (V_{CC})	+6 V
Reference voltage to pin 4 (V_{REF1}) and pin 7 (V_{REF2})	+3.2 V
DC supply current (I_{CC})	650 mA
Operating Temperature (T_A)	-40°C to +85°C
Storage Temperature (T_{STG})	-40°C to +120°C
Maximum Junction Temperature (T_J)	+150°C
Surface Mount Solder Reflow Temperature	260°C for 10 seconds

TABLE 5-1: OPERATING RANGE

Range	Ambient Temp	V_{CC}
Industrial	-20°C to +85°C	3.3 to 5.0V

TABLE 5-2: DC ELECTRICAL CHARACTERISTICS AT 25°C

Symbol	Parameter	Min.	Typ	Max.	Unit
V_{CC}	Supply Voltage	3.3	5.0	5.5	V
I_{CC}	DC Current				
	for 802.11g, 28 dBm		500		mA
I_{CQ}	for 802.11b, 28 dBm		500		mA
	Idle Current for 802.11g to meet EVM<3% @24.5 dBm, $V_{CC} = 5.0V$		280		mA
I_{REG}	Idle Current, $V_{CC} = 3.3V$		205		mA
	Reference Voltage see Figure 6-8 on page 10	2.9	2.95	3.1	V
I_{REG}	Reference Current		8		mA

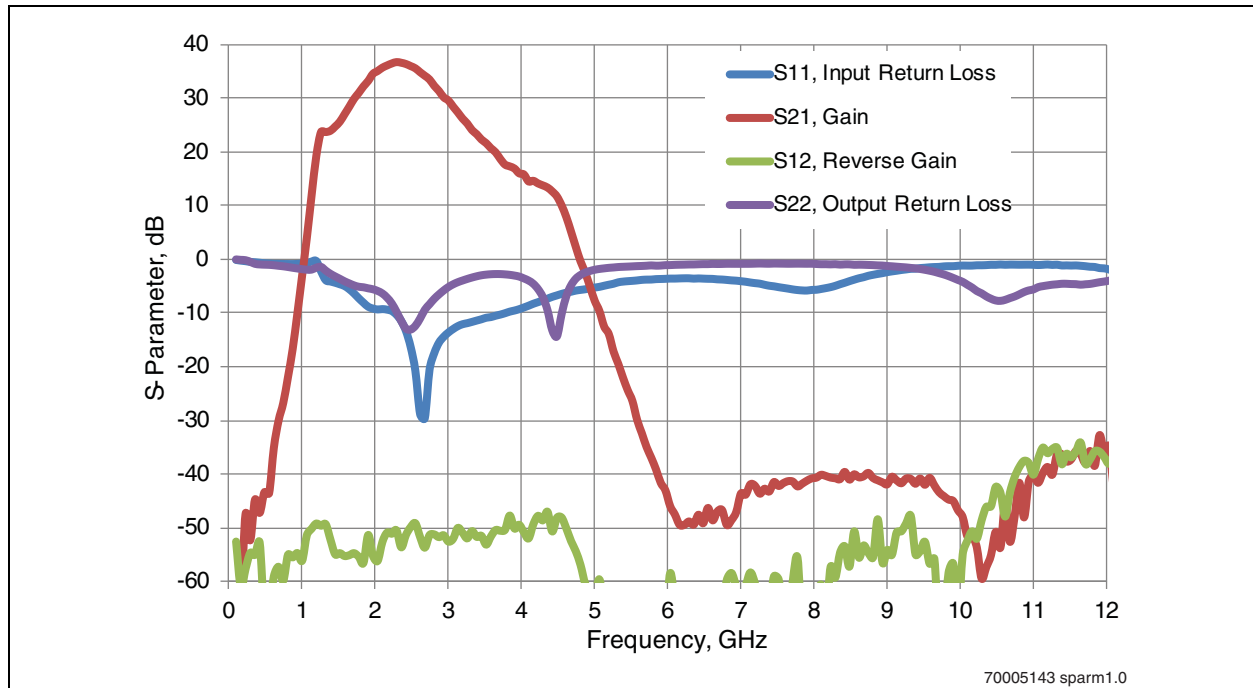
**TABLE 5-3: AC ELECTRICAL CHARACTERISTICS FOR CONFIGURATION AT $V_{CC} = 5V$,
 $V_{REF} = 2.95V$, 25°C, 50% DUTY CYCLE**

Symbol	Parameter	Min.	Typ	Max.	Unit
F_{L-U}	Frequency range in 802.11b/g applications	2400		2500	MHz
P_{OUT}	Output power at 3% EVM with 802.11g OFDM at 54 Mbps		25		dBm
	Output power at 2.5% EVM with 802.11n MCS7 HT20		24		dBm
	Output power at 1.75% EVM with 256 QAM MCS9 HT40		23.5		dBm
	Output power meeting 802.11g spectral mask		28		dBm
	Output power meeting 802.11n HT20 spectral mask		26		dBm
	Output power meeting MCS9-HT40 spectral mask		26		dBm
	Output power meeting 802.11b spectral mask		28		dBm
	Output power at 3% EVM with 802.11g, $V_{CC} = 3.3V$		20.5		dBm
G	Power gain for 802.11b/g/n/256 QAM	35	37		dB
	Power gain for 802.11b/g/n/256 QAM, $V_{CC} = 3.3V$		38		dB
G_{VAR}	Gain variation over band			±0.5	dB
2f	Second Harmonic at 28 dBm, 802.11b mask compliance		-15		dBm/MHz
	Second Harmonic at 26 dBm		-30		dBm/MHz
3f	Third Harmonic at 28 dBm, 802.11b mask compliance		-20		dBm/MHz
	Third Harmonic at 26 dBm		-50		dBm/MHz

6.0 TYPICAL PERFORMANCE CHARACTERISTICS

Test Conditions: $V_{CC} = 5.0V$, $V_{REG} = 2.95V$, $T_A = 25^\circ C$, unless otherwise specified

FIGURE 6-1: S-PARAMETERS



Test Conditions: $V_{CC} = 5.0V$, $V_{REG} = 2.95V$, $T_A = 25^\circ C$, IEEE 802.11g, 54 Mbps, 50% duty cycle unless otherwise specified

FIGURE 6-2: DYNAMIC EVM VERSUS OUTPUT POWER

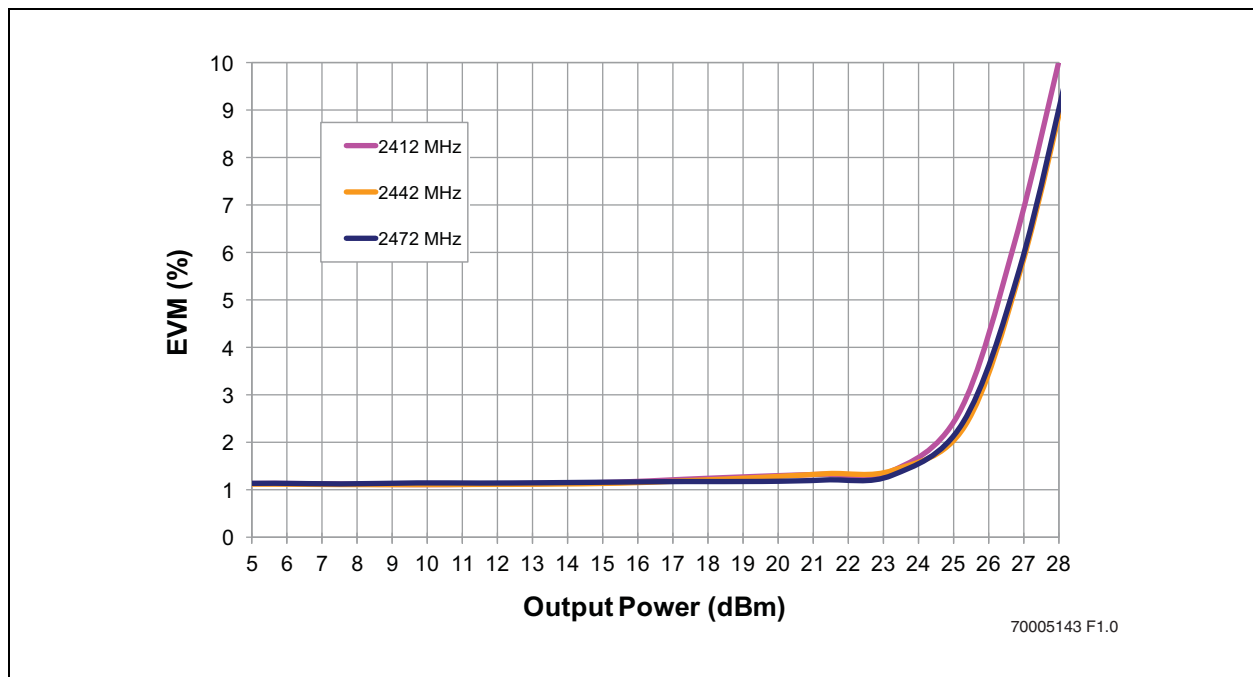


FIGURE 6-3: DYNAMIC EVM VERSUS OUTPUT POWER, WITH MSCS7-20 MHz

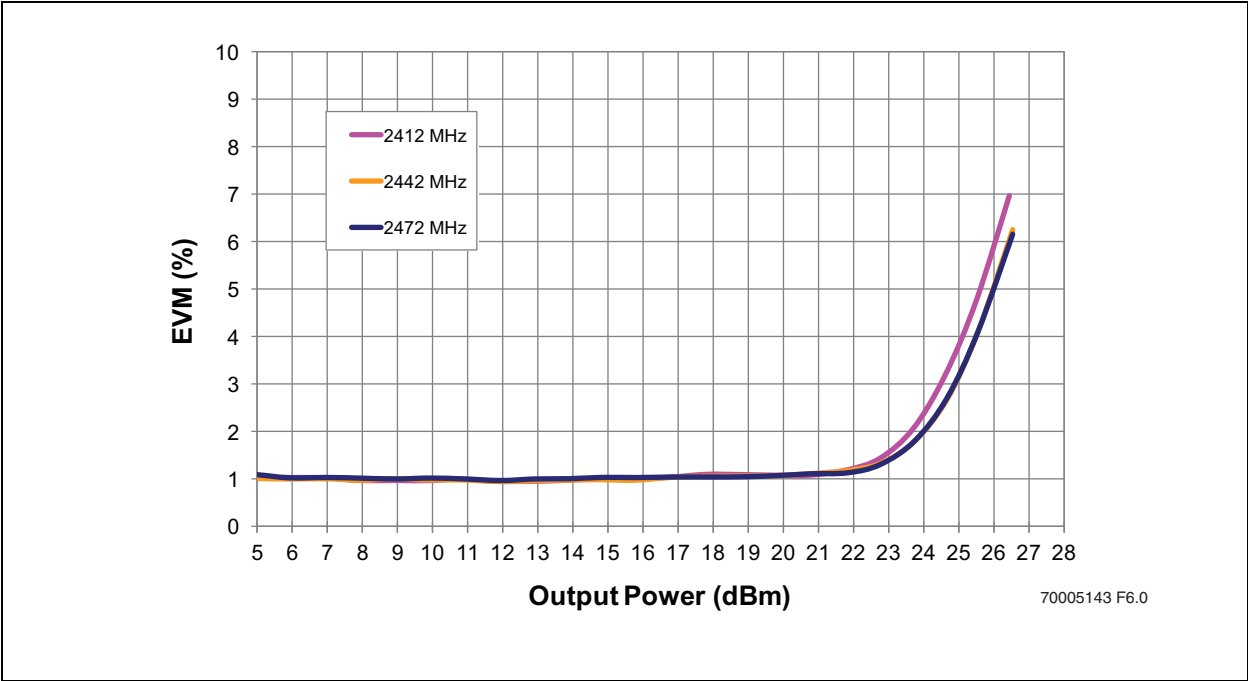


FIGURE 6-4: DYNAMIC EVM VERSUS OUTPUT POWER, WITH MSCS9-40 MHz, 50% DUTY CYCLE

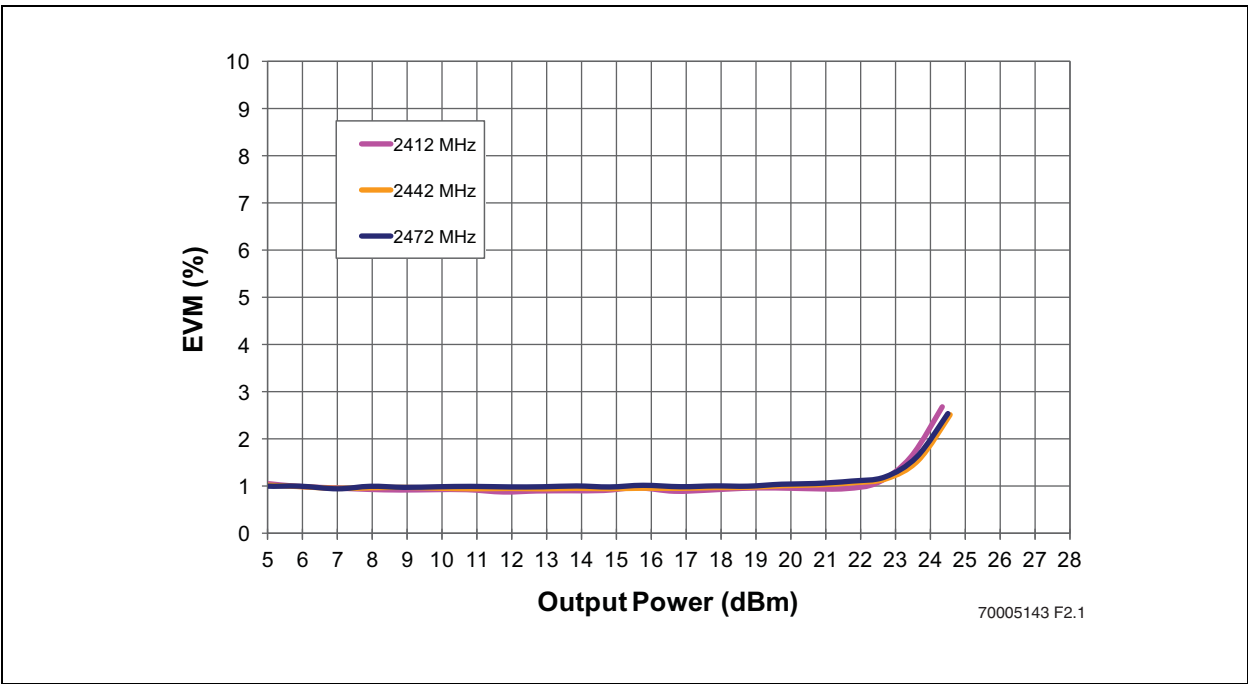


FIGURE 6-5: POWER GAIN VERSUS OUTPUT POWER

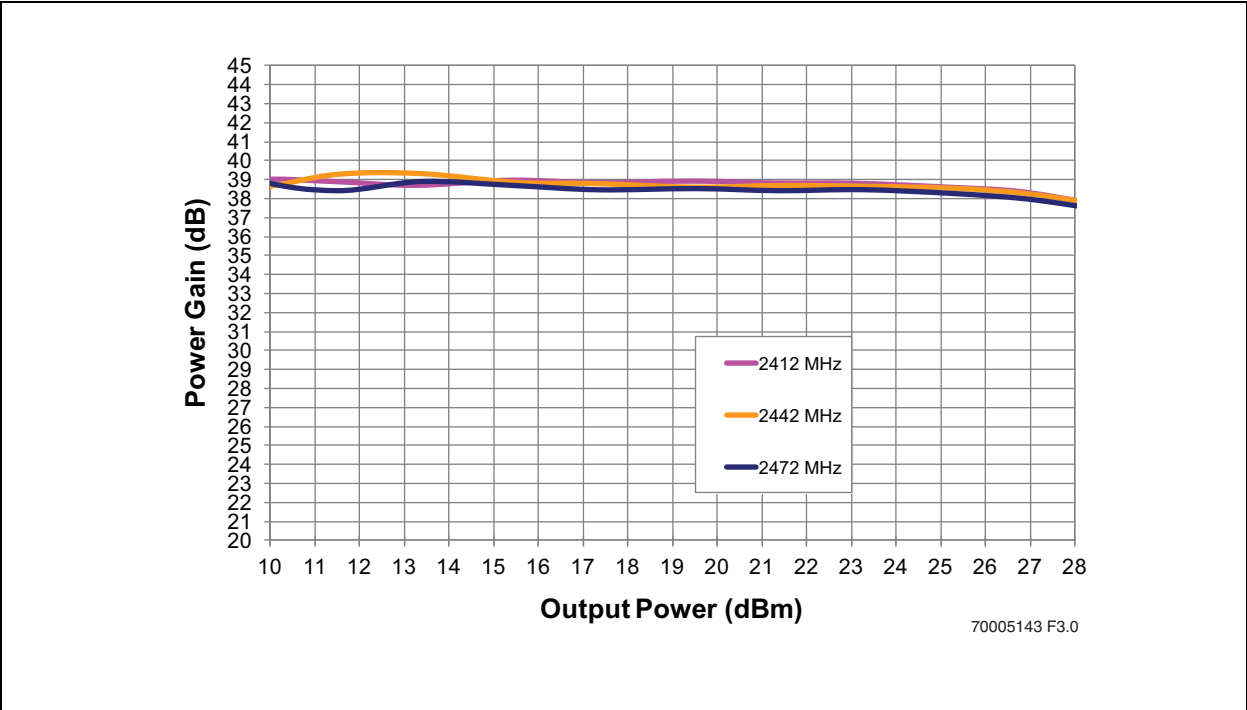


FIGURE 6-6: SUPPLY CURRENT VERSUS OUTPUT POWER

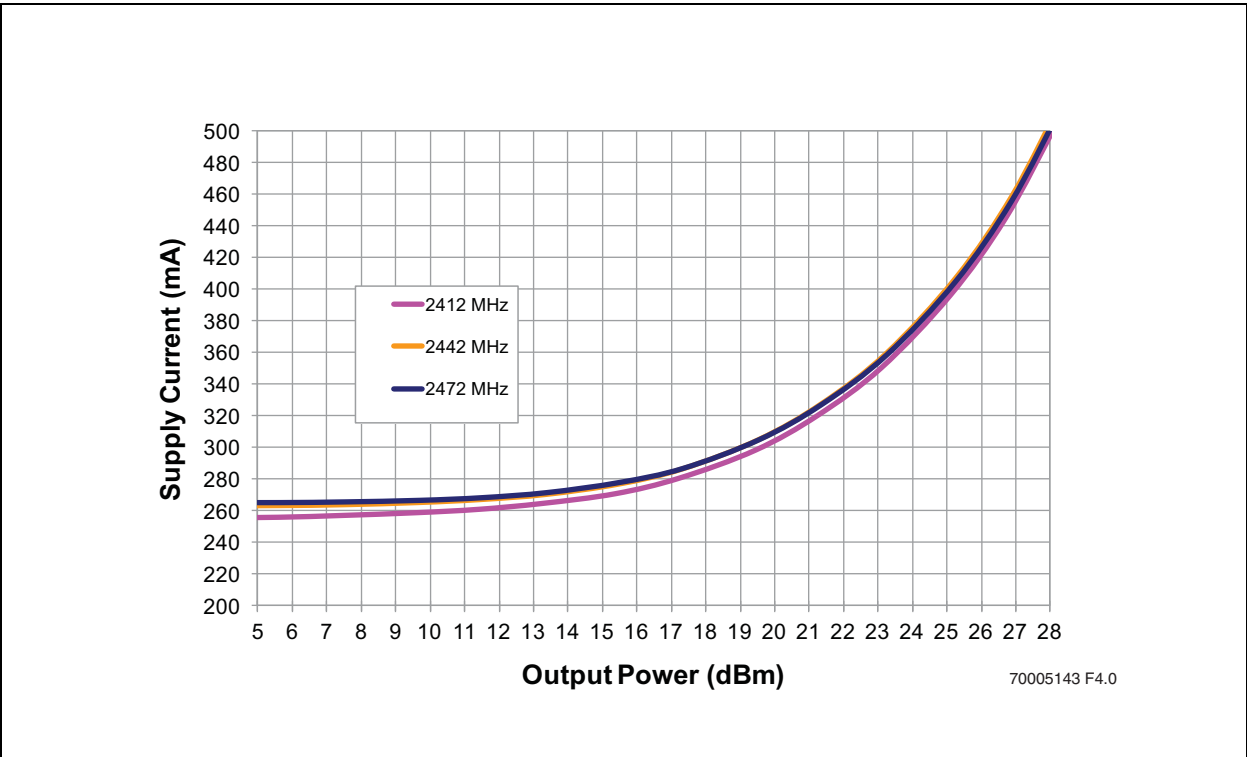


FIGURE 6-7: DETECTOR CHARACTERISTIC VERSUS OUTPUT POWER

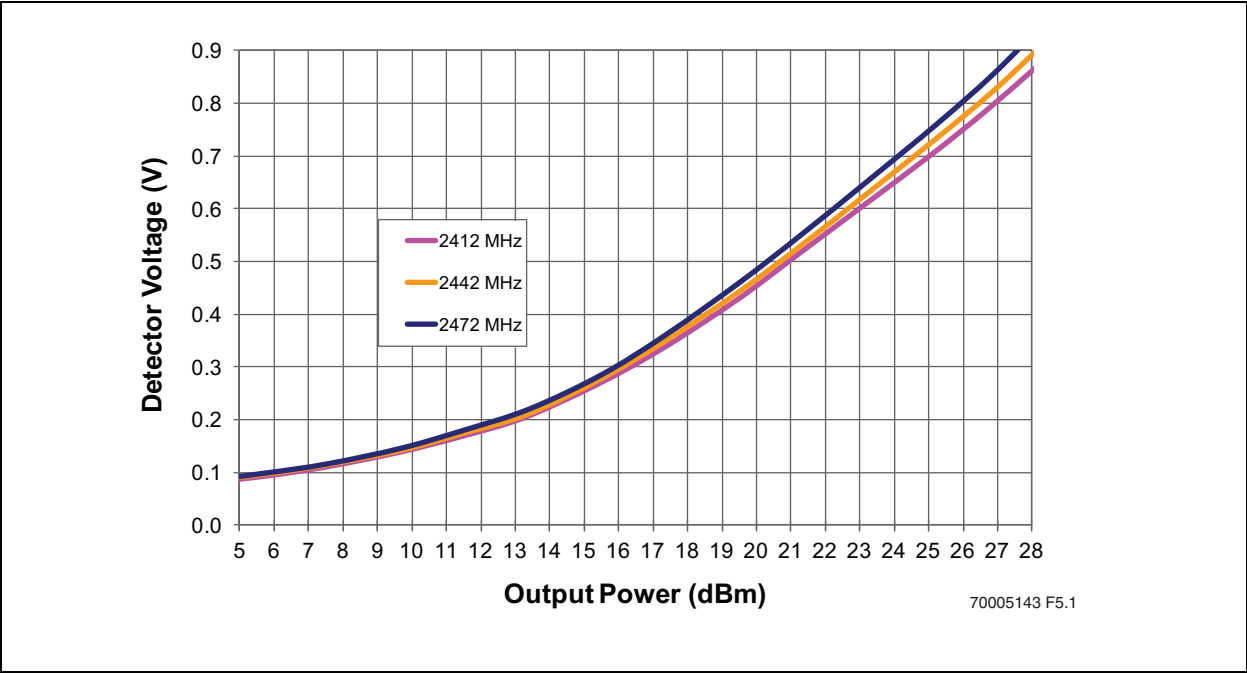
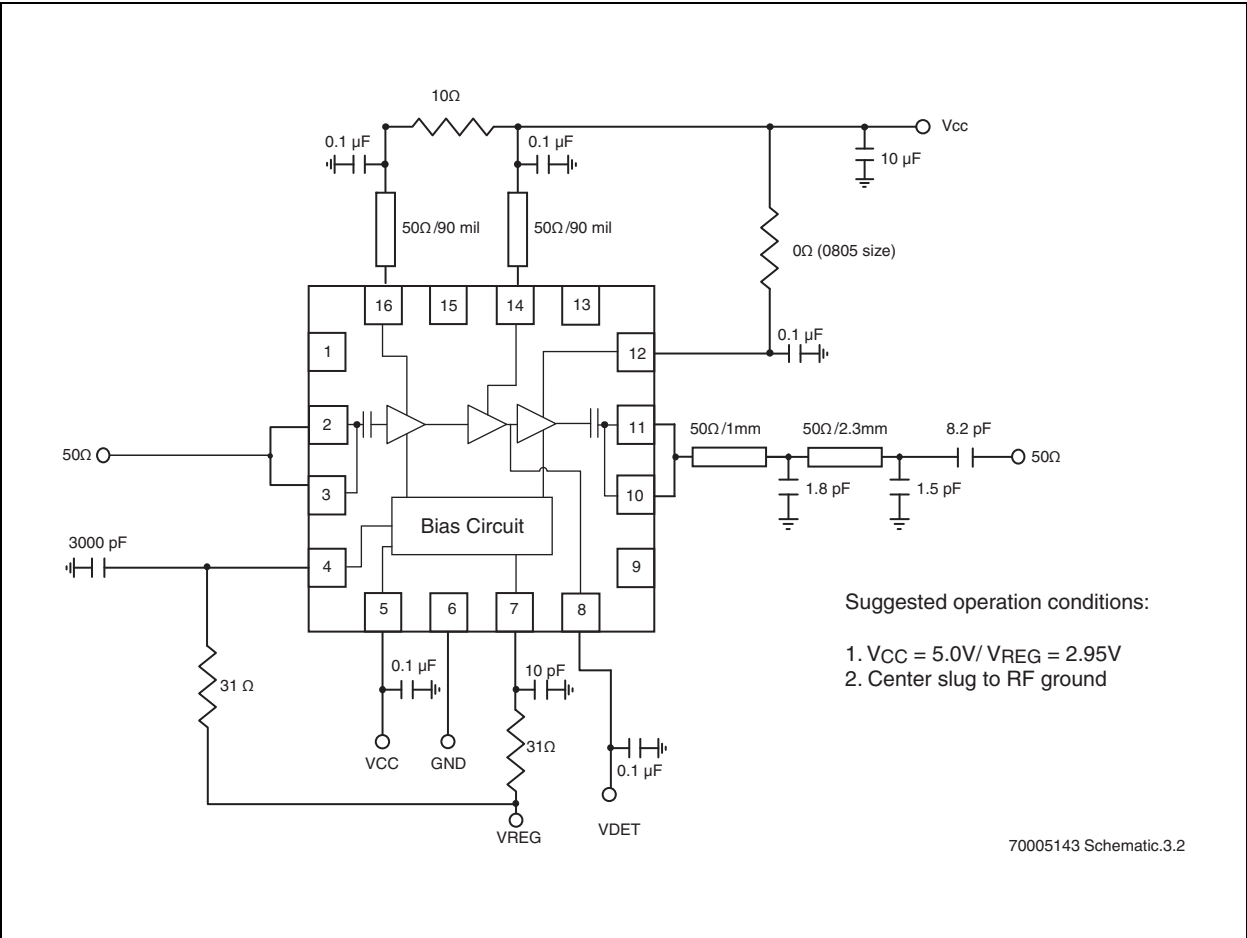


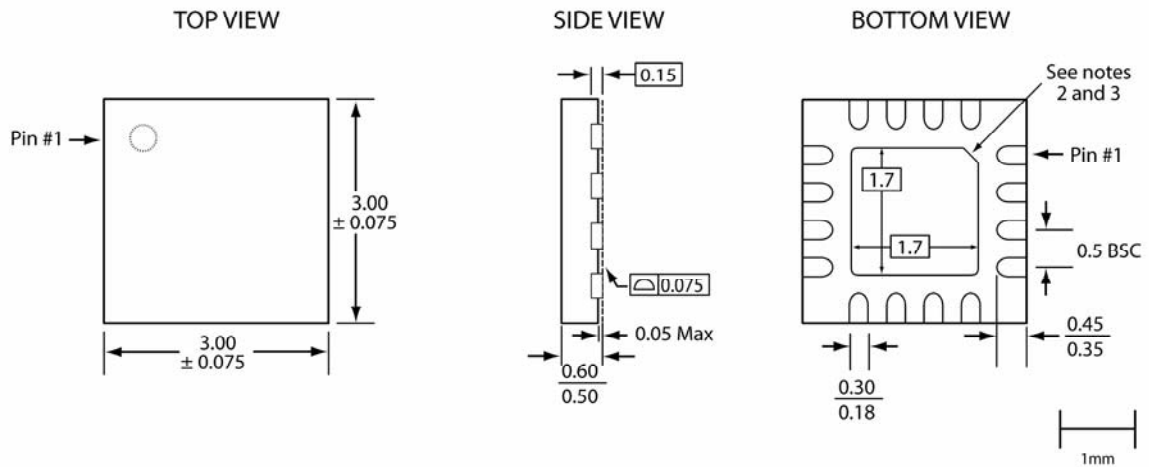
FIGURE 6-8: TYPICAL SCHEMATIC FOR 256 QAM APPLICATIONS



7.0 PACKAGING DIAGRAMS

16-Lead Ultra Thin Quad Flatpack No-Leads (QUCE/F) - 3x3 mm Body [UQFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



16-uqfn-3x3-QUC-0.0

Note:

1. Complies with JEDEC JEP95 MO-248D, variant UEED-4 except external paddle nominal dimensions.
2. From the bottom view, the pin #1 indicator may be either a 45-degree chamfer or a half-circle notch.
3. The external paddle is electrically connected to the die back-side and possibly to certain VSS leads. This paddle can be soldered to the PC board; it is suggested to connect this paddle to the VSS of the unit. Connection of this paddle to any other voltage potential can result in shorts and/or electrical malfunction of the device.
4. Untoleranced dimensions are nominal target dimensions.
5. All linear dimensions are in millimeters (max/min).

TABLE 7-1: REVISION HISTORY

Revision	Description	Date
A	<ul style="list-style-type: none">Initial release of data sheet	Apr 2014
B	<ul style="list-style-type: none">Revised Tables 5-1, 5-2, and 5-3 to reflect 3.3V information.	Feb 2015

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<div><div><div>PART NO.</div><div>Device</div></div><div><div>XXX</div><div>Package</div></div></div>	<div><div>Device: SST12CP11C = 2.4 GHz High-Gain, High-Efficiency Power Amplifier</div><div>Package: QUCE = UQFN (3mm x 3mm), 0.6 max thickness 16-contact</div><div>Evaluation Kit K = Evaluation Kit Flag</div></div>	<div><div>Valid Combinations:</div><div>SST12CP11C-QUCE</div><div>SST12CP11C-QUCE-K</div></div>
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