

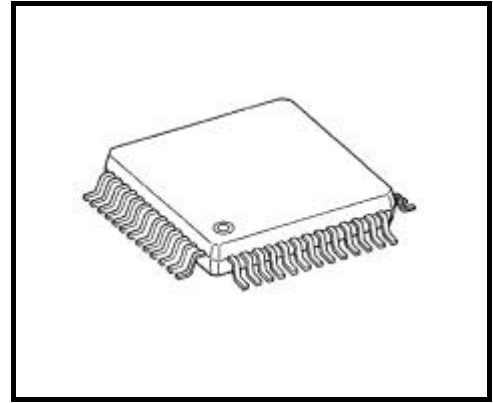
T B 3 1 2 6 2 F

RF 1chip IC for 900 MHz Cordless Telephone

One package involve three systems about RF, IF, and AF. Involving LNA, MIX, PA, VCO (TX,RX), PLL, IF-AMP, Detector, Comander, and 4 useful audio amplifiers. It is possible to reduce many external parts. This IC is suitable for ISM 900 MHz cordless telephone.

Features

- Same system & software almost compatible as TB31261AF (Single Conversion, IF Frequency: 10.7 MHz,)
- Built-in LNA
- Built-in 1st MIX
→ Double Balanced MIX (DBM) Type.
- Built-in Differential VCO, Variable capacitor (TX, RX) and Doubler (450 MHz×2)
- Built-in PA
- A substitution from TB31261AF is easy (Same package, Software almost compatible)
- Low operating voltage: $V_{CC} = 2.0 \sim 5.0$ V
- Current operating current: $I_{CC} = 70$ mA (All On)
- PLL operating frequency :around 450 MHz
- Serial control for all status
- Built in pre-amp, receiver-amp, mic-amp, and spl-amp
- Receiver output Level adjustment.
- Variable battery alarm setting. (7 thresholds)
- Built in battery saving function for Intermittent receiving.
- Small package: QFP52pin (0.65 mm pitch)



QFP52-P-1010-0.65

* Handle with care to prevent devices from deterioration by static electricity.

The diagram illustrates a complex integrated circuit for a software-defined radio, featuring both reception and transmission capabilities. Key functional blocks include:

- Antenna Interface:** An external antenna connects through a P-Matching Network and a Duplexer (DUP) to the LNA-C stage.
- LNA Stage:** A Low Noise Amplifier (LNA-C) with feedback (C45, R48) provides initial signal gain.
- Mixer Section:** A Double Balanced Mixer is driven by a 90MHz Oscillator (OSC). It handles both received signals and transmitted signals from the TX-VCO.
- Frequency Synthesis:** Includes a Phase Compensator, Divider, Buffer, and Double Balanced Mixer for precise frequency control.
- IF Stages:** Two Intermediate Frequency (IF) amplifiers (IF-AMP1, IF-AMP2) provide additional gain and filtering for both RX and TX paths.
- Baseband Processor:** Contains various filter networks (LPF, HPF), comparators, and logic for signal processing.
- Power Amplifier (PA):** Drives the TX-VCO and provides output power for transmission.
- Control & Monitoring:** Includes pins for DATA-IN, DATA-OUT, CLK, DATA, STB, REF-IN, and PA-GAIN-CONT.

The circuit is densely packed with components, including numerous resistors (R1-R47), capacitors (C1-C47), and inductors (L1-L6), all meticulously labeled with their values and connections.

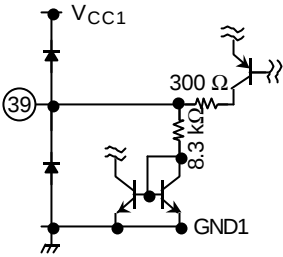
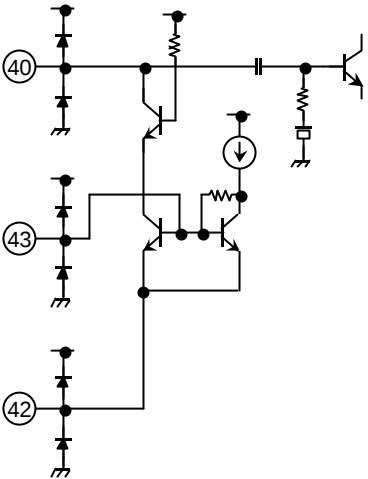
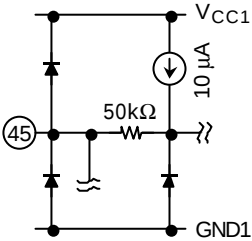
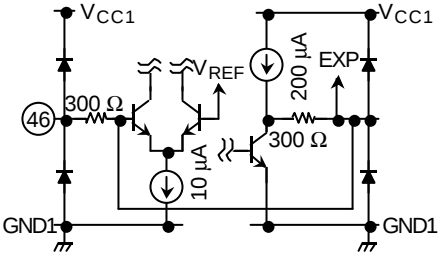
Pin Function (The values of internal components are typical)

Pin No.	Pin Name	Function	Internal Equivalent Circuit
1	PA-V _{CC}	V _{CC} terminal	
2	PA-OUT1	Differential output terminal1 of Power Amp	
3	PA-OUT2	Differential output terminal2 of Power Amp	
4	PA-GND	GND terminal	
5	SPL-OUT	Output terminal of Splatter Amp	
6	SPL-IN	Input terminal of Splatter Amp	
7	COMP-OUT	Output terminal of Compressor	
8	MIC-OUT	Output terminal of MIC Amp	
9	MIC-IN	Input terminal of MIC Amp	

Pin No.	Pin Name	Function	Internal Equivalent Circuit
10	TX-V _{CC}	V _{CC} terminal	
11	TXVCO-L1	Terminal1 for external inductor of differential TXVCO	
12	TXVCO-L2	Terminal2 for external inductor of differential TXVCO	
13	TX-GND	GND terminal	
14	TX-LOOP	Terminal1 for TX loop filter	
15	C-NF	Terminal for compressor's negative feedback capacitor	
16	PA-GAIN-CONT	PA gain control terminal for external variable resistance to GND	
17	GND2	GND terminal	—
18	REF-IN	Reference clock input terminal	

Pin No.	Pin Name	Function	Internal Equivalent Circuit
19	STB	Strobe input terminal for serial data setting	
20	DATA	Data input terminal for serial data setting	
21	CLK	Clock input terminal for serial data setting	
22	SIG-OUT	Signal output terminal	
23	RSSI	RSSI linear output terminal	
24	DATA-OUT	Output terminal of Data comparater	
25	V _{CC3}	V _{CC} terminal	—
26	MIX-OUT	Output terminal from Mixer	

Pin No.	Pin Name	Function	Internal Equivalent Circuit
27	IFAMP1IN	Input terminal for IF-AMP1	
28	V _{CC1}	V _{CC} terminal	
30	IFAMP2IN	Input terminal for IF-AMP2	
29	IF-AMP-REF	Reference terminal for IF-AMP1 and IF-AMP2	—
31	E-RECT	Expander's external rectifier capacitor terminal	—
32	IFAMP1OUT	Output terminal from Expander	
33	VREF	Reference voltage output terminal with external Bi-pass capacitor	—
34	RX-GND	GND terminal	
35	RX-VCOL1	Terminal1 for external inductor of differential RXVCO	
36	RX-VCOL2	Terminal2 for external inductor of differential RXVCO	
37	RX-V _{CC}	V _{CC} terminal	
38	RX-LOOP	Terminal1 for RX loop filter	

Pin No.	Pin Name	Function	Internal Equivalent Circuit
39	C-RECT	Terminal for Compressor's rectifire capacitor	
40	LNA-C	Corrector terminal of LNA	
42	LNA-E	Emitter terminal of LNA	
43	LNA-B	Base terminal of LNA	
41	GND1	GND terminal	—
44	VCC2	VCC terminal	—
45	DATA-IN	Input terminal of data comparator	
46	PRE-IN	Input terminal of Pre Amp	

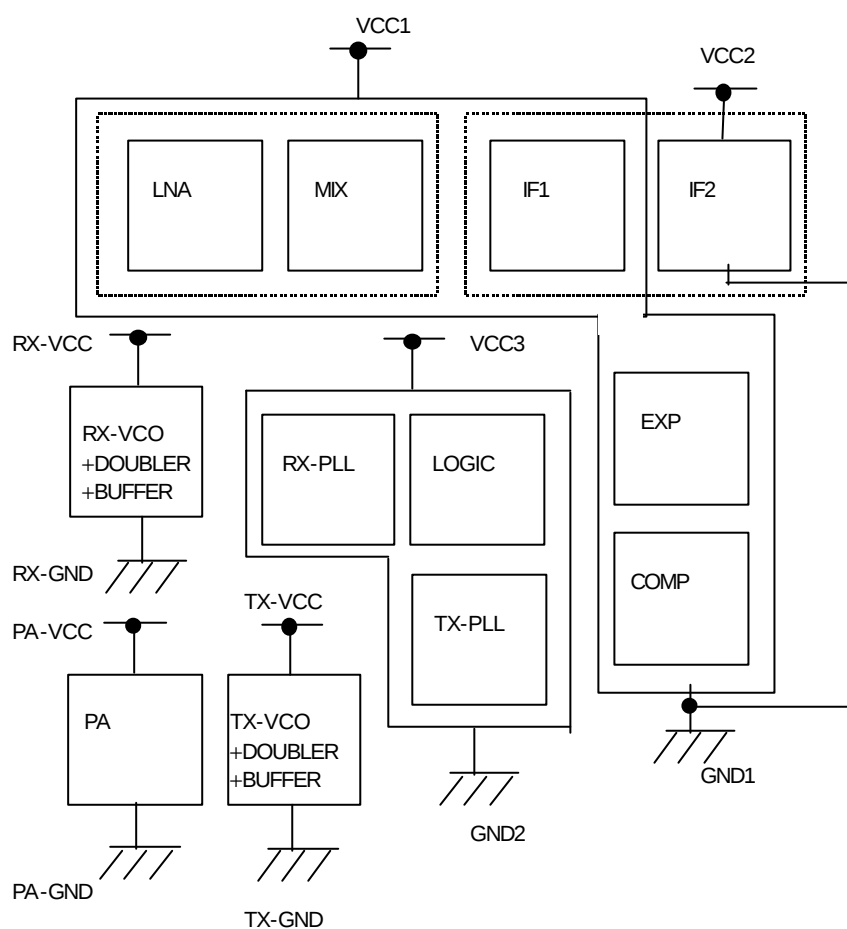
Pin No.	Pin Name	Function	Internal Equivalent Circuit
47	AF-OUT	Audio frequency output terminal of Quadrature detection	
48	QUAD	Terminal for external Quad-Coil for detection	
49	EXP-OUT	Output terminal of Expander	
50	REC-IN	Input terminal of Receiver Amp	
51	REC-OUT1	Differential output terminal1 of Receiver Amp	
52	REC-OUT2	Differential output terminal2 of Receiver Amp	

1. General Description

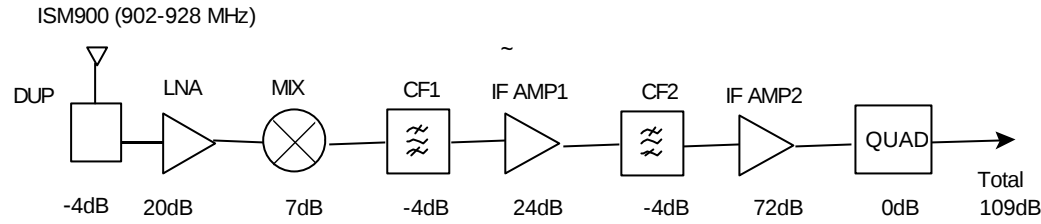
TB31262F is controlled all status by serial data. This IC is included IF detector, PLL, and compander. IF detector function is for wide-band system, dual PLL function, and compander with MIC amp and receiver amp.

+ • POWER SUPPLY BLOCK ASSIGN

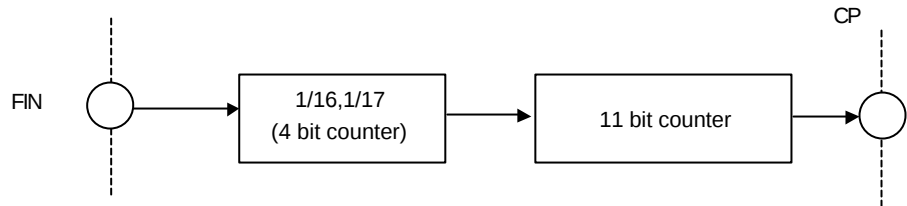
V _{CC1}	GND1	LNA, MIX, IF-AMP1, DATA-COMP, MIC-AMP, COMPRESSOR, RECEIVER-AMP
V _{CC2}		IF-AMP2, QUAD
V _{CC3}	GND2	RX-PLL, TX-PLL, REF-INPUT, DATA LATCH CONTROL
RX-V _{CC}	RX-GND	RX-VCO + DOUBLER+BUFFER
TX-V _{CC}	TX-GND	TX-VCO + DOUBLER+BUFFER
PA-V _{CC}	PA-GND	POWER-AMP



Gv distribution for receiving



2. PLL block

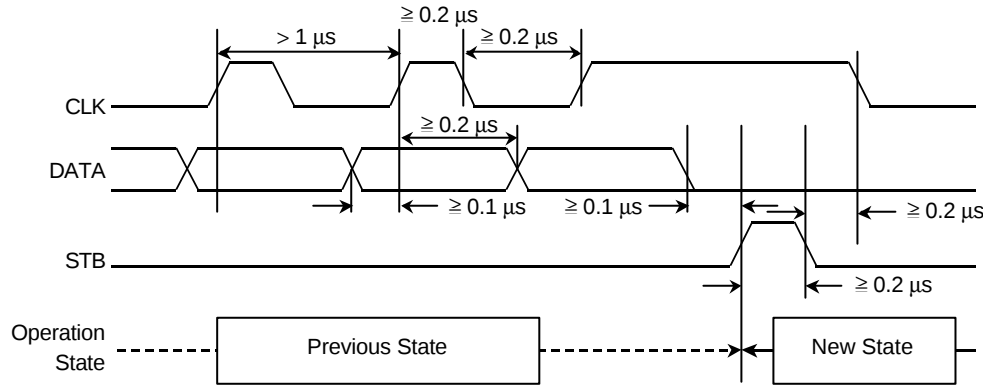


3. Data Latch Control

This block has 4 registers assigned by 2 or 3 bits CODE. DATA is read on the time of up edge of CLK. When STB receives high signal, DATA in shift register is sent into LATCH to control block which CODE indicates and the operation starts.

INPUT TIMING FOR SERIAL DATA

When both CLK “H” and DATA “L”, STB “H” leads data active.



Code			Control Block	Function
*	1	0	TX divider (18 bits)	Setting frequency for TX-PLL
*	0	1	RX divider (18 bits)	Setting frequency for RX-PLL
*	1	1	REF divider (12 bits)	Setting phase comparison frequency
0	0	0	Option control 1	Battery save, Mute control, etc
1	0	0	Option control 2	Volume control

4. Serial data format

(1) TX DIVIDER (Set VCO Doubler Output Frequency (EX 900 MHz, Not 450 MHz))

Swallow counter (4 bit)				Programmable counter (11 bit)											Code		
A0	A1	A2	A3	M0	M1	M2	M3	M4	M5	M6	M7	M8	M9	M10	*	1	0

← 1st

*don't care

$$N = 2 \times (16M + A) \quad (480 - 65534)$$

$$A = A0 + 2A1 + 4A2 + 8A3$$

$$M = M0 + 2M1 + 4M2 + 8M3 + 16M4 + 32M5 + 64M6 + 128M7 + 256M8 + 512M9 + 1024M10$$

↑
STB

(2) RX DIVIDER (Set VCO Doubler Output Frequency (EX 900 MHz, Not 450 MHz))

Swallow counter (4 bit)				Programmable counter (11 bit)											Code		
A0	A1	A2	A3	M0	M1	M2	M3	M4	M5	M6	M7	M8	M9	M10	*	0	1

← 1st

*don't care

$$N = 2 \times (16M + A) \quad (480 - 65534)$$

$$A = A0 + 2A1 + 4A2 + 8A3$$

$$M = M0 + 2M1 + 4M2 + 8M3 + 16M4 + 32M5 + 64M6 + 128M7 + 256M8 + 512M9 + 1024M10$$

↑
STB

(3) REF DIVIDER

Programmable counter (10bit)										Code	
R0	R1	R2	R3	R4	R5	R6	R7	R8	R9	1	1

← 1st

$$N = R(4 - 1023)$$

$$R = R0 + 2R1 + 4R2 + 8R3 + 16R4 + 32R5 + 64R6 + 128R7 + 256R8 + 512R9$$

↑
STB

(4) Option control 1

SIG OUT				TX control				RX control				BAT-ALM (Setting)			Code		
TXLD	RXLD	RSSI	BALM	RF	AF	CP	MUT	RF	AF	CP	MUTE	BA1	BA2	BA3	0	0	0

← 1st

↑
STB

1) Battery saving (BS) control

0	Operation
1	Battery Saving (BS)

Bit	Control Block
RX-RF	RX-PLL,RX-Buffer Tr, IF AMP,QUAD,DATA COMP,RSSI, LNA, MIX, RX – VCO + DOUBLER → I _{CC} 2
RX-AF	PRE AMP,EXPANDER,RECEIVER AMP→ I _{CC} 3
TX-RF	TX-PLL,TX-Buffer Tr , PA ,TX-VCO + DOUBLER → I _{CC} 4
TX-AF	MIC AMP, COMPRESSOR, SPLATTER-FILTER → I _{CC} 5

REF INPUT = OFF at TX-RF = 1 and RX-RF = 1

2) Charge Pump Output Current Select

CP	Current
0	400 μ A
1	800 μ A

3) MUTE control

0	Operation
1	MUTE ON

TX-MUTE control for COMPRESSOR output.

RX-MUTE control for EXPANDER output.

4) Battery Alarm Detection Setting

This IC has 5 threshold levels for detection of battery dropping.

These threshold levels are given by below table.

BA1	BA2	BA3	DET. Voltage
1	0	1	2.15 V
0	0	0	2.25 V
0	0	1	3.00 V
0	1	0	3.15 V
0	1	1	3.30 V
1	0	0	2.85 V
1	1	0	2.75 V
1	1	1	BS

5) SIG OUT selection

SIG OUT terminal generates combination states of RX and TX LOCK DETECTOR and RSSI.

0	OFF
1	OUT PUT

BIT	FUNCTION
TXLD	TX-PLL LOCK DETECTOR
RXLD	RX-PLL LOCK DETECTOR
RSSI	RSSI COMPARATOR OUTPUT
BALM	BATTERY ALARM

(5) Option control 2

RECEIVER OUTPUT LEVEL CONTROL

It is possible to volume control to set these bits.

And this register includes TEST bits which must be set 0 in customer side.

1.5dB steps from 0dB to -22.5dB.

Receiver Volume					Code		
VOL1	VOL2	VOL3	VOL4	TEST	1	0	0

VOL1	VOL2	VOL3	VOL4	GAIN
0	0	0	0	0dB
0	0	0	1	-1.5dB
0	0	1	0	-3.0dB
0	0	1	1	-4.5dB
0	1	0	0	-6.0dB
0	1	0	1	-7.5dB
0	1	1	0	-9.0dB
0	1	1	1	-10.5dB
1	0	0	0	-12.0dB
1	0	0	1	-13.5dB
1	0	1	0	-15.0dB
1	0	1	1	-16.5dB
1	1	0	0	-18.0dB
1	1	0	1	-19.5dB
1	1	1	0	-21.0dB
1	1	1	1	-22.5dB

MAXIMUM RATINGS (Ta = 25°C)

Characteristic	Symbol	Rating	Unit
Power Supply Voltage	VCC	6	V
Power Dissipation	PD	*1) 900	mW
Operating Temperature	T opr	-20~70	°C
Storage Temperature	T stg	-50~150	°C

*1) IC single unit

TENTATIVE ELECTRICAL CHARACTERISTICS

(1) System Characteristics

– TOTAL

(VCC = 3.6 V, Ta = 25°C, Δf = ±25 kHz, fmod = 1 kHz)

Characteristic	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Operating Power Supply Voltage	VCC (opr)	—	—	2.0	3.6	5.0	V
Consumption Current 1	ICC1	1	ALL ON , PA-GAIN CONT = 20 kΩ	56.0	70.0	84.0	mA
Consumption Current 2	ICC2	1	RX-RF ON	18.0	26.0	34.0	mA
Consumption Current 3	ICC3	1	RX-AF ON	2.0	2.9	3.8	mA
Consumption Current 4	ICC4	1	TX-RF ON , PA-GAIN CONT = 20 kΩ	32.0	40.0	48.0	mA
Consumption Current 5	ICC5	1	TX-AFON	1.1	1.7	2.3	mA
Alarm Supply Current	ICC (A)	1	RL = 100kΩ, 3.3Vmode	80	115	180	μA
Supply Current at BS	ICC (BS)	1	ALL OFF	—	0	5	μA
Data Input Threshold1	V IH	—	—	0.8 × VCC	VCC	4.0	V
	V IL	—	—	-0.2	0	0.2 × VCC	V
Data Input Current	I IH	1	V IH = VCC	—	0	1	μA
	I IL	1	V IL = GND	—	0	1	μA
CK Input Frequency	f CK	1	—	—	100	4000	KHz

– DETECTORS

(Unless Otherwise Specified, V_{CC} = 3.6 V, Ta = 25°C)

DETECTOR-1: BATTERY ALARM

Characteristic	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Detection Voltage0	VBAT0-L	1	—	2.07	2.15	2.23	V
	VBAT0-H		—	—	2.22	2.30	V
Detection Voltage1	VBAT1-L	1	—	2.17	2.25	2.33	V
	VBAT1-H		—	—	2.32	2.40	V
Detection Voltage2	VBAT2-L	1	—	2.67	2.75	2.83	V
	VBAT2-H		—	—	2.83	2.91	V
Detection Voltage3	VBAT3-L	1	—	2.77	2.85	2.93	V
	VBAT3-H		—	—	2.93	3.01	V
Detection Voltage4	VBAT4-L	1	—	2.92	3.00	3.08	V
	VBAT4-H		—	—	3.08	3.16	V
Detection Voltage5	VBAT5-L	1	—	3.05	3.15	3.25	V
	VBAT5-H		—	—	3.25	3.35	V
Detection Voltage6	VBAT6-L	1	—	3.20	3.30	3.40	V
	VBAT6-H		—	—	3.40	3.50	V

DETECTOR-2: DATA COMPARATOR

Characteristic	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Duty Ratio1	Duty1	2	V _{IN} (Data Comparator Input) = 40mVrms, "H"Level, F = 500 kHz	42	46	50	%
Duty Ratio2	Duty2	2	V _{IN} (Data Comparator Input) = 120mVrms, "H"Level, F = 500 kHz	43	48.5	50	%
Output Low Level Voltage	V _{OL2}	1	I _{SINK} = 0.2 mA	—	0.1	0.5	V
Output Leak Current	I _{LEAK2}	1	H LEVEL	—	0	5	μA

DETECTOR-3: SIG OUT

Characteristic	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Output Low Level Voltage	VOL3	1	I _{SINK} = 0.2 mA	—	0.1	0.5	V
Output Leak Current	I _{LEAK3}	1	H Level	—	0	5	μA

– PLL (Doubler Type Differential VCO System with Vari-Cap)

(Unless Otherwise Specified, V_{CC} = 3.6 V, Ta = 25°C)

Characteristic	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
PLL Operating Frequency	f _{IN}	—	—	—	450	—	MHz
XIN Operating Frequency	f _{XI}	1	V _{IN} = 280mVp-p	2	4	10	MHz
XIN Input Sensitivity	V _{XIH}	1	f _{IN} = 4 MHz	200	280	—	mVp-p
Charge Pump Output Current	ICP1	—	V _{CP} = 1.8 V	—	±400	—	μA
	ICP2	—	V _{CP} = 1.8 V	—	±800	—	μA
Charge Pump Leak Current	I _{LEAK}	1	—	—	0	5	μA

(2) RX CHARACTERISTICS

– RF

(V_{CC} = 3.6 V, T_a = 25°C, Δf = ±25 kHz, f_{mod} = 1 kHz)

Characteristic	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
12dB SINAD Sensitivity	12dB SINAD	—	LNA MATCHING INPUT	—	2.5	—	dBu V _{EMF}
LNA + MIX Gain	G _v	—		—	27	—	
IF AMP1 Gain	G _{IF1}	—	—	—	24	—	dB
IF AMP2 Gain	G _{IF2}	—	—	—	72	—	dB
Demodulated Output level	V _{OD}	2	V _{IN} (RF (DUP)) = 50dBμV _{EMF}	88	108	128	mVrms
Demodulated Output level2	ΔV _{OD}	2	V _{IN} (RF (DUP)) = 15dBμV _{EMF} ΔV _{OD} V _{OD} -3dB	-3.0	0	—	dB
S/N Ratio	SN	2	V _{IN} (RF (DUP)) = 50dBμV _{EMF} with 300 ~ 3kHz filter	40	47.5	—	dB
AM Rejection Ratio	AMR	—	V _{IN} (RF (DUP)) = 50dBμV _{EMF}	—	40	—	dB
IFAMP1 input Resistance	R _{IF1IN}	—	IF1-IN	—	330	—	Ω
IFAMP1 Output Resistance	R _{IF1OUT}	—	IF1-OUT	—	330	—	Ω
IFAMP2 Input Resistance	R _{IFOUT}	—	IF2-IN	—	330	—	Ω
RSSI Output Voltage	VRSSI1	2	V _{IN} (RF (DUP)) = 15dBμV _{EMF}	0.33	0.63	0.93	V
	VRSSI2		V _{IN} (RF (DUP)) = 50dBμV _{EMF}	1.17	1.47	1.77	V
RX VCO Control voltage	V _{cont RX}	2	f = 936.7MHz	0.7	1.0	1.3	V

– AF

PRE AMP + EXPANDER + RECEIVER AMP

Characteristic	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
EXP Output Reference Level	V _{refE}	2	V _{IP} = -20dBV PRE-AMP INPUT RESISTANCE: 150kΩ	-14.0	-10.0	-6.0	dBV
EXP Output Deviation	VOE	2	V _{OP} = -45dBV	-1.0	0.0	+1.0	dB
Total Harmonic Distortion	THD _R	2	R _L = 150 Ω V _{RI} = -15dBV	—	1.15	2.0	%
Output Noise Level	V _{NOR}	2	Input -GND Short	—	-90	-65	dBV
Maximum Output Level	DR	—	THD = 3%, 150 Ωload	—	2.2	—	V _{p-p}
MUTE Output Level	V _{MUTE}	—	—	—	-70	—	dBV
PRE AMP Voltage Gain Setting Range	GRNG2	—	—	0	—	20	dB
RECEIVER AMP Voltage Gain Setting Range	GRNG1	—	—	6	—	20	dB
Offset Voltage	TOF2	1	RO1• RO2	-50	0	50	mV
Crosstalk CE	CTCE	—	V _{IM} = -10dBV	—	-65	—	dB
Attack Time	T _{AE}	—	V _{IP} = -18 → -12dBV	—	8.5	—	ms
Recovery Time	T _{RE}	—	V _{IP} = -12 → -18dBV	—	4.5	—	ms

(3) TX CHARACTERISTICS
– RF

(VCC = 3.6 V, Ta = 25°C, Δf = ±25 kHz, fmod = 1 kHz)

Characteristic	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
PA OUTPUT LEVEL	PA-OUT	2	AFTER MATCHING NETWORK VR = 20 kΩ	0	+3.0	+6.0	dBm
PA GAIN CONTROL	PA-CONT	2	VR = 100 kΩ, PA-OUT Deviation	-9.0	-6.5	-4.0	dB
PA OUTPUT IMPEDANCE	PA-R-OUT	—	AFTER MATCHING NETWORK	—	50	—	Ω
PA OUTPUT CAPACITANCE	PA-C-OUT	—	AFTER MATCHING NETWORK	—	30	—	pF
TX VCO Control voltage	Vcont TX	2	f = 904MHz	0.4	0.7	1.0	V
TX VCO Deviation	Δ f TX	2	FILOUT = -30dBV, f = 904MHz	± 25	± 30	± 35	KHz
TX VCO Distortion	THD TX	2	FILOUT = -30dBV, f = 904MHz	—	1.0	3.0	%

– AF

(Unless Otherwise Specified, VCC = 3.6 V, fin = 1 kHz, Ta = 25°C)

MIC AMP + COMPRESSOR

Characteristic	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
COMP Output Reference Level	VrefC	2	VOM = -10dBV	-11.5	-10.0	-8.5	DBV
COMP Output Deviation	VOC	2	VOM = -30dBV	-0.7	0.0	+0.7	DB
MIC AMP Voltage Gain Setting range	VGR	—		0	—	30	DB
Total Harmonic Distortion	THD C	2	VOM = -10dBV	—	0.15	1.0	%
Output Noise Level	V NOC	2	Input-GND Short	—	-61	-48	dBV
Limiting Level	V lim1	—	COMP OUT, VIM = 0dBV	—	1.3	—	Vp-p
	V lim2		MIC OUT, VIM = 0dBV	—	2.5	—	Vp-p
MUTE Output Level	V MUTE	—	—	-80	-90	—	dBV
Crosstalk EC	CTEC	—	VIP = -10dBV	—	-50.0	—	dB
Attack Time	TAC	—	VIM = -46 → -34dBV	—	3.5	—	m S
Recovery Time	TRC	—	VIM = -34 → -46dBV	—	5.0	—	m S

FILTERAMP

Voltage Gain	G5	—	—	—	0	—	dB
Maximum Output Level	DR5	—	THD = 3%	—	3	—	Vp-p
Input Bias Current	I BIAS	1	—	—	1.5	2.5	μA
Output DC Voltage	Vop	1	—	0.7	1.0	1.3	V

VCC ICC1-5, (A),(BS)

1k 2.2 0.1 0.1 2.2 2.2 4.7 0.1 2.2 1 1 0.1 1

RXVCO -L2 RXVCO -L1 2.2n 2.2n 450MHz OSC RXGND VREF

C-RECT RX-LOOP 450MHz OSC RXGND VREF

LNA-C Bias Phase Compalator Divider Buffer Double (x 2) 900MHz Double Balanced MIX

GND1 LNA-E LNA-B

0.1 μ VCC2

DATA-IN Differential TX OSC

470k PRE-IN 470k 22pF PRE-AMP

Det Coil AF-OUT QUAD LPF: Fc = 15kHz IF-AMP2 (2nd)

EXP-OUT SOFT VOLUME (ATT) TX-MUTE EXP

20k 330k TOF2 REVERSE 1 REVERSE 2

PA-VCC PA-OUT1 PA-OUT2 PA-GND

20k 20k 0.022 μ V OP

SPLAMP COMP MIC-AMP MIC IN TX-MUTE TX IN TX OUT

Buffer Doubler (x 2) 900MHz 450MHz

IF-AMP1 OUT IF-AMP2 IN IF-AMP2 REF IF-AMP1 IN

E-RECT IF-AMP1 IN IF-AMP2 REF IF-AMP1 IN

DATA-COMP DATA-OUT ILEAK2 VOL2 RSSI ILEAK3 VBAT1-6 VOL3

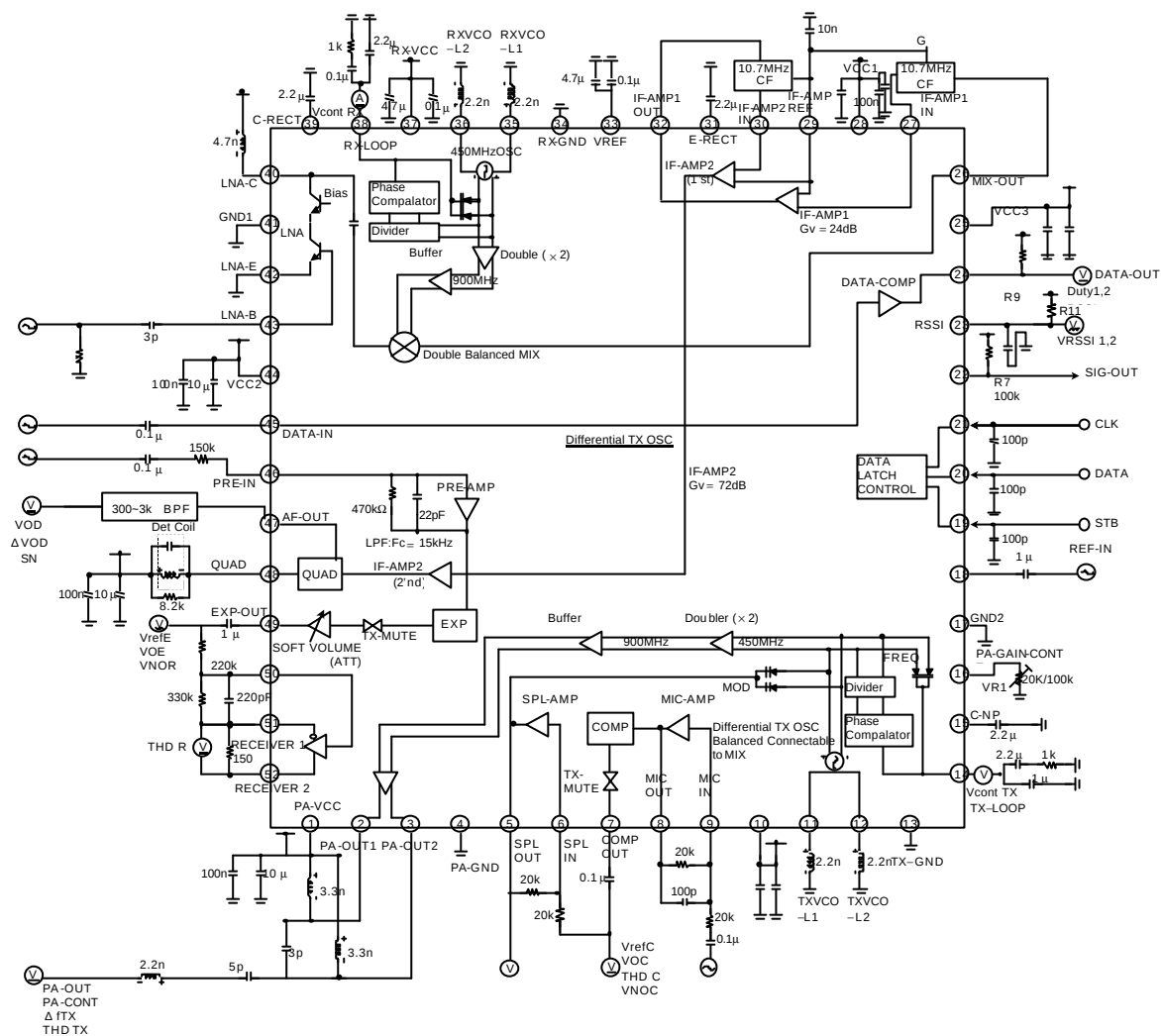
SIG-OUT

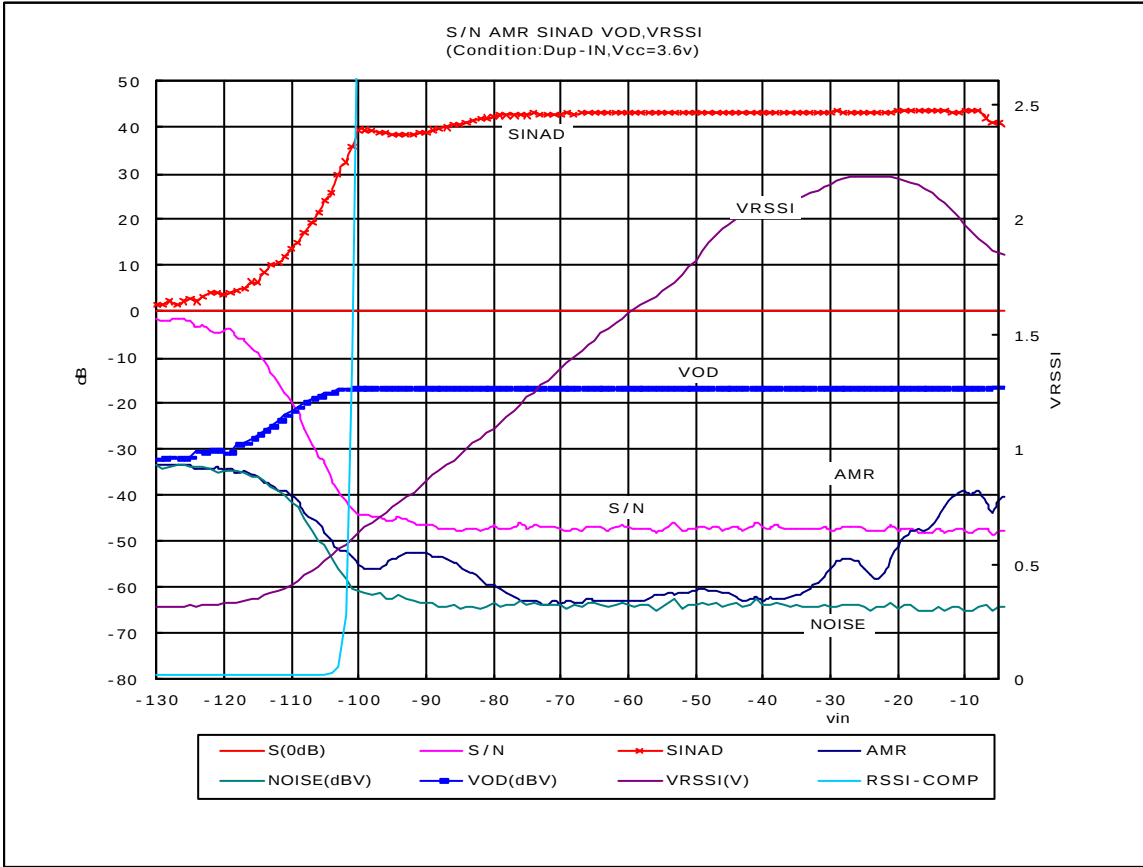
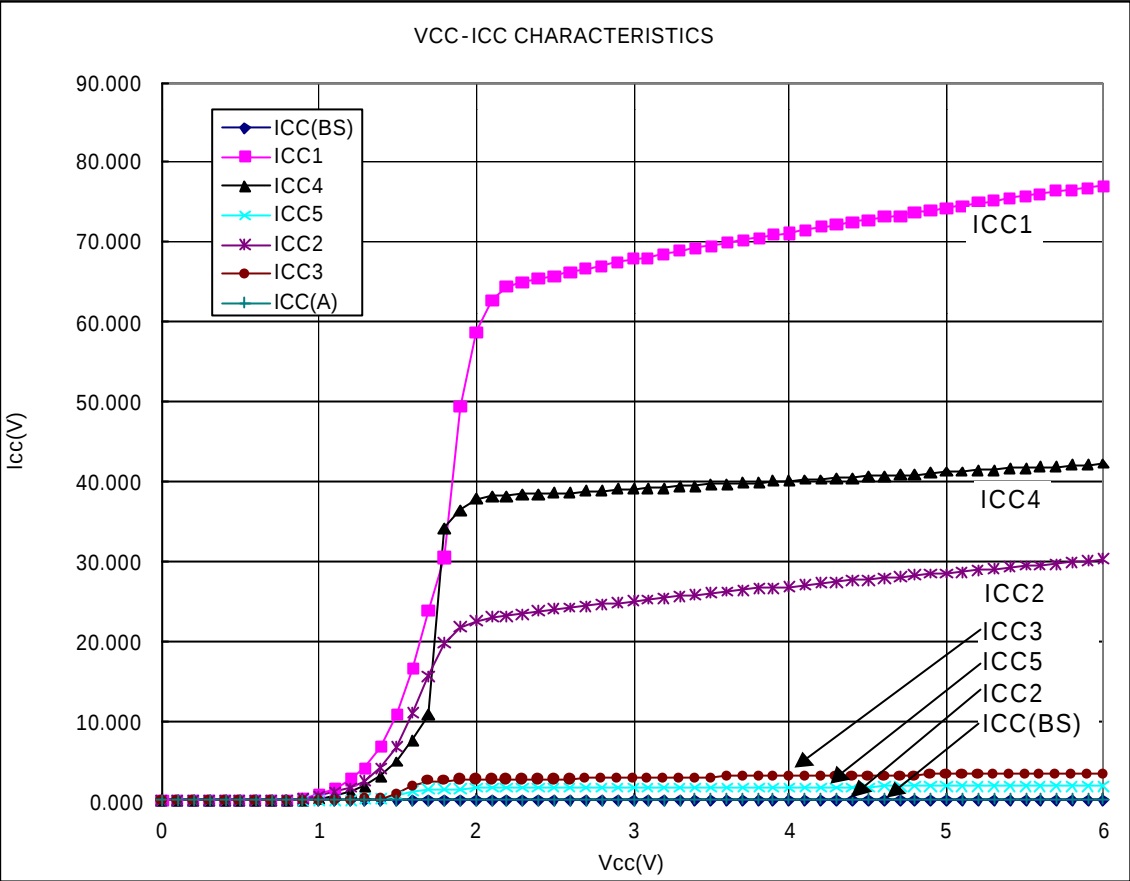
DATA LATCH CONTROL

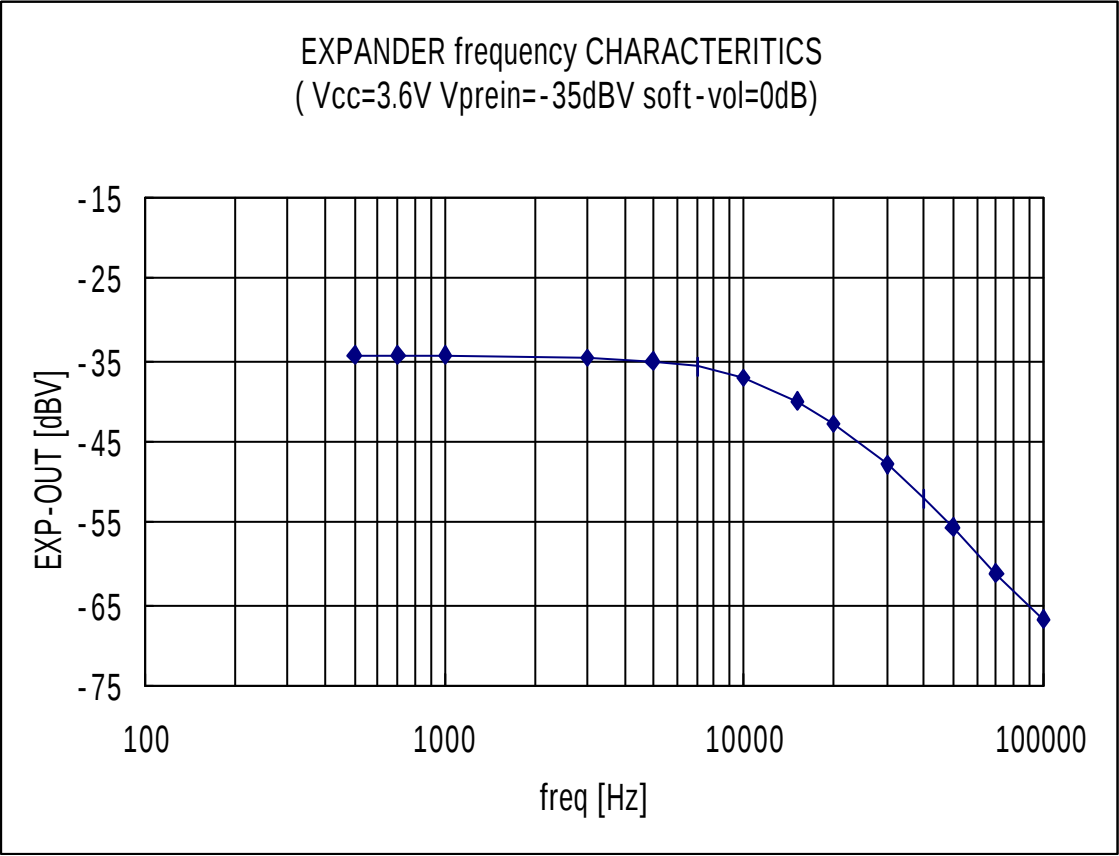
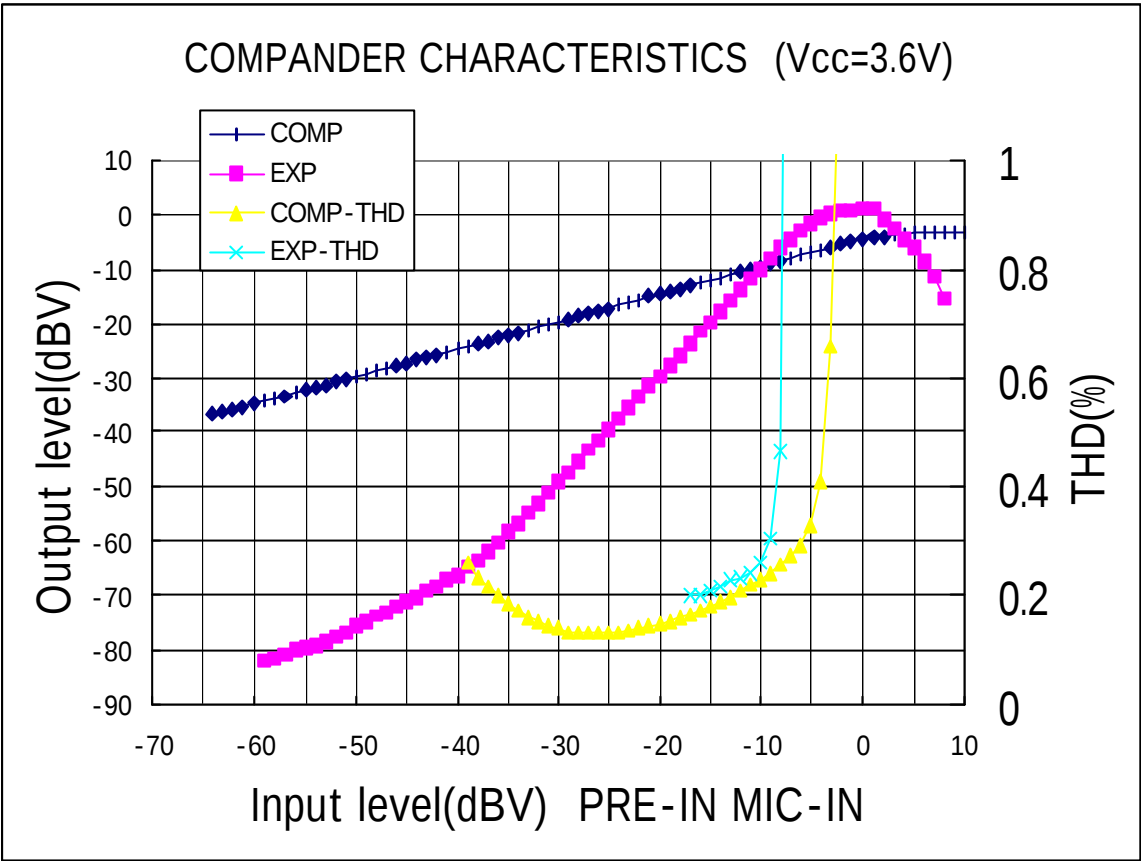
100k 100p 100p 100p 1 μ f XI VXIH

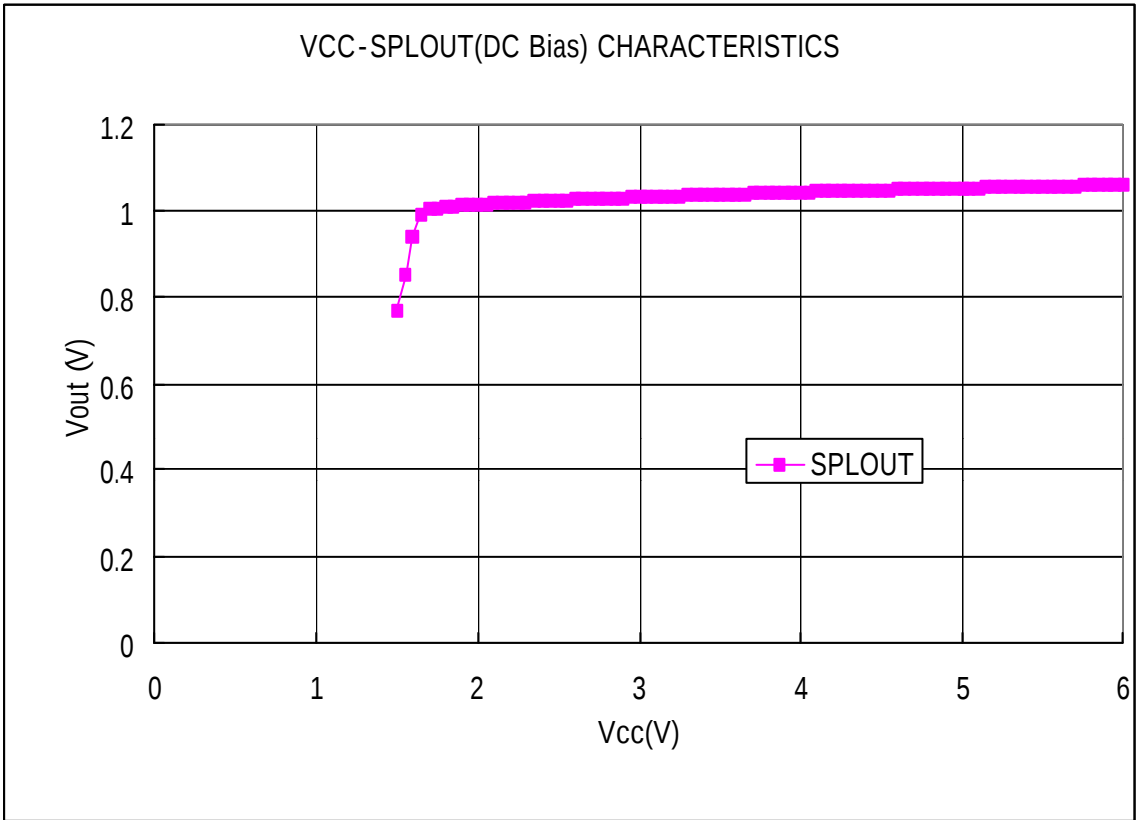
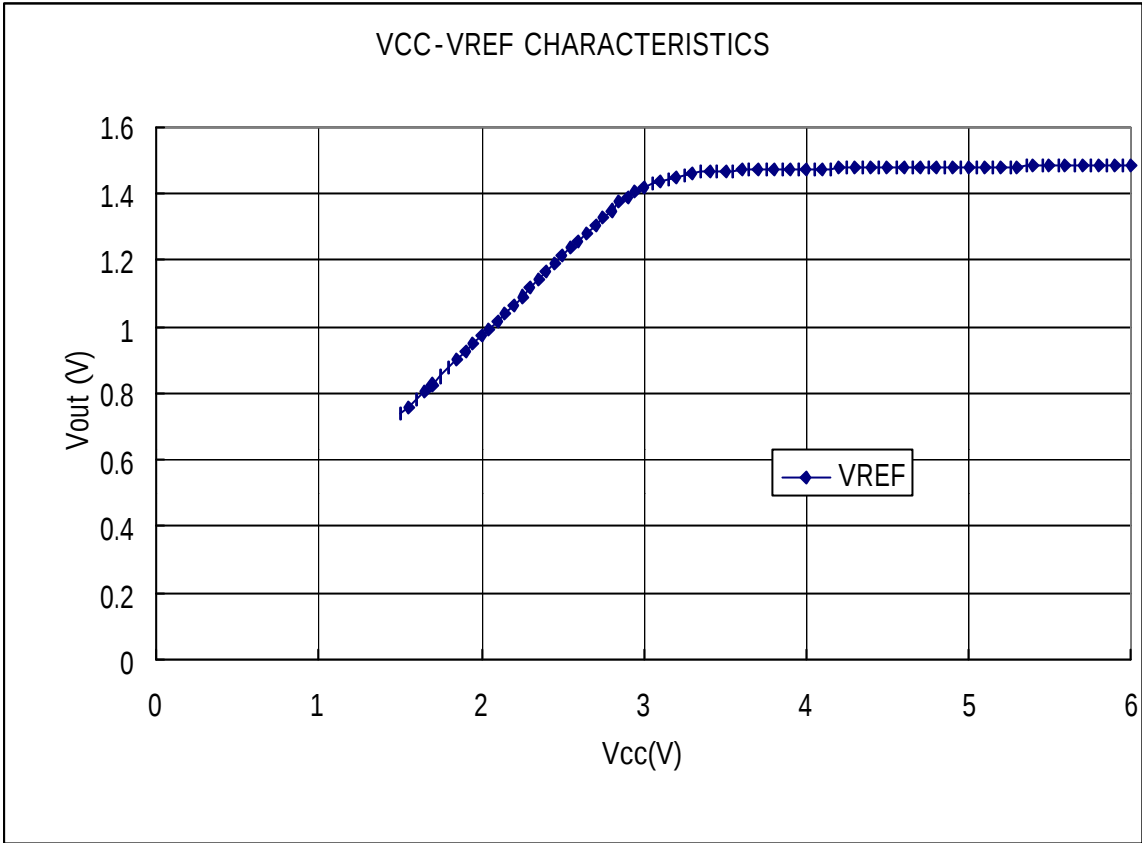
GND2 PA-GAIN-CONT VR1 20k C-NP 2.2 2.2 1k ILEAK TX-LOOP

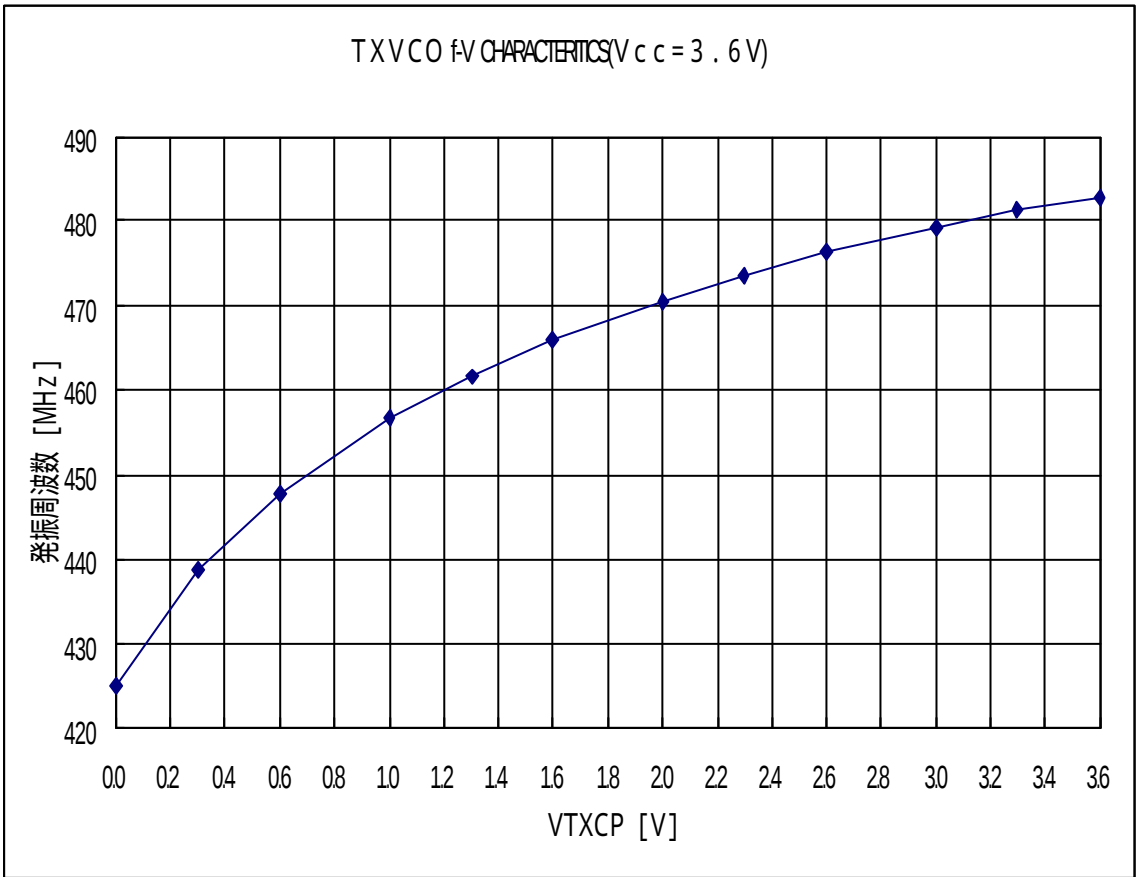
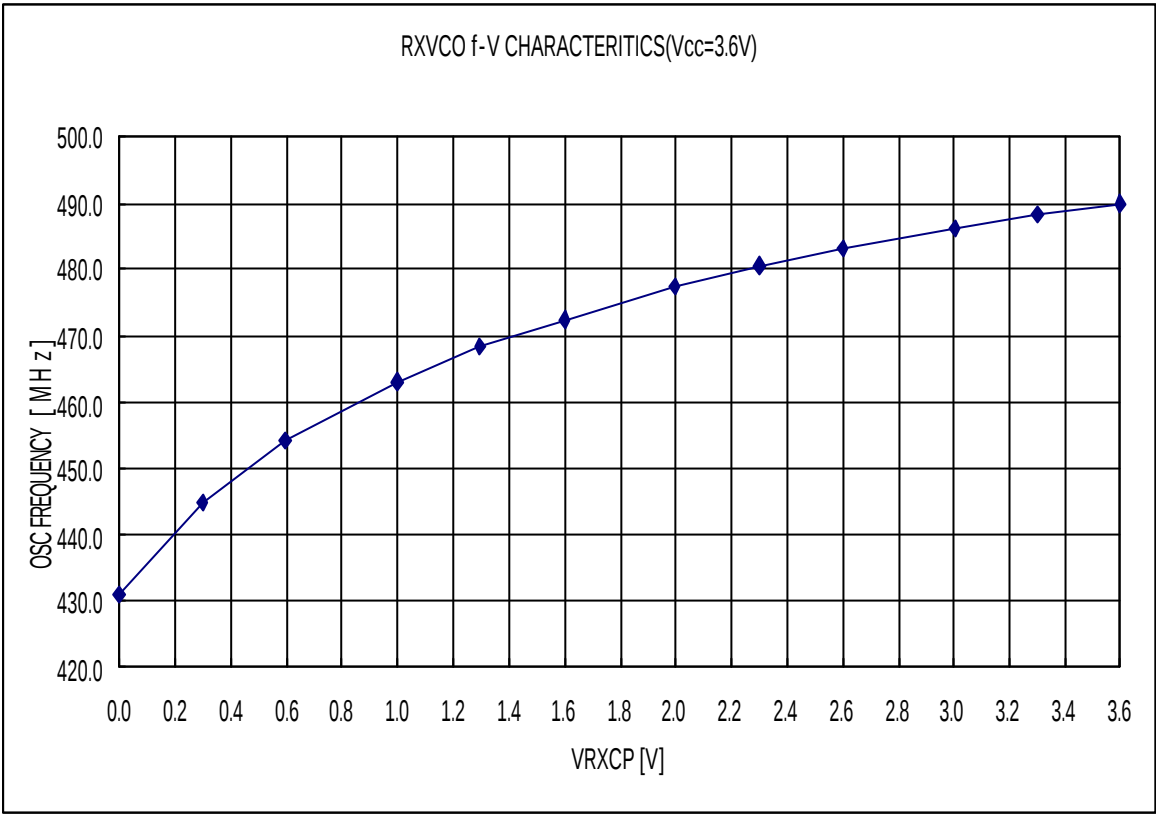
TXVCO TXVCO -L1 -L2 2.2n 2.2n TXVCO TXVCO -L1 -L2

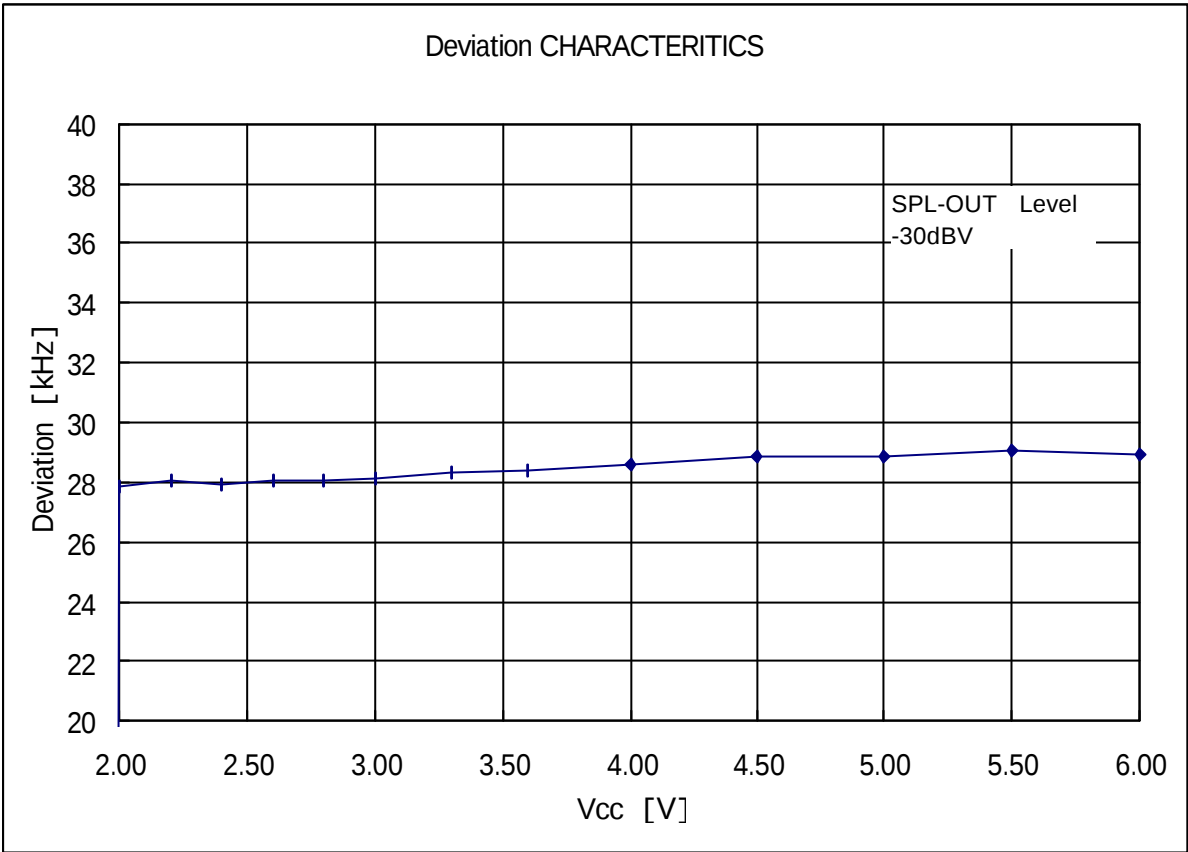






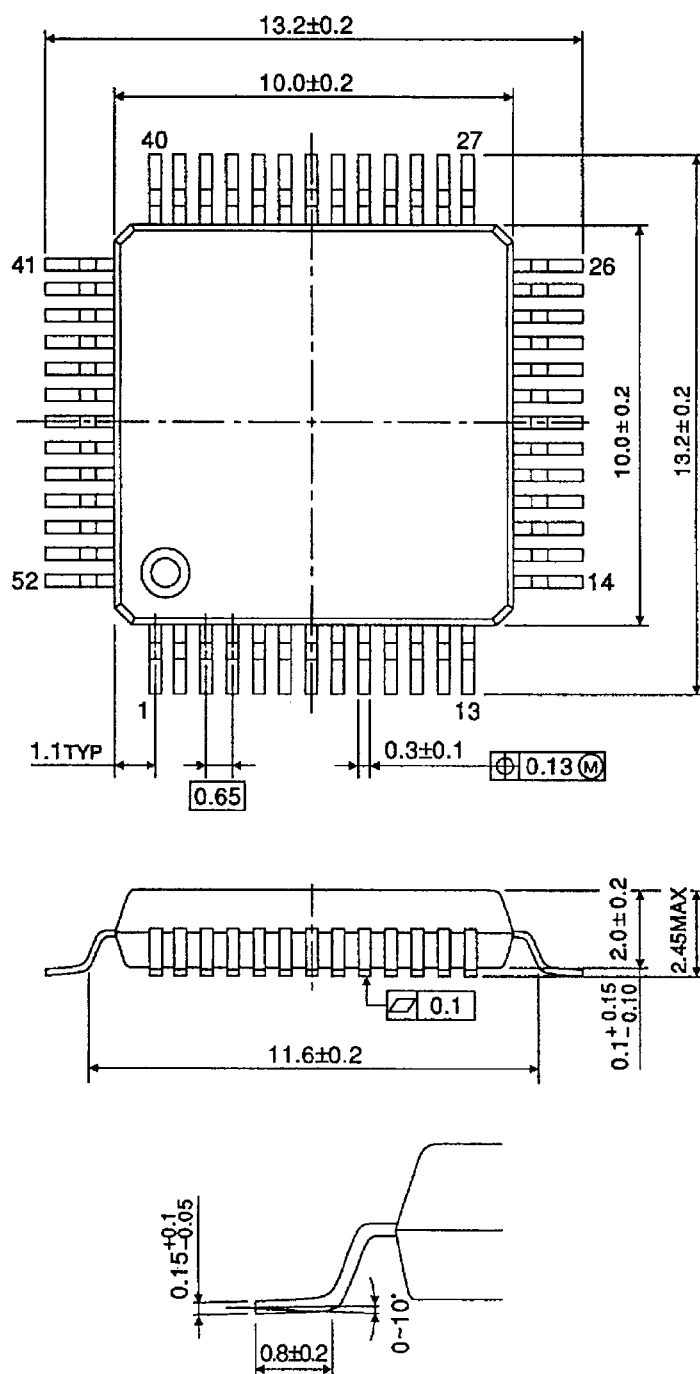






QFP52-P-1010-0.65

Unit : mm



RESTRICTIONS ON PRODUCT USE

000707EBA_S

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