



DEM-PCM1800 INSTRUCTION MANUAL

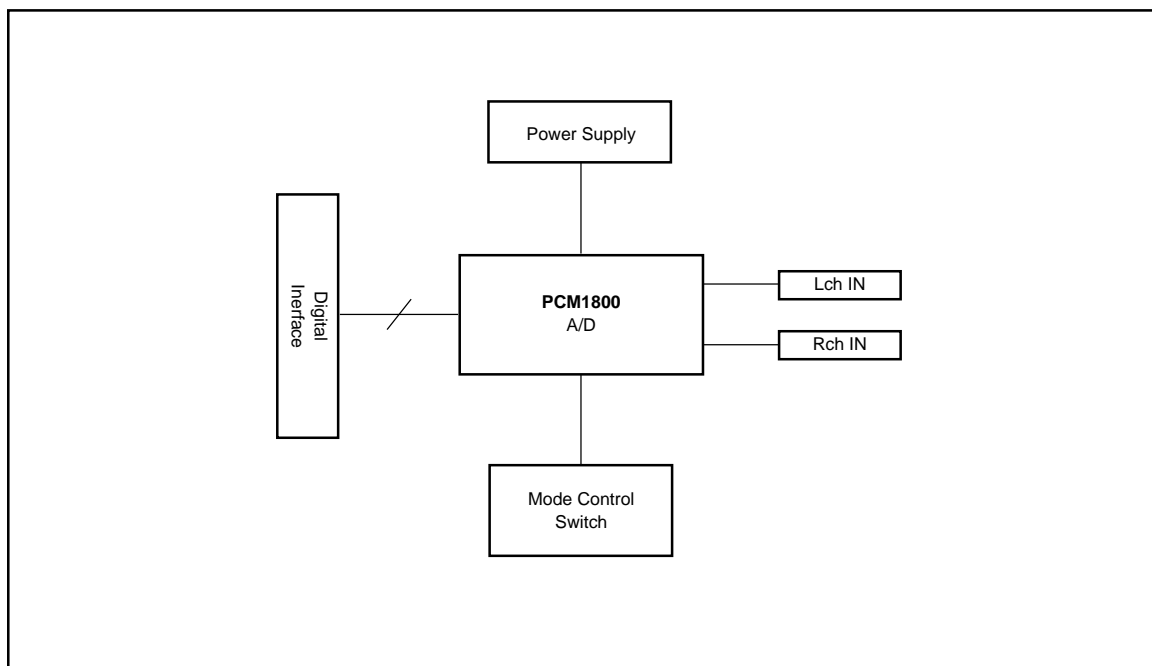
DESCRIPTION

DEM-PCM1800 is an evaluation board for the PCM1800 20-bit stereo audio analog-to-digital converter. The board contains a 24-pin SSOP IC socket, mode control switch, and some bypass capacitors.

DEM-PCM1800 can be operated by connecting only a power supply and system clock (either of $256f_s$ or $384f_s$ or $512f_s$). There are two kinds of operation modes: Master Mode, and Slave Mode for operation of the PCM1800.

In Master Mode, LRCK, BCK, FSYNC, and DATA, are outputs. In Slave Mode, DEM-PCM1800 requires LRCK, BCK, FSYNC inputs, and outputs DATA.

BLOCK DIAGRAM



DEM-PCM1800 BASIC CONNECTIONS AND OPERATION

- Power supply can be provided at $+V_{CC}$, GND connector CN1.
- Audio analog inputs are V_{INL} , V_{INR} connector CN2.
- Digital ground return to digital interface source should be connected at GND, connector CN3.
- System clock (either of $256f_s$ or $384f_s$ or $512f_s$) should be provided at SCLK, connector CN3.
- Operation Mode (master mode or slave mode) and selection of system clock can be controlled by switch MODE 0, MODE 1.
- The high pass filter function can be controlled by the switch bypass.

- Audio data format can be controlled by switch FMT0, FMT1.

- To enable the reset function push RESET (switch SW2).

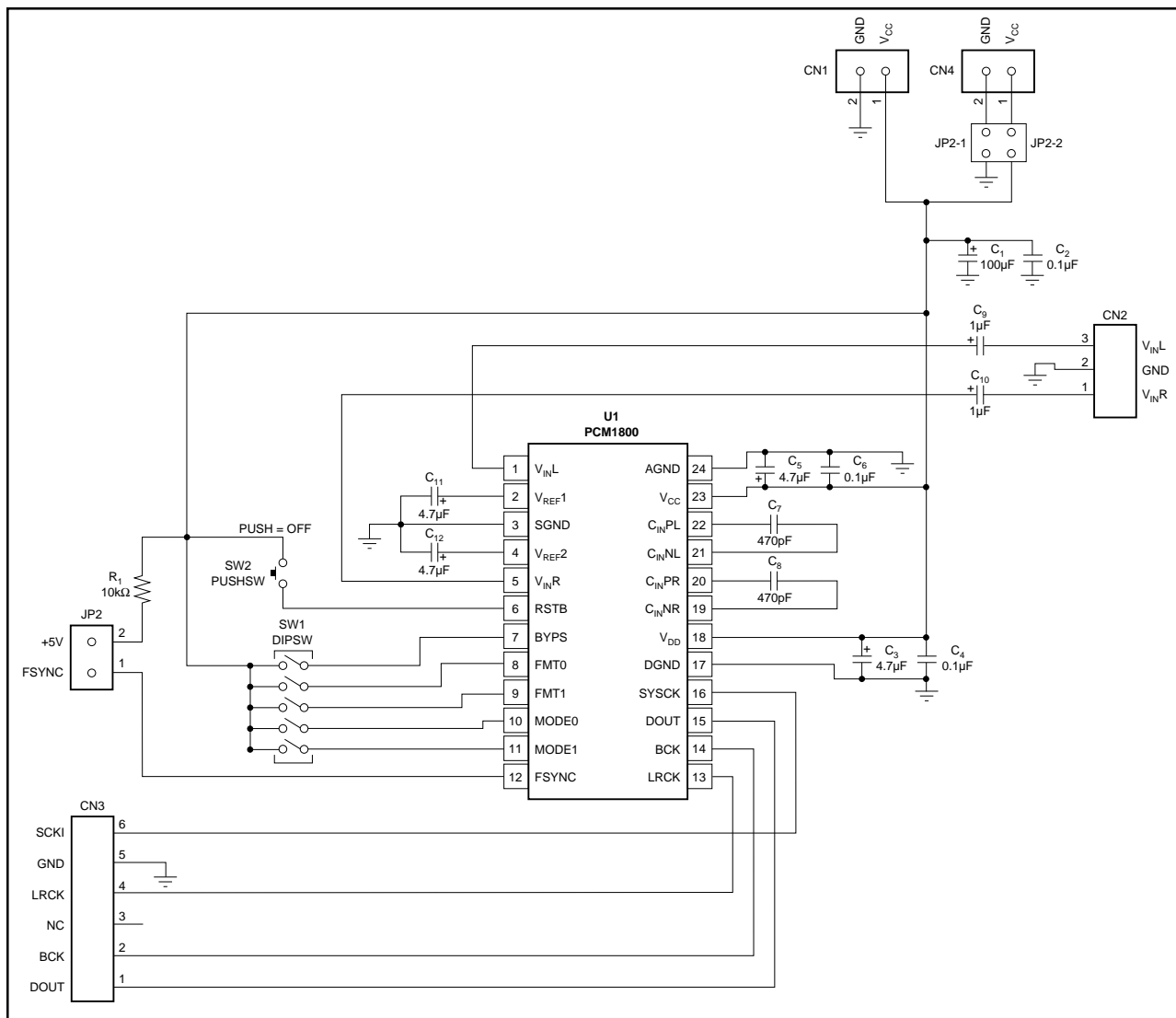
Master Mode Operation

- LRCK, BCK, DATA, are outputs for PCM Audio data.
- LRCK, BCK, DATA, outputs are located at connector CN3.

Slave Mode Operation

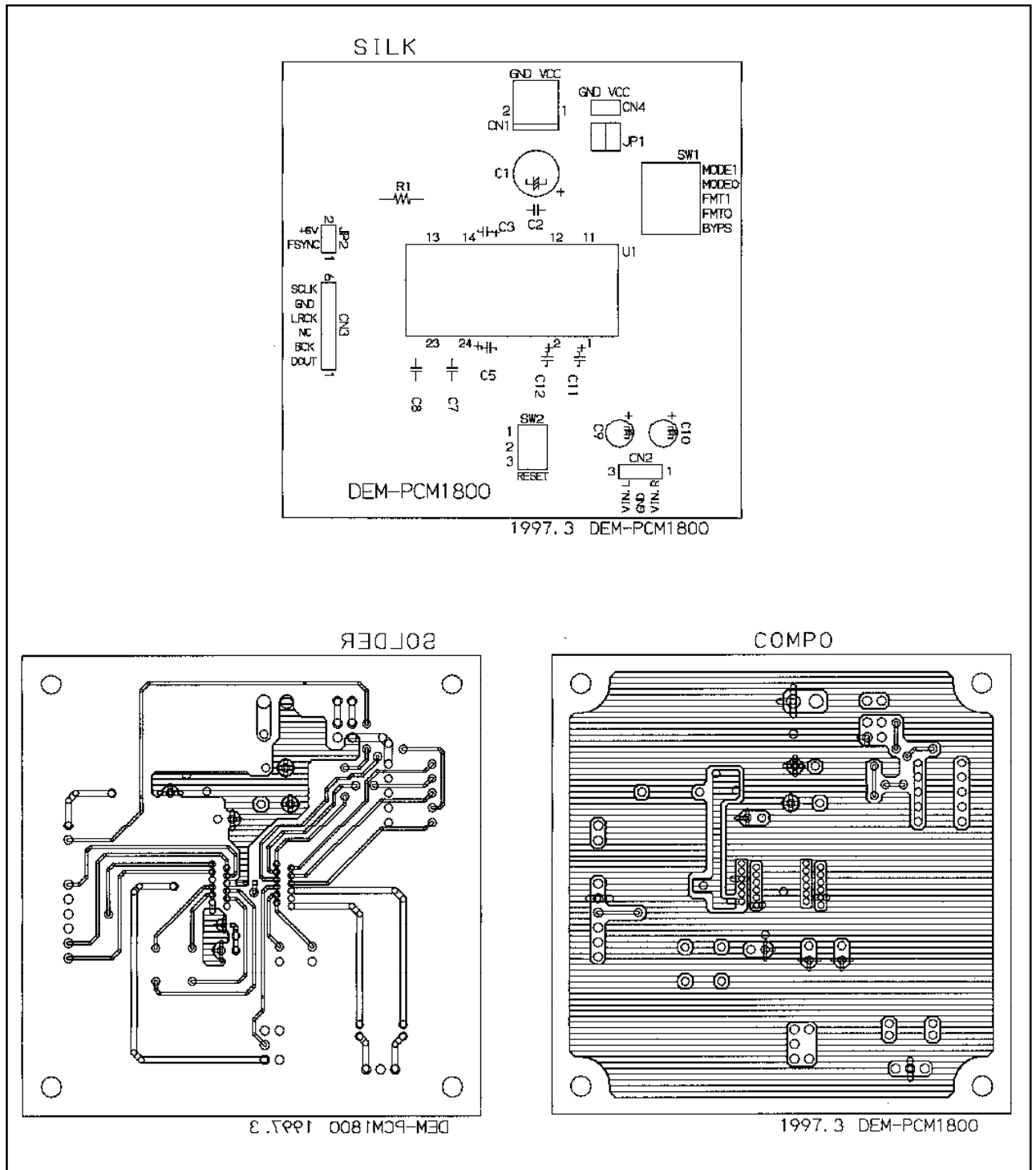
- LRCK, BCK, DATA, are inputs for PCM Audio data. Synchronized timing between LRCK (f_s) and system clock ($256f_s$, $384f_s$, $512f_s$) is required.
- LRCK, BCK, DATA, inputs are located at connector CN3 and are selected by setting FSYNC = H connecting JP2.

SCHEMATIC DIAGRAM



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PCB LAYOUT



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