SLA5000 Series

CMOS GATE ARRAY

- **3 Micron Dual Layer Metal**
- **5 Sizes**
- **Fast Design Cycle**

■DESCRIPTION

The SLA5000 Series consists of a group of five CMOS gate arrays with gate counts from 413 to 3,082 gates. The series is fabricated utilizing our 3 micron high speed CMOS silicon gate technology to achieve propagation delays of 3ns for the internal gates and 8 to 10ns for the I/O buffers. All I/O buffers are TTL and CMOS compatible which make this series an ideal choice for replacing existing discrete logic as well as for new designs.

■FEATURES

- High speed silicon gate CMOS technology
- TTL and CMOS I/O compatible
- High output drive capability
- Gate densities from 413 to 3,082 gates
- "Hard" MSI macrocells for superior AC performance
- Cell libraries, software, and documentation available for IBM® PC-XT FutureNet, Daisy, Mentor and Calma systems

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■SLA5000 SERIES

Parameter \ Series		SLA5040	SLA5080	SLA5120	SLA5210	SLA5300
Gates (2-input Nand)		413	790	1,264	2,140	3,082
Technology		Si-CMOS 2 Layer Metallization				
I/O level		TTL, CMOS				
Delay time	Internal gate*	3ns (standard)				
	Input buffer	t_{PLH}=8ns, t_{PHL}=10ns : (standard)				
	Output buffer	t_{PLH}=8ns, t_{PHL}=8ns : (standard) C_L=30pF				
Total ports for I/O (Terminals only for input port)		46 (8)	60 (8)	72 (8)	90 (6)	108 (8)
Output mode		Normal, open-drain, 3-state, Bi-directional				

*Typical, 3 unit+load+100 mils of aluminum interconnect.

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■ ABSOLUTE MAXIMUM RATINGS

(V_{SS}=0V)

Parameter	Symbol	Ratings	Unit
Supply voltage	V_{DD}	−0.3 to 7.0	V
Input voltage	V_I	−0.3 to V_{DD}+0.3	V
Output voltage	V_O	−0.3 to V_{DD}+0.3	V
Storage temperature	T_{stg}	−65 to 150	°C

■ RECOMMENDED OPERATING CONDITIONS

(V_{SS}=0V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply voltage	V_{DD}		4.75	5.00	5.25	V
Operating temperature	T_{opr}		0	—	70	°C

■ ELECTRICAL CHARACTERISTICS

(V_{DD}=5V±5%, V_{SS}=0V, Ta=0 to 70°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply current	I_{DD}	Standby	—	—	10	μA
High level output voltage	V_{OH}	V_{DD}=4.75V I_{OH}=−6mA	2.4	—	—	V
Low level output voltage	V_{OL}	V_{DD}=4.75V I_{OL}=6mA	—	—	0.4	V
High level input voltage	V_{IH}	V_{DD}=5.25V	2.0	—	—	V
Low level input voltage	V_{IL}	V_{DD}=4.75V	—	—	0.8	V
Input leakage current	I_{LI}	—	−1	—	1	μA

■ PACKAGE LIST

Type	Pin No.	Package name	SLA5040	SLA5080	SLA5120	SLA5210	SLA5300
Plastic DIP	16pin	C16	○				
	18pin	C18	○	○			
	24pin	C24	○	○	○		
	40pin	C40	○	○	○	□	
	42pin	C42	○	○	○	○	
CERDIP	16pin	H16	○	○			
	18pin	H18	○	○			
	20pin	H20	○	○			
	24pin	H24	○	○	○	○	
	28pin	H28	○	○	○	○	
	40pin	H40	○	○	○	○	
Plastic FP	44pin	F44-2	○	○	○		
	46pin	F46-5	□	□	□	□	
	60pin	F60-2	○	○	○	□	
	60pin	F60-5	□	□	□	□	□
	80pin	F80-5		○	○	○	○
	100pin	F100-5				○	○
Plastic SOP	24pin	M24	○	○			
	28pin	M28-2	□	□			
Shrink DIP	64pin	S64			○	□	
Ceramic PGA	64pin	P64			○	○	□
	72pin	P72			○	○	○
	132pin	P132			○	○	○
PLCC	68pin	J68			○	○	
	84pin	J84					○

○ : Available □ : Under development

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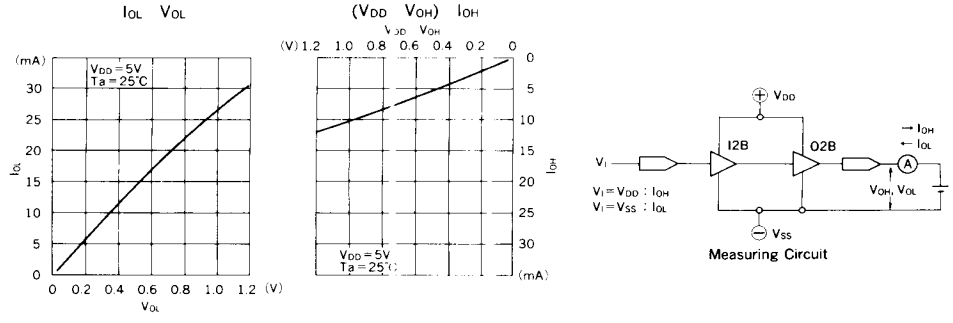
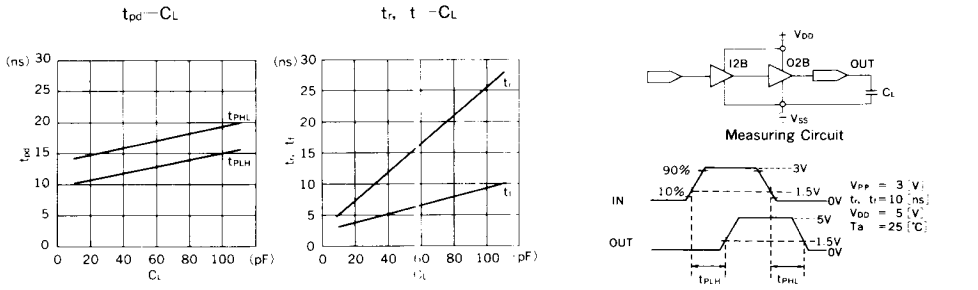
■PERFORMANCE CURVES

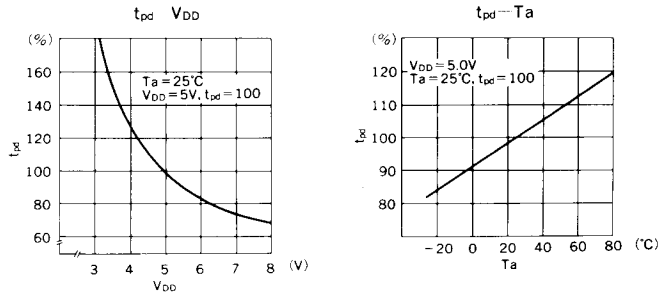
●Output Current



● t_{pd}, t_r, t_f—C_L



●Delay Time



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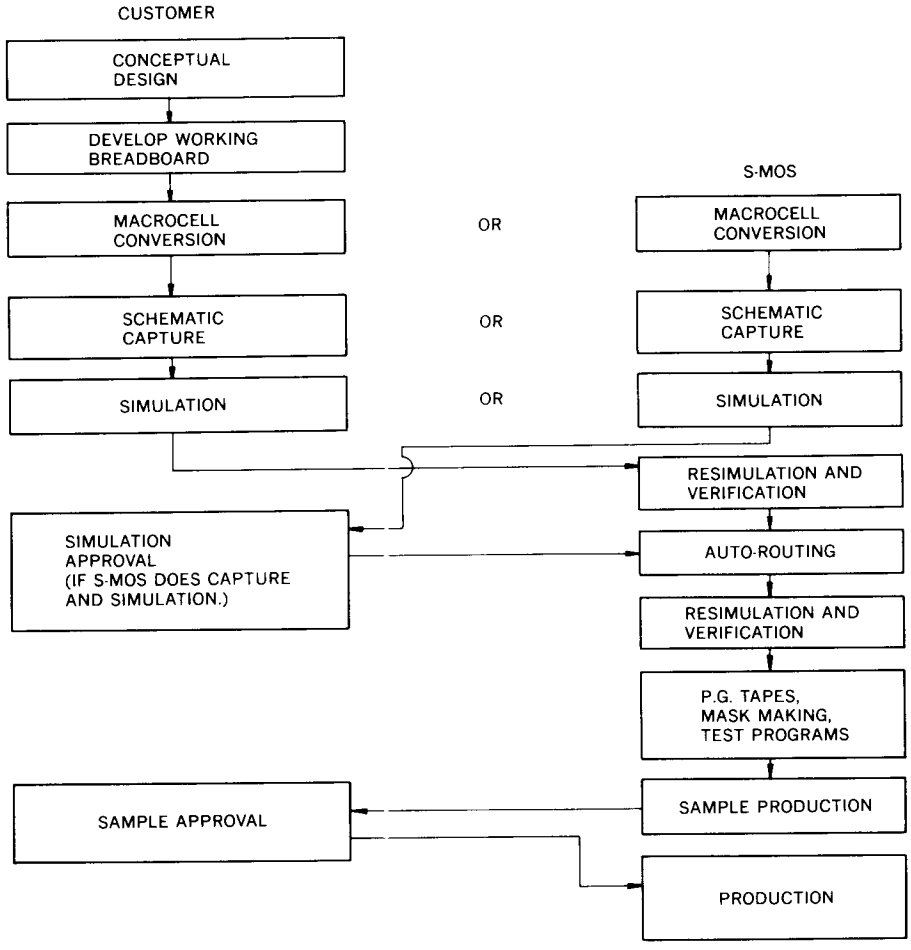
■ GATE ARRAY DESIGN FLOW



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