

# ThunderLAN™ TNETE110A PCI ETHERNET™ CONTROLLER SINGLE-CHIP 10 BASE-T

SPWS022A – APRIL 1996 – REVISED NOVEMBER 1996

- **Single-Chip Ethernet™ Adapter for the Peripheral Component Interconnect (PCI) Local Bus**
  - 32-Bit PCI† Glueless Host Interface
  - Compliant With PCI Local-Bus Specification (Revision 2.0)
  - 33-MHz Operation
  - 3-V or 5-V I/O Operation
  - Adaptive Performance Optimization™ (APO) by Texas Instruments (TI™) for Highest Available PCI Bandwidth
  - High-Performance Bus Master Architecture With Byte-Aligning DMA Controller for Low Host CPU and Bus Utilization
  - Plug-and-Play Compatible
- **Supports 32-Bit Data Streaming on PCI Bus**
  - Time Division Multiplexed SRAM
  - 2-Gbps Internal Bandwidth
- **Driver Compatible With All Previous ThunderLAN Components**
- **Switched-Ethernet Compatible**
- **Full-Duplex Compatible With Independent Transmit and Receive Channels**
- **No On-Board Memory Required**
- **Auto-Negotiation (N-Way) Compatible**
- **Supports the Card Bus CIS Pointer Register**
- **Integrated 10 Base-T, and 10 Base-5 Attachment Unit Interface (AUI) Physical Layer Interface**
  - Single-Chip IEEE 802.3 and Blue Book Ethernet-Compliant Solution
  - DSP-Based Digital Phase-Locked Loop
  - Smart Squelch Allows for Transparent Link Testing
  - Transmission Waveshaping
  - Autopolarity (Reverse Polarity Correction)
  - External/Internal Loopback Including Twisted Pair and AUI
  - 10 Base-2 Supported Via AUI Interface
- **Low-Power CMOS Technology**
  - Green PC Compatible
  - Microsoft™ Advanced Power Management
- **EEPROM Interface Supports Jumperless Design and Autoconfiguration**
- **Hardware Statistics Registers for Management Information Base (MIB)**
- **DMTF (Desktop Management Task Force) Compatible**
- **IEEE Standard 1149.1‡ Test Access Port (JTAG)**
- **144-Pin Quad Flat Packages (PCM Suffix) and Thin Quad Flat Packages (PGE Suffix)**

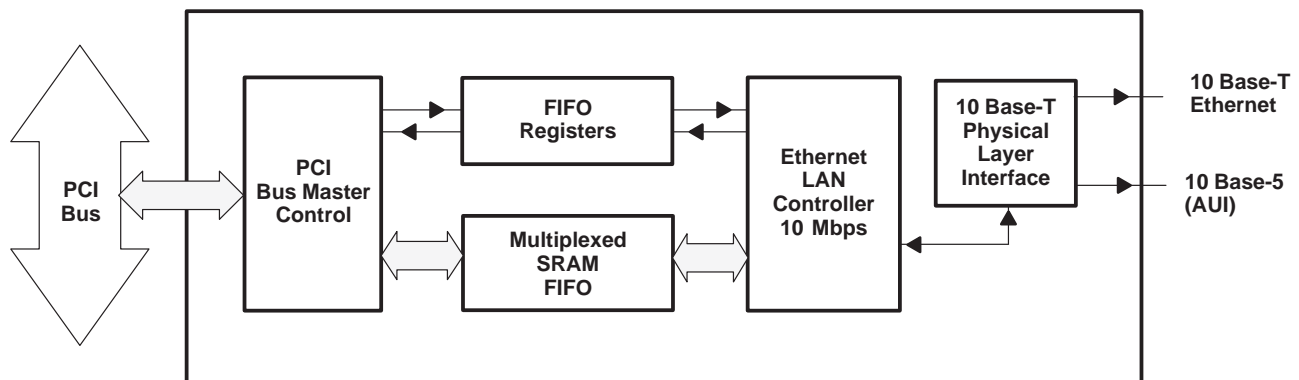


Figure 1. ThunderLAN Architecture



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† The PCI Local-Bus Specification, Revision 2.0 should be used as a reference with this document.

‡ IEEE Standard 1149.1–1990, IEEE Standard Test-Access Port and Boundary-Scan Architecture

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## description

ThunderLAN is a high-speed networking architecture that provides a complete PCI-to-10 Base-T/AUI Ethernet solution. The TNETE110A, one implementation of the ThunderLAN architecture, is an intelligent protocol network interface. The ThunderLAN SRAM FIFO-based architecture eliminates the need for external memory and offers a single-chip glueless PCI-to-10 Base-T/AUI (IEEE 802.3) solution with an on-board physical layer interface. See Figure 1.

The glueless PCI interface supports 32-bit streaming, operates at speeds up to 33 MHz and is capable of internal data-transfer rates up to 2 Gbps, taking full advantage of all available PCI bandwidth. The TNETE110A offers jumperless autoconfiguration using PCI configuration read/write cycles. Customizable configuration registers, which can be autoloading from an external serial EEPROM, allow designers of TNETE110A-based systems to give their systems a unique identification code. The TNETE110A PCI interface, developed in conjunction with other leaders in the semiconductor and computer industries, has been vigorously tested on multiple platforms to ensure compatibility across a wide array of available PCI products. In addition, the ThunderLAN drivers and ThunderLAN architecture use TI's patented adaptive performance optimization (APO) technology to dynamically adjust critical parameters for minimum latency, minimum host CPU utilization, and maximum system performance. This technology ensures that the maximum capabilities of the PCI interface are used by automatically tuning the adapter to the specific system in which it is operating.

An intelligent protocol handler (PH) implements the serial protocols of the network. The PH is designed for minimum overhead related to multiple protocols, using common state machines to implement 95 percent of the total protocol handler. On transmit, the PH serializes data, adds framing and cyclic redundancy check (CRC) fields, and interfaces to the network physical layer (PHY) chip. On receive, it provides address recognition, CRC and error checking, frame disassembly, and deserialization. Data for multiple channels is passed to and from the PH by way of circular-buffer FIFOs in the FIFO SRAM.

Compliant with IEEE Standard 1149.1, the TNETE110A provides a 5-pin test-access port that is used for boundary-scan testing.

The TNETE110A is available in a 144-pin quad flat package and thin quad flat package.

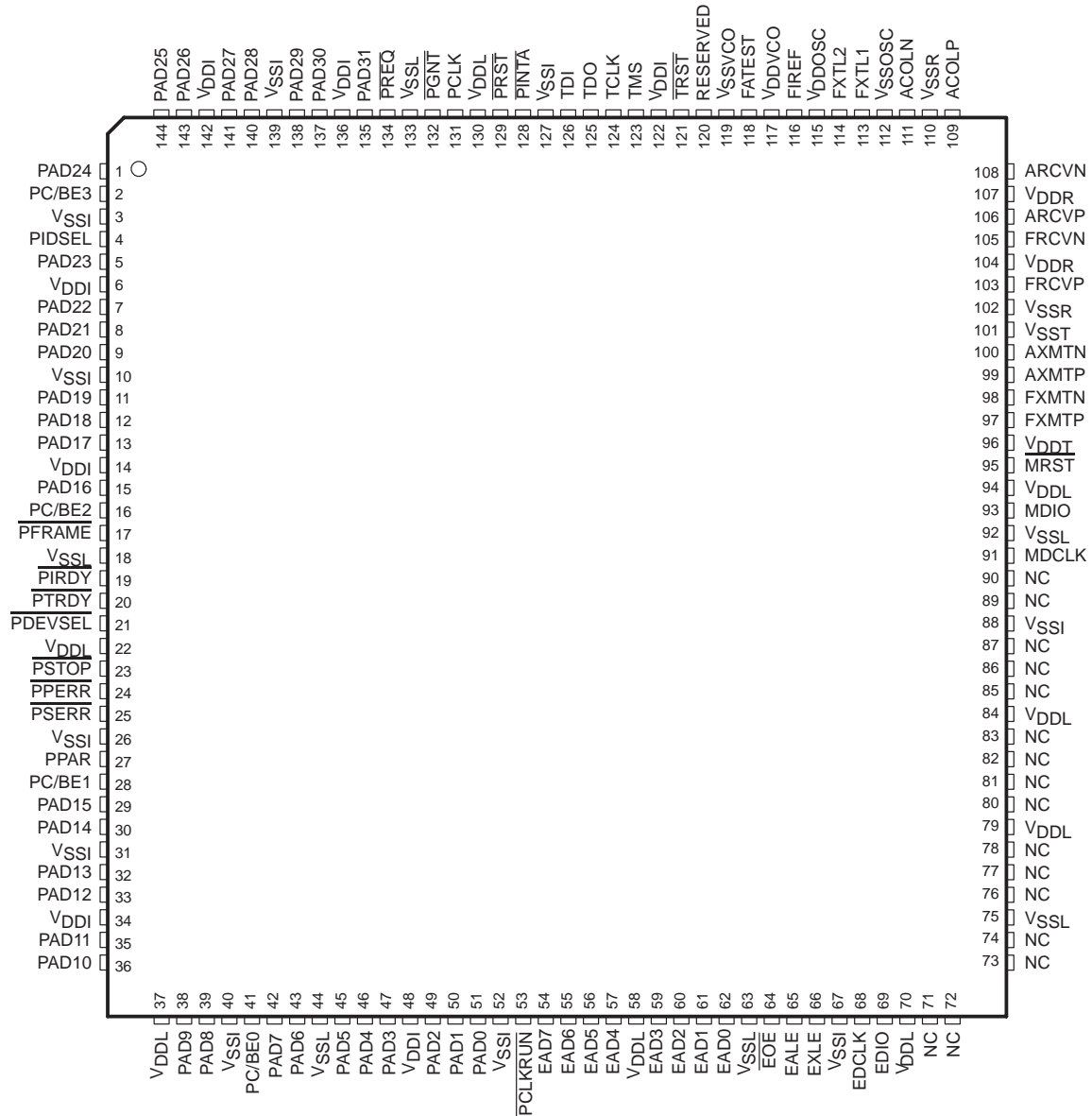
## differences between TNETE110 and TNETE110A:

The TNETE110A implements the CIS pointer register as defined in the PC card standard. This register can be found in the PCI configuration registers at offset 28h. For other differences between the TNETE110 and TNETE110A, consult the *ThunderLAN Programmer's Guide* (literature number SPWU013).



## pin assignments

### PCM and PGE PACKAGES (TOP VIEW)



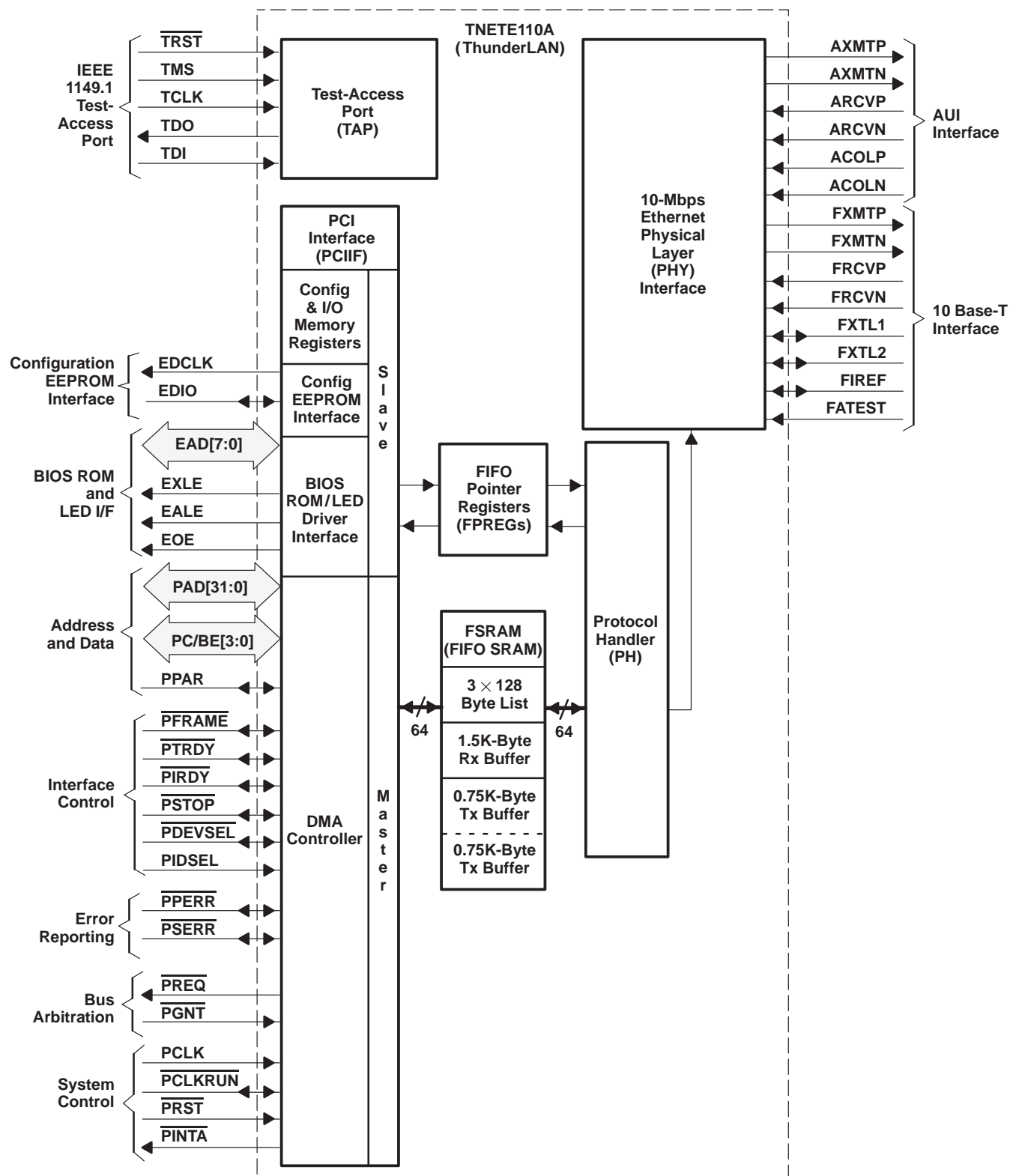
# ThunderLAN™ TNETE110A

## PCI ETHERNET™ CONTROLLER

### SINGLE-CHIP 10 BASE-T

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#### functional block diagram



### Pin Functions

PIN NAME	NO.	TYPE†	DESCRIPTION
<b>TEST PORT</b>			
TCLK	124	I	Test clock. TCLK is used to clock state information and test data into and out of the device during operation of the test port.
TDI	126	I	Test data input. TDI is used to shift test data and test instructions serially into the device during operation of the test port.
TDO	125	O	Test data output. TDO is used to shift test data and test instructions serially out of the device during operation of the test port.
TMS	123	I	Test mode select. TMS is used to control the state of the test port controller within TNETE110A.
TRST	121	I	Test reset. TRST is used for asynchronous reset of the test port controller.
<b>PCI INTERFACE</b>			
PAD31	135	I/O	PCI address/data bus. Byte 3 (most significant) of the PCI address/data bus.
PAD30	137		
PAD29	138		
PAD28	140		
PAD27	141		
PAD26	143		
PAD25	144		
PAD24	1		
PAD23	5	I/O	PCI address/data bus. Byte 2 of the PCI address/data bus.
PAD22	7		
PAD21	8		
PAD20	9		
PAD19	11		
PAD18	12		
PAD17	13		
PAD16	15		
PAD15	29	I/O	PCI address/data bus. Byte 1 of the PCI address/data bus.
PAD14	30		
PAD13	32		
PAD12	33		
PAD11	35		
PAD10	36		
PAD9	38		
PAD8	39		

† I = input, O = output, I/O = 3-state input/output

# ThunderLAN™ TNETE110A

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#### Pin Functions (Continued)

PIN NAME	NO.	TYPE†	DESCRIPTION
PCI INTERFACE (CONTINUED)			
PAD7	42	I/O	PCI address/data bus. Byte 0 (least significant) of the PCI address/data bus.
PAD6	43		
PAD5	45		
PAD4	46		
PAD3	47		
PAD2	49		
PAD1	50		
PAD0	51		
PCLK	131	I	PCI clock. PCLK is the clock reference for all PCI bus operations. All other PCI pins except $\overline{\text{PRST}}$ and $\overline{\text{PINTA}}$ are sampled on the rising edge of PCLK. All PCI bus timing parameters are defined with respect to this edge.
$\overline{\text{PCLKRUN}}$	53	I/O‡	Clock run control. $\overline{\text{PCLKRUN}}$ is the active-low PCI clock request/grant signal that allows the TNETE110AA to indicate when an active PCI clock is required. (This is an open drain.)
PC/BE3	2	I/O	PCI bus command and byte enables. PC/BE3 enables byte 3 (MSB) of the PC/BE pins.
PC/BE2	16		PCI bus command and byte enables. PC/BE2 enables byte 2 of PCI address/data bus.
PC/BE1	28		PCI bus command and byte enables. PC/BE1 enables byte 1 of PCI address/data bus.
PC/BE0	41		PCI bus command and byte enables. PC/BE0 enables byte 0 of PCI address/data bus.
$\overline{\text{PDEVSEL}}$	21	I/O	PCI device select. $\overline{\text{PDEVSEL}}$ indicates that the driving device has decoded one of its addresses as the target of the current access. The TNETE110A drives $\overline{\text{PDEVSEL}}$ when it decodes an access to one of its registers. As a bus master, the TNETE110A monitors $\overline{\text{PDEVSEL}}$ to detect accesses to illegal memory addresses.
$\overline{\text{PFRAME}}$	17	I/O	PCI cycle frame. $\overline{\text{PFRAME}}$ is driven by the active bus master to indicate the beginning and duration of an access. $\overline{\text{PFRAME}}$ is asserted to indicate the start of a bus transaction and remains asserted during the transaction, only being deasserted in the final data phase.
$\overline{\text{PGNT}}$	132	I	PCI bus grant. $\overline{\text{PGNT}}$ is asserted by the system arbiter to indicate that the TNETE110A has been granted control of the PCI bus.
$\overline{\text{PIDSEL}}$	4	I	PCI initialization device select. $\overline{\text{PIDSEL}}$ is the chip select for access to PCI configuration registers.
$\overline{\text{PINTA}}$	128	O/D	PCI interrupt. $\overline{\text{PINTA}}$ is the interrupt request from the TNETE110A. PCI interrupts are shared, so this is an open-drain (wired-OR) output.
$\overline{\text{PIRDY}}$	19	I/O	PCI initiator ready. $\overline{\text{PIRDY}}$ is driven by the active bus master to indicate that it is ready to complete the current data phase of a transaction. A data phase is not completed until both $\overline{\text{PIRDY}}$ and $\overline{\text{PTRDY}}$ are sampled asserted. When the TNETE110A is a bus master, it uses $\overline{\text{PIRDY}}$ to align incoming data on reads or outgoing data on writes with its internal RAM-access synchronization (maximum one cycle at the beginning of burst). When the TNETE110A is a bus slave, it extends the access appropriately until both $\overline{\text{PIRDY}}$ and $\overline{\text{PTRDY}}$ are asserted.
$\overline{\text{PTRDY}}$	20	I/O	PCI target ready. $\overline{\text{PTRDY}}$ is driven by the selected device (bus slave or target) to indicate that it is ready to complete the current data phase of a transaction. A data phase is not completed until both $\overline{\text{PIRDY}}$ and $\overline{\text{PTRDY}}$ are sampled asserted. ThunderLAN uses $\overline{\text{PTRDY}}$ to ensure every direct I/O (DIO) operation is correctly interlocked.
PPAR	27	I/O	PCI parity. PPAR carries even parity across PAD[31:0] and PC/BE[3:0]. It is driven by the TNETE110A during all address and write cycles as a bus master and during all read cycles as a bus slave.
$\overline{\text{PPER}}$	24	I/O	PCI parity error. $\overline{\text{PPER}}$ indicates a data parity error on all PCI transactions except special cycles.

† I = input, I/O = 3-state input/output, O/D = open-drain output

‡ Open drain



### Pin Functions (Continued)

PIN NAME	NO.	TYPE†	DESCRIPTION
<b>PCI INTERFACE (CONTINUED)</b>			
$\overline{\text{PREQ}}$	134	I/O	PCI bus request. $\overline{\text{PREQ}}$ is asserted by the TNETE110A to request control of the PCI bus. This is not a shared signal.
$\overline{\text{PRST}}$	129	I	PCI reset signal.
$\overline{\text{PSERR}}$	25	O/D	PCI system error. $\overline{\text{PSERR}}$ indicates parity errors, or special cycle data parity errors.
$\overline{\text{PSTOP}}$	23	I/O	PCI stop. $\overline{\text{PSTOP}}$ indicates the current target is requesting the master to stop the current transaction.
<b>BIOS ROM/LED DRIVER INTERFACE</b>			
EAD7 EAD6 EAD5 EAD4 EAD3 EAD2 EAD1 EAD0	54 55 56 57 59 60 61 62	I/O	<p>EPROM address/data. EAD[7:0] is a multiplexed byte bus that is used to address and read data from an external BIOS ROM.</p> <ul style="list-style-type: none"> <li>On the cycle when EXLE is asserted low, EAD[7:0] is driven with the high byte of the address.</li> <li>On the cycle when EALE is asserted low, EAD[7:0] is driven with the low byte of the address.</li> <li>When <math>\overline{\text{EOE}}</math> is asserted, BIOS ROM data should be placed on the bus.</li> </ul> <p>These pins can also be used to drive external status LEDs. Low-current (2–5 mA) LEDs can be connected directly (through appropriate resistors). High-current LEDs can be driven through buffers or from the BIOS ROM address latches.</p>
EALE	65	O	EPROM address latch enable. EALE is driven low to latch the low (least significant) byte of the BIOS ROM address from EAD[7:0].
$\overline{\text{EOE}}$	64	O	EPROM output enable. When $\overline{\text{EOE}}$ is active (low) EAD[7:0] is in the high-impedance state and the output of the BIOS ROM should be placed on EAD[7:0].
EXLE	66	O	EPROM extended address latch enable. EXLE is driven low to latch the high (most significant) byte of the BIOS ROM address from EAD[7:0].
<b>CONFIGURATION EEPROM INTERFACE</b>			
EDCLK	68	O	EEPROM data clock. EDCLK transfers serial clocked data to the 2K-bit serial EEPROMs (24C02) (see Note 1).
EDIO	69	I/O	EEPROM data I/O. EDIO is the bidirectional serial data/address line to the 2K-bit serial EEPROM (24C02). EDIO requires an external pullup for EEPROM operation. Tying EDIO to ground disables the EEPROM interface and prevents autoconfiguration of the PCI configuration register.
<b>NETWORK INTERFACE (10 Base-T AND AUI)</b>			
ACOLN ACOLP	111 109	A	AUI receive pair. ACOLN and ACOLP are differential line-receiver inputs and connect to receive pair via transformer isolation, etc.
ARCVN ARCVP	108 106	A	AUI receive pair. ARCVN and ARCVP are differential line-receiver inputs and connect to receive pair via transformer isolation, etc.
AXMTP AXMTN	99 100	A	AUI transmit pair. AXMTP and AXMTN are differential line-transmitter outputs.
FATEST	118	A	Analog test pin. FATEST provides access to the filter of the reference PLL. This pin should be left as a no connect.
FIREF	116	A	Current reference. FIREF is used to set a current reference for the analog circuitry.
FRCVN FRCVP	105 103	A	10 Base-T receive pair. FRCVN and FRCVP are differential line receiver inputs and connect to receive pair via transformer isolation, etc.
FXTL1 FXTL2	113 114	A	Crystal oscillator pins. Drive FXTL1 from a 20-MHz crystal oscillator module.

† I = input, O = output, I/O = 3-state input/output, O/D = open-drain output, A = analog

NOTE 1: This pin should be tied to  $V_{DD}$  with a 4.7-k $\Omega$  – 10-k $\Omega$  pullup resistor.

# ThunderLAN™ TNETE110A

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#### Pin Functions (Continued)

PIN NAME	NO.	TYPE†	DESCRIPTION
<b>NETWORK INTERFACE (10 Base-T AND AUI) (CONTINUED)</b>			
FXMTP FXMTN	97 98	A	10 Base-T transmit pair. FXMTP and FXMTN are differential line transmitter outputs.
RESERVED	120	I	Reserved. Tie this pin low.
<b>SERIAL MANAGEMENT INTERFACE</b>			
MDIO	93	I/O	Management data I/O. MDIO is part of the serial management interface.
MDCLK	91	O	Management data clock. MDCLK is part of the serial management interface to physical-media independent (PMI)/PHY chip.
MRST	95	O	MII reset. MRST is the reset signal.
<b>POWER</b>			
VDDI	6, 14, 34, 48, 122, 136, 142	PWR	PCI V <sub>DD</sub> pins. V <sub>DDI</sub> pins provide power for the PCI I/O pin drivers. Connect V <sub>DDI</sub> pins to a 5-V power supply when using 5-V signals on the PCI bus. Connect V <sub>DDI</sub> pins to a 3-volt power supply when using 3-V signals on the PCI bus.
VDDL	22, 37, 58, 70, 79, 84 94, 130	PWR	Logic V <sub>DD</sub> pins (5 V). V <sub>DDL</sub> pins provide power for internal TNETE110A logic, and they should always be connected to 5 V.
VDDOSC	115	PWR	Analog power pin. VDDOSC is the 5-V power for the crystal oscillator circuit.
VDDR	104 107	PWR	Analog power pin. VDDR is the 5-V power for the receiver circuitry.
VDDT	96	PWR	Analog power pin. VDDT is the 5-V power for the transmitter circuitry.
VDDVCO	117	PWR	Analog power pin. VDDVCO is the 5-V power for the voltage controller oscillator (VCO) and filter input.
VSSI	3, 10, 26, 31, 40, 52, 67, 88, 127, 139	PWR	PCI I/O ground pins
VSSL	18, 44, 63, 75, 92, 133	PWR	Logic ground pins
VSSOSC	112	PWR	Analog power pin. Ground for crystal oscillator circuit
VSSR	102 110	PWR	Analog power pin. Ground for receiver circuitry
VSST	101	PWR	Analog power pin. Ground for transmitter circuitry
VSSVCO	119	PWR	Analog power pin. Ground for VCO and filter input

† I = input, A = analog, PWR = power

#### architecture

The major blocks of the TNETE110A include the PCI interface (PCIIF), protocol handler (PH), physical layer (PHY), FIFO pointer registers (FPREGS), FIFO SRAM (FSRAM), and a test-access port (TAP). The functionality of these blocks is described in the following sections.



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## **PCI interface (PCIIF)**

The TNETE110A PCIIF contains a byte-aligning DMA controller that allows frames to be fragmented into any byte length and transferred to any byte address while supporting 32-bit data streaming. For multipriority networks it can provide multiple data channels, each with separate lists, commands, and status. Data for the channels is passed to and from the PH by way of circular buffer FIFOs in the SRAM, controlled through FIFO registers. The configuration EEPROM interface (CEI), BIOS ROM/LED driver interface (BRI), configuration and I/O memory registers (CIOREGS), and DMA controller are subblocks of the PCIIF. The features of these subblocks are as follows:

### ***configuration EEPROM interface (CEI)***

The CEI provides a means for autoconfiguration of the PCI configuration registers. Certain registers in the PCI configuration space may be loaded using the CEI. Autoconfiguration allows builders of TNETE110A-based systems to customize the contents of these registers to identify their own system, rather than using the TI defaults. The EEPROM is read at power up and can then be read from, and written to, under program control.

### ***BIOS ROM/LED driver interface (BRI)***

The BRI addresses and reads data from an external BIOS ROM via a multiplexed byte-wide bus. The ROM address/data pins can also be multiplexed to drive external status LEDs.

### ***configuration and I/O memory registers (CIOREGS)***

The CIOREGS reside in the configuration space, which is 256 bytes in length. The first 64 bytes of the configuration space is the header region, which is explicitly defined by the PCI standard.

### ***DMA controller (DMAC)***

The DMAC is responsible for coordinating TNETE110A requests for mastership of the PCI bus. The DMAC provides byte-aligning DMA control allowing byte-size fragmented frames to be transferred to any byte address while supporting 32-bit data streaming.

## **protocol handler (PH)**

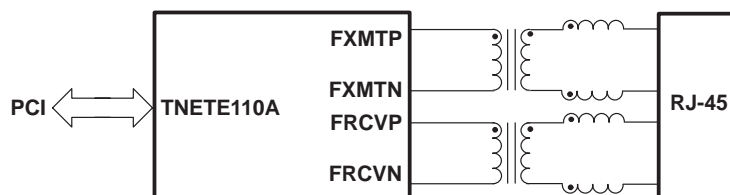
The PH implements the serial protocols of the network. On transmit, it serializes data, adds framing and CRC fields, and interfaces to the network PHY. On receive, it provides address recognition, CRC and error checking, frame disassembly, and deserialization. Data for multiple channels is passed to and from the PH by way of circular buffer FIFOs in the FSRAM controlled through FPREGS.

## **10 Base-T physical layer (PHY)**

The PHY acts as an on-chip front-end providing physical layer functions for 10 Base-5 (AUI), 10 Base-2, and 10 Base-T (twisted pair). The PHY provides Manchester encoding/decoding from smart squelch, jabber detection, link pulse detection, autopolarity control, 10 Base-T transmission waveshaping, and antialiasing filtering. Connection to the AUI drop cable for the 10 Base-T twisted pair is made via simple isolation transformers (see Figure 2) and no external filter networks are required. Suitable external termination components allow the use of either shielded or unshielded twisted-pair cable (150  $\Omega$  or 100  $\Omega$ ). Some of the key features of the on-chip PHY include the following:

- Integrated filters
- 10 Base-T transceiver
- AUI transceiver
- 10 Base-2 transceiver
- Autopolarity (reverse polarity correction)
- Loopback for twisted pair and AUI
- Full-duplex mode for simultaneous 10 Base-T transmission and reception
- Low power

## 10 Base-T physical layer (continued)



**Figure 2. Schematic for 10 Base-T Network Interface Using TNETE110A**

## FIFO pointer registers (FPREGS)

The FPREGS are used to implement circular buffer FIFOs in the SRAM. They are a collection of pointer and counter registers used to maintain the FIFO operation. Both the PCIIF and PH use FPREGS to determine where to read or write data in the SRAM and to determine how much data the FIFO contains.

## FIFO SRAM (FSRAM)

The FSRAM is a conventional SRAM array accessed synchronously to the PCI bus clock. Access to the RAM is allocated on a time-division multiplexed (TDM) basis, rather than through a conventional shared bus. This removes the need for bus arbitration and provides ensured bandwidth. Half of the RAM accesses (every other cycle) are allocated to the PCI controller. It has a 64-bit access port to the RAM, giving it 1 Gbps of bandwidth, sufficient to support 32-bit data streaming on the PCI bus. The PH has one quarter of the RAM accesses, and its port may be up to 64 bits wide. A 64-bit port for the PH provides 512 Mbps of bandwidth, more than sufficient for a full-duplex 100-Mbps network. The remaining RAM accesses can be allocated toward providing even more PH bandwidth. The RAM also is accessible (for diagnostic purposes) from the TNETE110A internal data bus. Host DIO (mapped I/O) accesses are used by the host to access internal TNETE110A registers and for adapter test.

Some of the features of the FSRAM follow:

- 3.375K bytes of FSRAM
- 1.5K-byte FIFO for receive channel
- One 1.5K-byte FIFO for transmit channel
- Three 128-byte lists

Supporting 1.5K byte of FIFO per channel allows full-frame buffering of Ethernet frames.

## test-access port (TAP)

Compliant with IEEE Standard 1149.1, the TAP is composed of five pins that are used to interface serially with the device and the board on which it is installed for boundary-scan testing.

**absolute maximum ratings over operating case temperature range (unless otherwise noted)†**

Supply voltage range, $V_{DD}$ (see Note 2)	– 0.5 V to 7 V
Input voltage range (see Note 2)	– 0.5 V to 7 V
Output voltage range	– 0.5 V to 7 V
Power dissipation	1.15 W
Operating case temperature range, $T_C$	0°C to 95°C
Junction to ambient package thermal impedance, airflow = 100 LFPM, $T_{JA(100)}$ PGE	45.4°C/W
Junction to ambient package thermal impedance, airflow = 0 LFPM, $T_{JA(0)}$ PGE	51°C/W
Junction to ambient package thermal impedance, airflow = 0 LFPM, $T_{JA(0)}$ PCM	41.4°C/W
Junction to ambient package thermal impedance, airflow = 100 LFPM, $T_{JA(100)}$ PCM	38.0°C/W
Junction to case package thermal impedance, $T_{JC}$	0.22°C/W
Storage temperature range, $T_{stg}$	– 65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 2: Voltage values are with respect to  $V_{SS}$ , and all  $V_{SS}$  pins should be routed so as to minimize inductance to system ground.

The recommended operating conditions and the electrical characteristics tables are divided into groups, depending on pin function:

- PCI interface pins
- Logic pins
- Physical layer pins

The PCI signal pins are operated in one of two modes shown in the PCI tables.

- 5-V signal mode
- 3-V signal mode

**recommended operating conditions (PCI interface pins) (see Note 3)**

		3-V SIGNALING OPERATION			5-V SIGNALING OPERATION			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
$V_{DD}$	Supply voltage (PCI)	3	3.3	3.6	4.75	5	5.25	V
$V_{IH}$	High-level input voltage	$0.5 \times V_{DD}^{\ddagger}$			$V_{DD} + 0.5^{\ddagger}$			V
$V_{IL}$	Low-level input voltage, TTL-level signal (see Note 4)	$-0.5^{\ddagger}$			$-0.5$			V
$I_{OH}$	High-level output current	TTL outputs		$-0.5^{\ddagger}$			$-2$	mA
$I_{OL}$	Low-level output current (see Note 5)	TTL outputs		$1.5^{\ddagger}$			$6$	mA

$^{\ddagger}$  Specified by design spice IV curve (please refer to PCI specification revision 2.1, section 4.2, paragraph 2 for explanation)

NOTES: 3. PCI interface pins include  $V_{DDI}$ ,  $PCLKRUN$ ,  $PFRAME$ ,  $PTRDY$ ,  $PIRDY$ ,  $PSTOP$ ,  $PDEVSEL$ ,  $PIDSEL$ ,  $PPERR$ ,  $PSERR$ ,  $PREQ$ ,  $PGNT$ ,  $PCLK$ ,  $PPAR$ ,  $PRST$ ,  $PINTA$ ,  $PAD[31:0]$ ,  $PC/BE[3:0]$ ,  $TRST$ ,  $TMS$ ,  $TCLK$ ,  $TDO$ ,  $TDI$ .

4. The algebraic convention, where the more negative (less positive) limit is designated as a minimum, is used for logic-voltage levels only.

5. Output current of 2 mA is sufficient to drive five low-power Schottky TTL loads or ten advanced low-power Schottky TTL loads (worst case).

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**electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (PCI interface pins)**

PARAMETER		TEST CONDITIONS †	3-V SIGNALING OPERATION		5-V SIGNALING OPERATION		UNIT
			MIN	MAX	MIN	MAX	
V <sub>OH</sub>	High-level output voltage, TTL-level signal (see Note 6)	V <sub>DD</sub> = MIN, I <sub>OH</sub> = MAX	0.9 × V <sub>DD</sub> ‡		2.4		V
V <sub>OL</sub>	Low-level output voltage, TTL-level signal	V <sub>DD</sub> = MAX, I <sub>OL</sub> = MAX	0.1 × V <sub>DD</sub> ‡		0.5		V
I <sub>OZ</sub>	High-impedance output current	V <sub>DD</sub> = MAX, V <sub>O</sub> = 0 V	10		10		μA
		V <sub>DD</sub> = MAX, V <sub>O</sub> = V <sub>DD</sub>	−10		−10		
I <sub>I</sub>	Input current, any input or input/output	V <sub>I</sub> = V <sub>SS</sub> to V <sub>DD</sub>	± 10		± 10		μA
I <sub>DD</sub>	Supply current	V <sub>DD</sub> = MAX	50		60		mA
C <sub>i</sub>	Input capacitance, any input§	f = 1 MHz, Others at 0 V	10		10		pF
C <sub>O</sub>	Output capacitance, any output or input/output§	f = 1 MHz, Others at 0 V	10		10		pF

† For conditions shown as MIN/MAX, use the appropriate value specified under the recommended operating conditions.

‡ Assured by SPICE IV Curve (see PCI specification revision 2.1, section 4.2, paragraph 2 for explanation)

§ Specified by design

NOTE 6: The following signals require an external pullup resistor:  $\overline{\text{PSERR}}$ ,  $\overline{\text{PINTA}}$ .

### recommended operating conditions (logic pins) (see Note 7)

	MIN	NOM	MAX	UNIT
V <sub>DD</sub> Supply voltage (5 V only)	4.75	5	5.25	V
V <sub>IH</sub> High-level input voltage	2		V <sub>DD</sub> + 0.3	V
V <sub>IL</sub> Low-level input voltage, TTL-level signal (see Note 4)	–0.3		0.8	V
I <sub>OH</sub> High-level output current	TTL outputs		–4	mA
I <sub>OL</sub> Low-level output current (see Note 5)	TTL outputs		4	mA

NOTES: 4. The algebraic convention, where the more negative (less positive) limit is designated as a minimum, is used for logic-voltage levels only.

5. Output current of 2 mA is sufficient to drive five low-power Schottky TTL loads or ten advanced low-power Schottky TTL loads (worst case).

7. Logic pins include V<sub>DDL</sub>, EAD[7:0], EXLE, EALE,  $\overline{\text{EOE}}$ , EDCLK, EDIO.

### electrical characteristics over recommended ranges of supply voltage (unless otherwise noted) (logic pins)

PARAMETER	TEST CONDITIONS †	MIN	NOM	MAX	UNIT
V <sub>OH</sub> High-level output voltage, TTL-level signal	V <sub>DD</sub> = MIN, I <sub>OH</sub> = MAX	2.4			V
V <sub>OL</sub> Low-level output voltage, TTL-level signal	V <sub>DD</sub> = MAX, I <sub>OL</sub> = MAX			0.5	V
I <sub>O</sub> High-impedance output current	V <sub>DD</sub> = MIN, V <sub>O</sub> = V <sub>DD</sub>			10	μA
	V <sub>DD</sub> = MIN, V <sub>O</sub> = 0 V			–10	
I <sub>I</sub> Input current	V <sub>I</sub> = V <sub>SS</sub> to V <sub>DD</sub>			± 10	μA
I <sub>DD</sub>	Supply current @ 25 MHz (PCLK)			190¶	mA
	Supply current @ 33 MHz (PCLK)			228¶	mA
C <sub>i</sub> Input capacitance, any input§	f = 1 MHz, Others at 0 V			10	pF
C <sub>O</sub> Output capacitance, any output or input/output§	f = 1 MHz, Others at 0 V			10	pF

† For conditions shown as MIN/MAX, use the appropriate value specified under the recommended operating conditions.

§ Specified by design

¶ Characterized in system test not tested



**recommended operating conditions (physical layer pins) (see Note 8)**

	MIN	NOM	MAX	UNIT
V <sub>DD</sub> Supply voltage	4.75	5	5.25	V

NOTE 8: Physical layer pins include V<sub>DDOSC</sub>, V<sub>DDR</sub>, V<sub>DDT</sub>, V<sub>DDVCO</sub>, ACOLN, ACOLP, ARCVN, ARCV, AXMTP, AXMTN, FATEST, FIREF, FRCVN, FRCVP, FXTL1, FXTL2, FXMTP, and FXMTN.

**electrical characteristics over recommended ranges of supply voltage (unless otherwise noted) (physical interface pins)**

**10 Base-T receiver input (FRCVP, FRCVN)**

PARAMETER	JEDEC SYMBOL	TEST CONDITIONS	MIN	MAX	UNIT
V <sub>I(DIFF)</sub> Differential input voltage†	V <sub>ID</sub>		0.6	2.8	V
I <sub>(CM)</sub> Common-mode current†	I <sub>IC</sub>			4	mA
V <sub>SQ+</sub> Rising input pair squelch threshold (see Note 9)		V <sub>CM</sub> = V <sub>SB</sub> , See Note 10		360	mV
V <sub>SQ-</sub> Falling input pair squelch threshold (see Note 9)		V <sub>CM</sub> = V <sub>SB</sub> , See Note 10	-360		mV

† See recommended operating conditions.

NOTES: 9. V<sub>SQ</sub> is the voltage at which input is assured to be seen as data.

10. V<sub>SB</sub> is the self-bias of the input FRCVP and FRCVN.

**10 Base-T transmitter drive characteristics (FXMTP, FXMTN)**

PARAMETER	JEDEC SYMBOL	TEST CONDITIONS	MIN	MAX	UNIT
V <sub>SLW</sub> Differential voltage at specified slew rate	V <sub>OD(SLEW)</sub>		± 2.2	± 2.8	V
V <sub>O(CM)</sub> Common-mode output voltage	V <sub>OC</sub>	See Figure 3d	0	4	V
V <sub>O(DIFF)</sub> Differential output voltage	V <sub>OD</sub>	Into open circuit		5.25	V
V <sub>O(I)</sub> Output idle differential voltage	V <sub>OD(IDLE)</sub>			± 50	mV
I <sub>O(FC)</sub> Output current, fault condition‡	I <sub>O(FC)</sub>			300	mA

‡ Specified by design

**AUI receiver input (ARCV, ARCVN, ACOLP, ACOLN)**

PARAMETER	JEDEC SYMBOL	TEST CONDITIONS	MIN	MAX	UNIT
V <sub>I(DIFF)1</sub> Differential input voltage 1†	V <sub>ID(1)</sub>	See Note 11	0	3	V
V <sub>I(DIFF)2</sub> Differential input voltage 2†	V <sub>ID(2)</sub>	See Note 12	0	100	mV
V <sub>(SQ)</sub> Falling input pair squelch threshold		See Note 13	-325		mV

† See recommended operating conditions.

NOTES: 11. Common-mode frequency range – 10 Hz to 40 kHz

12. Common-mode frequency range – 40 kHz to 10 MHz

13. Input bias over the common mode dc voltage range

**AUI transmitter drive characteristics (AXMTP, AXMTN)**

PARAMETER	JEDEC SYMBOL	TEST CONDITIONS	MIN	MAX	UNIT
V <sub>O(DIFF)1</sub> Differential output voltage†	V <sub>OD(1)</sub>	See Note 14	± 240	± 1300	mV
V <sub>OI(DIFF)</sub> Output idle differential voltage†	V <sub>OD(IDLE)</sub>			± 50	mV
V <sub>OI(DIFF)U</sub> Output differential undershoot‡	V <sub>OD(IDLE)U</sub>			100	mV
I <sub>O(FC)</sub> Output current, fault condition‡	I <sub>O(FC)</sub>			150	mA

† See recommended operating conditions.

‡ Specified by design

NOTE 14: The differential voltage is measured as per Figure 3b.

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### SINGLE-CHIP 10 BASE-T

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**electrical characteristics over recommended ranges of supply voltage (unless otherwise noted)  
(physical interface pins) (continued)**

#### crystal-oscillator characteristics

PARAMETER	JEDEC SYMBOL	TEST CONDITIONS	MIN	MAX	UNIT
V <sub>SB(FXTL1)</sub> Input self-bias voltage	V <sub>IB</sub>		1.7	2.8	V
I <sub>OH(FXTL2)</sub> High-level output current	I <sub>OH</sub>	V <sub>(FXTL2)</sub> = V <sub>SB(FXTL1)</sub> V <sub>(FXTL1)</sub> = V <sub>SB(FXTL1)</sub> + 0.5 V	– 1.3	– 5.0	mA
I <sub>OL(FXTL2)</sub> Low-level output current	I <sub>OL</sub>	V <sub>(FXTL2)</sub> = V <sub>SB(FXTL1)</sub> V <sub>(FXTL1)</sub> = V <sub>SB(FXTL1)</sub> – 0.5 V	– 0.4	1.5	mA

#### PARAMETER MEASUREMENT INFORMATION

Outputs are driven to a minimum high-logic level of 2.4 V and to a maximum low-logic level of 0.6 V. These levels are compatible with TTL devices.

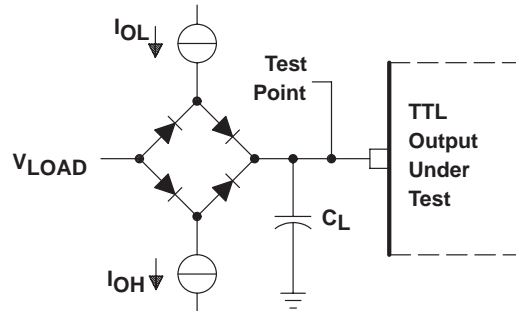
Output transition times are specified as follows: For a high-to-low transition on either an input or output signal, the level at which the signal is said to be no longer high is 2 V and the level at which the signal is said to be low is 0.8 V. For a low-to-high transition, the level at which the signal is said to be no longer low is 0.8 V and the level at which the signal is said to be high is 2 V, as shown below.

The rise and fall times are not specified but are assumed to be those of standard TTL devices, which are typically 1.5 ns.

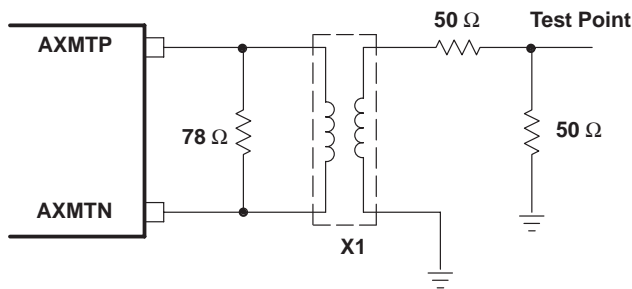


## test measurement

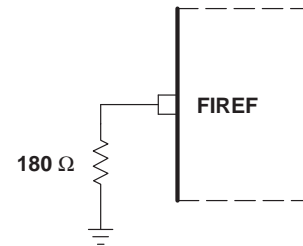
The test-load circuit shown in Figure 3 represents the programmable load of the tester pin electronics that are used to verify timing parameters of the TNETE110A output signals.



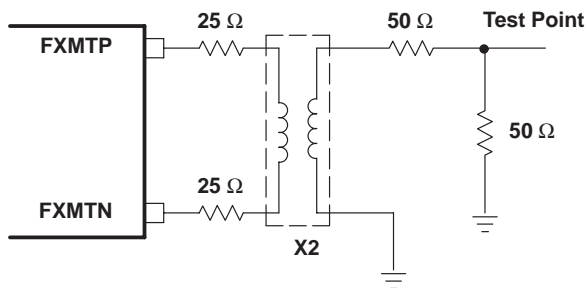
(a) TTL OUTPUT TEST LOAD



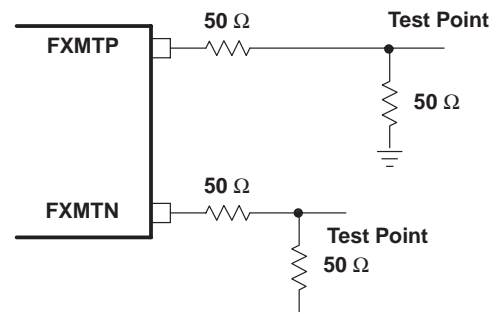
(b) AXMTP AND AXMTN TEST LOAD (AC TESTING)  
X1–Fil–Mag 23Z90(1:1)



(c) FIREF TEST CIRCUIT



(d) FXMTP AND FXMTN TEST LOAD (AC TESTING)  
X2–Fil–Mag 23Z128(1:√2)



(e) FXMTP and FXMTN TEST LOAD (DC TESTING)

Where:  $I_{OL}$  = Refer to  $I_{OL}$  in recommended operating conditions  
 $I_{OH}$  = Refer to  $I_{OH}$  in recommended operating conditions  
 $V_{LOAD}$  = 1.5 V, typical dc-level verification or  
0.7 V, typical timing verification  
 $C_L$  = 18 pF, typical load-circuit capacitance

Figure 3. Test and Load Circuit

# ThunderLAN™ TNETE110A

## PCI ETHERNET™ CONTROLLER

### SINGLE-CHIP 10 BASE-T

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#### switching characteristics, PCI 5-V and 3.3-V (see Note 15 and Figure 3 and Figure 4)

PARAMETER		MIN	MAX	UNIT
t <sub>VAL</sub>	Delay time, PCLK to bused signals valid (see Notes 16 and 17) <sup>†</sup>	2	11	ns
t <sub>VAL(PTP)</sub>	Delay time, PCLK to bused signals valid point-to-point (see Notes 16 and 17)	2	12	ns
t <sub>on</sub>	Float-to-active delay	2		ns
t <sub>off</sub>	Active-to-float delay		28	ns

<sup>†</sup> Characterized by design

NOTES: 15. Some of the timing symbols in this table are not currently listed with EIA or JEDEC standards for semiconductor symbology but are consistent with the PCI Local-Bus Specification, Revision 2.0.

16. Minimum times are measured with a 0-pF equivalent load; maximum times are measured with a 50-pF equivalent load. Actual test capacitance may vary, but results should be correlated to these specifications.

17.  $\overline{\text{PREQ}}$  and  $\overline{\text{PGNT}}$  are point-to-point signals, and have different output valid delay and input setup times than do bused signals.  $\overline{\text{PGNT}}$  has a setup time of 10 ns;  $\overline{\text{PREQ}}$  has a setup time of 12 ns. All other signals are bused.

#### timing requirements, PCI 5-V and 3.3-V (see Note 15 and Figure 4)

		MIN	MAX	UNIT
t <sub>su</sub>	Setup time, bused signals valid to PCLK (see Note 17)	7		ns
t <sub>su(PTP)</sub>	Setup time to PCLK—point-to-point (see Note 17)	10, 12		ns
t <sub>h</sub>	Input hold time from PCLK	0		ns
t <sub>c</sub>	Cycle time, PCLK (see Note 18)	30	500 <sup>‡</sup>	ns
t <sub>w(H)</sub>	Pulse duration, PCLK high	12		ns
t <sub>w(L)</sub>	Pulse duration, PCLK low	12		ns
t <sub>slew</sub>	Slew rate, PCLK (see Note 19) <sup>‡</sup>	1	4	V/ns

<sup>‡</sup> Specified by design and system specification.

NOTES: 15. Some of the timing symbols in this table are not currently listed with EIA or JEDEC standards for semiconductor symbology but are consistent with the PCI Local-Bus Specification, Revision 2.0.

17.  $\overline{\text{PREQ}}$  and  $\overline{\text{PGNT}}$  are point-to-point signals, and have different output valid delay and input setup times than do bused signals.  $\overline{\text{PGNT}}$  has a setup time of 10 ns;  $\overline{\text{PREQ}}$  has a setup time of 12 ns. All other signals are bused.

18. As a requirement for frame transmission/reception, the minimum PCLK frequency varies with network speed. The clock may only be stopped in a low state.

19. Rise and fall times are specified in terms of the edge rate measured in V/ns. This slew rate must be met across the minimum peak-to-peak portion of the clock waveform.





timing requirements, PCI 5-V and 3.3-V (see Note 15 and Figure 4) (continued)

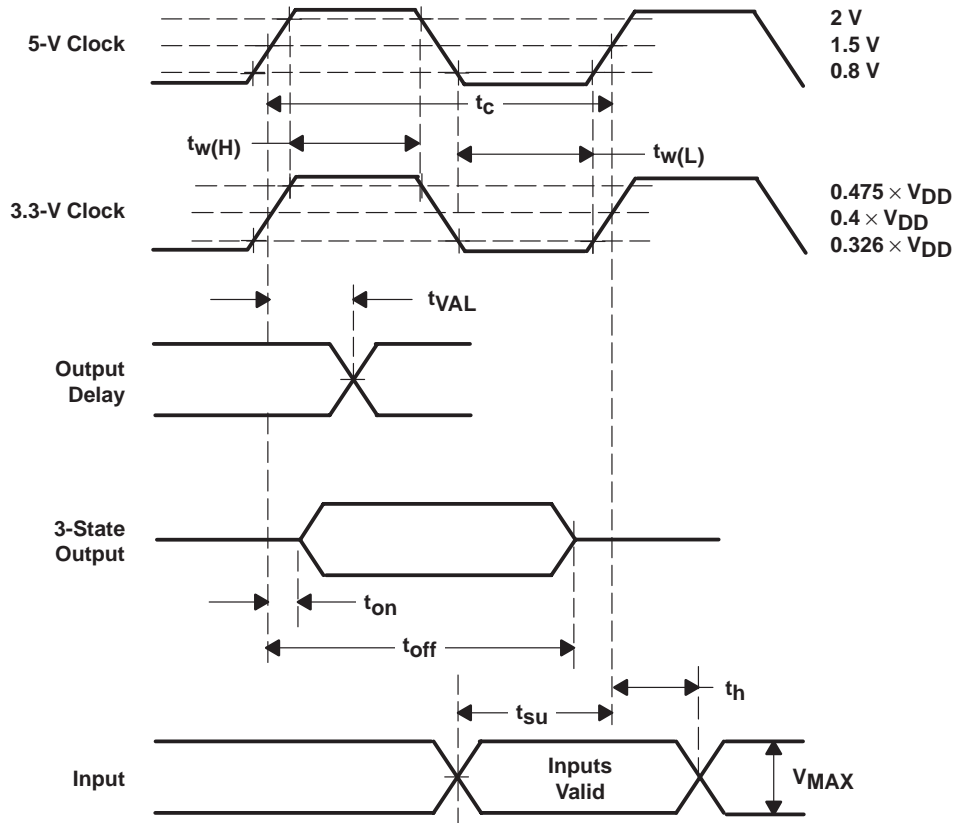


Figure 4. PCI 5-V and 3.3-V Timing

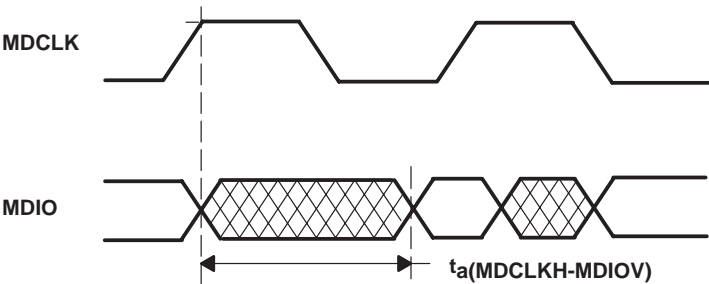
**timing requirements for management data I/O (MDIO) (see Figure 3 and Figure 5)**

	MIN	MAX	UNIT
$t_a(\text{MDCLKH-MDIOV})$ Access time, MDIO valid from MDCLK high (see Note 20)	0	300	ns

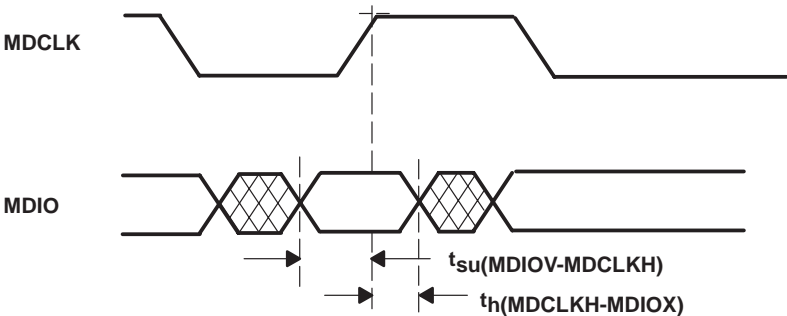
**switching characteristics for management data I/O (MDIO) (see Figure 6)**

PARAMETER	MIN	MAX	UNIT
$t_{su}(\text{MDIOV-MDCLKH})$ Setup time, MDIO valid to MDCLK high (see Note 21)	10		ns
$t_h(\text{MDCLKH-MDIOX})$ Hold time, MDCLK high to MDIO changing (see Note 21)	10		ns

NOTES: 20. When the MDIO signal is sourced by the PMI/PHY, it is sampled by TNETE110A synchronous to the rising edge of MDCLK.  
21. MDIO is a bidirectional signal that can be sourced by TNETE110A or the PMI/PHY. When TNETE110A sources the MDIO signal, TNETE110A asserts MDIO synchronous to the rising edge of MDCLK.



**Figure 5. Management Data I/O Timing (Sourced by PHY)**



**Figure 6. Management Data I/O Timing (Sourced by TNETE110A)**

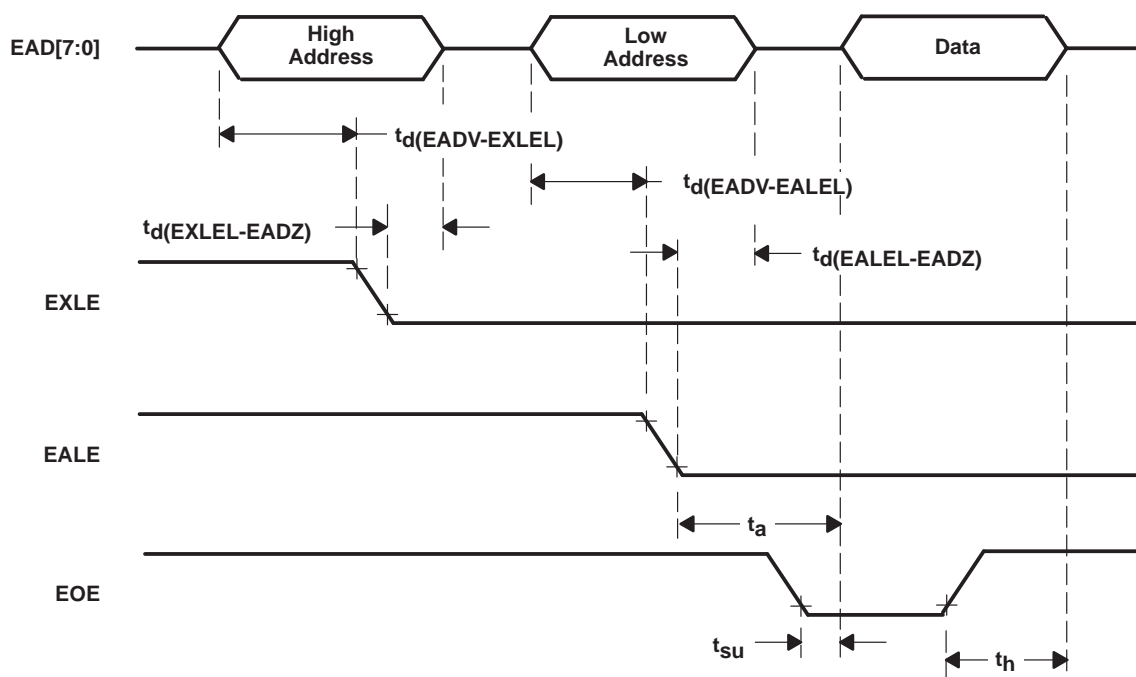
**timing requirements, BIOS ROM and LED interface (see Figure 3 and Figure 7)†**

		MIN	MAX	UNIT
$t_{su}$	Setup time, data		250	ns
$t_h$	Hold time, data	0		ns

**switching characteristics, BIOS ROM and LED interface (see Figure 7)†**

PARAMETER		MIN	MAX	UNIT
$t_d(\text{EADV-EXLEL})$	Delay time, address high byte valid to EXLE low (address high byte setup time for external latch)	0		ns
$t_d(\text{EXLEL-EADZ})$	Delay time, EXLE low to address high byte invalid (address high byte hold time for external latch)	10		ns
$t_d(\text{EADV-EALEL})$	Delay time, address low byte valid to EALE low (address low byte setup time for external latch)	0		ns
$t_d(\text{EALEL-EADZ})$	Delay time, EALE low to address low byte invalid (address low byte hold time for external latch)	10		ns
$t_a$	Access time, address	288		ns

† The EPROM interface, consisting of 11 pins, requires only two TTL '373 latches to latch the high and low addresses.



**Figure 7. BIOS ROM and LED Interface Timing**

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#### switching characteristics, configuration EEPROM interface (see Figure 3 and Figure 8)

PARAMETER		MIN	MAX	UNIT
$f_{CLK}(EDCLK)$	Clock frequency, EDCLK	0	100	kHz
$t_d(EDCLKL-EDIOV)$	EDCLK low to EDIO data in valid	0.3	3.5	$\mu s$
$t_d(EDIO \text{ free})$	Time the bus must be free before a new transmission can start	4.7		$\mu s$
$t_d(EDIOV-EDCLKL)$	Delay time, EDIO valid after EDCLK low (start condition hold time for EEPROM)	4		$\mu s$
$t_w(L)$	Low period, clock	4.7		$\mu s$
$t_w(H)$	High period, clock	4		$\mu s$
$t_d(EDCLKH-EDIOV)$	Delay time, EDCLK high to EDIO valid (start condition setup time)	4.7		$\mu s$
$t_d(EDCLKL-EDIOX)$	Delay time, EDCLK low to EDIO changing (data out hold time)	0		$\mu s$
$t_d(EDIOV-EDCLKH)$	Delay time, EDIO valid to EDCLK high (data out setup time)	250		ns
$t_r$	Rise time, EDIO and EDCLK		1	$\mu s$
$t_f$	Fall time, EDIO and EDCLK		300	ns
$t_d(EDCLKH-EDIOH)$	Delay time, EDCLK high to EDIO high (stop condition setup time)	4.7		$\mu s$
$t_d(EDCLKL-EDIOX)$	Delay time, EDCLK low to EDIO changing (data in hold time)	300		ns

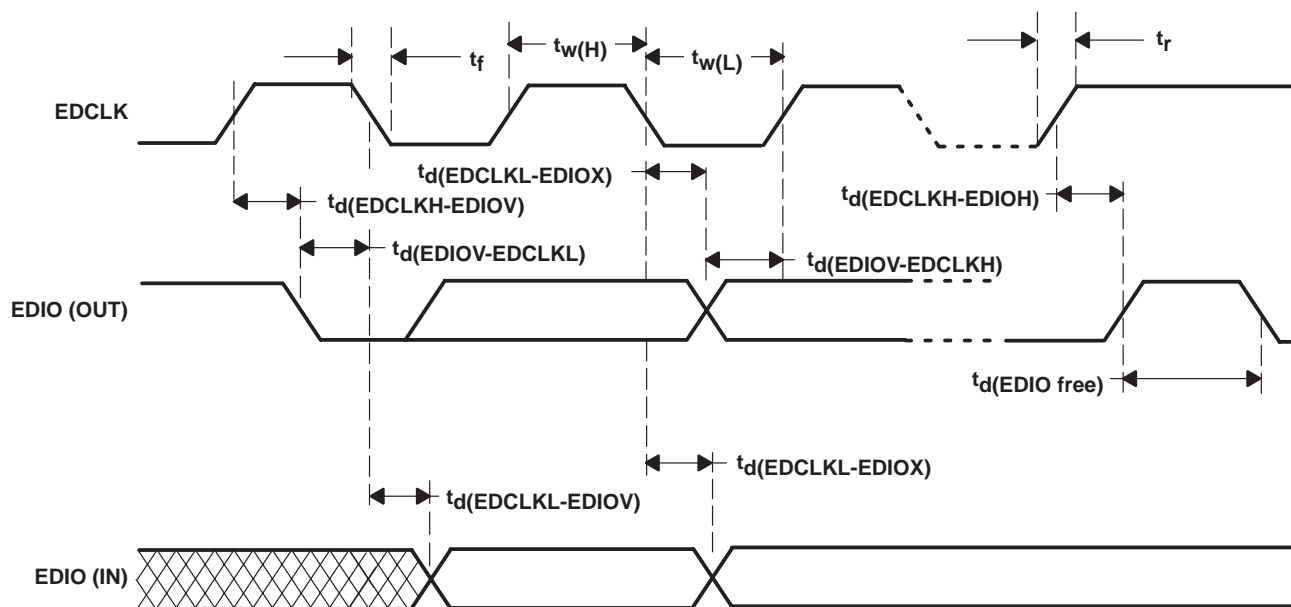


Figure 8. Configuration EEPROM Interface Timing

timing requirements, crystal oscillator (see Figure 9)<sup>†</sup>

		MIN	TYP	MAX	UNIT
$t_d(VDDH-FXTL1V)$	Delay time from minimum $V_{DD}$ high level to first valid FXTL1V full swing period			100 <sup>‡</sup>	ms
$t_w(H)$	Pulse duration at FXTL1 high	13 <sup>‡</sup>			ns
$t_w(L)$	Pulse duration at FXTL1 low	13 <sup>‡</sup>			ns
$t_t$	Transition time of FXTL1		7		ns
$t_c$	Cycle time, FXTL1		50		ns
	Tolerance of FXTL1 input frequency		± 0.01		%

<sup>†</sup> The FXTL signal may be implemented by either connecting a 20-MHz crystal across the FXTL1 and FXTL2 pins or by driving the FXTL1 from a 20-MHz crystal oscillator module.

<sup>‡</sup> This specification is provided as an aid to board design. This specification is not tested during manufacturing testing.

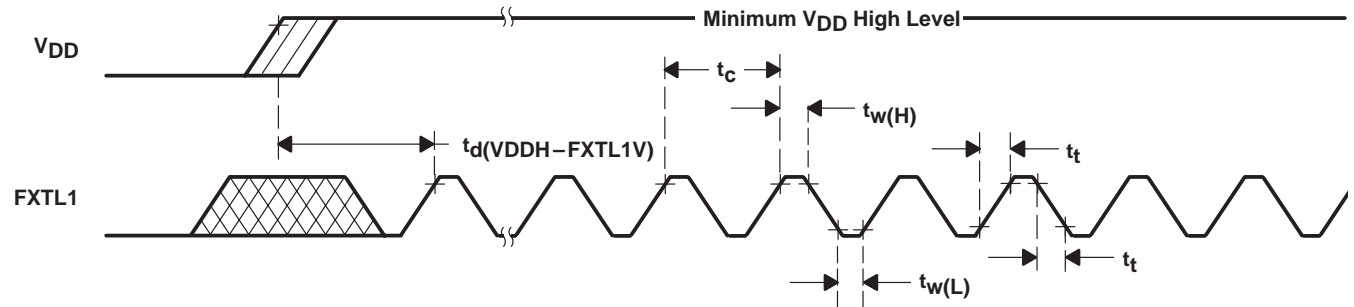


Figure 9. Crystal Oscillator Timing

# ThunderLAN™ TNETE110A

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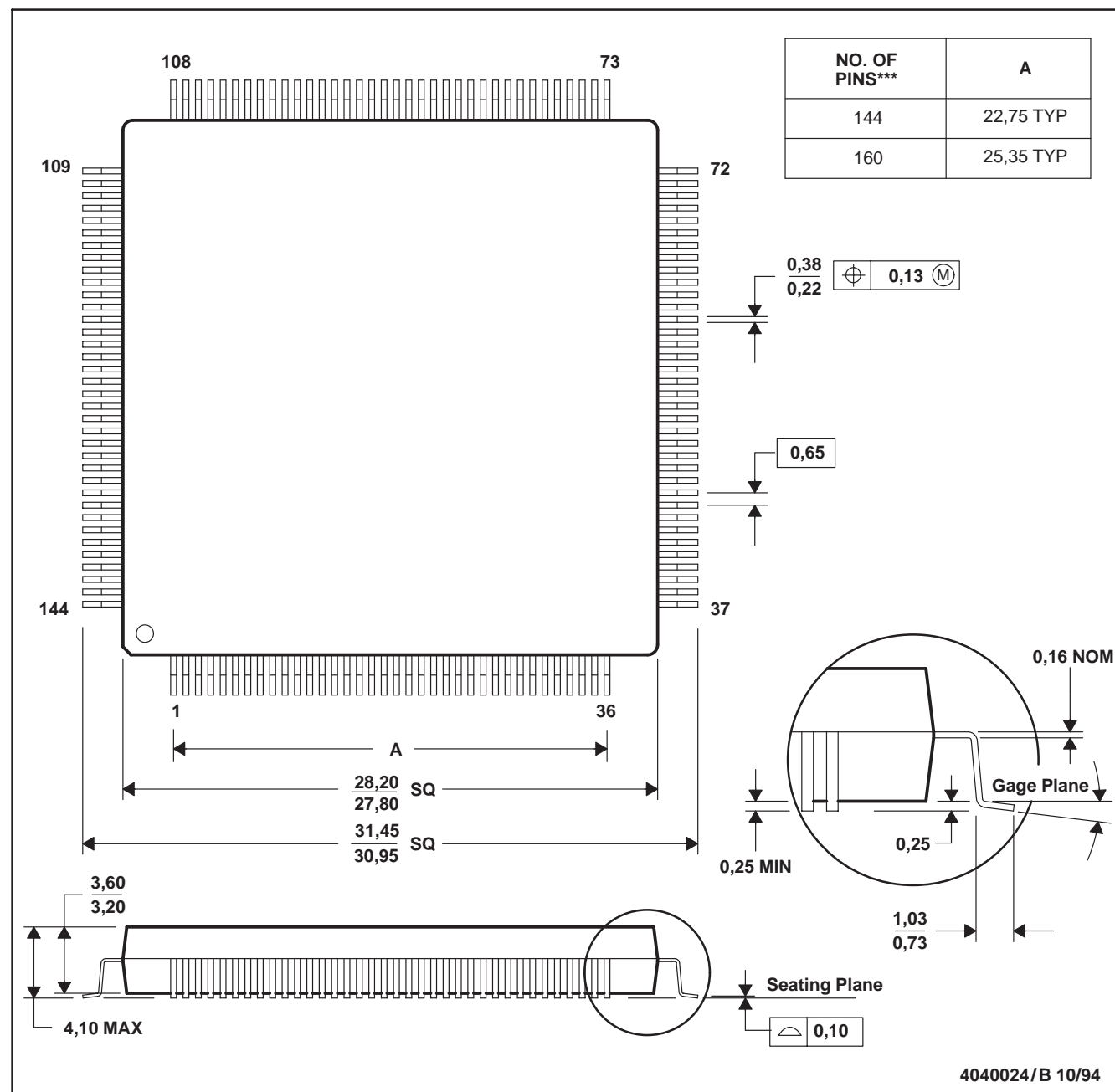
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#### MECHANICAL DATA

PCM (S-PQFP-G\*\*\*)

144 PIN SHOWN

PLASTIC QUAD FLATPACK

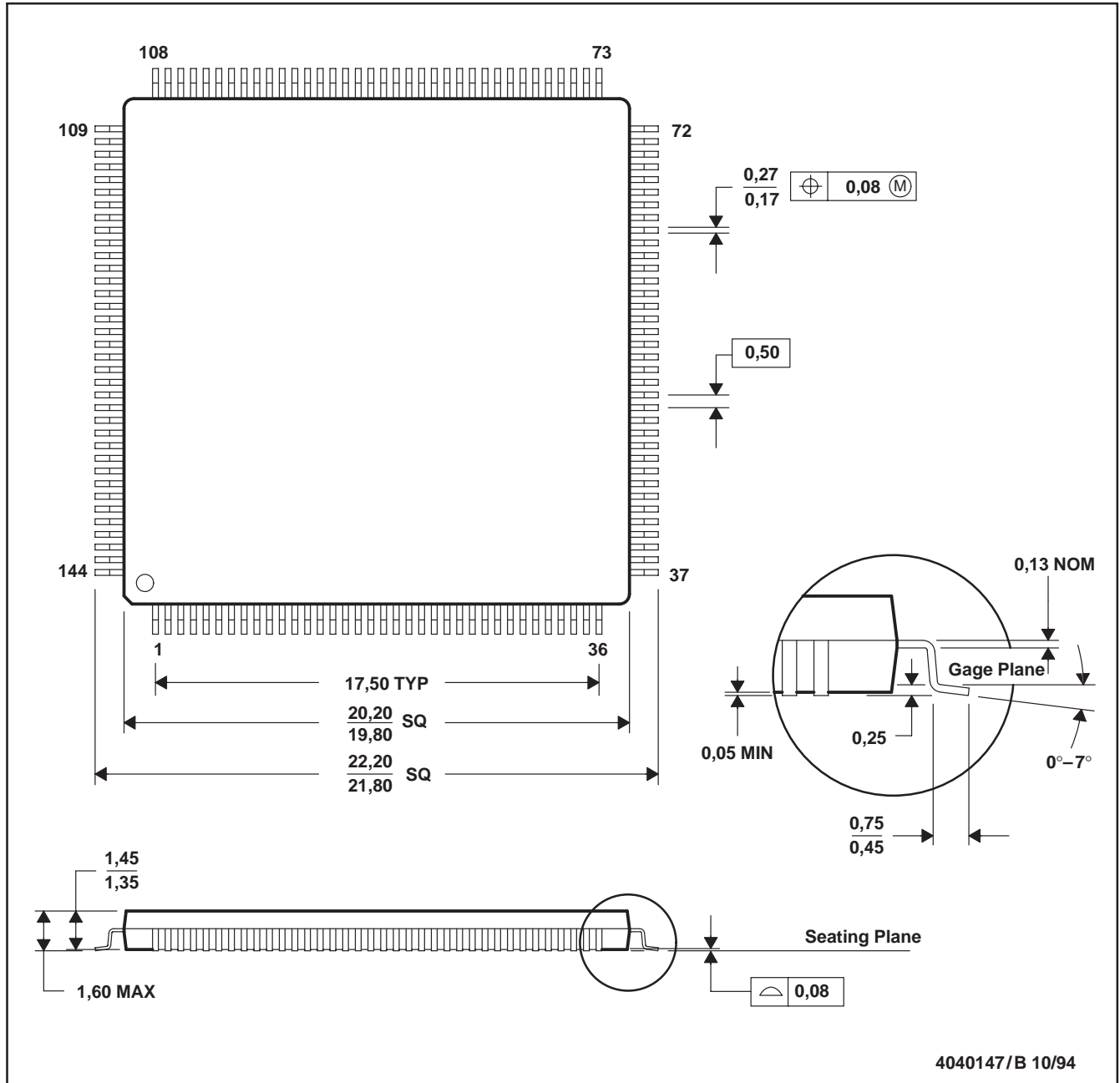


- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Falls within JEDEC MS-022
  - D. The 144 PCM is identical to the 160 PCM except that four leads per corner are removed.

## MECHANICAL DATA

PGE (S-PQFP-G144)

PLASTIC QUAD FLATPACK



- NOTES: A. All linear dimensions are in millimeters.  
B. This drawing is subject to change without notice.  
C. Falls within JEDEC MO-136

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