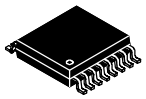
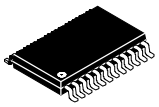



QUAD HIGH-SPEED DIFFERENTIAL RECEIVERS

FEATURES

- **Meets or Exceeds the Requirements of ANSI TIA/EIA-644A Standard**
- **Single-Channel Signaling Rates up to 560 Mbps**
- **-4 V to 5 V Common-Mode Input Voltage Range**
- **Flow-Through Architecture**
- **Active Failsafe Assures a High-level Output When an Input Signal Is not Present**
- **SN65LVDS348 Provides a Wide Common-Mode Range Replacement for the SN65LVDS048A or the DS90LV048A**

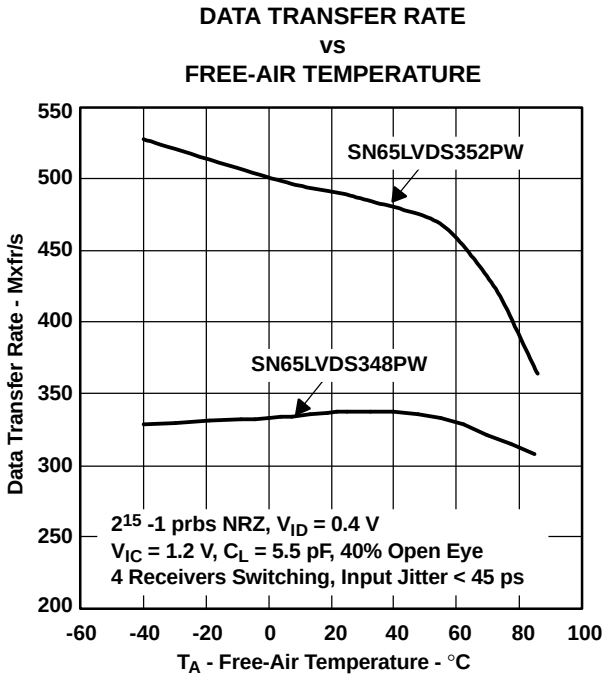
APPLICATIONS

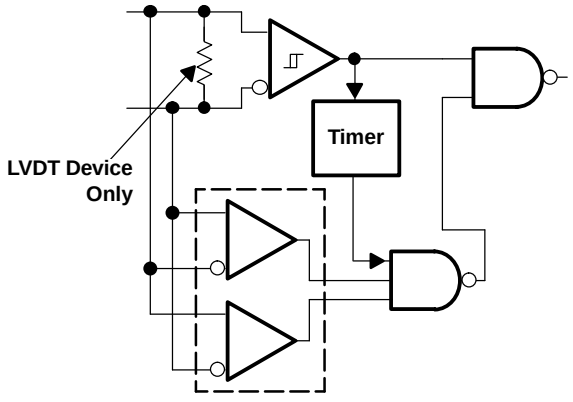
- **Logic Level Translator**
- **Point-to-Point Baseband Data Transmission Over 100-Ω Media**
- **ECL/PECL-to-LVTTL Conversion**
- **Wireless Base Stations**
- **Central Office or PABX Switches**

DESCRIPTION

The SN65LVDS348, SN65LVDT348, SN65LVDS352, and SN65LVDT352 are high-speed, quadruple differential receivers with a wide common-mode input voltage range. This allows receipt of TIA/EIA-644 signals with up to 3-V of ground noise or a variety of differential and single-ended logic levels. The '348 is in a 16-pin package to match the industry-standard footprint of the DS90LV048. The '352 adds two additional V_{CC} and GND pins in a 24-pin package to provide higher data transfer rates with multiple receivers in operation. All offer a flow-through architecture with all inputs on one side and outputs on the other to ease board layout and reduce crosstalk between receivers. LVDT versions of both integrate a 110-Ω line termination resistor.

These receivers also provide 3x the standard's minimum common-mode noise voltage tolerance. The -4 V to 5 V common-mode range allows usage in harsh operating environments or accepts LVPECL, PECL, LVECL, ECL, CMOS, and LVCMOS levels without level shifting circuitry. See the Application Information Section for more details on the ECL/PECL to LVDS interface.





(One of Four Shown)

DESCRIPTION (CONTINUED)

Precise control of the differential input voltage thresholds allows for inclusion of 50 mV of input-voltage hysteresis to improve noise rejection. The differential input thresholds are still no more than ±50 mV over the full input common-mode voltage range.

The receiver inputs can withstand ±15 kV human-body model (HBM), with respect to ground, without damage. This provides reliability in cabled and other connections where potentially damaging noise is always a threat.

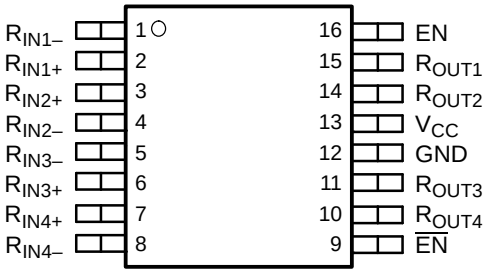
The receivers also include a (patent-pending) failsafe circuit that provides a high-level output approximately 600 ns after loss of the input signal. The most common causes of signal loss are disconnected cables, shorted lines, or powered-down transmitters. This prevents noise from being received as valid data under these fault conditions. This feature may also be used for Wired-Or bus signaling.

The SN65LVDT348 and SN65LVDT352 include an integrated termination resistor. This reduces board space requirements and parts count by eliminating the need for a separate termination resistor. This can also improve signal integrity at the receiver by reducing the stub length from the line termination to the receiver.

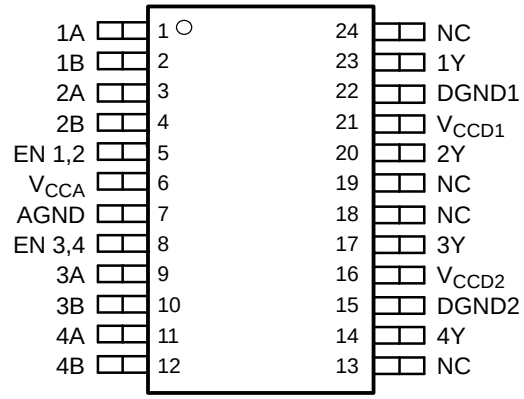
The intended application of these devices and signaling technique is for point-to-point baseband data transmission over controlled impedance media of approximately 100 Ω. The transmission media may be printed-circuit board traces, backplanes, or cables. The ultimate rate and distance of data transfer is dependent upon the attenuation characteristics of the media and the noise coupling to the environment.

The SN65LVDS348, SN65LVDT348, SN65LVDS352 and SN65LVDT352 are characterized for operation from -40°C to 85°C.

SN65LVDS348, SN65LVDT348
D or PW PACKAGE
(TOP VIEW)

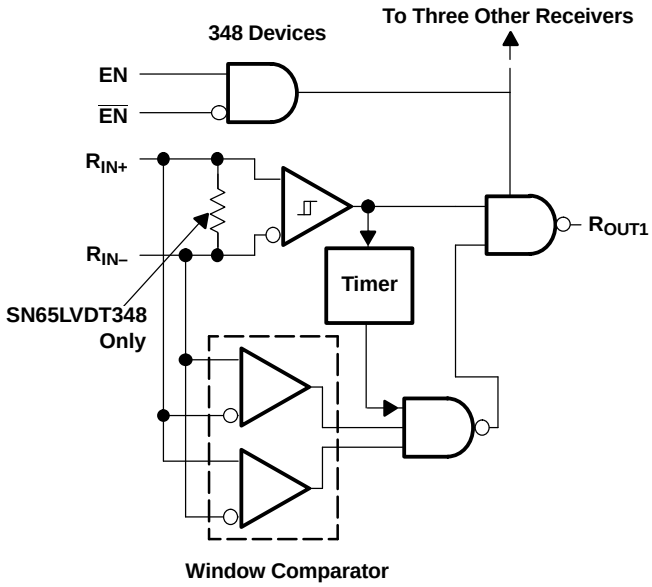


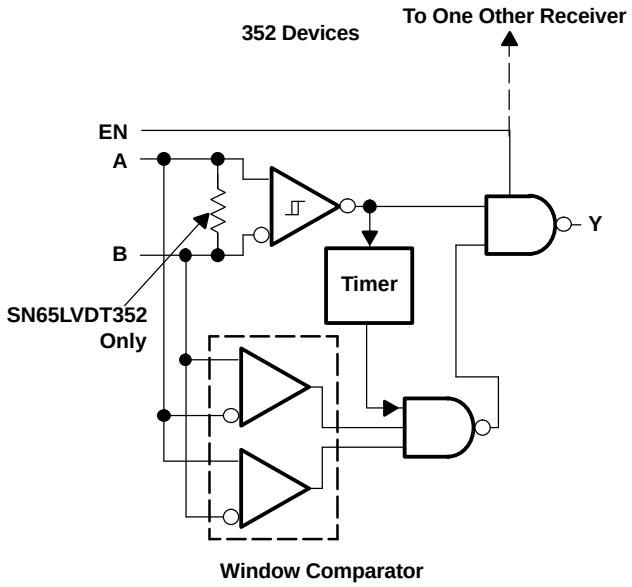
SN65LVDS352, SN65LVDT352
PW PACKAGE
(TOP VIEW)



NC – No internal connection

FUNCTIONAL BLOCK DIAGRAMS (one of four receivers shown)





AVAILABLE OPTIONS

PART NUMBER(1)	INTEGRATED TERMINATION	PACKAGE TYPE	PACKAGE MARKING
SN65LVDS348D		SOIC	LVDS348
SN65LVDT348D	√	SOIC	LVDT348
SN65LVDS348PW		TSSOP	DL348
SN65LVDT348PW	√	TSSOP	DE348
SN65LVDS352PW		TSSOP	DL352
SN65LVDT352PW	√	TSSOP	DE352

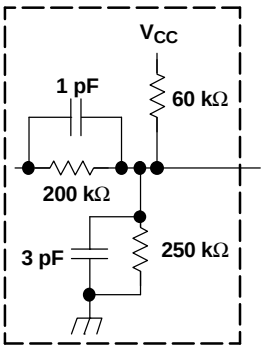
(1) Add the R suffix to the device type (e.g., SN65LVDS348DR) for taped and reeled carrier.

FUNCTION TABLES

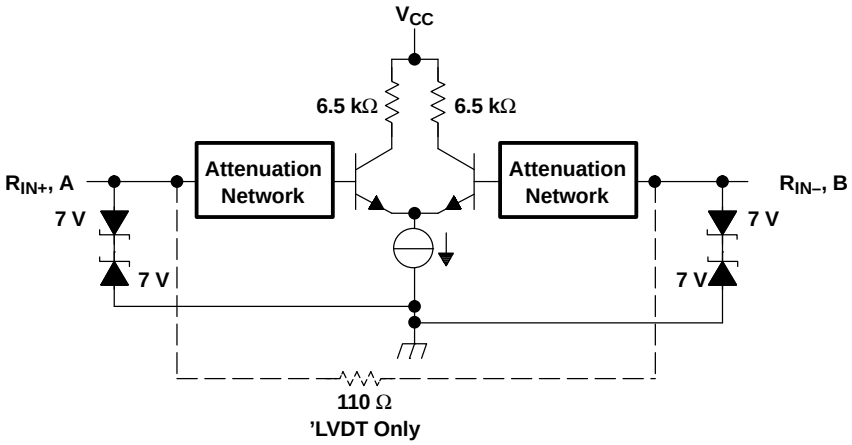
348 DEVICES			
INPUTS			OUTPUTS
$V_{ID} = V_{RIN+} - V_{RIN-}$	EN	$\overline{EN}$	R_{OUT}
$V_{ID} \geq$ -32 mV	H	L or OPEN	H
100 mV < V_{ID} < -32 mV	H	L or OPEN	?
$V_{ID} \leq$ -100 mV	H	L or OPEN	L
Open	H	L or OPEN	H
X	L or OPEN	X	Z
	X	H	Z

352 DEVICES		
INPUTS		OUTPUTS
$V_{ID} = V_{IA} - V_{IB}$	EN	Y
$V_{ID} \geq$ -32 mV	H	H
100 mV < V_{ID} < -32 mV	H	?
$V_{ID} \leq$ -100 mV	H	L
X	L or OPEN	Z
Open	H	H

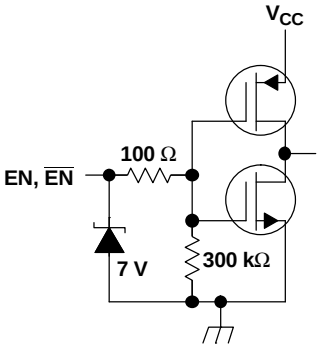
EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS

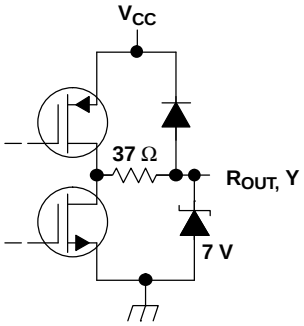


Attenuation Network



'LVDT Only





ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

			UNIT
Supply voltage range(2), V_{CC},V_{CCA},V_{CCD1}, and V_{CCD2}			-0.5 V TO 4 V
Voltage range	Enables, R_{OUT}, or Y		-0.5 V to 6 V
	Differential input magnitude $MV_{ID}M$ (LVDT only)		1 V
	R_{IN+}, R_{IN-}, A or B		-5 V to 6 V
Electrostatic discharge	Human body model(3)	A, B, R_{IN+}, R_{IN-} and GND	±15 kV
		All pins	±7 kV
	Charged-device model(4)	All pins	±500 V
Continuous power dissipation			See Dissipation Rating Table
Storage temperature range			-65°C to 150°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal (GND, AGND).
(3) Tested in accordance with JEDEC Standard 22, Test Method A114-A.
(4) Tested in accordance with JEDEC Standard 22, Test Method C101.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	OPERATING FACTOR(1) ABOVE $T_A = 25°C$	$T_A = 85°C$ POWER RATING
D16	950 mW	7.6 mW/°C	494 mW
PW16	774 mW	6.2 mW/°C	402 mW
PW24	1087 mW	8.7 mW/°C	565 mW

(1) This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.

RECOMMENDED OPERATING CONDITIONS

			MIN	NOM	MAX	UNIT
V_{CC},V_{CCA},V_{CCD1}, and V_{CCD2}	Supply voltage		3	3.3	3.6	V
V_{IH}	High-level input voltage	Enables	2		5	V
V_{IL}	Low-level input voltage	Enables	0		0.8	V
	Magnitude of differential input voltage	$\|V_{ID}\|$ (LVDT348, 352)	0.1		0.8	V
		$\|V_{ID}\|$ (LVDS348, 352)	0.1		3	
	Input voltage (any combination of common mode or input signals)		-4		5	V
T_A	Operating free-air temperature		-40		85	°C

ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
V_{ITH1}	Positive-going differential input voltage threshold		See Figure 1 and Figure 2			50	mV
V_{ITH2}	Negative-going differential input voltage threshold			-50			
V_{ITH3}	Differential input failsafe voltage threshold		See Figure 1 and Table 1	-32		-100	mV
$V_{ID(HYS)}$	Differential input voltage hysteresis, V_{ITH1} - V_{ITH2}				50		mV
V_{OH}	High-level output voltage		I_{OH} = -4 mA	2.4			V
V_{OL}	Low-level output voltage		I_{OL} = 4 mA			0.4	V
I_{CC}	Supply current	LVDS348, LVDT348	Enabled, EN at V_{CC}, $\overline{EN}$ at 0 V, No load		16	20	mA
			Disabled, EN at 0 or $\overline{EN}$ at V_{CC}		1.1	4	
		LVDS352, LVDT352	Enabled, EN at V_{CC}, No load		16	20	mA
			Disabled, EN at 0		1.1	4	
I_I	Input current (RIN+, RIN-, A or B inputs)	LVDS348, LVDS352	V_I = -4 V, Other input open	-75		0	µA
			0 V ≤ V_I ≤ 2.4 V, Other input 1.2 V	-20		0	
			V_I = 5 V, Other input open	0		40	
		LVDT348, LVDT352	V_I = -4 V, Other input open	-150		0	µA
			0 V ≤ V_I ≤ 2.4 V, Other input open	-40		0	
			V_I = 5 V, Other input open	0		80	
$I_{I(OFF)}$	Power-off input current (RIN+, RIN-, A or B inputs)	LVDS348, LVDS352	V_{CC} = 1.5 V, V_I = -4 V or 5 V, Other input open	-50		50	µA
			V_{CC} = 1.5 V, 0 V ≤ V_I≤ 2.4 V, Other input at 1.2 V	-20		20	
		LVDT348, LVDT352	V_{CC} = 1.5 V, V_I = -4 V or 5 V, Other input open	-100		100	µA
			V_{CC} = 1.5 V, V_I = 0 V or 2.4 V, Other input open	-40		40	
I_{ID}	Differential input current (I_{RIN+} - I_{RIN-}, or I_{IA} - I_{IB})	LVDS348, LVDS352	V_{ID} = 100 mV, V_{IC} = -3.9 V or 4.9 V	-4		4	µA
R_T	Differential input resistance	LVDT348, LVDT352	V_{CC} = 0 V, V_{ID} = 250 mV, V_I = 0 V or 2.4 V	90	111	132	Ω
I_{IH}	High-level input current	Enables	V_{IH} = 2 V	0		10	µA
I_{IL}	Low-level input current	Enables	V_{IL} = 0.8 V	0		10	µA
I_{OZ}	High-impedance output current		V_O = 0 V	-10		10	µA
C_{IN}	Input capacitance, R_{IN+}, R_{IN-} input to GND or A or B input to AGND		V_I = 0.4 sin (4E6πft) + 0.5 V		5		pF

(1) All typical values are at 25°C and with a 3.3-V supply.

SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 10 pF, See Figure 3	2.5	4	6	ns
t_{PHL}	Propagation delay time, high-to-low-level output		2.5	4	6	ns
t_{d1}	Delay time, failsafe disable time				12	ns
t_{d2}	Delay time, failsafe enable time		0.3		1.5	µs
$t_{sk(p)}$	Pulse skew ($\lvert t_{pHL1} - t_{pLH1} \rvert$)			200		ps
$t_{sk(o)}$	Output skew(2)			150		ps
$t_{sk(pp)}$	Part-to-part skew(3)				1	ns
t_r	Output signal rise time			1.2		ns
t_f	Output signal fall time			1		ns
t_r	Output signal rise time	C_L = 1 pF, See Figure 3		650		ps
t_f	Output signal fall time			400		ps
t_{PHZ}	Propagation delay time, high-level-to-high-impedance output	See Figure 4 and Figure 5		5	9	ns
t_{PLZ}	Propagation delay time, low-level-to-high-impedance output			5	9	ns
t_{PZH}	Propagation delay time, high-impedance-to-high-level output			8	12	ns
t_{PZL}	Propagation delay time, high-impedance-to-low-level output			8	12	ns

(1) All typical values are at 25°C and with a 3.3-V supply.
(2) $t_{sk(o)}$ is the magnitude of the time difference between the t_{PHL} or t_{PLH} of all receivers of a single device with all of their inputs connected together.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

PARAMETER MEASUREMENT INFORMATION

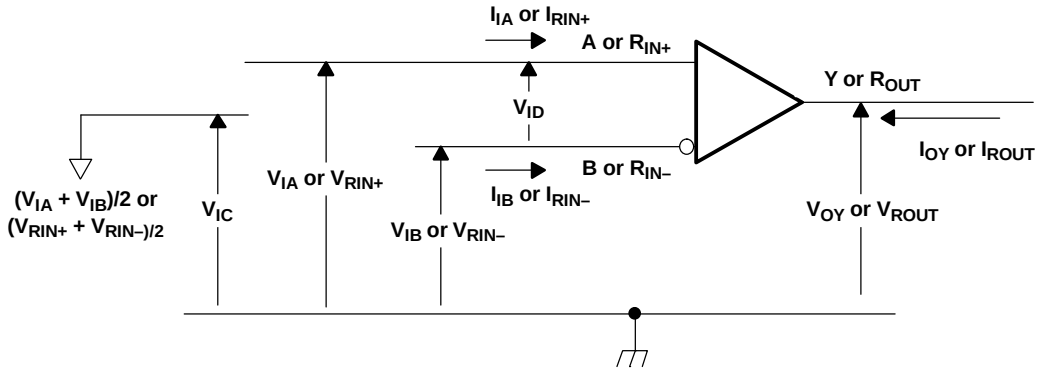
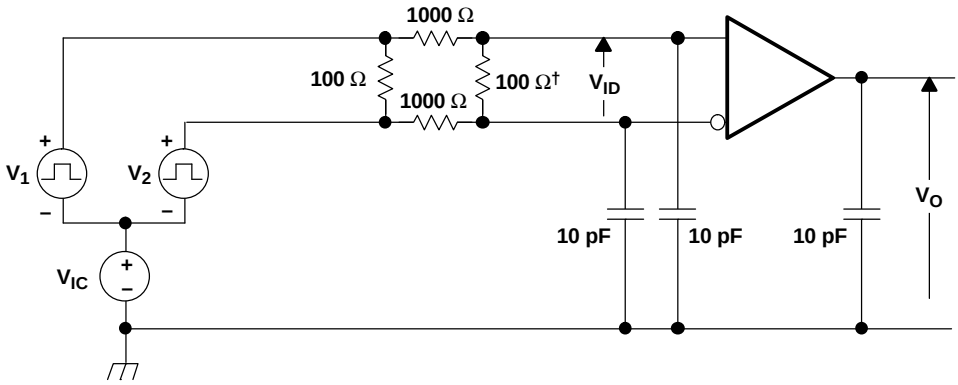


Figure 1. Voltage and Current Definitions

PARAMETER MEASUREMENT INFORMATION (continued)



A. Remove for testing LVDT device.

B. Input signal of 3 MHz, duty cycle of 50±0.2%, and transition time of < 1ns.

C. Fixture capacitance ±20%.

D. Resistors are metal film, 1% tolerance, and surface mount

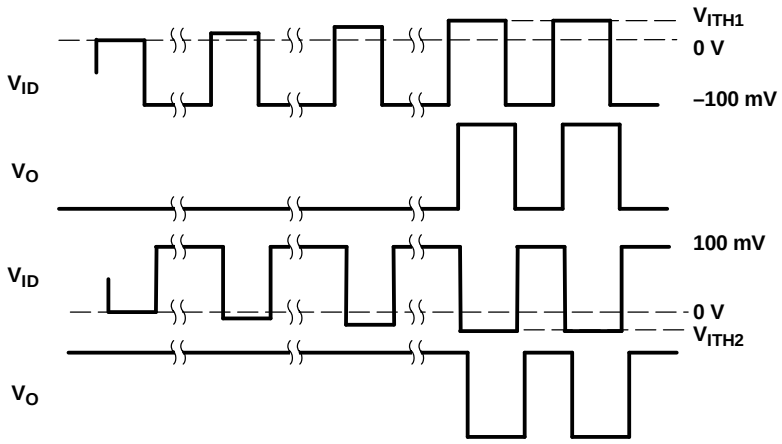
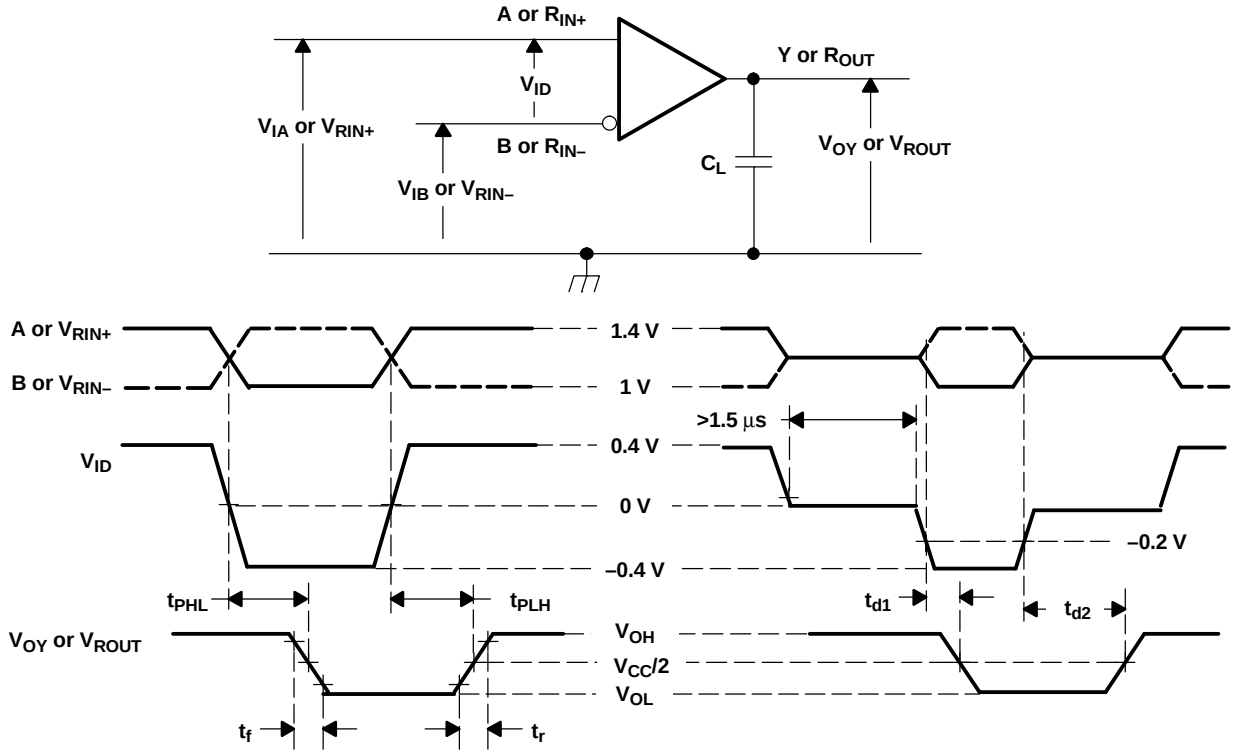


Figure 2. V_{ITH1} and V_{ITH2}, Input Voltage Threshold Test Circuit and Definitions

Table 1. Receiver Minimum and Maximum Failsafe Input Voltage

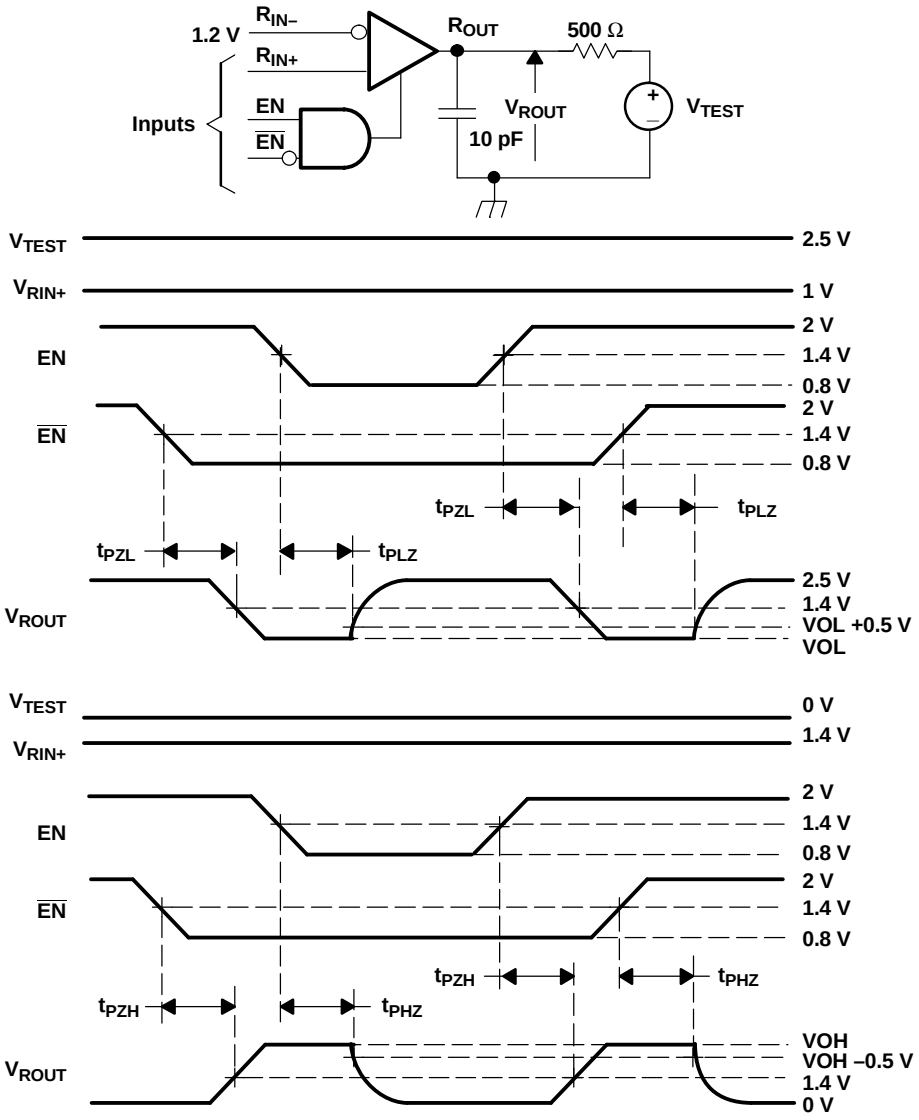
FAILSAFE THRESHOLD TEST VOLTAGES				
APPLIED VOLTAGES(1)		RESULTANT INPUTS		Output
V_{IA} (mV)	V_{IB} (mV)	V_{ID} (mV)	V_{IC} (mV)	
-4000	-3900	-100	-3950	L
-4000	-3968	-32	-3984	H
4900	5000	-100	4950	L
4968	5000	-32	4984	H

(1) Voltage applied for greater than 1.5 µs.



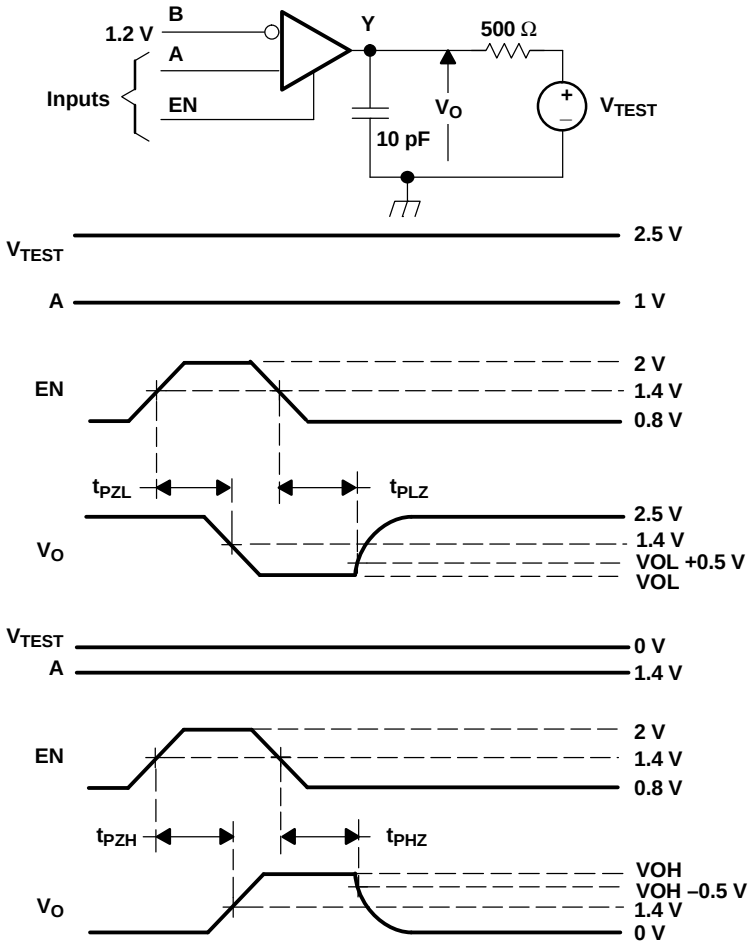
A. All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, signaling rate = 250 kHz, duty cycle = 50 ±2%, C_L includes instrumentation and fixture capacitance within 0,06 mm of the D.U.T and is ±20%.

Figure 3. Timing Test Circuit and Waveforms



A. All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, signaling rate = 500 kHz, duty cycle = 50 ±2%, C_L includes instrumentation and fixture capacitance within 0,06 mm of the D.U.T and is ±20%.

Figure 4. 348 Enable/Disable Time Test Circuit and Waveforms



A. All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, signaling rate = 500 kHz, duty cycle = 50 ±2 %, C_L includes instrumentation and fixture capacitance within 0,06 mm of the D.U.T and is ±20%.

Figure 5. 352 Enable/Disable Time Test Circuit and Waveforms

TYPICAL CHARACTERISTICS

LOW-TO-HIGH PROPAGATION DELAY
vs
FREE-AIR TEMPERATURE

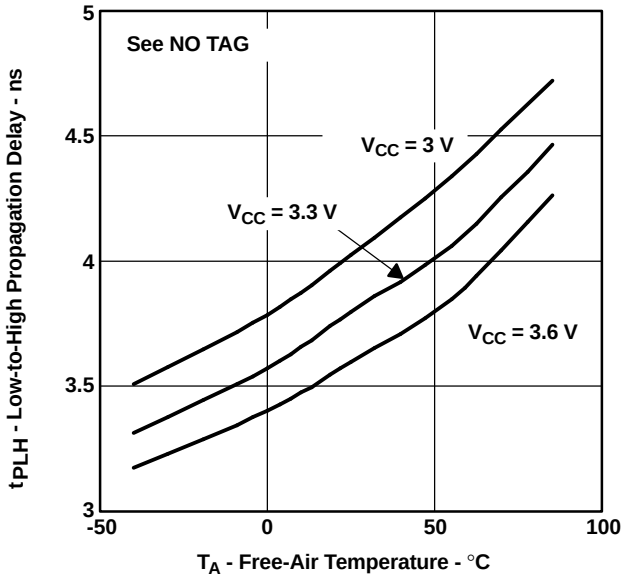


Figure 6.

HIGH-TO-LOWPROPAGATION DELAY
vs
FREE-AIR TEMPERATURE

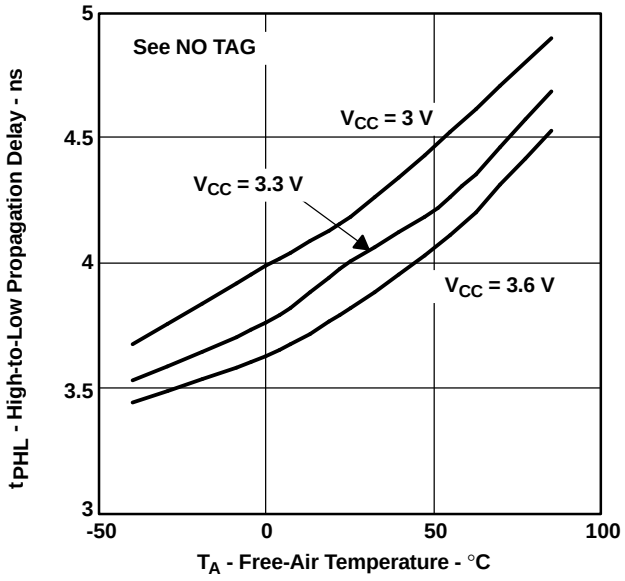


Figure 7.

LOW-LEVEL OUTPUT CURRENT
vs
LOW-LEVEL OUTPUT VOLTAGE

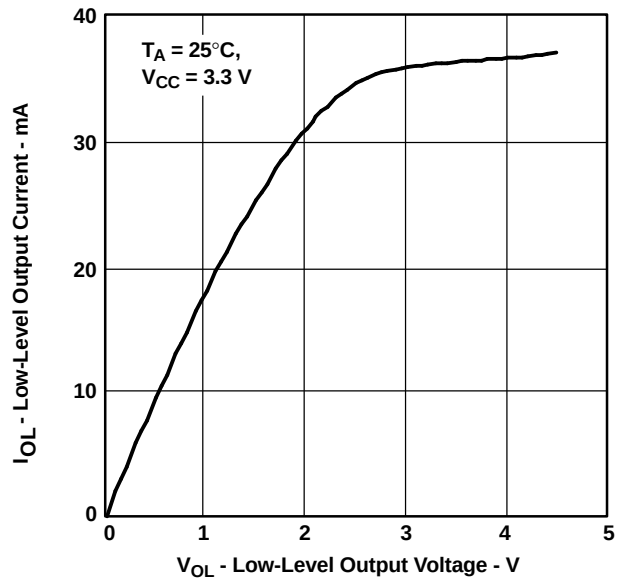


Figure 8.

HIGH-LEVEL OUTPUT CURRENT
vs
HIGH-LEVEL OUTPUT VOLTAGE

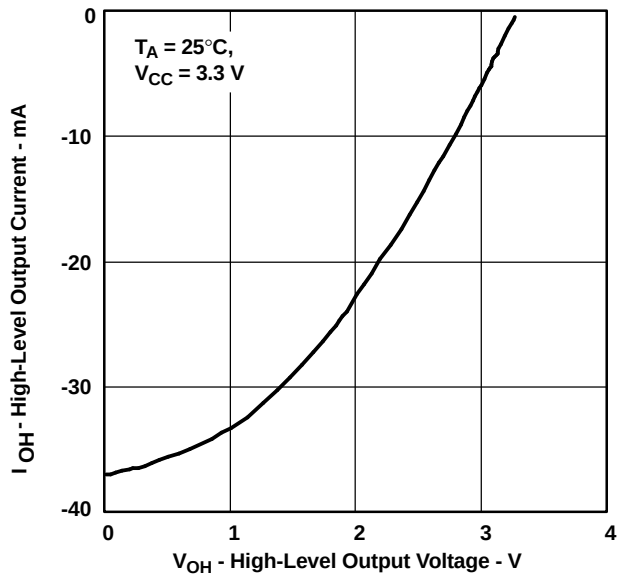


Figure 9.

TYPICAL CHARACTERISTICS (continued)

DATA TRANSFER RATE vs FREE-AIR TEMPERATURE

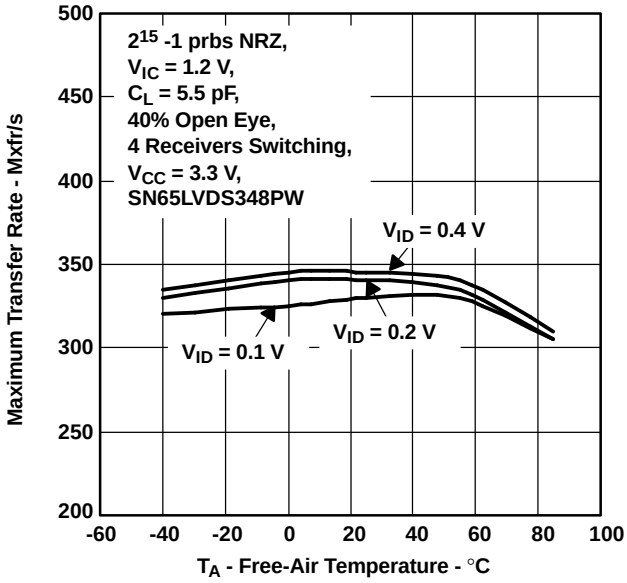


Figure 10.

2^{23} -1 prbs NRZ, T_A = 25°C, C_L = 5.5 pF, 4 Receivers Switching, V_{CC} = 3.3 V

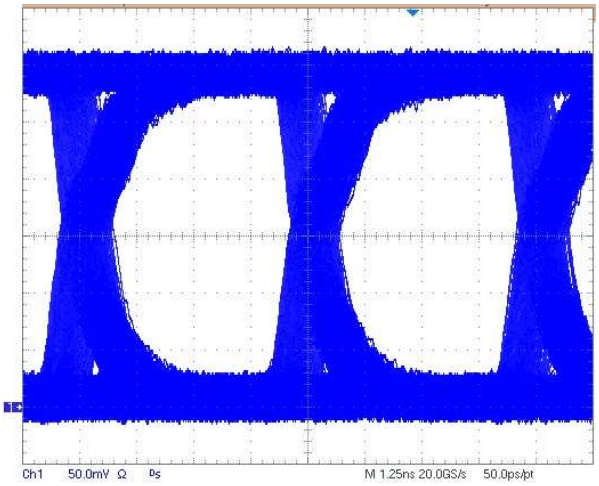


Figure 12. SN65LVDS348 Eye Pattern Running at 200 Mxfr/s

RMS SUPPLY CURRENT vs SWITCHING FREQUENCY

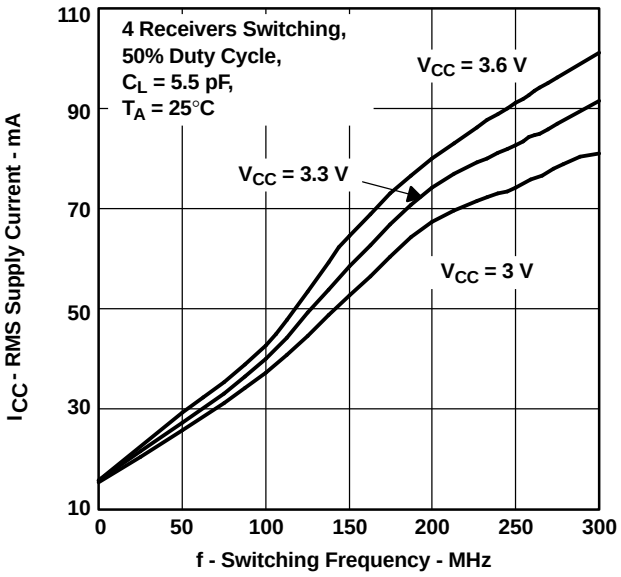


Figure 11.

2^{23} -1 prbs NRZ, T_A = 25°C, C_L = 5.5 pF, 4 Receivers Switching, V_{CC} = 3.3 V

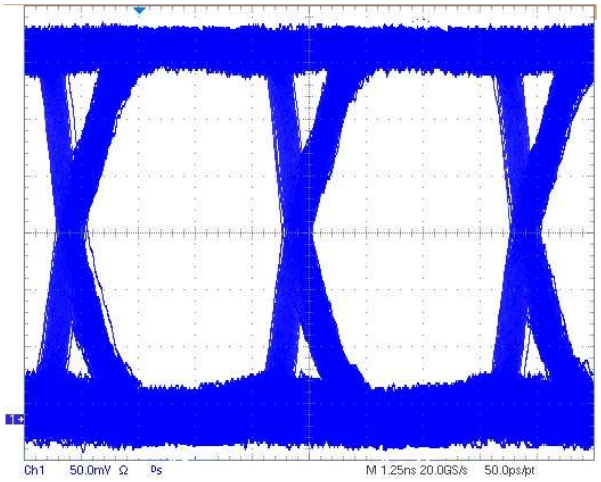


Figure 13. SN65LVDS352 Eye Pattern Running at 200 Mxfr/s

APPLICATION INFORMATION

IMPEDANCE MATCHING AND REFLECTIONS

A termination mismatch can result in reflections that degrade the signal at the load. A low source impedance causes the signal to alternate polarity at the load (oscillates) as shown in Figure 14. High source impedance results in the signal accumulating monotonically to the final value (stair step) as shown in Figure 15. Both of these modes result in a delay in valid signal and reduce the opening in the eye pattern. A 10% termination mismatch results in a 5% reflection ($r = Z_L - Z_O/Z_L + Z_O$), even a 1:3 mismatch absorbs half of the incoming signal. This shows that termination is important in the more critical cases, however, in a general sense, a rather large termination mismatch is not as critical when the differential output signal is much greater than the receiver sensitivity.

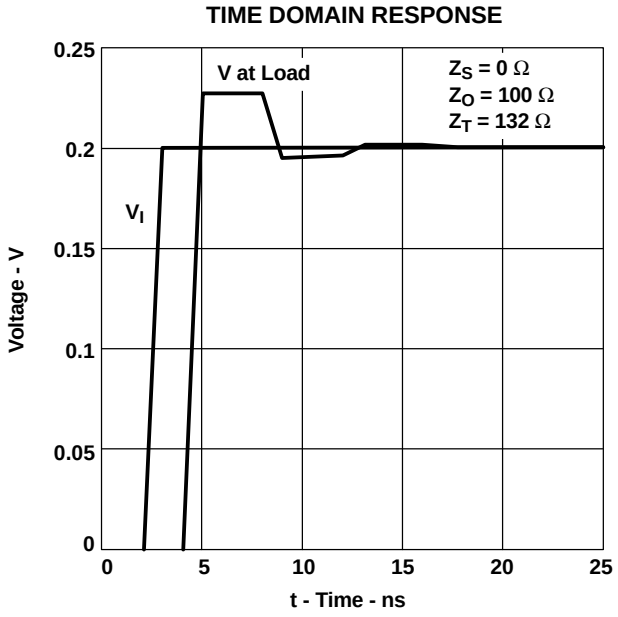


Figure 14. Low-Source Impedance

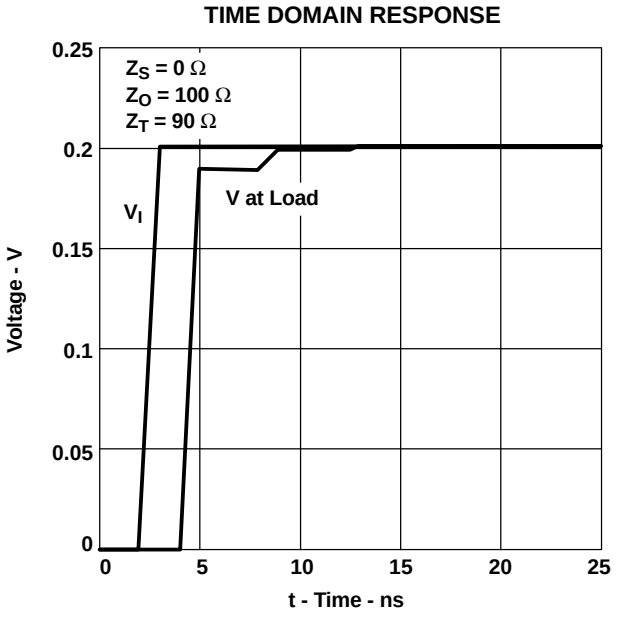


Figure 15. High-Source Impedance

For example a 200-mV drive signal into a 100-Ω lossless transmission media with a termination resistor of 90 Ω to 132Ω results in ~227 mV to 189 mV into the receiver. This would typically be more than enough signal into a receiver with a sensitivity of ±50 mV assuming no other disturbance or attenuation on the line. The other factors, which reduce the signal margin, do affect this and therefore it is important to match the impedance as closely as possible to allow more noise immunity at the receiver.

APPLICATION INFORMATION (continued)

ACTIVE FAILSAFE FEATURE

A differential line receiver commonly has a failsafe circuit to prevent it from switching on input noise. Current LVDS failsafe solutions require either external components with subsequent reductions in signal quality or integrated solutions with limited application. This family of receivers has a new integrated failsafe that solves the limitations seen in present solutions. A detailed theory of operation is presented in application note *The Active Fail-Safe in TI's LVDS Receivers,* literature number SLLA082B.

The following figure shows one receiver channel with active failsafe. It consists of a main receiver that can respond to a high-speed input differential signal. Also connected to the input pair are two failsafe receivers that form a window comparator. The window comparator has a much slower response than the main receiver and it detects when the input differential falls below 80 mV. A 600-ns failsafe timer filters the window comparator outputs. When failsafe is asserted, the failsafe logic drives the main receiver output to logic high.

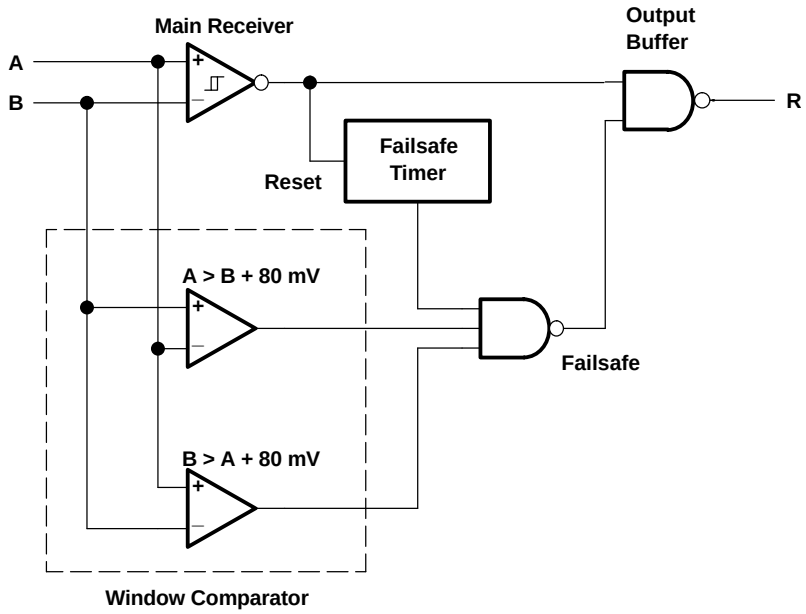


Figure 16. Receiver With Active Failsafe

ECL/PECL-to-LVTTL CONVERSION WITH TI's LVDS RECEIVER

The various versions of emitter-coupled logic (i.e., ECL, PECL and LVPECL) are often the physical layer of choice for system designers. Designers know that established technology is capable of high-speed data transmission. In the past, system requirements often forced the selection of ECL. Now technologies like LVDS provide designers with another alternative. While the total exchange of ECL for LVDS may not be a design option, designers have been able to take advantage of LVDS by implementing a small resistor divider network at the input of the LVDS receiver. TI has taken the next step by introducing a wide common-mode LVDS receiver (no divider network required) which can be connected directly to an ECL driver with only the termination bias voltage required for ECL termination (V_{CC} - 2 V).

Figure 17 shows the use of an LV/PECL driver driving 5 meters of CAT-5 cable and being received by TI's wide common-mode receiver and the resulting eye-pattern. The values for R3 are required in order to provide a resistor path to ground for the LV/PECL driver. With no resistor divider, R1 simply needs to match the characteristic load impedance of 50 Ω. The R2 resistor is a small value intended to minimize common-mode reflections.

APPLICATION INFORMATION (continued)

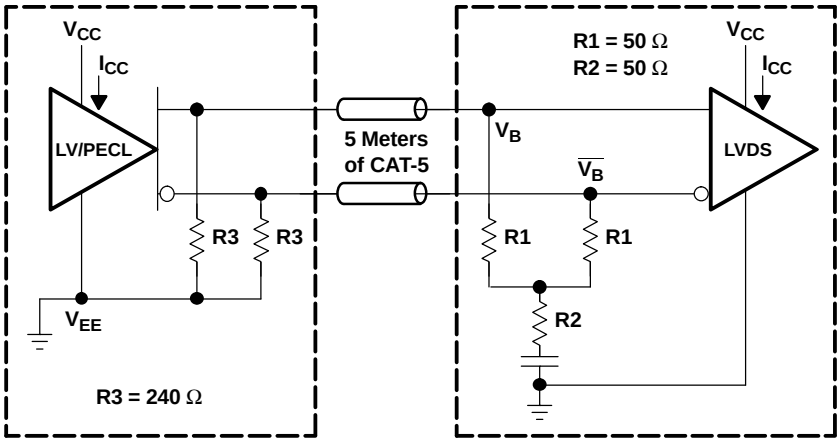


Figure 17. LVPECL or PECL to Remote Wide Common-Mode LVDS Receiver

DEVICE POWER AND GROUNDING

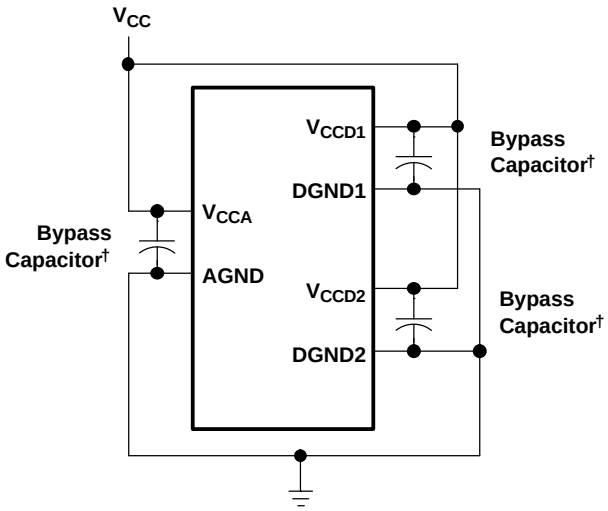
The SN65LVDS352 device provides separate power and ground pins for the analog input section and the two digital output sections. All of the power pins and all of the ground pins of the device must be tied together at some point in the system. Figure 18 shows one recommended scheme for power and ground to the device. This point will be determined by the power and grounding distribution design, which can greatly affect system performance.

Key points to remember when routing power and grounds in your system are:

- The grounding system must provide a low impedance path back to the power source.
- The signal return must be close to the signal path.
- Ground noise occurs due to ground loops and common-mode noise pick-up.
- Closely spaced power and ground planes reduce inductance and increase capacitance.

A good rule to remember when doing your power distribution and board layout is that the current always flows in the lowest impedance path. At dc the lowest resistance is the lowest impedance, but at high frequencies the lowest impedance is the lowest inductance path.

APPLICATION INFORMATION (continued)



† Bypass capacitors used for data sheet electrical testing were low ESR ceramic, surface mount, 0.01 µF ±10%. For a more accurate determination of these values refer to the application note, *The Bypass Capacitor in High-Speed Environments*, literature number SCBA007A.

Figure 18. Recommended Power and Ground Connection

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN65LVDS348D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS348	Samples
SN65LVDS348DG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS348	Samples
SN65LVDS348PW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	DL348	Samples
SN65LVDS348PWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	DL348	Samples
SN65LVDS348PWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	DL348	Samples
SN65LVDS348PWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	DL348	Samples
SN65LVDS352PW	ACTIVE	TSSOP	PW	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DL352	Samples
SN65LVDS352PWG4	ACTIVE	TSSOP	PW	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DL352	Samples
SN65LVDT348D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDT348	Samples
SN65LVDT348DG4	ACTIVE	SOIC	D	16		TBD	Call TI	Call TI	-40 to 85		Samples
SN65LVDT348DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDT348	Samples
SN65LVDT348DRG4	ACTIVE	SOIC	D	16		TBD	Call TI	Call TI	-40 to 85		Samples
SN65LVDT348PW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	DE348	Samples
SN65LVDT348PWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	DE348	Samples
SN65LVDT348PWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	DE348	Samples
SN65LVDT348PWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	DE348	Samples
SN65LVDT352PW	ACTIVE	TSSOP	PW	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DE352	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN65LVDT352PWG4	ACTIVE	TSSOP	PW	24		TBD	Call TI	Call TI	-40 to 85		Samples
SN65LVDT352PWR	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DE352	Samples
SN65LVDT352PWRG4	ACTIVE	TSSOP	PW	24		TBD	Call TI	Call TI	-40 to 85		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

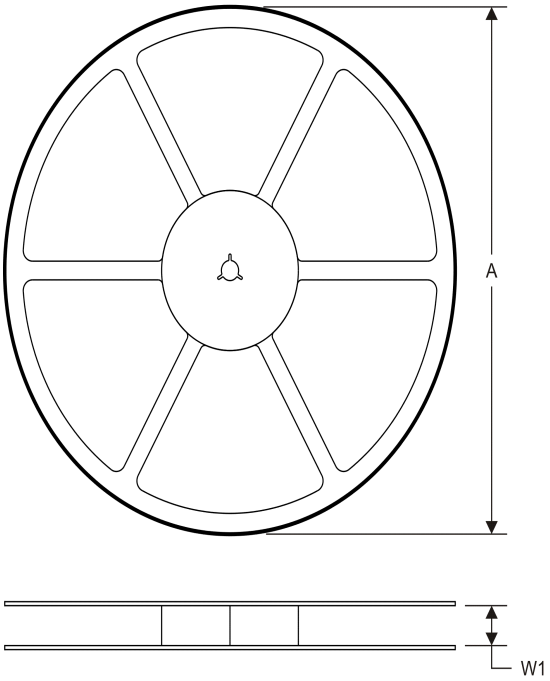
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

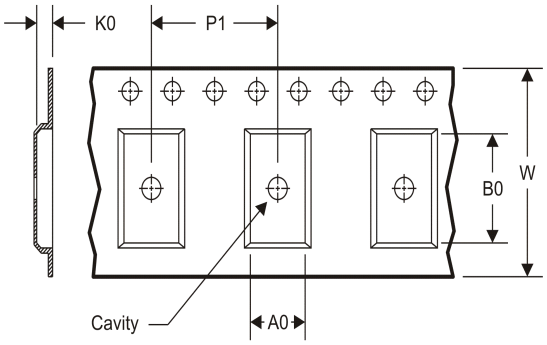
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



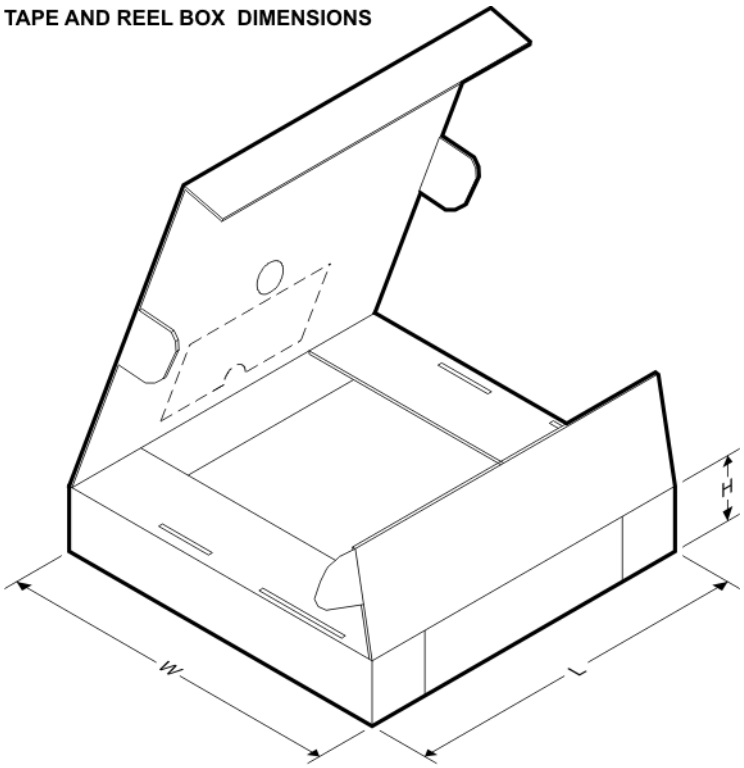
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65LVDS348PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN65LVDT348DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN65LVDT348PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN65LVDT352PWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1

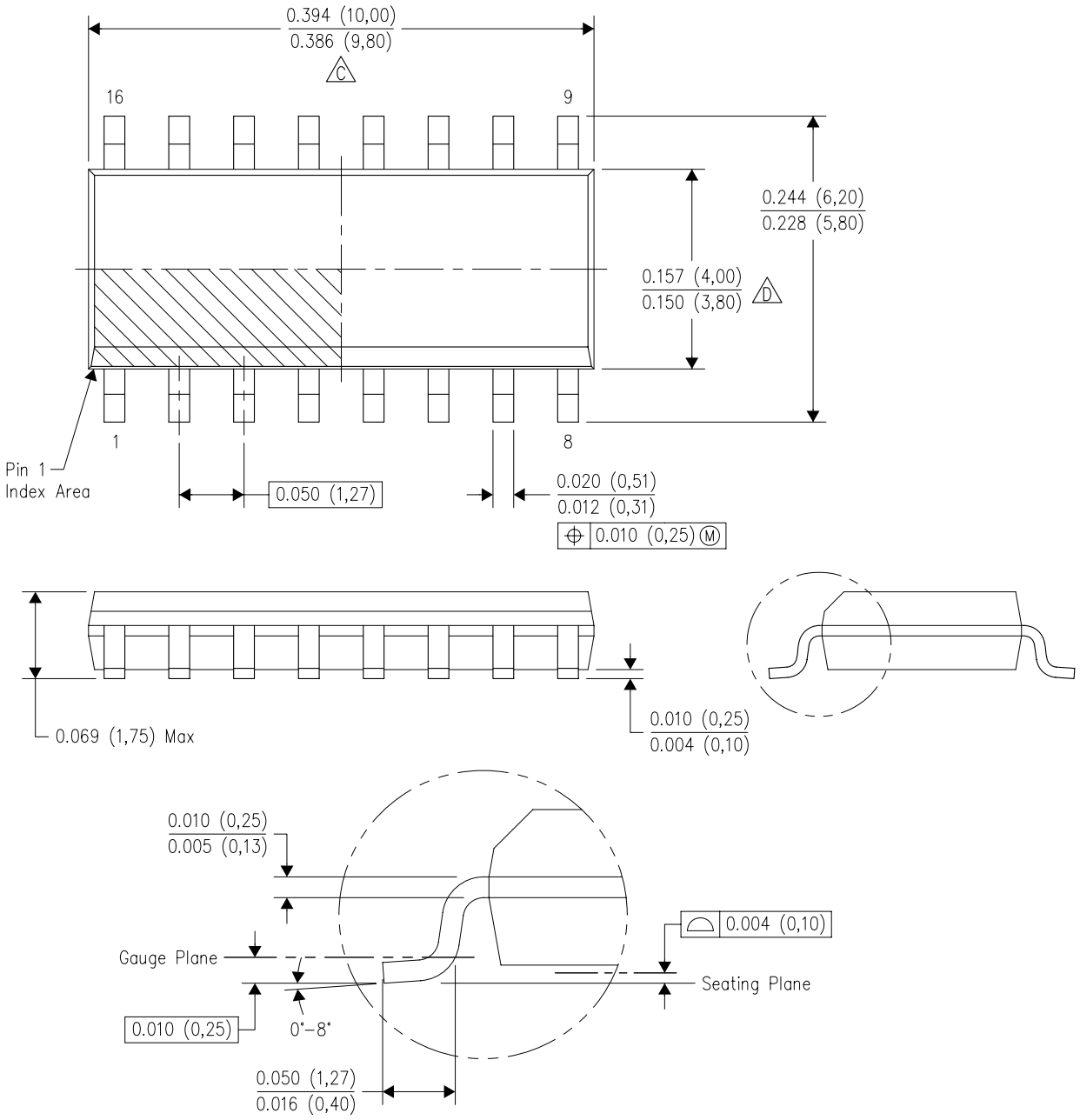
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

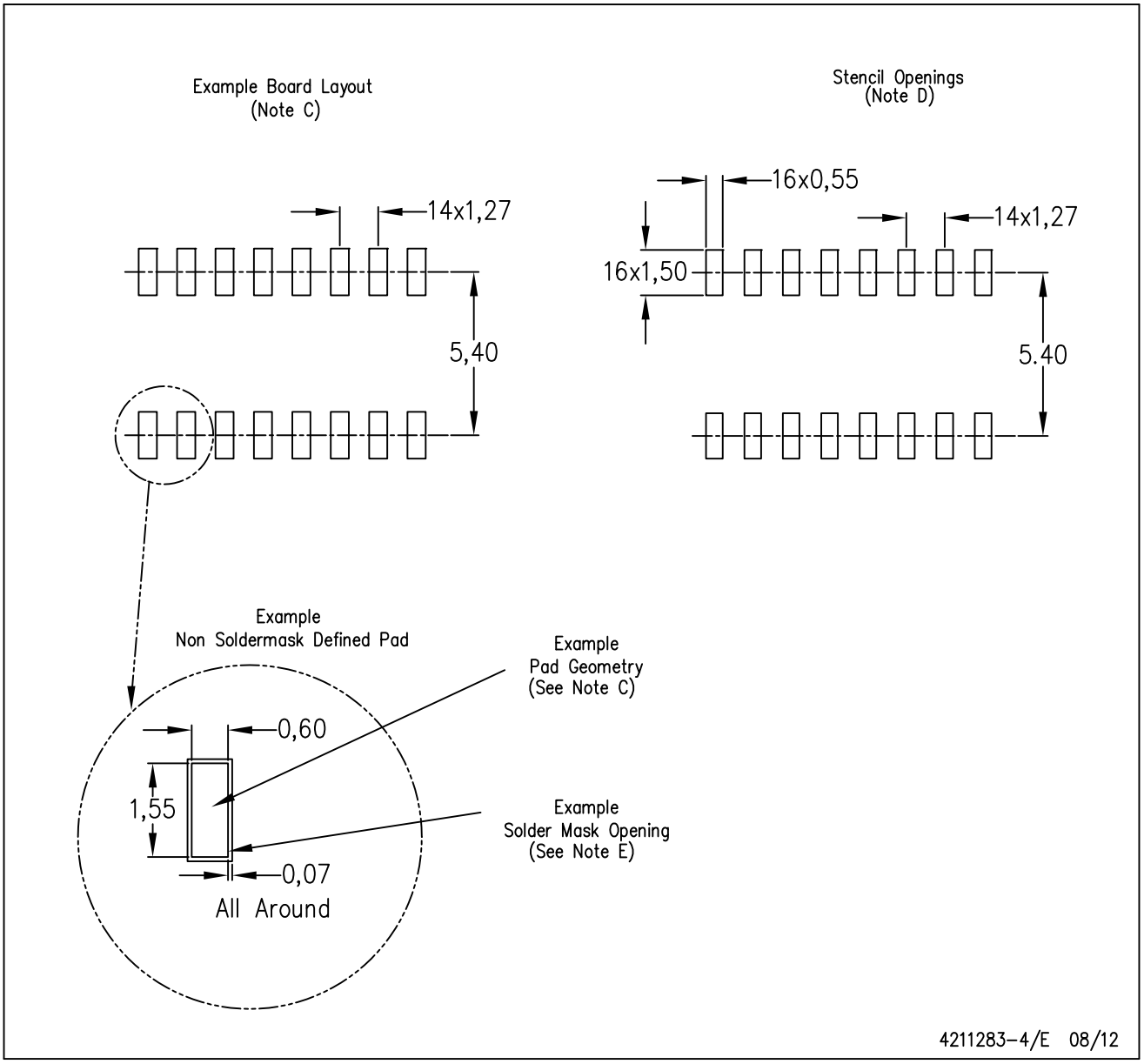
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65LVDS348PWR	TSSOP	PW	16	2000	367.0	367.0	35.0
SN65LVDT348DR	SOIC	D	16	2500	367.0	367.0	38.0
SN65LVDT348PWR	TSSOP	PW	16	2000	367.0	367.0	35.0
SN65LVDT352PWR	TSSOP	PW	24	2000	367.0	367.0	38.0

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



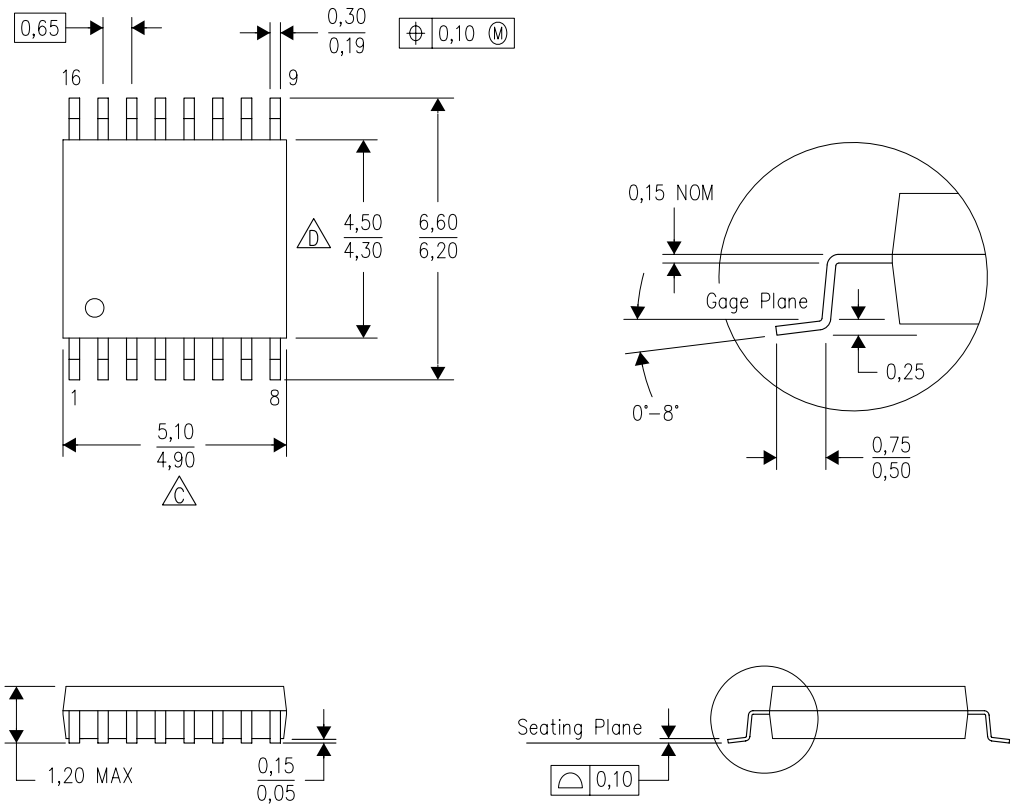
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R–PDSO–G16) PLASTIC SMALL OUTLINE



4040064–4/G 02/11

NOTES:
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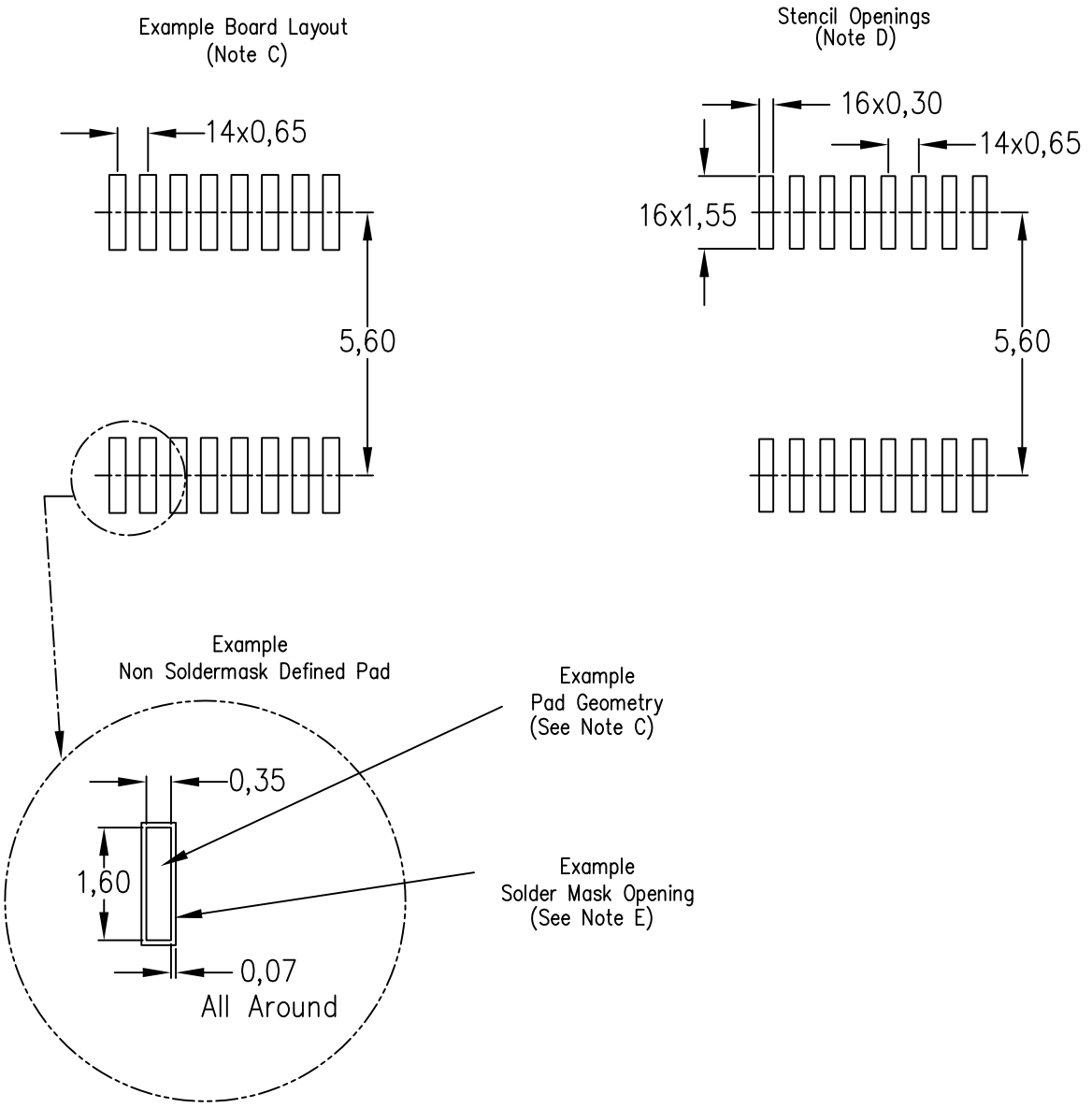
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G16) PLASTIC SMALL OUTLINE



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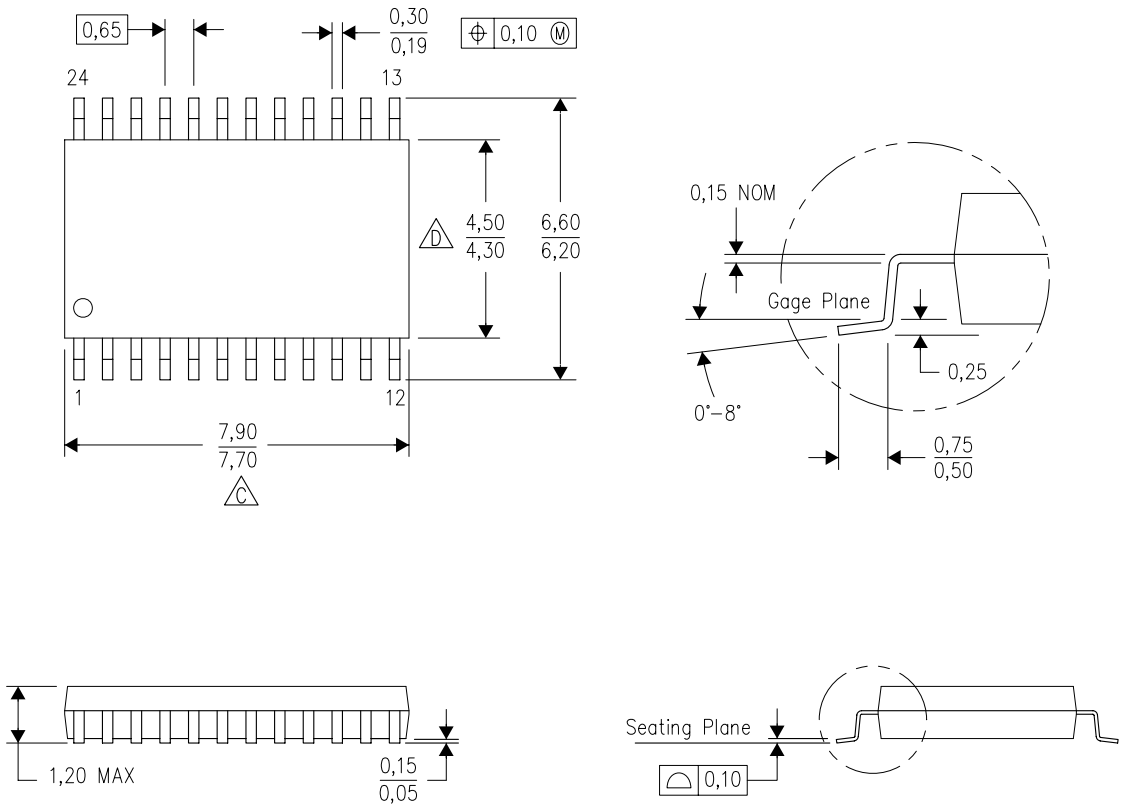
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R–PDSO–G24) PLASTIC SMALL OUTLINE



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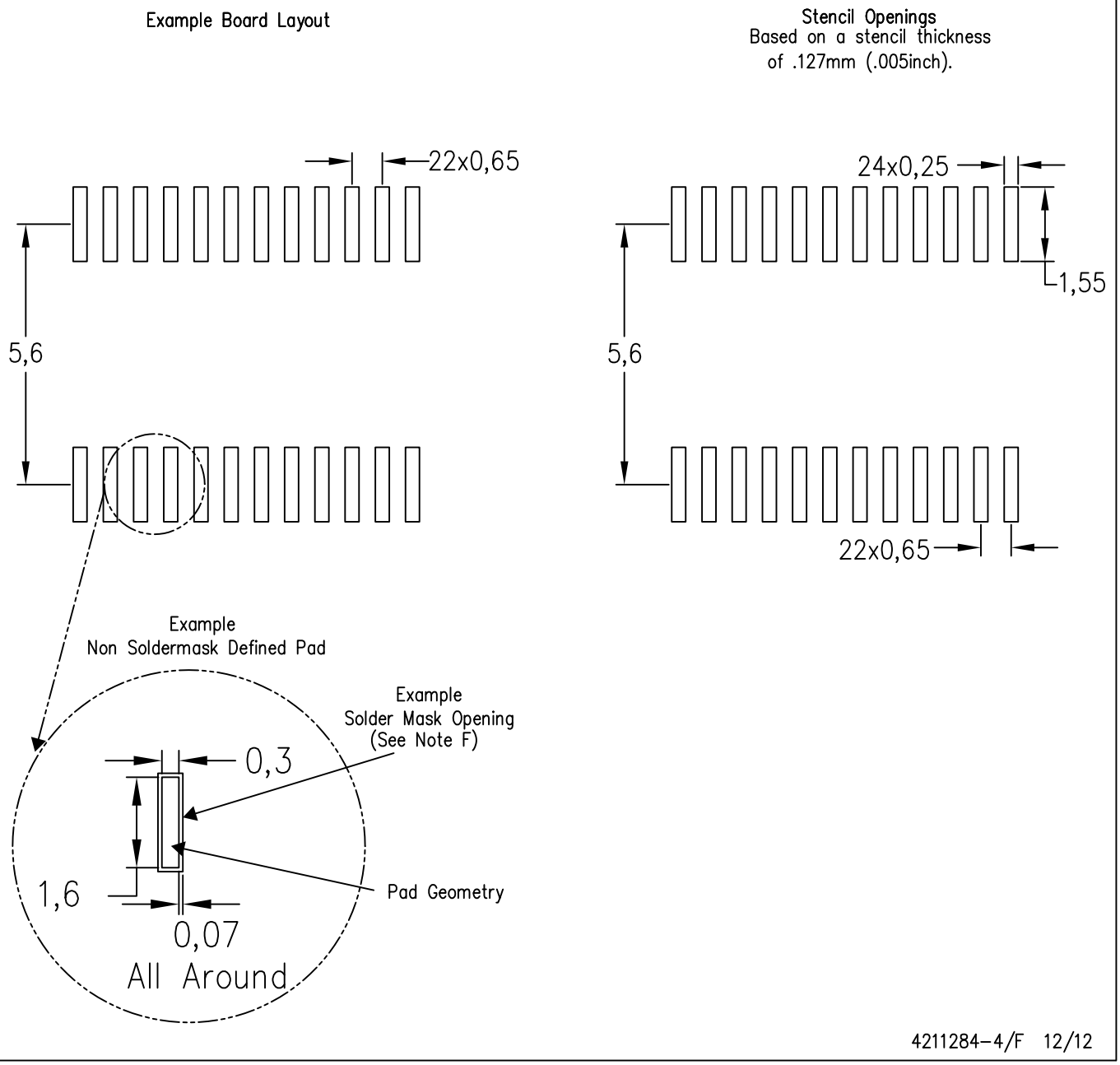
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G24) PLASTIC SMALL OUTLINE



NOTES:
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B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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