

SN54AHC158, SN74AHC158 QUADRUPLE 2-LINE TO 1-LINE DATA SELECTORS/MUXES

SCLS346G – MAY 1996 – REVISED JULY 2003

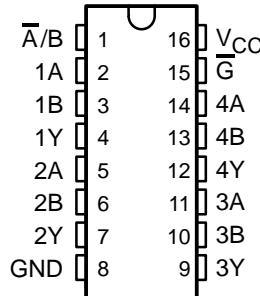
- Operating Range 2-V to 5.5-V V_{CC}
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

description/ordering information

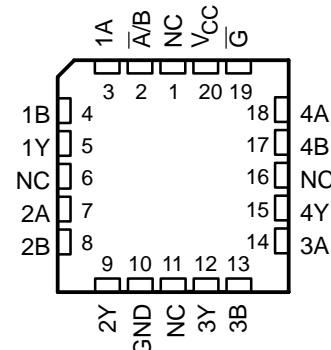
These quadruple 2-line to 1-line data selectors/multiplexers are designed for 2-V to 5.5-V V_{CC} operation.

The 'AHC158 devices feature a common strobe (\bar{G}) input. When the strobe is high, all outputs are high. When the strobe is low, a 4-bit word is selected from one of two sources and is routed to the four outputs. These devices provide inverted data.

SN54AHC158 . . . J OR W PACKAGE
SN74AHC158 . . . D, DB, DGV, N, NS, OR PW PACKAGE
(TOP VIEW)



SN54AHC158 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

ORDERING INFORMATION

TA	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	PDIP – N	Tube	SN74AHC158N	SN74AHC158N
	SOIC – D	Tube	SN74AHC158D	AHC158
		Tape and reel	SN74AHC158DR	
	SOP – NS	Tape and reel	SN74AHC158NSR	AHC158
	SSOP – DB	Tape and reel	SN74AHC158DBR	HA158
	TSSOP – PW	Tube	SN74AHC158PW	HA158
		Tape and reel	SN74AHC158PWR	
–55°C to 125°C	TVSOP – DGV	Tape and reel	SN74AHC158DGVR	HA158
	CDIP – J	Tube	SNJ54AHC158J	SNJ54AHC158J
	CFP – W	Tube	SNJ54AHC158W	SNJ54AHC158W
	LCCC – FK	Tube	SNJ54AHC158FK	SNJ54AHC158FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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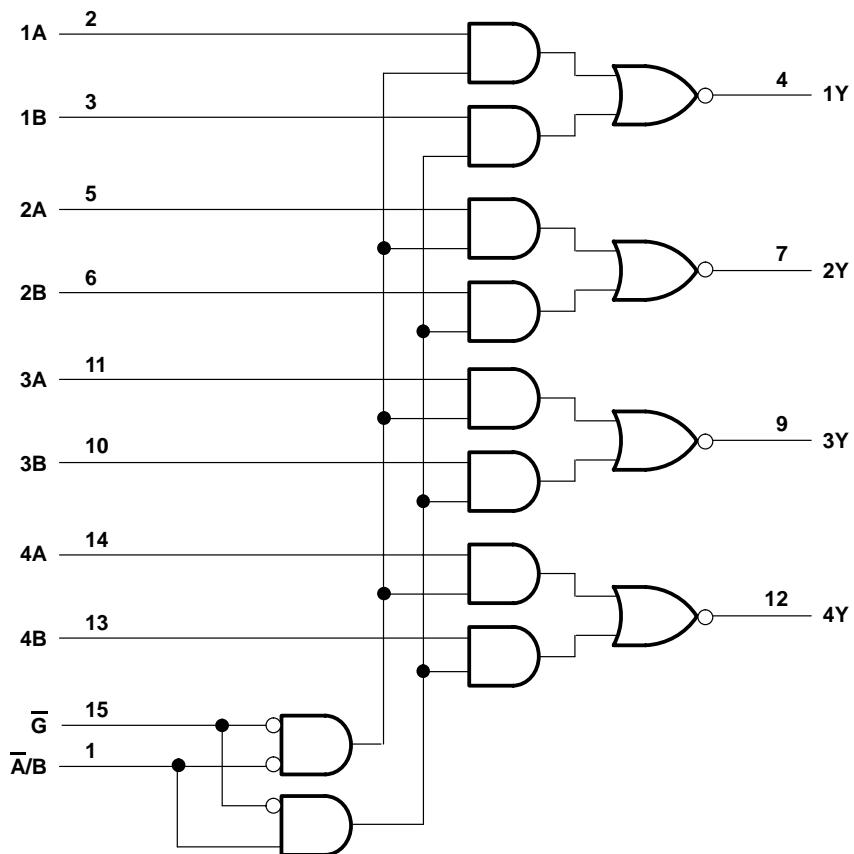
SN54AHC158, SN74AHC158 QUADRUPLE 2-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS

SCLS346G – MAY 1996 – REVISED JULY 2003

FUNCTION TABLE
(each data selector/multiplexer)

INPUTS				OUTPUT
\bar{G}	\bar{A}/B	A	B	Y
H	X	X	X	H
L	L	L	X	H
L	L	H	X	L
L	H	X	L	H
L	H	X	H	L

logic diagram (positive logic)



Pin numbers shown are for the D, DB, DGV, J, N, NS, PW, and W packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	–0.5 V to 7 V			
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V			
Output voltage range, V_O (see Note 1)	–0.5 V to V_{CC} + 0.5 V			
Input clamp current, I_{IK} ($V_I < 0$)	–20 mA			
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±20 mA			
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±25 mA			
Continuous current through V_{CC} or GND	±50 mA			
Package thermal impedance, θ_{JA} (see Note 2): D package	73°C/W			
DB package	82°C/W			
DGV package	120°C/W			
N package	67°C/W			
NS package	64°C/W			
PW package	108°C/W			
Storage temperature range, T_{STG}	–65°C to 150°C			

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

		SN54AHC158		SN74AHC158		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	2	5.5	2	5.5	V
V_{IH}	High-level input voltage	$V_{CC} = 2$ V	1.5	1.5	1.5	V
		$V_{CC} = 3$ V	2.1	2.1	2.1	
		$V_{CC} = 5.5$ V	3.85	3.85	3.85	
V_{IL}	Low-level input voltage	$V_{CC} = 2$ V	0.5	0.5	0.5	V
		$V_{CC} = 3$ V	0.9	0.9	0.9	
		$V_{CC} = 5.5$ V	1.65	1.65	1.65	
V_I	Input voltage	0	5.5	0	5.5	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	$V_{CC} = 2$ V	–50	–50	–50	μ A
		$V_{CC} = 3.3$ V ± 0.3 V	–4	–4	–4	mA
		$V_{CC} = 5$ V ± 0.5 V	–8	–8	–8	
I_{OL}	Low-level output current	$V_{CC} = 2$ V	50	50	50	μ A
		$V_{CC} = 3.3$ V ± 0.3 V	4	4	4	mA
		$V_{CC} = 5$ V ± 0.5 V	8	8	8	
$\Delta t/\Delta v$	Input transition rise or fall rate	$V_{CC} = 3.3$ V ± 0.3 V	100	100	100	ns/V
		$V_{CC} = 5$ V ± 0.5 V	20	20	20	
T_A	Operating free-air temperature	–55	125	–40	85	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

SN54AHC158, SN74AHC158 QUADRUPLE 2-LINE TO 1-LINE DATA SELECTORS/MUXES

SCLS346G – MAY 1996 – REVISED JULY 2003

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			SN54AHC158	SN74AHC158	UNIT
			MIN	TYP	MAX	MIN	MAX	
V _{OH}	I _{OH} = -50 µA	2 V	1.9	2		1.9	1.9	V
		3 V	2.9	3		2.9	2.9	
		4.5 V	4.4	4.5		4.4	4.4	
	I _{OH} = -4 mA	3 V	2.58			2.48	2.48	
	I _{OH} = -8 mA	4.5 V	3.94			3.8	3.8	
		2 V		0.1		0.1	0.1	
V _{OL}	I _{OL} = 50 µA	3 V		0.1		0.1	0.1	V
		4.5 V		0.1		0.1	0.1	
		3 V		0.36		0.5	0.44	
	I _{OL} = 4 mA	4.5 V		0.36		0.5	0.44	
I _I	A or B inputs	V _I = 5.5 V or GND	0 V to 5.5 V		±0.1	±1*	±1	µA
I _{CC}		V _I = V _{CC} or GND, I _O = 0	5.5 V		4	40	40	µA
C _i		V _I = V _{CC} or GND	5 V	2	10		10	pF

* On products compliant to MIL-PRF-38535, this parameter is not production tested at V_{CC} = 0 V.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T _A = 25°C			SN54AHC158	SN74AHC158	UNIT	
				MIN	TYP	MAX	MIN	MAX		
t _{PLH}	A or B	Y	C _L = 15 pF	6.2**	9.7**	1**	11.5**	1	11.5	ns
t _{PHL}				6.2**	9.7**	1**	11.5**	1	11.5	
t _{PLH}	A/B	Y	C _L = 15 pF	8.4**	13.2**	1**	15.5**	1	15.5	ns
t _{PHL}				8.4**	13.2**	1**	15.5**	1	15.5	
t _{PLH}	G	Y	C _L = 15 pF	8.7**	13.6**	1**	16**	1	16	ns
t _{PHL}				8.7**	13.6**	1**	16**	1	16	
t _{PLH}	A or B	Y	C _L = 50 pF	8.7	13.2	1	15	1	15	ns
t _{PHL}				8.7	13.2	1	15	1	15	
t _{PLH}	A/B	Y	C _L = 50 pF	10.9	16.7	1	19	1	19	ns
t _{PHL}				10.9	16.7	1	19	1	19	
t _{PLH}	G	Y	C _L = 50 pF	11.2	17.1	1	19.5	1	19.5	ns
t _{PHL}				11.2	17.1	1	19.5	1	19.5	

** On products compliant to MIL-PRF-38535, this parameter is not production tested.

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



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QUADRUPLE 2-LINE TO 1-LINE DATA SELECTORS/MUXES

SCLS346G – MAY 1996 – REVISED JULY 2003

**switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$ (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54AHC158	SN74AHC158	UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{PLH}	A or B	Y	$C_L = 15 \text{ pF}$	4.1*	6.4*	1*	7.5*	1	7.5
t_{PHL}				4.1*	6.4*	1*	7.5*	1	7.5
t_{PLH}	\bar{A}/B	Y	$C_L = 15 \text{ pF}$	5.3*	8.1*	1*	9.5*	1	9.5
t_{PHL}				5.3*	8.1*	1*	9.5*	1	9.5
t_{PLH}	\bar{G}	Y	$C_L = 15 \text{ pF}$	5.6*	8.6*	1*	10*	1	10
t_{PHL}				5.6*	8.6*	1*	10*	1	10
t_{PLH}	A or B	Y	$C_L = 50 \text{ pF}$	5.6	8.4	1	9.5	1	9.5
t_{PHL}				5.6	8.4	1	9.5	1	9.5
t_{PLH}	\bar{A}/B	Y	$C_L = 50 \text{ pF}$	6.8	10.1	1	11.5	1	11.5
t_{PLH}				6.8	10.1	1	11.5	1	11.5
t_{PLH}	\bar{G}	Y	$C_L = 50 \text{ pF}$	7.1	10.6	1	12	1	12
t_{PHL}				7.1	10.6	1	12	1	12

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

noise characteristics $V_{CC} = 5 \text{ V}$, $C_L = 50 \text{ pF}$, $T_A = 25^\circ\text{C}$ (see Note 4)

PARAMETER	SN74AHC158			UNIT
	MIN	TYP	MAX	
$V_{OL(P)}$ Quiet output, maximum dynamic V_{OL}			0.8	V
$V_{OL(V)}$ Quiet output, minimum dynamic V_{OL}			-0.8	V
$V_{OH(V)}$ Quiet output, minimum dynamic V_{OH}			4.8	V
$V_{IH(D)}$ High-level dynamic input voltage			3.5	V
$V_{IL(D)}$ Low-level dynamic input voltage			1.5	V

NOTE 4: Characteristics are for surface-mount packages only.

operating characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
C_{pd} Power dissipation capacitance	No load, $f = 1 \text{ MHz}$	11	pF

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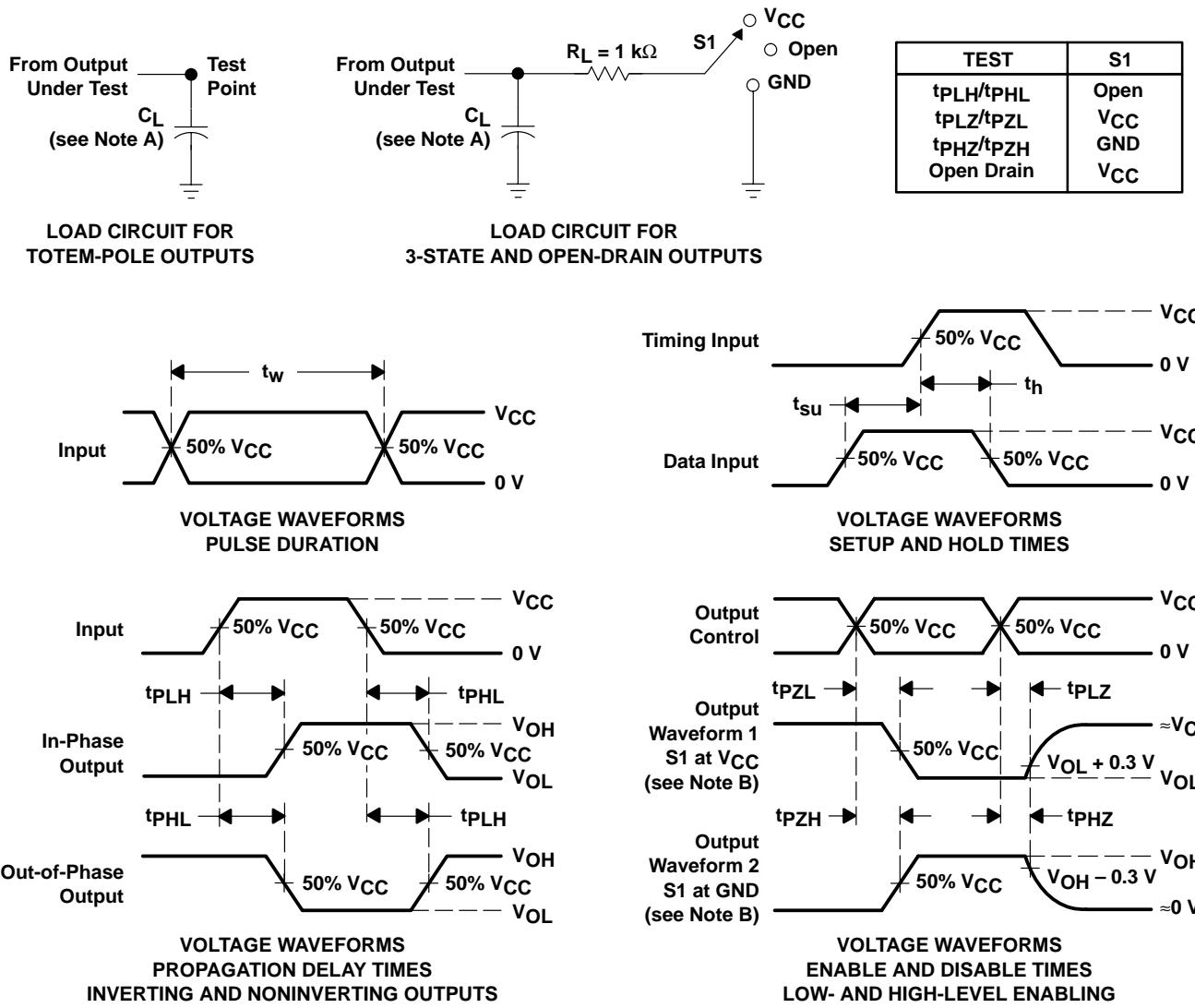


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SN54AHC158, SN74AHC158 QUADRUPLE 2-LINE TO 1-LINE DATA SELECTORS/MUXES

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PARAMETER MEASUREMENT INFORMATION



NOTES:

- C_L includes probe and jig capacitance.
- Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- All input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz, $Z_O = 50 \Omega$, $t_r \leq 3$ ns, $t_f \leq 3$ ns.
- The outputs are measured one at a time with one input transition per measurement.
- All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74AHC158D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AHC158	Samples
SN74AHC158DBLE	OBsolete	SSOP	DB	16		TBD	Call TI	Call TI	-40 to 85		
SN74AHC158DBR	ACTIVE	SSOP	DB	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HA158	Samples
SN74AHC158DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AHC158	Samples
SN74AHC158N	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	SN74AHC158N	Samples
SN74AHC158NSR	OBsolete	SO	NS	16		TBD	Call TI	Call TI	-40 to 85	AHC158	
SN74AHC158NSRE4	OBsolete	SO	NS	16		TBD	Call TI	Call TI	-40 to 85		
SN74AHC158NSRG4	OBsolete	SO	NS	16		TBD	Call TI	Call TI	-40 to 85		
SN74AHC158PW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HA158	Samples
SN74AHC158PWLE	OBsolete	TSSOP	PW	16		TBD	Call TI	Call TI	-40 to 85		
SN74AHC158PWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HA158	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

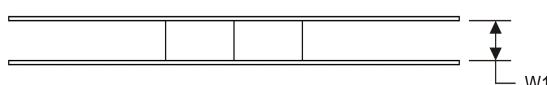
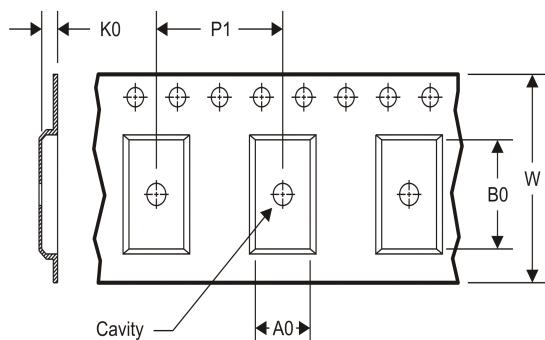
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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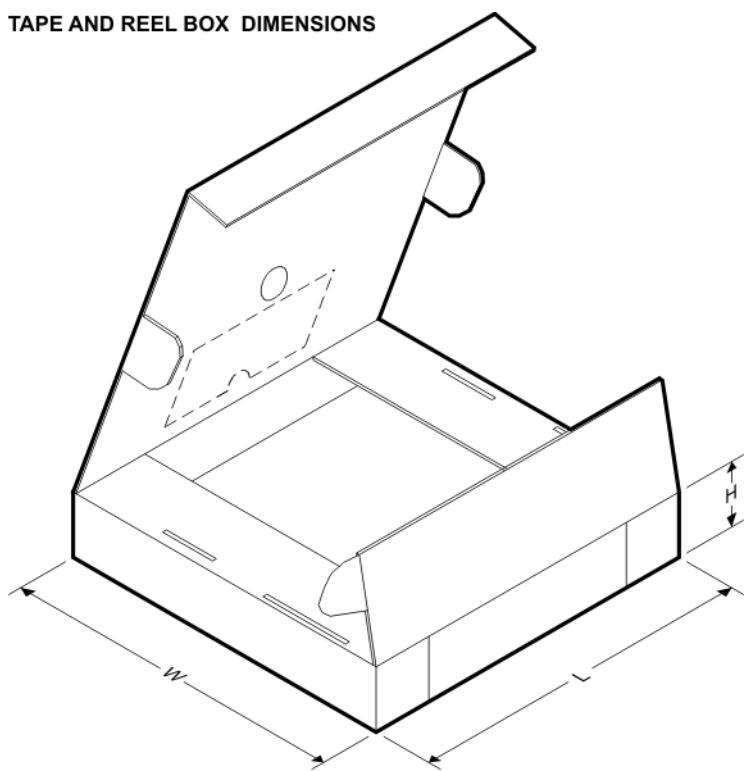
TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AHC158DBR	SSOP	DB	16	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1
SN74AHC158DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74AHC158PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AHC158DBR	SSOP	DB	16	2000	367.0	367.0	38.0
SN74AHC158DR	SOIC	D	16	2500	333.2	345.9	28.6
SN74AHC158PWR	TSSOP	PW	16	2000	367.0	367.0	35.0

N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.

△ Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).

△ The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

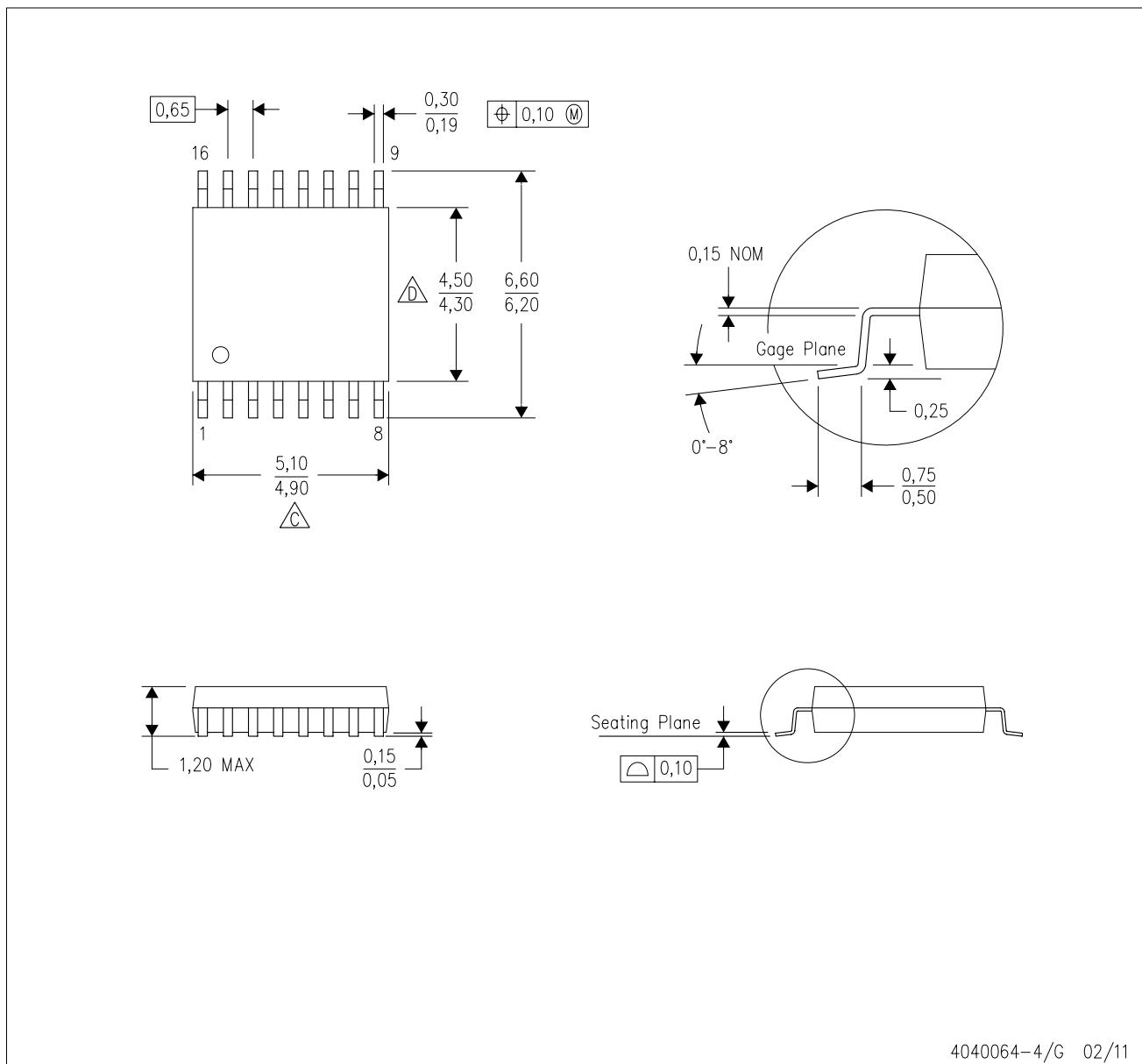
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.

D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.

E. Reference JEDEC MS-012 variation AC.

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4040064-4/G 02/11

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

B. This drawing is subject to change without notice.

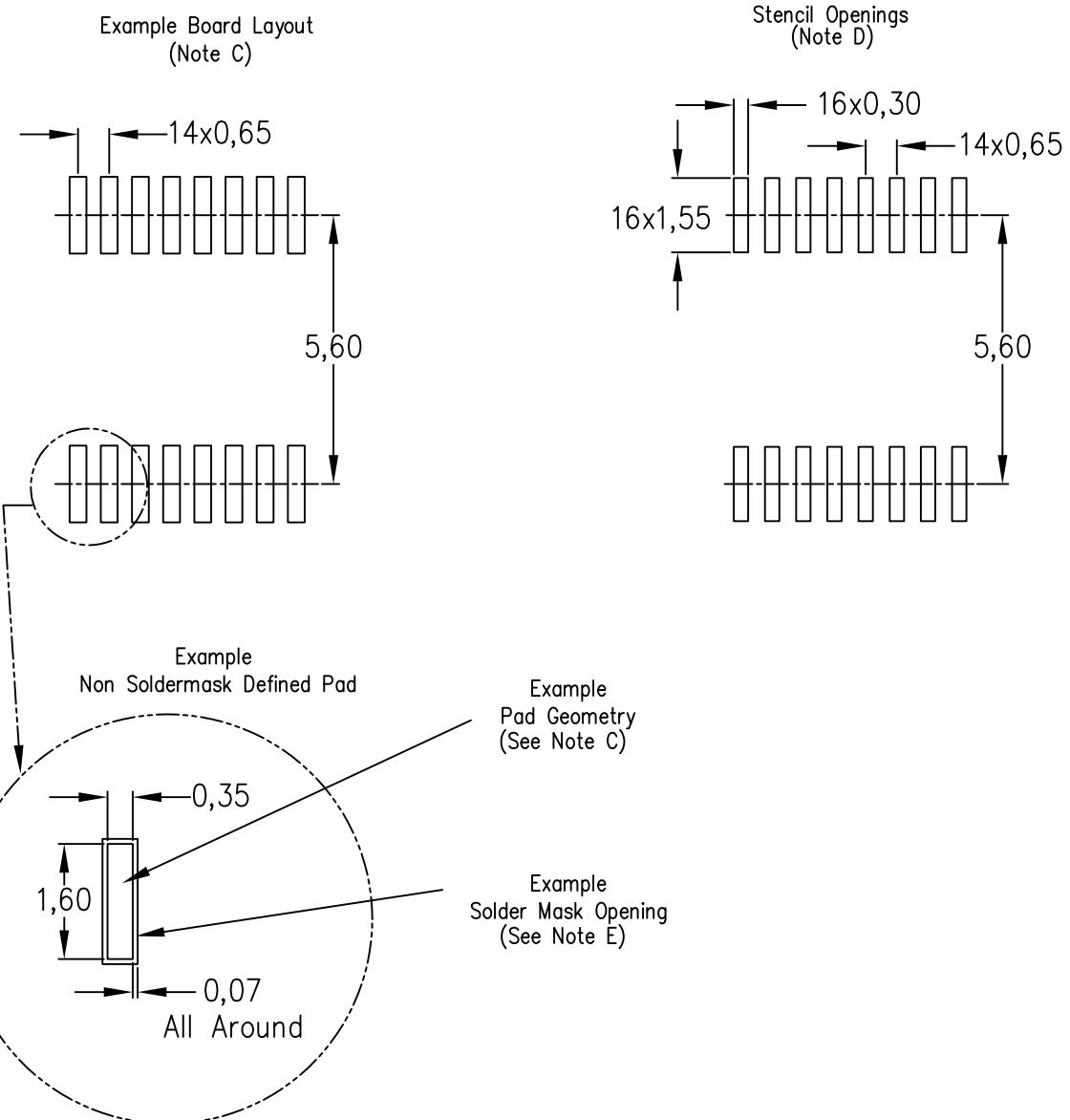
△ C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.

△ D Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.

E. Falls within JEDEC MO-153

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4211284-3/F 12/12

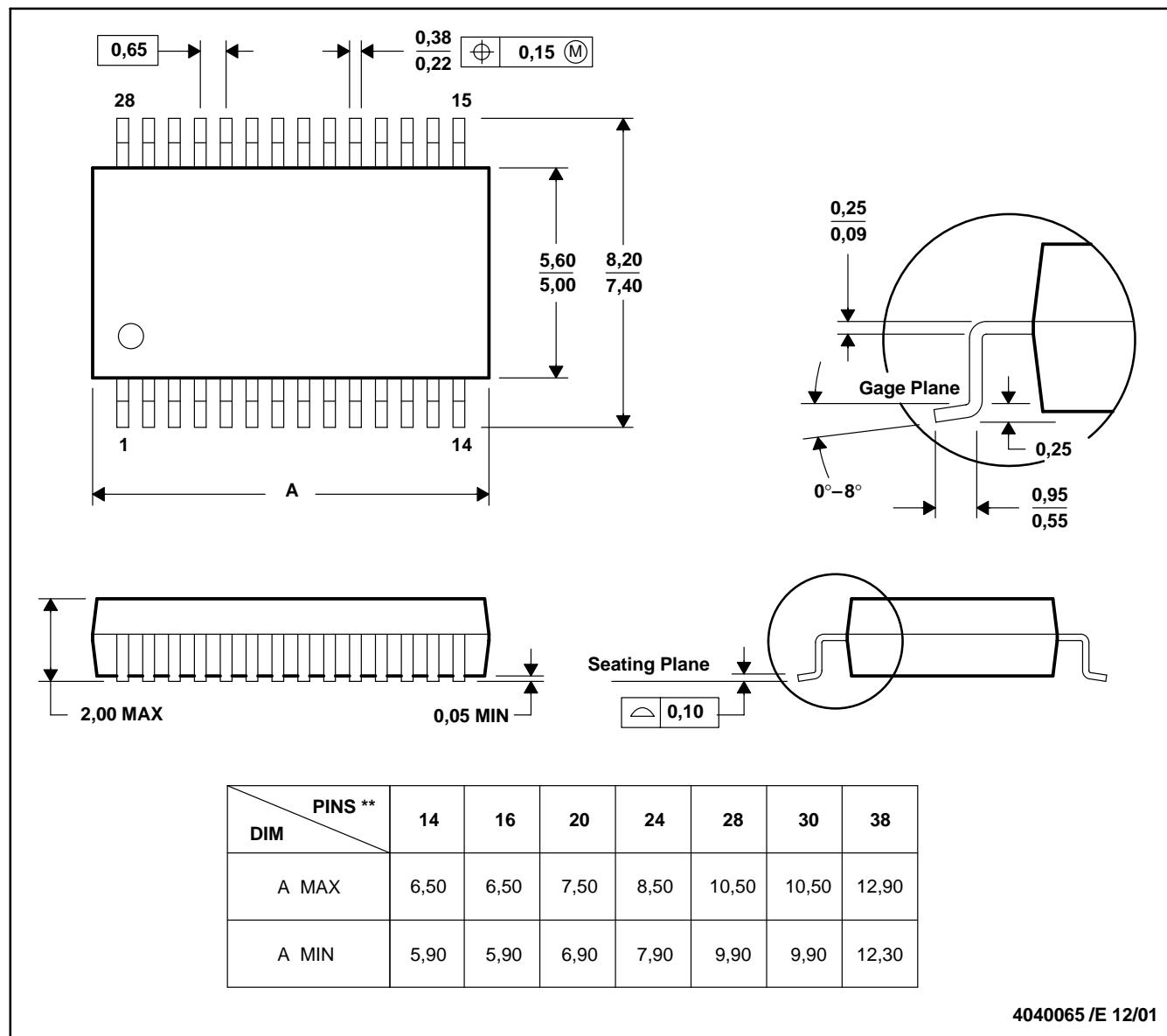
NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



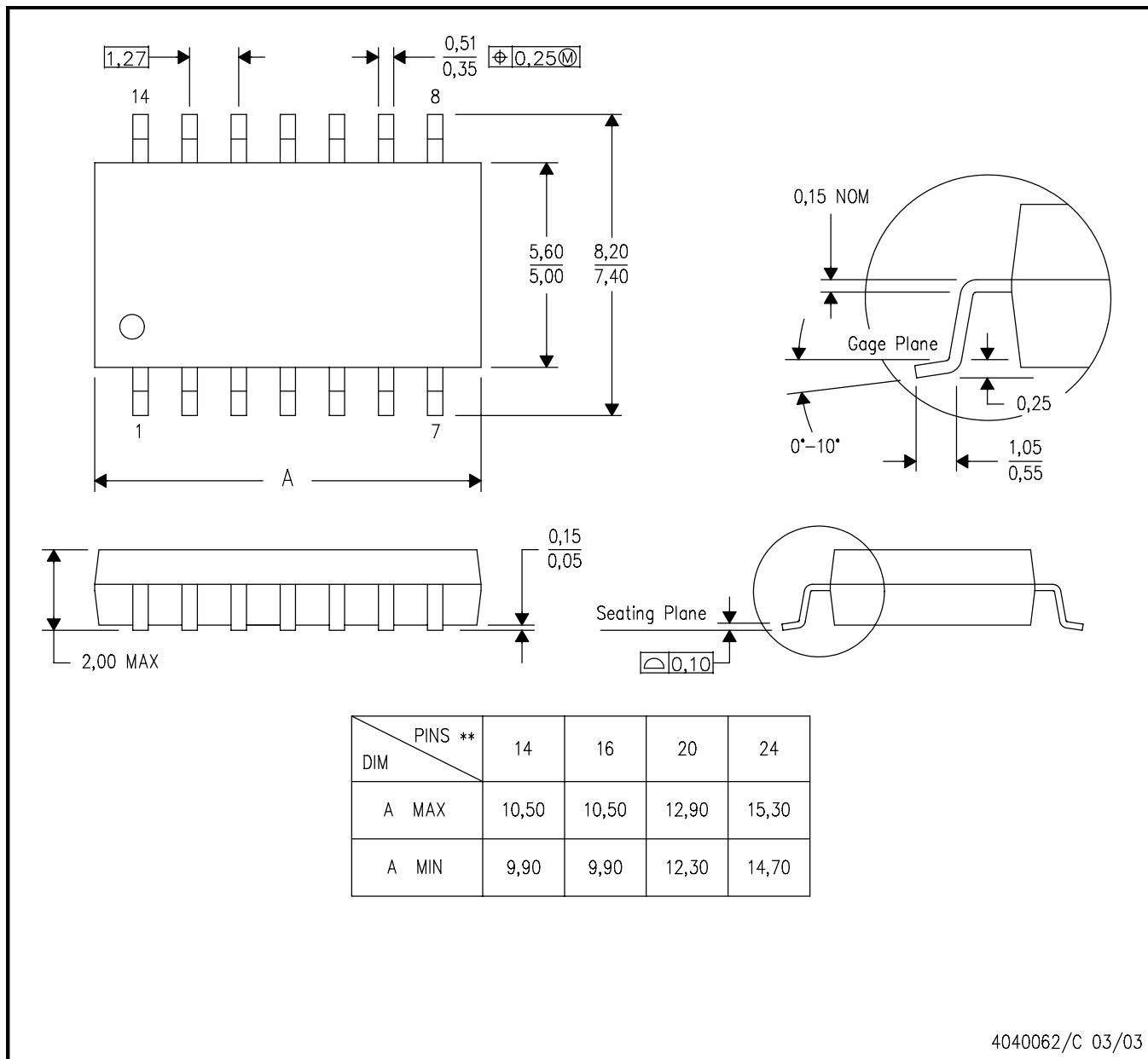
NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

MECHANICAL DATA

NS (R-PDSO-G)**

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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