



Z86C33/C43

CMOS Z8®

CONSUMER CONTROLLER PROCESSOR

FEATURES

Part	ROM (KB)	RAM* (Bytes)	Speed (MHz)
Z86C33	4	237	12, 16
Z86C43	4	236	12, 16

* General-Purpose

- 40-Pin DIP, 44-Pin PLCC and QFP Packages (C43)
28-Pin DIP, 28-Pin SOIC (C33)
- 3.0- to 5.5-Volt Operating Range
- Low-Power Consumption
- -40°C to +105°C Operating Range
- Expanded Register File (ERF)
- 32 Input/Output Lines (C43)
24 Input/Output Lines (C33)
- Vectored, Prioritized Interrupts with Programmable Polarity
- Two Analog Comparators
- Two Programmable 8-Bit Counter/Timers, Each with Two 6-Bit Programmable Prescaler
- Watch-Dog Timer (WDT)/Power-On Reset (POR)
- On-Chip Oscillator that Accepts a Crystal, Ceramic Resonator, LC, RC, or External Clock
- RAM and ROM Protect

GENERAL DESCRIPTION

The Z86C33/C43 Consumer Controller Processor (CCP™) is a member of Zilog's Z8® single-chip microcontroller family with enhanced wake-up circuitry, programmable Watch-Dog Timers (WDT), and low-noise/EMI options. These enhancements result in a more efficient, cost-effective design and provide the user with increased design flexibility over the standard Z8 microcontroller core. This low-power consumption CMOS microcontroller offers fast execution, efficient use of memory, sophisticated interrupts, input/output bit manipulation capabilities, and easy hardware/software system expansion.

The Z86C33/C43 features an Expanded Register File (ERF) to allow access to register-mapped peripheral and I/O circuits. Four basic address spaces are available to support this wide range of configurations: Program Memory, Register File, Data Memory, and ERF. The Register File is composed of 236 bytes of general-purpose registers, four I/O port registers, and 15 control and status registers. The ERF consists of three control registers

For applications demanding powerful I/O capabilities, the Z86C33 provides 24 pins, and the Z86C43 provides 32 pins dedicated to input and output. These lines are configurable under software control to provide timing,

status signals, parallel I/O with or without handshake, and address/data bus for interfacing external memory.

To unburden the system from coping with real-time tasks such as counting/timing and data communication, the Z86C33/C43 offers two on-chip counter/timers with a large number of user-selectable modes.

With ROM/ROMless selectivity, the Z86C43 provides both external memory and pre-programmed ROM, which enables this Z8 microcontroller to be used in high-volume applications, or where code flexibility is required.

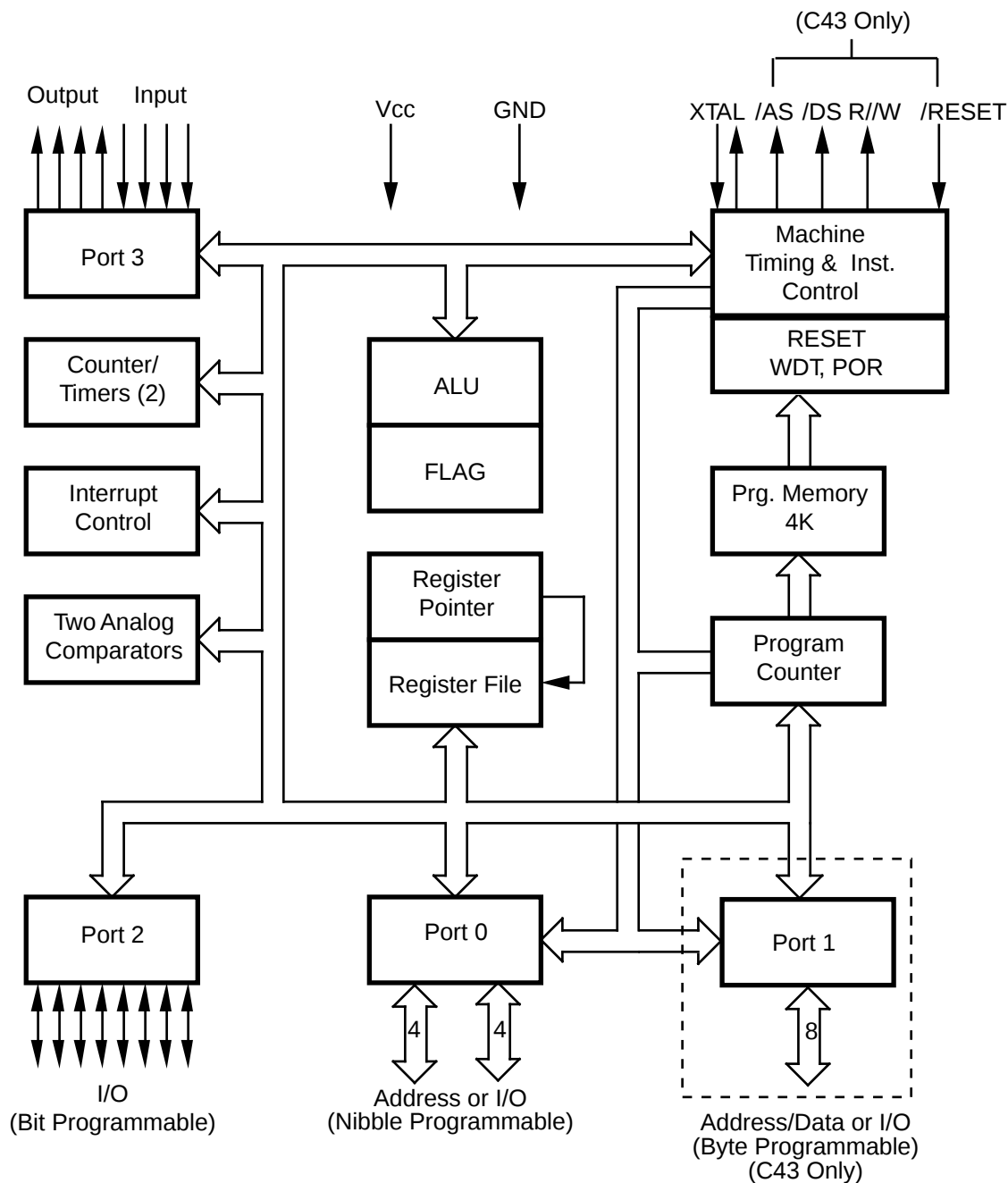
Notes:

All Signals with a preceding front slash, "/", are active Low, e.g.: B/W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

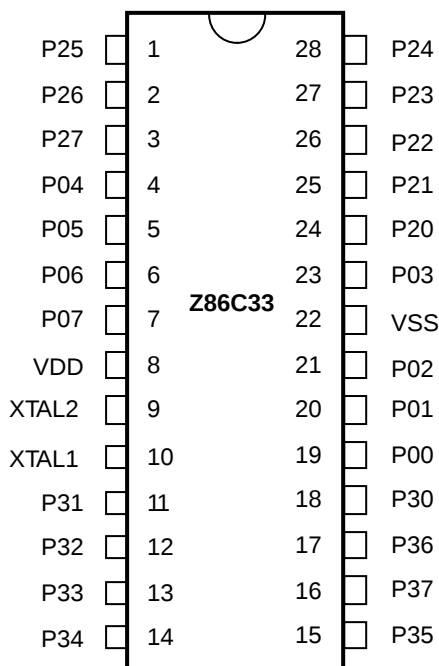
Connection	Circuit	Device
Power Ground	V _{CC} GND	V _{DD} V _{SS}

GENERAL DESCRIPTION (Continued)



Functional Block Diagram

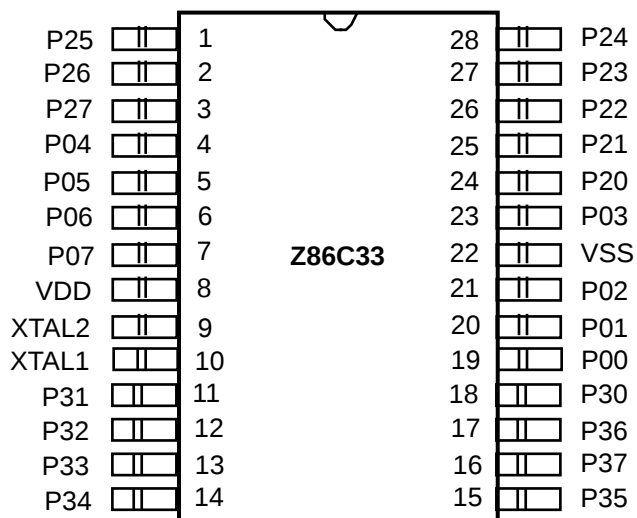
PIN DESCRIPTION



28-Pin DIP/SOIC Pin Identification

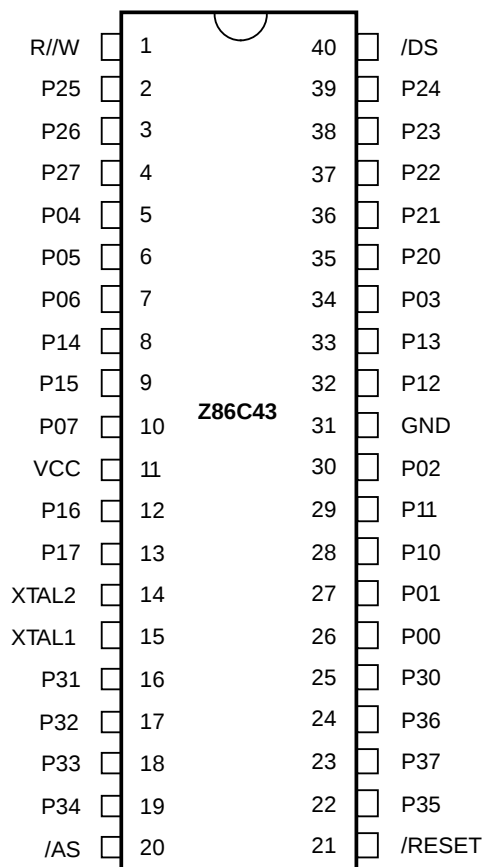
Pin #	Symbol	Function	Direction
1-3	P27-25	Port 2, Pins 5,6,7	In/Output
4-7	P07-04	Port 0, Pins 4,5,6,7	In/Output
8	V _{DD}	Power Supply	
9	XTAL2	Crystal Oscillator	Output
10	XTAL1	Crystal Oscillator	Input
11-13	P33-31	Port 3, Pins 1,2,3	Fixed Input
14-15	P35-4	Port 3, Pins 4,5	Fixed Output
16	P37	Port 3, Pin 7	Fixed Output
17	P36	Port 3, Pin 6	Fixed Output
18	P30	Port 3, Pin 0	Fixed Input
19-21	P02-00	Port 0, Pins 0,1,2	In/Output
22	V _{SS}	Ground	
23	P03	Port 0, Pin 3	In/Output
24-28	P24-20	Port 2, Pins 0,1,2,3,4	In/Output

28-Pin DIP Pin Configuration



28-Pin SOIC Pin Configuration

PIN DESCRIPTION (Continued)

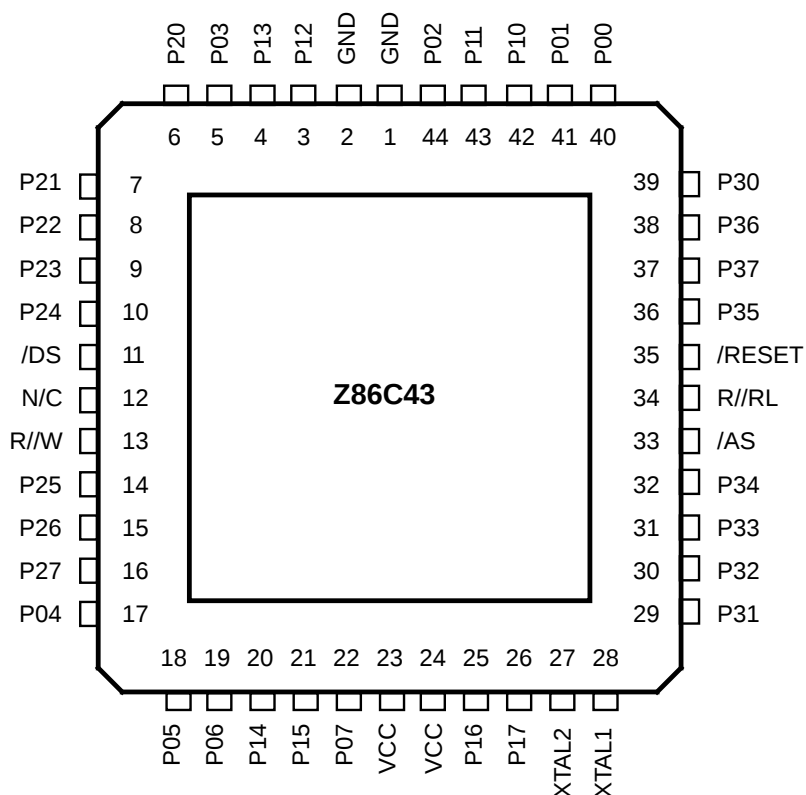


40-Pin DIP Assignments

40-Pin Dual-In-Line Package Pin Identification

Pin #	Symbol	Function	Direction	Pin #	Symbol	Function	Direction
1	R/W	Read/Write	Output	22	P35	Port 3, Pin 5	Output
2-4	P25-27	Port 2, Pins 5,6,7	In/Output	23	P37	Port 3, Pin 7	Output
5-7	P04-06	Port 0, Pins 4,5,6	In/Output	24	P36	Port 3, Pin 6	Output
8-9	P14-15	Port 1, Pins 4,5	In/Output	25	P30	Port 3, Pin 0	Input
10	P07	Port 0, Pin 7	In/Output	26-27	P00-01	Port 0, Pin 0,1	In/Output
11	V _{CC}	Power Supply		28-29	P10-11	Port 1, Pin 0,1	In/Output
12-13	P16-17	Port 1, Pins 6,7	In/Output	30	P02	Port 0, Pin 2	In/Output
14	XTAL2	Crystal, Oscillator Clock	Output	31	GND	Ground	
15	XTAL1	Crystal, Oscillator Clock	Input	32-33	P12-13	Port 1, Pin 2,3	In/Output
16-18	P31-33	Port 3, Pins 1,2,3	Input	34	P03	Port 0, Pin 3	In/Output
19	P34	Port 3, Pin 4	Output	35-39	P20-24	Port 2, Pin 0,1,2,3,4	In/Output
20	/AS	Address Strobe	Output	40	/DS	Data Strobe	Output
21	/RESET	Reset	Input				

PIN DESCRIPTION (Continued)

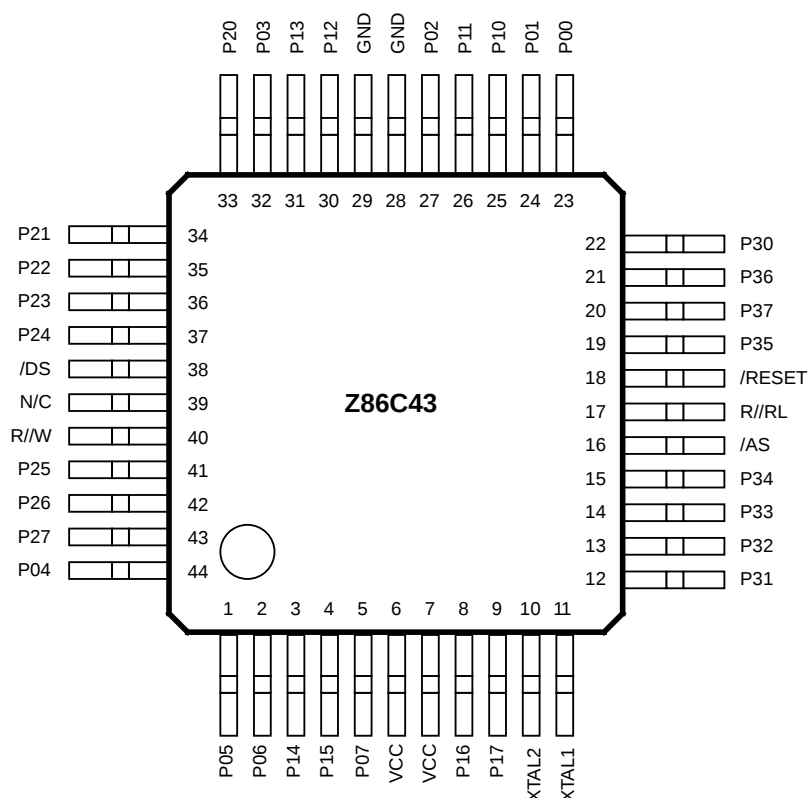


44-Pin PLCC Pin Assignments

44-Pin PLCC Pin Identification

Pin #	Symbol	Function	Direction	Pin #	Symbol	Function	Direction
1-2	GND	Ground		28	XTAL1	Crystal, Oscillator Clock	Input
3-4	P12-13	Port 1, Pins 2,3	In/Output	29-31	P31-33	Port 3, Pins 1,2,3	Input
5	P03	Port 0, Pin 3	In/Output	32	P34	Port 3, Pin 4	Output
6-10	P20-24	Port 2, Pins 0,1,2,3,4	In/Output	33	/AS	Address Strobe	Output
11	/DS	Data Strobe	Output	34	R//RL	ROM/ROMless Control	Input
12	N/C	Not Connected		35	/RESET	Reset	Input
13	R/W	Read/Write	Output	36	P35	Port 3, Pin 5	Output
14-16	P25-27	Port 2, Pins 5,6,7	In/Output	37	P37	Port 3, Pin 7	Output
17-19	P04-06	Port 0, Pins 4,5,6	In/Output	38	P36	Port 3, Pin 6	Output
20-21	P14-15	Port 1, Pins 4,5	In/Output	39	P30	Port 3, Pin 0	Input
22	P07	Port 0, Pin 7	In/Output	40-41	P00-01	Port 0, Pins 0,1	In/Output
23,24	V _{CC}	Power Supply		42-43	P10-11	Port 1, Pins 0,1	In/Output
25-26	P16-17	Port 1, Pins 6,7	In/Output	44	P02	Port 0, Pin 2	In/Output
27	XTAL2	Crystal, Oscillator Clock	Output				

PIN DESCRIPTION (Continued)



44-Pin QFP Pin Assignments

44-Pin QFP Pin Identification

Pin #	Symbol	Function	Direction	Pin #	Symbol	Function	Direction
1-2	P05-06	Port 0, Pins 5,6	In/Output	21	P36	Port 3, Pin 6	Output
3-4	P14-15	Port 1, Pins 4,5	In/Output	22	P30	Port 3, Pin 0	Input
5	P07	Port 0, Pin 7	In/Output	23-24	P00-01	Port 0, Pins 0,1	In/Output
6-7	V _{CC}	Power Supply		25-26	P10-11	Port 1, Pins 0,1	In/Output
8-9	P16-17	Port 1 Pins 6,7	In/Output	27	P02	Port 0, Pin 2	In/Output
10	XTAL2	Crystal, Oscillator Clock	Output	28-29	GND	Ground	
11	XTAL1	Crystal, Oscillator Clock	Input	30-31	P12-13	Port 1, Pins 2,3	In/Output
12-14	P31-33	Port 3, Pins 1,2,3	Input	32	P03	Port 0, Pin 3	In/Output
15	P34	Port 3, Pin 4	Output	33-37	P20-24	Port 2, Pins 0,1,2,3,4	In/Output
16	/AS	Address Strobe	Output	38	/DS	Data Strobe	Output
17	R//RL	ROM/ROMless Control	Input	39	N/C	Not Connected	
18	/RESET	Reset	Input	40	R//W	Read/Write	Output
19	P35	Port 3, Pin 5	Output	41-43	P25-27	Port 2, Pins 5,6,7	In/Output
20	P37	Port 3, Pin 7	Output	44	P04	Port 0, Pin 4	In/Output

ABSOLUTE MAXIMUM RATINGS

Symbol	Description	Min	Max	Units
V_{CC}	Supply Voltage (*)	-0.3	+7.0	V
T_{STG}	Storage Temp	-65	+150	C
T_A	Oper Ambient Temp			C
	Power Dissipation		2.2	W

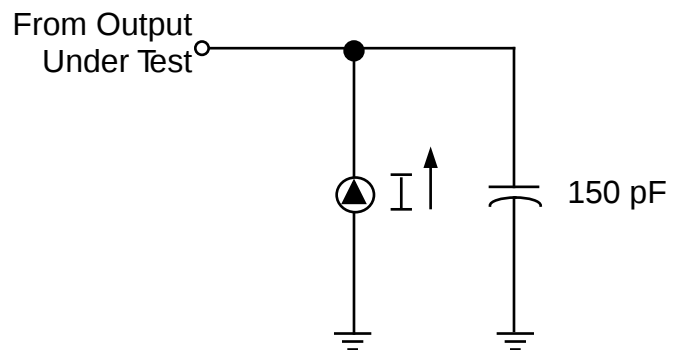
Notes:

* Voltage on all pins with respect to GND.
See Ordering Information.

Stress greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period may affect device reliability.

STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to GND. Positive current flows into the referenced pin (see Test Load Diagram).



Test Load Diagram

CAPACITANCE

$T_A = 25^\circ\text{C}$, $V_{CC} = \text{GND} = 0\text{V}$, $f = 1.0 \text{ MHz}$, Unmeasured pins to GND

Parameter	Max
Input capacitance	12 pF
Output capacitance	12 pF
I/O capacitance	12 pF

DC ELECTRICAL CHARACTERISTICS

Sym	Parameter	V _{CC} Note [3]	T _A = 0° C to +70°C		T _A = -40°C to +105°C		Typical [13] @ 25°C	Units	Conditions	Notes
			Min	Max	Min	Max				
	Max Input Voltage	3.0V		7		7		V	I _{IN} < 250 µA	
		5.5V		7		7		V	I _{IN} < 250 µA	
V _{CH}	Clock Input High Voltage	3.0V	0.7 V _{CC}	V _{CC} +0.3	0.7 V _{CC}	V _{CC} +0.3	1.3	V	Driven by External Clock Generator	
		5.5V	0.7 V _{CC}	V _{CC} +0.3	0.7 V _{CC}	V _{CC} +0.3	2.5	V	Driven by External Clock Generator	
V _{CL}	Clock Input Low Voltage	3.0V	GND-0.3	0.2 V _{CC}	GND-0.3	0.2 V _{CC}	0.7	V	Driven by External Clock Generator	
		5.5V	GND-0.3	0.2 V _{CC}	GND-0.3	0.2 V _{CC}	1.5	V	Driven by External Clock Generator	
V _{IH}	Input High Voltage	3.0V	0.7 V _{CC}	V _{CC} +0.3	0.7 V _{CC}	V _{CC} +0.3	1.3	V		
		5.5V	0.7 V _{CC}	V _{CC} +0.3	0.7 V _{CC}	V _{CC} +0.3	2.5	V		
V _{IL}	Input Low Voltage	3.0V	GND-0.3	0.2 V _{CC}	GND-0.3	0.2 V _{CC}	0.7	V		
		5.5V	GND-0.3	0.2 V _{CC}	GND-0.3	0.2 V _{CC}	1.5	V		
V _{OH1}	Output High Voltage	3.0V	V _{CC} -0.4		V _{CC} -0.4		3.1	V	I _{OH} = -2.0 mA	[8]
		5.5V	V _{CC} -0.4		V _{CC} -0.4		4.8	V	I _{OH} = -2.0 mA	[8]
V _{OL1}	Output Low Voltage	3.0V		0.6		0.6	0.2	V	I _{OL} = +4.0 mA	[8]
		5.5V		0.4		0.4	0.1	V	I _{OL} = +4.0 mA	[8]
V _{OL2}	Output Low Voltage	3.0V		1.2		1.2	0.3	V	I _{OL} = +6 mA	[8]
		5.5V		1.2		1.2	0.3	V	I _{OL} = +12 mA	[8]
V _{RH}	Reset Input High Voltage	3.0V	.8 V _{CC}	V _{CC}	.8 V _{CC}	V _{CC}	1.5	V		
		5.5V	.8 V _{CC}	V _{CC}	.8 V _{CC}	V _{CC}	2.1	V		
V _{RI}	Reset Input Low Voltage	3.0V	GND-0.3	0.2 V _{CC}	GND-0.3	0.2 V _{CC}	1.1	V		
		5.5V	GND-0.3	0.2 V _{CC}	GND-0.3	0.2 V _{CC}	1.7	V		
V _{OFFSET}	Comparator Input Offset Voltage	3.0V		25		25	10	mV		[10]
		5.5V		25		25	10	mV		[10]
I _{IL}	Input Leakage	3.0V	-1	2	-1	2	<1	µA	V _{IN} = 0V, V _{CC}	
		5.5V	-1	2	-1	2	<1	µA	V _{IN} = 0V, V _{CC}	
I _{OL}	Output Leakage	3.0V	-1	1	-1	2	<1	µA	V _{IN} = 0V, V _{CC}	
		5.5V	-1	1	-1	2	<1	µA	V _{IN} = 0V, V _{CC}	
I _{IR}	Reset Input Current	3.0V		-130		-130	-25	µA		
		5.5V		-180		-180	-40	µA		
I _{CC}	Supply Current	3.0V		20		20	7	mA	@ 16 MHz	[4]
		5.5V		25		25	20	mA	@ 16 MHz	[4]
		3.0V		15		15	5	mA	@ 12 MHz	[4]
		5.5V		20		20	15	mA	@ 12 MHz	[4]
I _{CC1}	Standby Current	3.0V		4.5		4.5	2.0	mA	HALT Mode V _{IN} = 0V, V _{CC} @ 16 MHz	[4]
		5.5V		8		8	3.7	mA	HALT Mode V _{IN} = 0V, V _{CC} @ 16 MHz	[4]
		3.0V		3.4		3.4	1.5	mA	Clock Divide-by-16 @ 16 MHz	[4]
		5.5V		7.0		7.0	2.9	mA	Clock Divide-by-16 @ 16 MHz	[4]
I _{CC2}	Standby Current	3.0V		8		8	1	µA	STOP Mode V _{IN} = 0V, V _{CC} WDT is not Running	[6,11]
		5.5V		10		10	2	µA	STOP Mode V _{IN} = 0V, V _{CC} WDT is not Running	[6,11]
		3.0V		500		600	310	µA	STOP Mode V _{IN} = 0V, V _{CC} WDT is Running	[6,11,14]
		5.5V		800		1000	600	µA	STOP Mode V _{IN} = 0V, V _{CC} WDT is Running	[6,11,14]

DC ELECTRICAL CHARACTERISTICS (Continued)

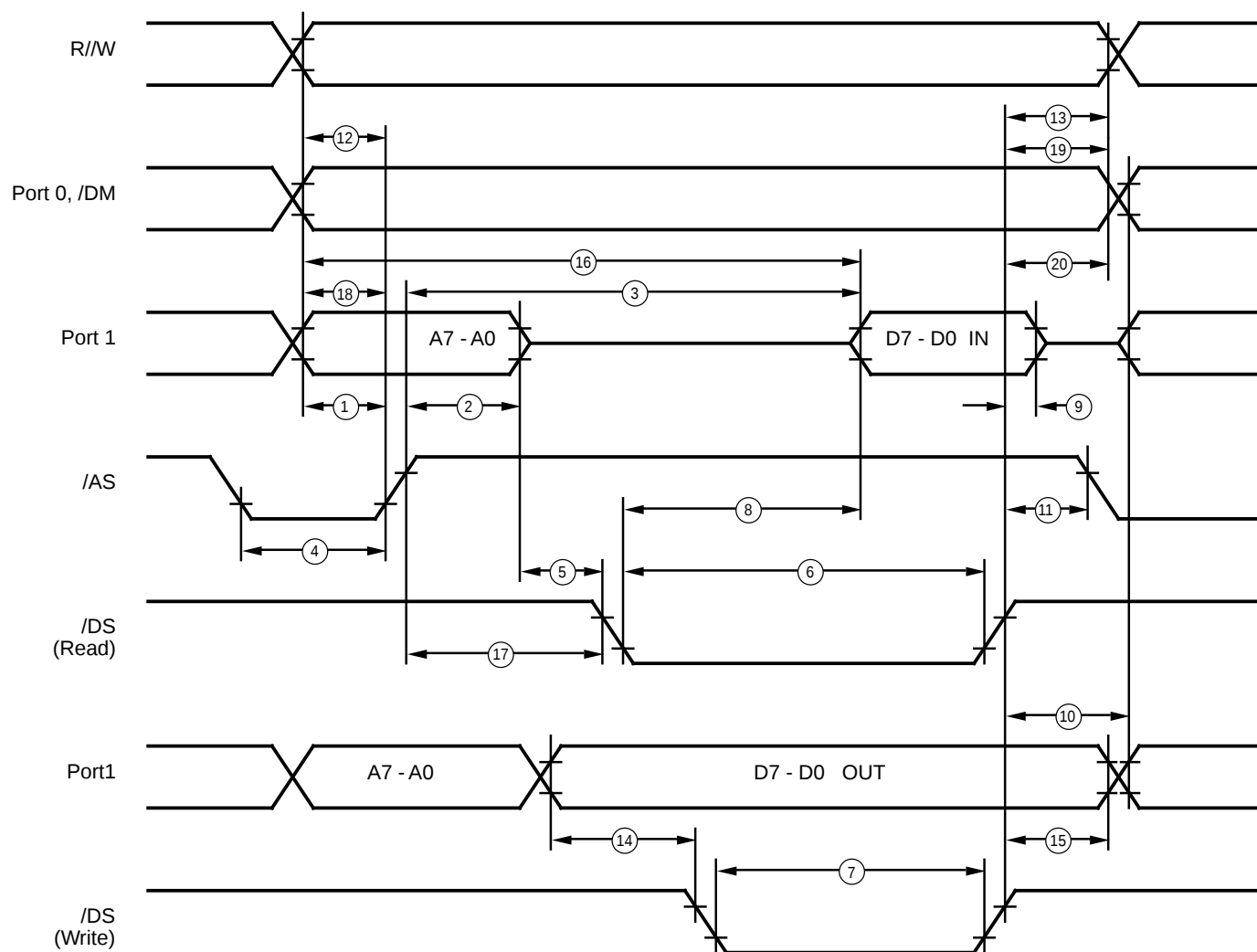
Sym	Parameter	V _{CC} Note [3]	T _A = 0° C to +70° C		T _A = -40° C to +105° C		Typical [13] @ 25° C	Units	Conditions	Notes
			Min	Max	Min	Max				
V ^{ICR}	Input Common Mode Voltage Range	3.0V	0	V _{CC} -1.0V	0	V _{CC} -1.5V		V		[10]
		5.5V	0	V _{CC} -1.0V	0	V _{CC} -1.5V		V		[10]
I _{ALL}	Auto Latch Low Current	3.0V	0.7	8	0.7	10	2.4	μA	0V < V _{IN} < V _{CC}	[9]
		5.5V	1.4	15	1.4	20	4.7	μA	0V < V _{IN} < V _{CC}	[9]
I _{ALH}	Auto Latch High Current	3.0V	-0.6	-5	-0.6	-7	-1.8	μA	0V < V _{IN} < V _{CC}	[9]
		5.5V	-1.0	-8	-1.0	-10	-3.8	μA	0V < V _{IN} < V _{CC}	[9]
V _{LV}	V _{CC} Low Voltage Protection Voltage		2.05	2.95	1.8	3.3	2.6	V	2 MHz max Int. CLK Freq.	[7]
V _{OH}	Output High Voltage (Low EMI Mode)	3.3V	V _{CC} -0.4		V _{CC} -0.4		3.1	V	I _{OH} = -0.5 mA	
		5.0V	V _{CC} -0.4		V _{CC} -0.4		4.8	V	I _{OH} = -0.5 mA	
V _{OL}	Output Low Voltage (Low EMI Mode)	3.3V		0.6		0.6	0.2	V	I _{OL} = 1.0 mA	
		5.0V		0.4		0.4	0.1	V	I _{OL} = 1.0 mA	

Notes:

- [1] I_{CC1} Typ Max Unit Freq
Clock-Driven 0.3 mA 5 mA 8 MHz
Resonator or Crystal 3.0 mA 5 mA 8 MHz [5]
- [2] GND = 0V.
- [3] The V_{DD} voltage specification of 3.0V guarantees 3.3V ±0.3V, and the V_{DD} voltage specification of 5.5V guarantees 5.0V ±0.5V.
- [4] All outputs unloaded, I/O pins floating, inputs at rail.
- [5] CL1 = CL2 = 10 pF.
- [6] Same as note [4] except inputs at V_{CC}.
- [7] The V_{LV} voltage increases as the temperature decreases and will overlap lower V_{CC} operating region.
- [8] Standard Mode (not Low EMI).
- [9] Auto Latch (Mask Option) selected.
- [10] For analog comparator, inputs when analog comparators are enabled.
- [11] Clock must be forced Low, when XTAL 1 is clock-driven and XTAL2 is floating.
- [12] Excludes clock pins.
- [13] Typicals are at V_{CC} = 5.0V and 3.3V.
- [14] Internal RC selected.

AC CHARACTERISTICS

External I/O or Memory Read and Write Timing Diagram (C43 Only)



External I/O or Memory Read/Write Timing
(Z86C43 Only)

AC CHARACTERISTICS

External I/O or Memory Read and Write Timing Table (C43 Only)

(SCLK/TCLK = XTAL/2)

No	Symbol	Parameter	Note [3] V _{CC}	T _A = -0°C to 70°C				T _A = -40°C to +105°C				Units	Notes
				12 MHz		16 MHz		12 MHz		16 MHz			
				Min	Max	Min	Max	Min	Max	Min	Max		
1	TdA(AS)	Address Valid to /AS Rise Delay	3.0	35		25		35		25	ns	[2]	
			5.5	35		25		35		25			
2	TdAS(A)	/AS Rise to Address Float Delay	3.0	45		35		45		35	ns	[2]	
			5.5	45		35		45		35	ns		
3	TdAS(DR)	/AS Rise to Read Data Req'd Valid	3.0		250		180		250		180	ns	[1,2]
			5.5		250		180		250		180	ns	
4	TwAS	/AS Low Width	3.0	55		40		55		40	ns	[2]	
			5.5	55		40		55		40	ns		
5	TdAS(DS)	Address Float to /DS Fall	3.0	0		0		0		0	ns		
			5.5	0		0		0		0	ns		
6	TwDSR	/DS (Read) Low Width	3.0	200		135		200		135	ns	[1,2]	
			5.5	200		135		200		135	ns		
7	TwDSW	/DS (Write) Low Width	3.0	110		80		110		80	ns	[1,2]	
			5.5	110		80		110		80	ns		
8	TdDSR(DR)	/DS Fall to Read Data Req'd Valid	3.0		150		75		150		75	ns	[1,2]
			5.5		150		75		150		75	ns	
9	ThDR(DS)	Read Data to /DS Rise Hold Time	3.00	0		0		0		0	ns	[2]	
			5.5	0		0		0		0	ns		
10	TdDS(A)	/DS Rise to Address Active Delay	3.0	45		50		45		50	ns	[2]	
			5.5	55		50		55		50	ns		
11	TdDS(AS)	/DS Rise to /AS Fall Delay	3.0	30		35		30		35	ns	[2]	
			5.5	45		35		45		55	ns		
12	TdR/W(AS)	R/W Valid to /AS Rise Delay	3.0	45		25		45		25	ns	[2]	
			5.5	45		25		45		25	ns		
13	TdDS(R/W)	/DS Rise to R/W Not Valid	3.0	45		35		45		35	ns	[2]	
			5.5	45		35		45		35	ns		
14	TdDW(DSW)	Write Data Valid to /DS Fall (Write) Delay	3.0	55		25		55		25	ns	[2]	
			5.5	55		25		55		25	ns		
15	TdDS(DW)	/DS Rise to Write Data Not Valid Delay	3.0	45		35		45		35	ns	[2]	
			5.5	45		35		45		35	ns		
16	TdA(DR)	Address Valid to Read Data Req'd Valid	3.0		310		230		310		230	ns	[1,2]
			5.5		310		230		310		230	ns	
17	TdAS(DS)	/AS Rise to /DS Fall Delay	3.0	65		45		65		45	ns	[2]	
			5.5	65		45		65		45	ns		
18	TdDM(AS)	/DM Valid to /AS Fall Delay	3.0	35		30		35		30	ns	[2]	
			5.5	35		30		35		30	ns		
19	TdDS(DM)	/DS Rise to DM Valid Delay		45		35		45		35	ns		
				45		35		45		35	ns		
20	ThDS(AS)	/DS Valid to Address Valid Hold Time		45		35		45		35	ns		
				45		35		45		35	ns		

Notes:

[1] When using extended memory timing add 2 TpC.

[2] Timing numbers given are for minimum TpC.

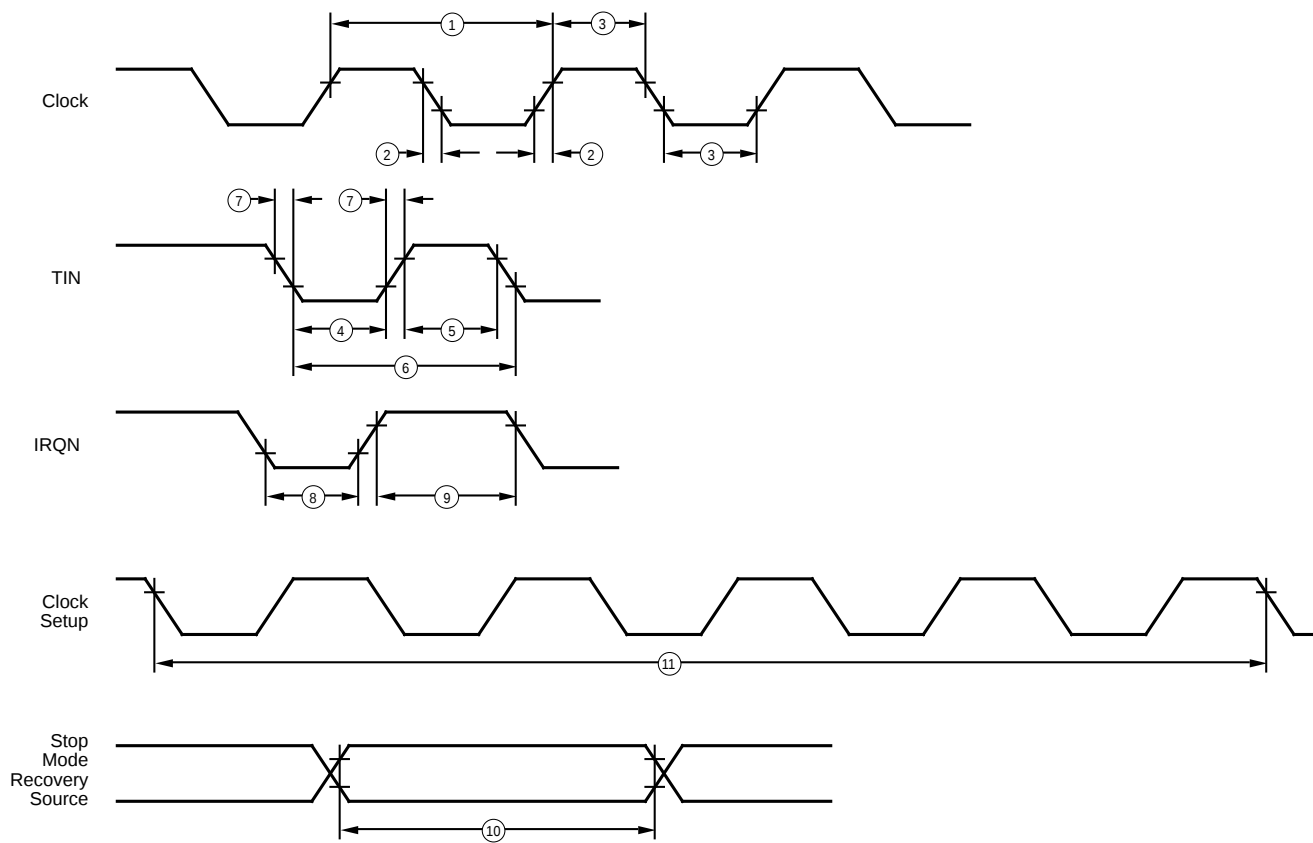
[3] The V_{CC} voltage specification of 3.0V guarantees 3.3V ± 0.3V, and the V_{DD} voltage specification of 5.5V guarantees 5.0V ± 0.5V.

Standard Test Load

All timing references use 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.

AC ELECTRICAL CHARACTERISTICS

Additional Timing Diagram



Additional Timing

AC ELECTRICAL CHARACTERISTICS

Additional Timing Table (SCLK/TCLK = XTAL/2)

No	Symbol	Parameter	V _{CC} Note [6]	T _A = 0°C to +70°C				T _A = -40°C to +105°C				Units	Notes
				12 MHz		16 MHz		12 MHz		16 MHz			
1	TpC	Input Clock Period	3.0V	83	DC	62.5	DC	83	DC	62.5	DC	ns	[1]
			5.5V	83	DC	62.5	DC	83	DC	62.5	DC	ns	[1]
2	TrC,TfC	Clock Input Rise & Fall Times	3.0V		15		15		15		15	ns	[1]
			5.5V		15		15		15		15	ns	[1]
3	TwC	Input Clock Width	3.0V	41		31		41		31		ns	[1]
			5.5V	41		31		41		31		ns	[1]
4	TwTinL	Timer Input Low Width	3.0V	100		100		100		100		ns	[1]
			5.5V	70		70		70		70		ns	[1]
5	TwTinH	Timer Input High Width	3.0V	5TpC		5TpC		5TpC		5TpC			[1]
			5.5V	5TpC		5TpC		5TpC		5TpC			[1]
6	TpTin	Timer Input Period	3.0V	8TpC		8TpC		8TpC		8TpC			[1]
			5.5V	8TpC		8TpC		8TpC		8TpC			[1]
7	TrTin, TfTin	Timer Input Rise & Fall Timer	3.0V		100		100		100		100	ns	[1]
			5.5V		100		100		100		100	ns	[1]
8A	TwIL	Int. Request Low Time	3.0V	100		100		100		100		ns	[1,2]
			5.5V	70		70		70		70		ns	[1,2]
8B	TwIL	Int. Request Low Time	3.0V	5TpC		5TpC		5TpC		5TpC			[1,3]
			5.5V	5TpC		5TpC		5TpC		5TpC			[1,3]
9	TwIH	Int. Request Input High Time	3.0V	5TpC		5TpC		5TpC		5TpC			[1,2]
			5.5V	5TpC		5TpC		5TpC		5TpC			[1,2]
10	Twsm	STOP Mode Recovery Width Spec	3.0V	12		12		12		12		ns	
			5.5V	12		12		12		12		ns	
11	Tost	Oscillator Startup Time	3.0V		5TpC		5TpC		5TpC		5TpC		[4]
			5.5V		5TpC		5TpC		5TpC		5TpC		[4]
12	Twdt	Watch-Dog Timer Delay Time	3.0V	7		7		7		7		ms	D1, D0 0, 0 [5]
			5.5V	3.5		3.5		3.5		3.5		ms	0, 0 [5]
			3.0V	14		14		14		14		ms	0, 1 [5]
			5.5V	7		7		7		7		ms	0, 1 [5]
			3.0V	28		28		28		28		ms	1, 0 [5]
			5.5V	14		14		14		14		ms	1, 0 [5]
			3.0V	112		112		112		112		ms	1, 1 [5]
			5.5V	56		56		56		56		ms	1, 1 [5]
13	T _{POR}	Power-On Reset Delay	3.0V	3	24	3	24	3	25	3	25	ms	
			5.5V	1.5	13	1.5	13	1	14	1	14	ms	

Notes:

[1] Timing Reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.

[2] Interrupt request via Port 3 (P31-P33).

[3] Interrupt request via Port 3 (P30).

[4] SMR-D5 = 0.

[5] Reg. WDTMR.

[6] The V_{CC} voltage specification of 3.0V guarantees 3.3V ± 0.3V, and the V_{DD} voltage specification of 5.5V guarantees 5.0V ± 0.5V.

AC ELECTRICAL CHARACTERISTICS

Additional Timing Table (Divide-By-One Mode, SCLK/TCLK = XTAL)

No	Symbol	Parameter	V _{cc} Note [6]	T _A = 0°C to +70°C		T _A = 40°C to +105°C		Units	Notes
				4 MHz		4 MHz			
1	TpC	Input Clock Period	3.0V	250	DC	250	DC	ns	[1,7,8]
			5.5V	250	DC	250	DC	ns	[1,7,8]
2	TrC,TfC	Clock Input Rise & Fall Times	3.0V		25		25	ns	[1,7,8]
			5.5V		25		25	ns	[1,7,8]
3	TwC	Input Clock Width	3.0V	125		125		ns	[1,7,8]
			5.5V	125		125		ns	[1,7,8]
4	TwTinL	Timer Input Low Width	3.0V	100		100		ns	[1,7,8]
			5.5V	70		70		ns	[1,7,8]
5	TwTinH	Timer Input High Width	3.0V	3TpC		3TpC			[1,7,8]
			5.5V	3TpC		3TpC			[1,7,8]
6	TpTin	Timer Input Period	3.0V	4TpC		4TpC			[1,7,8]
			5.5V	4TpC		4TpC			[1,7,8]
7	TrTin, TfTin	Timer Input Rise & Fall Timer	3.0V		100		100	ns	[1,7,8]
			5.5V		100		100	ns	[1,7,8]
8A	TwIL	Int. Request Low Time	3.0V	100		100		ns	[1,2,7,8]
			5.5V	70		70		ns	[1,2,7,8]
8B	TwIL	Int. Request Low Time	3.0V	3TpC		3TpC			[1,3,7,8]
			5.5V	3TpC		3TpC			[1,3,7,8]
9	TwIH	Int. Request Input High Time	3.0V	3TpC		3TpC			[1,2,7,8]
			5.5V	3TpC		2TpC			[1,2,7,8]
10	Twsm	STOP Mode Recovery Width Spec	3.0V	12		12		ns	[4,8]
			5.5V	12		12		ns	[4,8]
11	Tost	Oscillator Startup Time	3.0V		5TpC		5TpC		[4,8,9]
			5.5V		5TpC		5TpC		[4,8,9]

Notes:

[1] Timing Reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.

[2] Interrupt request via Port 3 (P31-P33).

[3] Interrupt request via Port 3 (P30).

[4] SMR-D5 = 1, POR STOP Mode Delay is on.

[5] Reg. WDTMR.

[6] The V_{CC} voltage specification of 3.0V guarantees 3.3V ± 0.3V, and the V_{DD} voltage specification of 5.5V guarantees 5.0V ± 0.5V.

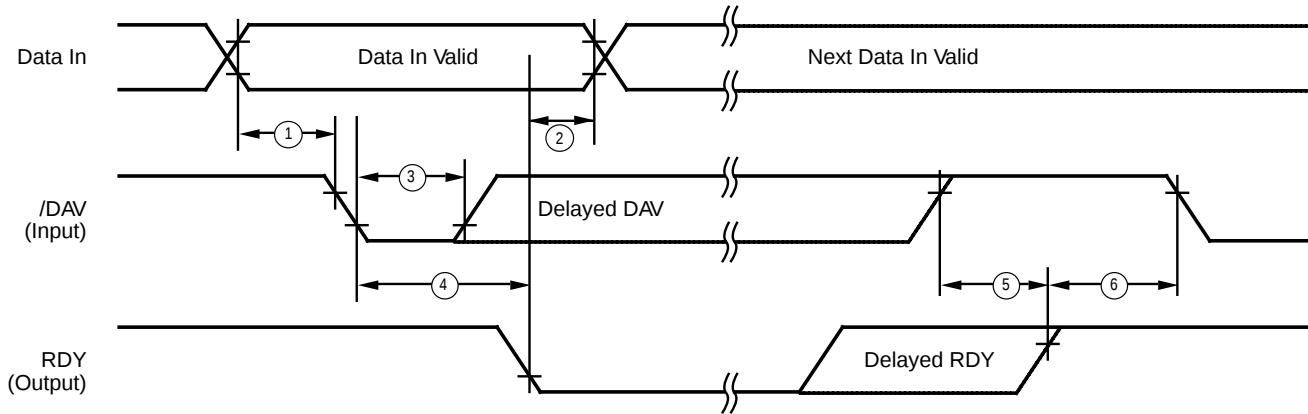
[7] SMR D1 = 0.

[8] Maximum frequency for internal system clock is 4 MHz when using XTAL divide-by-one mode.

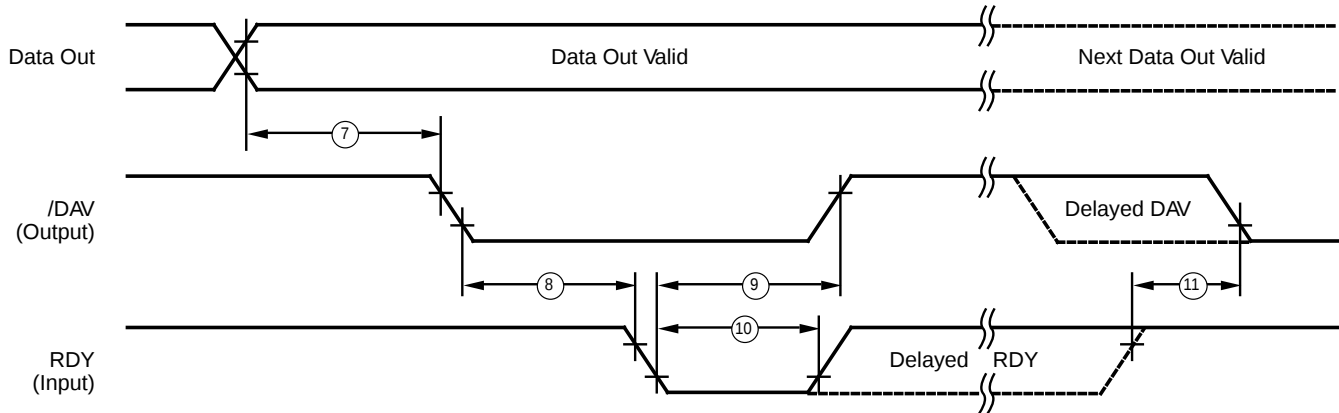
[9] For RC and LC oscillator, and for oscillator driven by clock driver.

AC ELECTRICAL CHARACTERISTICS

Handshake Timing Diagrams



Input Handshake Timing



Output Handshake Timing

AC ELECTRICAL CHARACTERISTICS

Handshake Timing Table

No	Symbol	Parameter	V _{CC} Note [1]	T _A = 0°C to +70°C				T _A = -40°C to +105°C				Direction Data
				12 MHz		16 MHz		12 MHz		16 MHz		
				Min	Max	Min	Max	Min	Max	Min	Max	
1	TsDI(DAV)	Data In Setup Time	3.0V	0		0		0		0		IN
			5.5V	0		0		0		0		IN
2	ThDI(RDY)	Data In Hold Time	3.0V	0		0		0		0		IN
			5.5V	0		0		0		0		IN
3	TwDAV	Data Available Width	3.0V	155		155		155		155		IN
			5.5V	110		110		110		110		IN
4	TdDAVI(RDY)	DAV Fall to RDY Fall Delay	3.0V		0		0		0		0	IN
			5.5V		0		0		0		0	IN
5	TdDAVId(RDY)	DAV Out to DAV Fall Delay	3.0V		120		120		120		120	IN
			5.5V		80		80		80		80	IN
6	RDY0d(DAV)	RDY Rise to DAV Fall Delay	3.0V	0		0		0		0		IN
			5.5V	0		0		0		0		IN
7	TdD0(DAV)	Data Out to DAV Fall Delay	3.0V	42		31		42		31		OUT
			5.5V	42		31		42		31		OUT
8	TdDAV0(RDY)	DAV Fall to RDY Fall Delay	3.0V	0		0		0		0		OUT
			5.5V	0		0		0		0		OUT
9	TdRDY0(DAV)	RDY Fall to DAV Rise Delay	3.0V		160		160		160		160	OUT
			5.5V		115		115		115		115	OUT
10	TwRDY	RDY Width	3.0V	110		110		110		110		OUT
			5.5V	80		80		80		80		OUT
11	TdRDY0d(DAV)	RDY Rise to DAV Fall Delay	3.0V		110		110		110		110	OUT
			5.5V		80		80		80		80	OUT

Notes:

[1] Timing Reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.

[2] The V_{CC} voltage specification of 3.0V guarantees 3.3V ± 0.3V and the V_{DD} voltage specification of 5.5V guarantees 5.0V ± 0.5V.