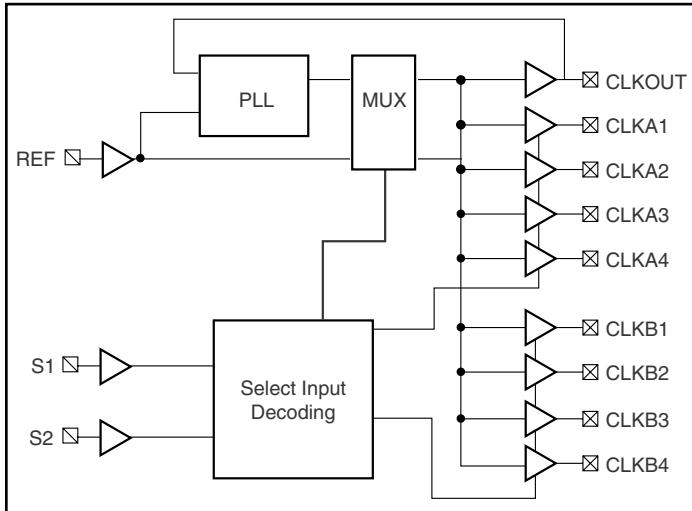


2.5/3.3V 200MHz High-Speed, Low-Jitter, Low-Skew, Zero-Delay Clock Buffer with 9 Outputs
Features

- Phase-Lock Loop Clock Distribution (Zero Input-to-Output Delay)
- Internal feedback connection
- Distributes one-to-two banks of four outputs w/ one CLKOUT (9 - outputs total)
- High-Performance
 - 30 MHz to 220 MHz operation frequency range
 - <100ps output-to-output skew
 - <100ps cycle-to-cycle jitter
 - Low Power Configuration - 26mA (outputs unloaded)
- Spread-spectrum capable
- Power supply: +2.5V ±5% ; +3.3V ±10%
- Industrial temperature range parts available
- Packaging (Pb-free & Green):
 - 16-pin TSSOP (L)
 - 16-pin SOIC (W)

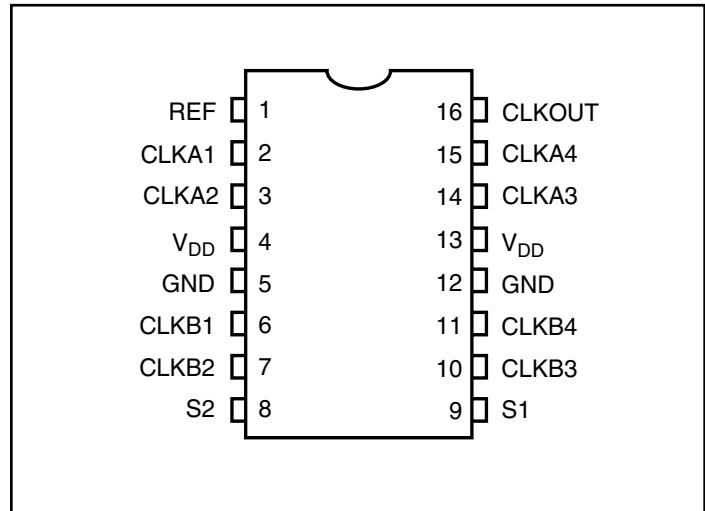
Block Diagram

Description

The PI6C22409 is a low-jitter, low-skew, high-speed Zero-Delay Buffer with 9 outputs designed to address high-speed clock distribution applications.

The PI6C22409 features an internal patented Phase Lock Loop (PLL) with high drive output capability and internal feedback.

The PI6C22409 operates from a 2.5V ±5% or 3.3V ±10% supply. All support documentation can be found on Pericom's web site at: www.pericom.com.

Pericom can customize these devices for specific requirements.

Pin Configuration

Pin Description

Pin	Signal	Description
1	REF	Reference clock input with weak pull down.
2,3,6,7,10,11,14,15	CLKA1, CLKA2, CLKB1, CLKB2, CLKB3, CLKB4, CLKA3, CLKA4, CLKOUT	Clock output. Clock outputs with weak pull-down.
16	CLKOUT	Clock output. Internal feedback on this pin.
5,12	GND	Ground
4,13	V _{DD}	Power
8,9	S2, S1	Select input with weak pull-ups.

Select Input Decoding

S2	S1	Clock A1 - A4	Clock B1 - B4	CLKOUT	Output Source	PLL shutdown
0	0	Tri-State	Tri-State	Driven	PLL	N
0	1	Driven	Tri-State	Driven	PLL	N
1	0	Driven	Driven	Driven	Reference	Y
1	1	Driven	Driven	Driven	PLL	N

Maximum Ratings⁽¹⁾

Supply Voltage	
V _{DD}	-0.5V to +4.6V
REF	-0.5V to +4.6V
Input Current	
Output Current	
Lead Temperature (cap soldering, 10 sec.)	
Storage Temperature (Ts)	
Junction Temperature	
Operating Temperature (cap industrial)	
Operating Temperature (cap commercial)	

Operation Ratings⁽²⁾

Supply voltage	
V _{DD}	+3.0V to +3.6V
V _{DD}	+2.375V to +2.625V
Ambient Temperature (T _A)	
Package Thermal Resistance ⁽²⁾	
θJA	
Still-Air (SOIC-16)	89°C/W
Still-Air (SOIC-16)	90°C/W
θJB	
Junction-to-Board (SOIC-16)	26°C
Junction-to-Board (TSSOP-16)	24°C

Notes:

1. Stresses greater than those listed under Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. θJA and θJB values are determined for a 4-layer board in still-air, unless otherwise stated.

DC Electrical Characteristics

Parameter	Description	Test Conditions		Min.	Max.	Units
V _{IL}	Input LOW Voltage	V _{DD} = 3.3V			0.8	V
		V _{DD} = 2.5V			0.7	
V _{IH}	Input HIGH Voltage	V _{DD} = 3.3V		2.0		V
		V _{DD} = 2.5V			1.7	
I _{IL}	Input LOW Current	V _{IN} = 0V			50	μA
I _{IH}	Input HIGH Current	V _{IN} = V _{DD}			125	
V _{OL}	Output LOW Voltage	I _{OL} = 12mA	V _{DD} = 3.3V		0.4	V
			V _{DD} = 2.5V		0.5	
V _{OH}	Output HIGH Voltage	V _{DD} = 2.5V, I _{OH} = -12mA		1.8		V
		V _{DD} = 3.3V, I _{OH} = -12mA			2.4	
I _{DD}	Supply Current	Unloaded outputs 66 MHz			32	mA

AC Electrical Characteristics

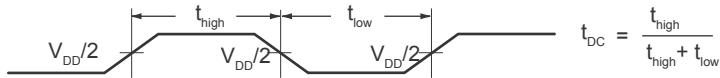
Parameter	Description	Test Conditions	Min.	Typ.	Max.	Units
F _O	Output Frequency	V _{DD} = 2.5V	10		200	MHz
		V _{DD} = 3.3V	10		220	MHz
BW	Bandwidth for PLL	V _{DD} = 2.5V		0.8		MHz
		V _{DD} = 3.3V		1.5		
t _{DC}	Duty Cycle ⁽⁴⁾	Measured at V _{DD} /2, 10 pF load	45	50	55	%
t _R	Rise Time ⁽¹⁾⁽⁴⁾	For 3.3V: Measured between 0.8V and 2.0V; @10pF			1	ns
		For 2.5V: Measured between 0.6V and 1.8V; @10pF			1.8	
t _F	Fall Time ⁽¹⁾⁽⁴⁾	For 3.3V: Measured between 0.8V and 2.0V; @10pF			1	
		For 2.5V: Measured between 0.6V and 1.8V; @10pF			1.8	
t _{sk(o)}	Output to Output skew ⁽¹⁾	All Outputs Equally Loaded	V _{DD} = 3.3V		100	ps
			V _{DD} = 2.5V		100	
t ₀	Delay, REF Rising Edge to CLKOUT Rising Edge ⁽¹⁾⁽²⁾⁽⁵⁾	Measured at V _{DD} /2, 66MHz	V _{DD} = 3.3V	-100	100	
			V _{DD} = 2.5V	-200	0	
t _{SK(D)}	Device-to-device skew ⁽¹⁾⁽³⁾	Measured at V _{DD} /2 on CLK _x pins of device	-300	0	+300	
t _{JIT}	Cycle-to-Cycle Jitter	15pF load, >66MHz, standard drive	V _{DD} = 3.3V		47	110
			V _{DD} = 2.5V		42	90
		15pF load, >66MHz, high drive	V _{DD} = 3.3V		45	100
			V _{DD} = 2.5V		40	80
		30pF load, >66MHz, standard drive	V _{DD} = 3.3V		63	120
			V _{DD} = 2.5V		83	130
		30pF load, >66MHz, high drive	V _{DD} = 3.3V		51	115
			V _{DD} = 2.5V		66	115
t _{PJ}	Period Jitter (Peak)	15pF load, >66MHz, standard drive	V _{DD} = 3.3V		39	90
			V _{DD} = 2.5V		28	60
		15pF load, >66MHz, high drive	V _{DD} = 3.3V		39	85
			V _{DD} = 2.5V		27	55
		30pF load, >66MHz, standard drive	V _{DD} = 3.3V		48	85
			V _{DD} = 2.5V		75	90
		30pF load, >66MHz, high drive	V _{DD} = 3.3V		43	75
			V _{DD} = 2.5V		60	80
t _{LOCK}	PLL Lock time ⁽¹⁾	Stable power supply, valid clocks presented on CLKOUT pin			1	ms

Note:

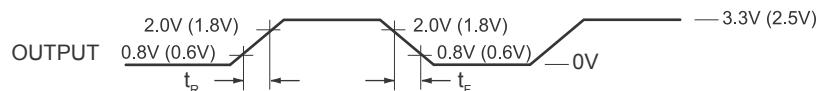
1. See Switching Waveforms
2. All clock output should have the same loading to achieve zero delay between the input and outputs and zero output-to-output skew. Since the CLKOUT pin is the internal feedback to the PLL, its relative loading can adjust to input-to-output delay. If input-to-output delay adjustments are needed, the CLKOUT load may be changed to vary the delay between the REF input to the clock outputs. Output-to-output skew includes CLKA1-4 and CLKB1-4.
3. Specifications are guaranteed by design and not production tested.
4. Measured at 100MHz.
5. Measured with 16-Pin SOIC package

Switching Waveforms

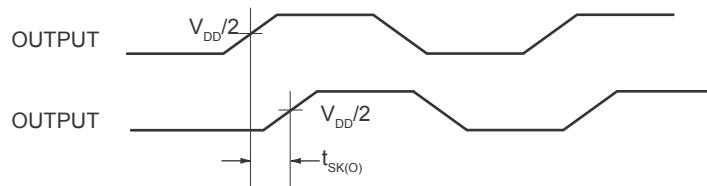
Duty Cycle Timing



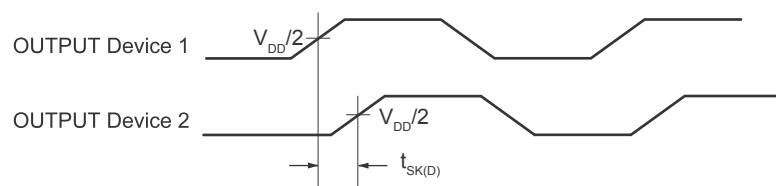
All Outputs Rise/Fall Time



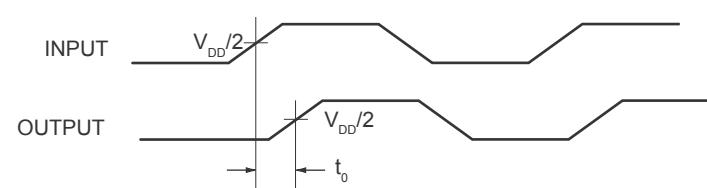
Output – Output Skew



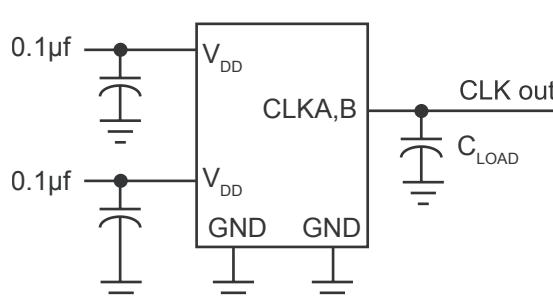
Device – Device Skew



Input-Output Propagation Delay

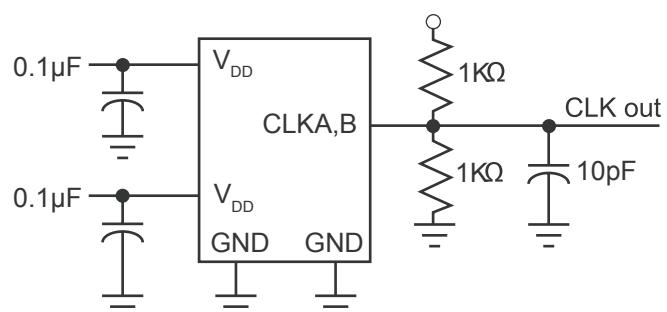


Test Circuit 1

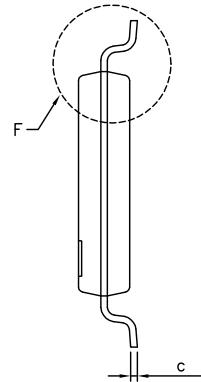
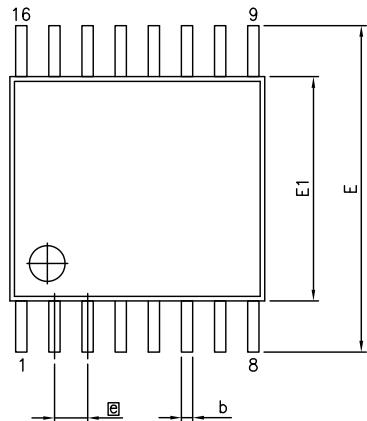


Test Circuit for all parameters except t_{SLEW}

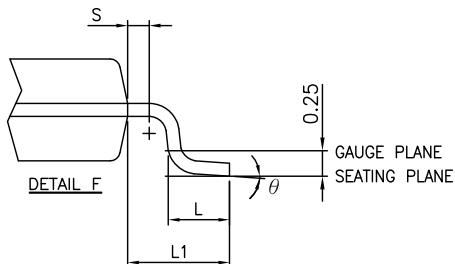
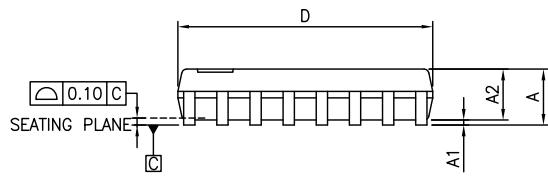
Test Circuit 2



Test Circuit for t_{SLEW} Output slew

Packaging Mechanical: 16-Pin TSSOP (L)

VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	NOM.	MAX.
A	—	—	1.20
A1	0.05	—	0.15
A2	0.80	—	1.05
b	0.19	—	0.30
c	0.09	—	0.20
D	4.90	5.00	5.10
E1	4.30	4.40	4.50
E	6.40 BSC		
[e]	0.65 BSC		
L1	1.00 REF		
L	0.45	0.60	0.75
S	0.20	—	—
θ	0°	—	8°


Notes:

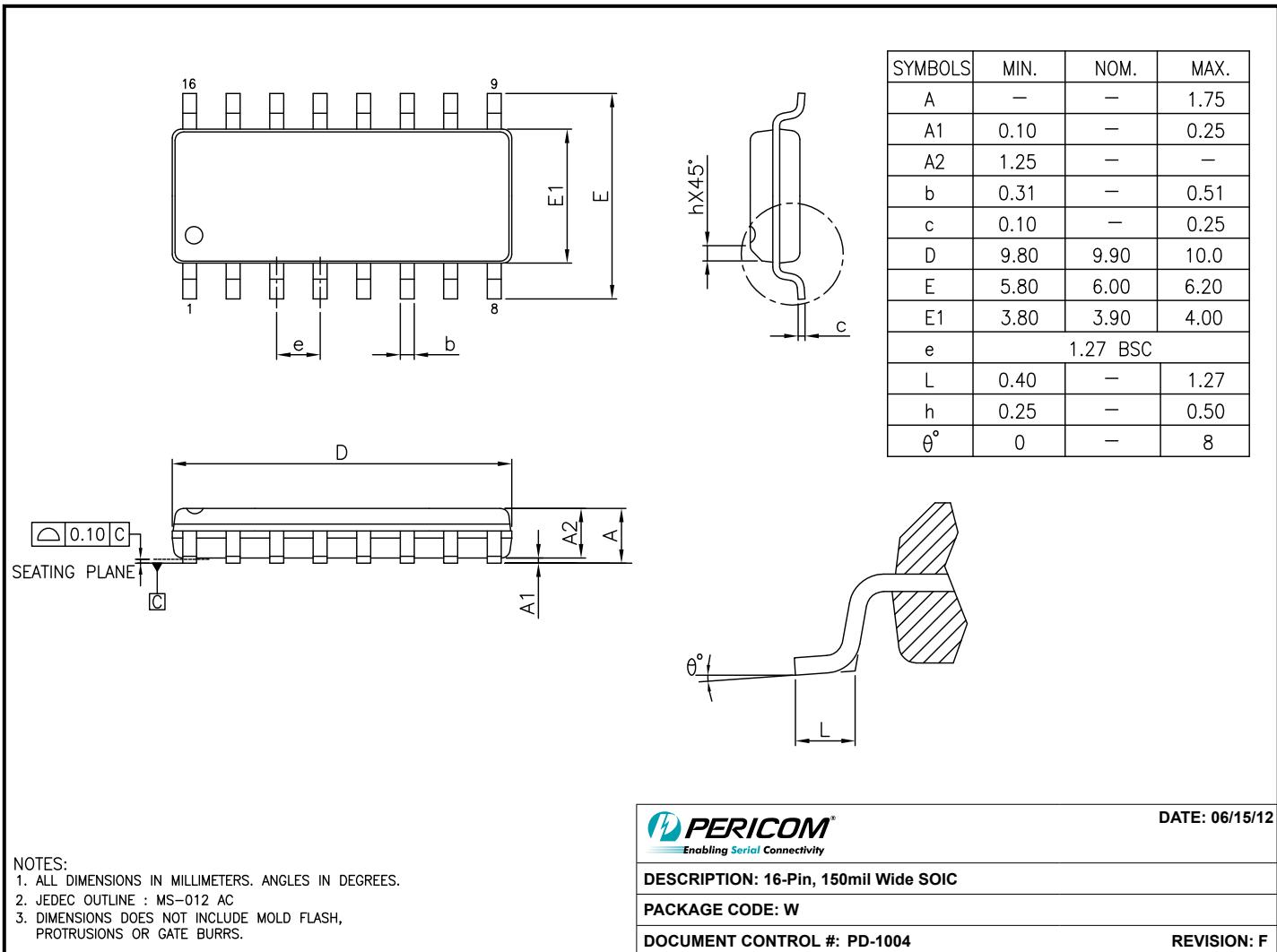
1. Refer JEDEC MO-153F/AB
2. Controlling dimensions in millimeters
3. Package outline exclusive of mold flash and metal burr


DATE: 05/03/12
DESCRIPTION: 16-Pin, 173mil Wide TSSOP
PACKAGE CODE: L
DOCUMENT CONTROL #: PD-1310
REVISION: F

12-0372

Note:

- For latest package info, please check: <http://www.pericom.com/products/packaging/mechanicals.php>

Packaging Mechanical: 16-Pin SOIC (W)


2012-0398

Note:

- For latest package info, please check: <http://www.pericom.com/products/packaging/mechanicals.php>

Ordering Information^(1,2,3)

Ordering Code	Package Code	Package Type
PI6C22409LE	L	Pb-free & Green, 16-pin TSSOP
PI6C22409LIE	L	Pb-free & Green, 16-pin TSSOP, Industrial temp range
PI6C22409WE	W	Pb-free & Green, 16-pin SOIC
PI6C22409WIE	W	Pb-free & Green, 16-pin SOIC, Industrial temp range

Notes:

1. Thermal characteristics can be found on the company web site at www.pericom.com/packaging/
2. E = Pb-free and Green
3. Adding an X suffix = Tape/Reel

Mouser Electronics

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Click to View Pricing, Inventory, Delivery & Lifecycle Information:

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[PI6C22409LIEX](#) [PI6C22409WIE](#) [PI6C22409LIE](#) [PI6C22409WEX](#) [PI6C22409WIEX](#) [PI6C22409LE](#) [PI6C22409LEX](#)
[PI6C22409WE](#)