

Z8 Encore! XP F1680 Series MCU for All Date Codes

The errata listed in Table 1 is found in Z8 Encore! XP F1680 Series devices with any package date code. When reviewing the following errata, it is recommended that you download the most recent version of the product specification, [Z8 Encore! XP F1680 Series Product Specification \(PS0250\)](#), from www.zilog.com.

Table 1. Errata to the Z8 Encore! XP F1680 Series Devices

No.	Summary	Detailed Description
1	Voltage Brown-Out Protection	<p>The VBO trip point specification for the Z8F1680 is 1.4V to 1.8V. Zilog does not guarantee functionality of the product outside the operating range of 1.8V to 3.6V. Because of this, there is a risk that the product might not function properly before reaching the VBO threshold. Bits 5–7 of trim bit address 0003H are now “Reserved” to preserve the 1.6V to 1.8V VBO trip point specification.</p> <p>Suggested Workarounds</p> <ol style="list-style-type: none"> 1. Enable the <i>WDT Always On</i> Flash Option 0 bit 3 (VBO_AO) and the <i>Flash Write Protect</i> Flash Option 0 bit 0 (FWP) features. If the device stops functioning, then the WDT will automatically reset the device. The WDT normally requires the WDT instruction to start the WDT counting. If the device happens to reset in a nonoperational region, then the WDT instruction might not get executed. Enabling the <i>WDT Always On</i> feature starts the WDT counting upon application of system power. Enabling the <i>Flash Write Protect</i> feature prevents the <i>WDT Always On</i>, the <i>Flash Write Protect</i> Flash option bits, and the Flash Program Memory from being erased or reprogrammed accidentally when the device becomes nonfunctional. In summary, set VBO_AO=0 and FWP=0. 2. If the user application requires erasing/programming of the Flash Program Memory so that the <i>Flash Write Protect</i> feature cannot be used in the normal operating supply voltage range, then the <i>Flash write operation protect</i> Flash Option 1 bit 5 (FLASH_WR_PRO_EN) and the Low Voltage Detection (LVD) feature can be used in conjunction with the Flash Option 0 <i>WDT Always On</i> feature instead. <p>For example, the user selects the LVD threshold at 2.0V. When the supply voltage drops below 2.0V and into a nonoperational region, the LVD is triggered to enable the <i>Flash Write Protect</i> Flash Option feature. Flash memory is now erase/program protected. If the device hangs, then the WDT will continue to reset the device. The supply voltage now rises above 2.0V. The LVD triggers the disabling of the <i>Flash Write Protect</i> Flash Option feature. The WDT time-out and device resets and continues proper execution.</p> <p>Enabling these three features will protect the device, Flash Program Memory, and Flash Option bits from corruption when the device is in a nonoperational supply voltage region. The LVD can be enabled in the Power Control Register by setting bit 4 (LVD/VBO) option to 0. The <i>Flash write operation protect</i> Flash Option 1 bit 5 (FLASH_WR_PRO_EN) is set to 1. In summary set LVD/VBO=0, VBO_AO=0, and FLASH_WR_PRO_EN=1.</p>

Table 1. Errata to the Z8 Encore! XP F1680 Series Devices (Continued)

No.	Summary	Detailed Description
2	IRDA Infrared Encoder/Decoder not functional	The IRDA Infrared Encoder/Decoder of the Z8F1680AC is currently not functional. After a power-on-reset event, the default condition of the IRDA Block is disabled. U0MDSTAT (Address = F44H) bits 7–5 default to 000H on reset, and U0CTL1 (Address = F43H) Bit 0 defaults to 0 (disabled) on reset. Bit 0 of F43H is now reserved and must be 0.
3	Flash Write Operation Protect	<p>Devices have V_{th_pro} too low to write protect Flash memory at low voltage. Device V_{th_pro} is below the minimum specification limit of 2.4V. Writing to Flash memory below 2.4V will be unreliable and is not recommended.</p> <p>Suggested Workaround Write to the Flash memory at 2.7V or above only.</p>
4	Analog Comparator Internal Reference	<p>The internal V_{REF} for the Analog Comparator meets a variation of 0.88V to 1.12V instead of the current specification limits of 0.9V to 1.1V.</p> <p>Workaround None</p>
5	IrDA has excessive error rate	<p>Due to insufficient synchronization, pulse widths less than 2.17μs can result in data corruption or loss of synchronization depending on the data being sent. The IrDA specification permits a minimum pulse width of 1.41μs.</p> <p>Workaround An external synchronizing circuit can be used to capture and synchronize data to the device. Possible software solutions exist. Contact Zilog technical support for further information.</p>
6	Reenabling VBO causes a System Reset	<p>The F1680 series has a Voltage Brown-Out (VBO) feature where the user can disable VBO circuit by setting bit 4=1 in the Power Control Register 0 and re-enable the VBO circuit by resetting bit 4=0. The User should beware that re-enabling the VBO circuit on some devices can cause a System Reset.</p> <p>Workaround</p> <ol style="list-style-type: none"> 1. Keep the VBO always enabled by setting Program Memory Address 0000H Flash Option Bit 3 (VBO_AO) = 1. 2. Keep the VBO always disabled and use an external voltage supervisor circuit connected to the F1680 /RESET pin.

Table 1. Errata to the Z8 Encore! XP F1680 Series Devices (Continued)

No.	Summary	Detailed Description
7	Secondary Oscillator Ready (SECRDY) Flag in the Oscillator Control1 Register Does Not Function Properly	<p>The Secondary Oscillator Ready (SECRDY) flag in the Oscillator Control1 Register's Bit 6 location does not function properly. It does not monitor whether the Secondary Oscillator is oscillating. After it is set, the SECRDY flag remains in the 1 state after any VBO, WDT, or RESET pin Reset. Zilog recommends not using the SECRDY flag.</p> <p>The SECRDY Flag is used to determine when the external peripheral secondary 32kHz crystal oscillator is ready for use. A 0 state corresponds to 32kHz crystal oscillator is not ready for use, while a 1 state denotes that the 32kHz crystal oscillator is ready for use.</p> <p>During Power-On Reset (POR), the SECRDY flag is reset to a 0 state. When the Secondary Oscillator Enable (SECEN) bit is set to a 1 state, the SECRDY flag will be set to a 1 state after a delay of 11,111,111 system clocks, regardless of whether the 32kHz peripheral oscillator is oscillating or not. After it is set to a 1 state, only a rising transition of V_{DD} across the POR V_{TH} threshold (typically about 0.6V) will reset the SECRDY flag back to a 0 state. A VBO, WDT, or a RESET pin Reset will not reset the SECRDY flag back to a 0 state. In addition, disabling the 32kHz peripheral oscillator will not clear the SECRDY flag.</p> <p>Workaround</p> <p>Enable the 32kHz crystal and select it as the clock source for Timer #1. Set Timer #1 to count a set number of counts (e.g., 4000 counts), by setting the reload registers to this count value. When the timer reaches the reload value, the 32kHz crystal is ready for use.</p>



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