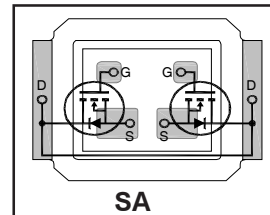


DirectFET[®]plus Power MOSFET ②

Typical values (unless otherwise specified)

V_{DSS}	V_{GS}	$R_{DS(on)}$		$R_{DS(on)}$	
25V max	±16V max	3.2mΩ @ 10V		4.5mΩ @ 4.5V	
$Q_g\ tot$	Q_{gd}	Q_{gs2}	Q_{rr}	Q_{oss}	$V_{gs(th)}$
8.8nC	3.1nC	1.1nC	22nC	13nC	1.6V

- RoHs Compliant Containing No Lead and Bromide ①
- Low Profile (<0.7 mm)
- Dual Sided Cooling Compatible ①
- Low Package Inductance
- Optimized for High Frequency Switching ①
- Ideal for CPU Core DC-DC Converters
- Optimized for Control FET socket of Sync. Buck Converter①
- Low Conduction and Switching Losses
- Compatible with existing Surface Mount Techniques ①
- 100% Rg tested



Applicable DirectFET Outline and Substrate Outline (see p.7,8 for details)①

SQ	SX	ST	SA	MQ	MX	MT	MP	MB		
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Description

The IRF6802SDTRPbF combines the latest HEXFET[®] Power MOSFET Silicon technology with the advanced DirectFET[®] packaging to achieve improved performance in a package that has the footprint of a MICRO-8 and only 0.7 mm profile. The DirectFET[®] package is compatible with existing layout geometries used in power applications, PCB assembly equipment and vapor phase, infra-red or convection soldering techniques, when application note AN-1035 is followed regarding the manufacturing methods and processes. The DirectFET[®] package allows dual sided cooling to maximize thermal transfer in power systems, improving previous best thermal resistance by 80%.

The IRF6802SDTRPbF has low gate resistance and low charge along with ultra low package inductance providing significant reduction in switching losses. The reduced losses make this product ideal for high efficiency DC-DC converters that power the latest generation of processors operating at higher frequencies. The IRF6802SDTRPbF has been optimized for the control FET socket of synchronous buck operating from 12 volt bus converters.

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{DS}	Drain-to-Source Voltage	25	V
V_{GS}	Gate-to-Source Voltage	±16	V
$I_D @ T_A = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$ ③	16	A
$I_D @ T_A = 70^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$ ③	13	A
$I_D @ T_C = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$ ④	57	A
I_{DM}	Pulsed Drain Current ⑤	130	A
E_{AS}	Single Pulse Avalanche Energy ⑥	66	mJ
I_{AR}	Avalanche Current ⑤	13	A

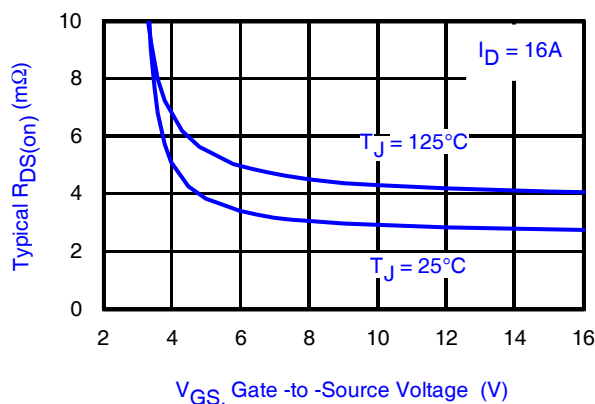


Fig 1. Typical On-Resistance vs. Gate Voltage

Notes:

- ① Click on this section to link to the appropriate technical paper.
- ② Click on this section to link to the DirectFET Website.
- ③ Surface mounted on 1 in. square Cu board, steady state.

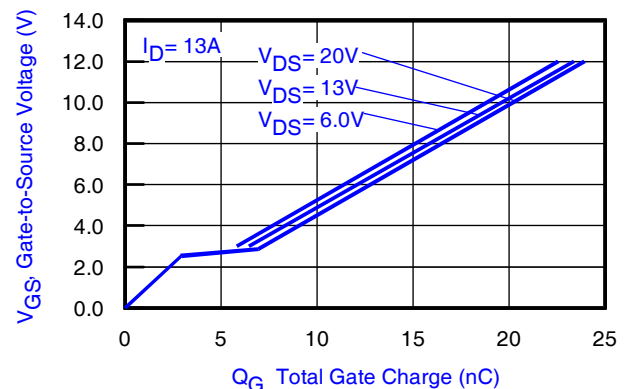


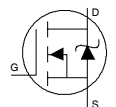
Fig 2. Typical Total Gate Charge vs. Gate-to-Source Voltage

- ④ T_C measured with thermocouple mounted to top (Drain) of part.
- ⑤ Repetitive rating; pulse width limited by max. junction temperature.
- ⑥ Starting $T_J = 25^\circ\text{C}$, $L = 0.78\text{mH}$, $R_G = 50\Omega$, $I_{AS} = 13\text{A}$.

Static @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	25	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.02	—	V/ $^\circ\text{C}$	Reference to $25^\circ\text{C}, I_D = 1.0\text{mA}$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	3.2	4.2	m Ω	$V_{GS} = 10V, I_D = 16A$ ⑦
		—	4.5	5.9		$V_{GS} = 4.5V, I_D = 13A$ ⑦
$V_{GS(th)}$	Gate Threshold Voltage	1.1	1.6	2.1	V	$V_{DS} = V_{GS}, I_D = 35\mu A$
$\Delta V_{GS(th)}/\Delta T_J$	Gate Threshold Voltage Coefficient	—	-5.9	—	mV/ $^\circ\text{C}$	$V_{DS} = V_{GS}, I_D = 35\mu A$
I_{DSS}	Drain-to-Source Leakage Current	—	—	1.0	μA	$V_{DS} = 20V, V_{GS} = 0V$
		—	—	150		$V_{DS} = 20V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 16V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -16V$
g_{fs}	Forward Transconductance	160	—	—	S	$V_{DS} = 13V, I_D = 13A$
Q_g	Total Gate Charge	—	8.8	13	nC	$V_{DS} = 13V$ $V_{GS} = 4.5V$ $I_D = 13A$ See Fig.15
Q_{gs1}	Pre-V _{th} Gate-to-Source Charge	—	2.3	—		
Q_{gs2}	Post-V _{th} Gate-to-Source Charge	—	1.1	—		
Q_{gd}	Gate-to-Drain Charge	—	3.1	—		
Q_{godr}	Gate Charge Overdrive	—	2.3	—		
Q_{sw}	Switch Charge ($Q_{gs2} + Q_{gd}$)	—	4.2	—	nC	$V_{DS} = 20V, V_{GS} = 0V$
Q_{oss}	Output Charge	—	13	—		
R_G	Gate Resistance	—	0.70	—	Ω	
$t_{d(on)}$	Turn-On Delay Time	—	9.7	—	ns	$V_{DD} = 13V, V_{GS} = 4.5V$ ⑦ $I_D = 13A$ $R_G = 1.5\Omega$ See Fig.17
t_r	Rise Time	—	50	—		
$t_{d(off)}$	Turn-Off Delay Time	—	13	—		
t_f	Fall Time	—	23	—		
C_{iss}	Input Capacitance	—	1350	—	pF	$V_{GS} = 0V$ $V_{DS} = 13V$ $f = 1.0\text{MHz}$
C_{oss}	Output Capacitance	—	400	—		
C_{rss}	Reverse Transfer Capacitance	—	97	—		

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	26	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ⑤	—	—	130		
V_{SD}	Diode Forward Voltage	—	—	1.0	V	$T_J = 25^\circ\text{C}, I_S = 13A, V_{GS} = 0V$ ⑦
t_{rr}	Reverse Recovery Time	—	18	27	ns	$T_J = 25^\circ\text{C}, I_F = 13A$
Q_{rr}	Reverse Recovery Charge	—	22	33	nC	$di/dt = 260A/\mu s$ ⑦

Notes:

 ⑦ Pulse width $\leq 400\mu s$; duty cycle $\leq 2\%$.

Absolute Maximum Ratings

	Parameter	Max.	Units
P_D @ $T_A = 25^\circ\text{C}$	Power Dissipation ③⑩	1.7	W
P_D @ $T_A = 70^\circ\text{C}$	Power Dissipation ③⑩	1.1	
P_D @ $T_C = 25^\circ\text{C}$	Power Dissipation ④	21	
T_P	Peak Soldering Temperature	270	$^\circ\text{C}$
T_J T_{STG}	Operating Junction and Storage Temperature Range	-40 to +150	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JA}$	Junction-to-Ambient ③⑩	—	72	$^\circ\text{C/W}$
$R_{\theta JA}$	Junction-to-Ambient ⑧⑩	12.5	—	
$R_{\theta JA}$	Junction-to-Ambient ⑨⑩	20	—	
$R_{\theta JC}$	Junction-to-Case ④	—	5.9	
$R_{\theta J-PCB}$	Junction-to-PCB Mounted	1.0	—	
	Linear Derating Factor ③	0.014		W/ $^\circ\text{C}$

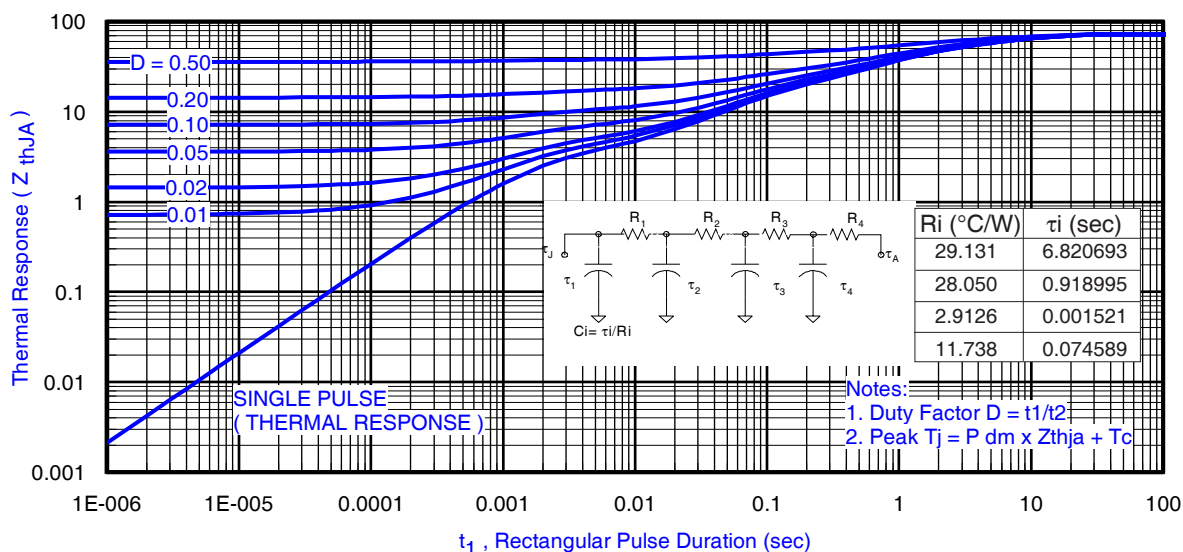
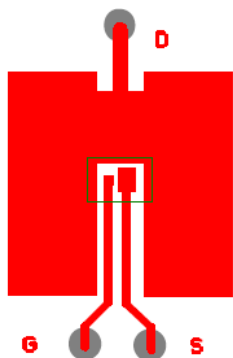


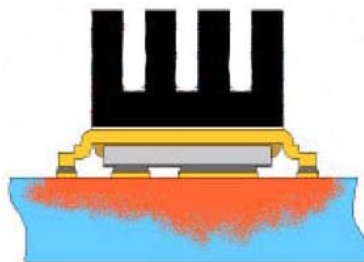
Fig 3. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient ③

Notes:

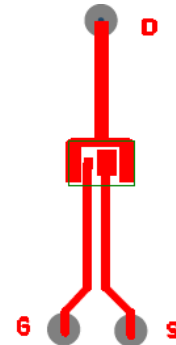
- ③ Used double sided cooling, mounting pad with large heatsink.
- ⑧ R_{θ} is measured at T_J of approximately 90°C .
- ⑨ Mounted on minimum footprint full size board with metalized back and with small clip heatsink.



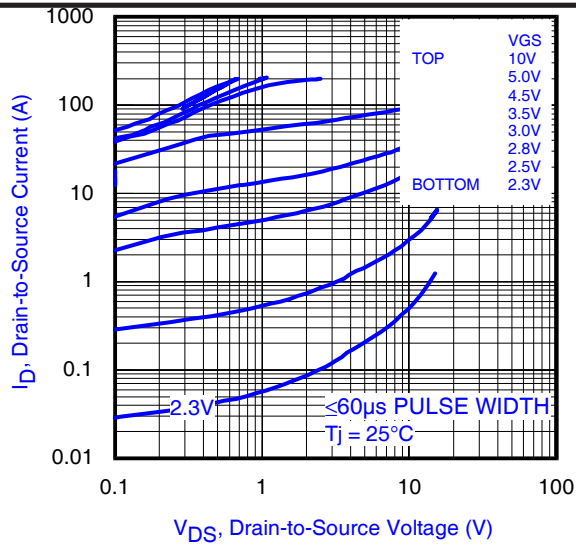
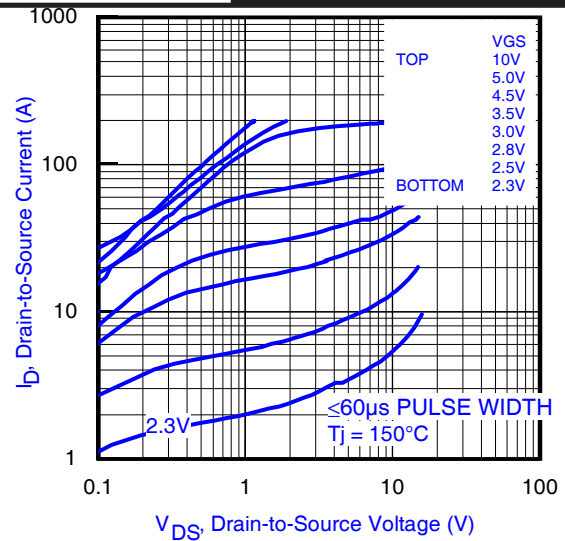
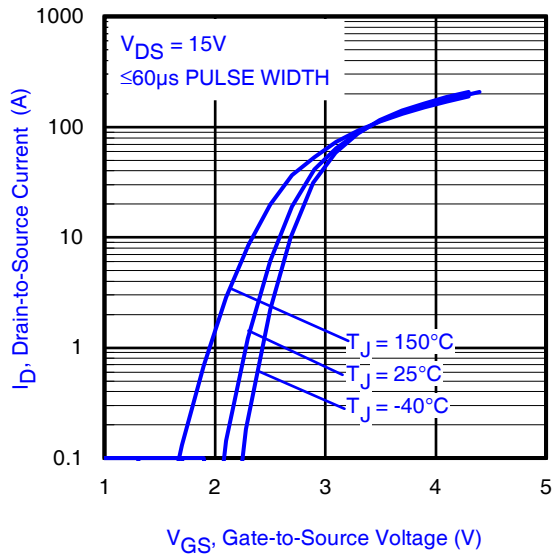
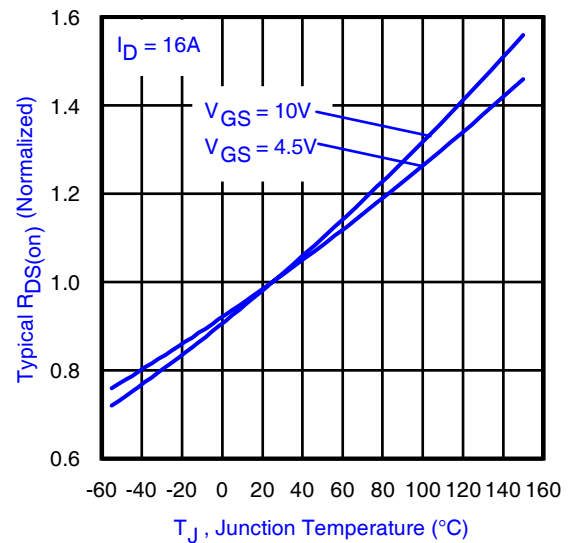
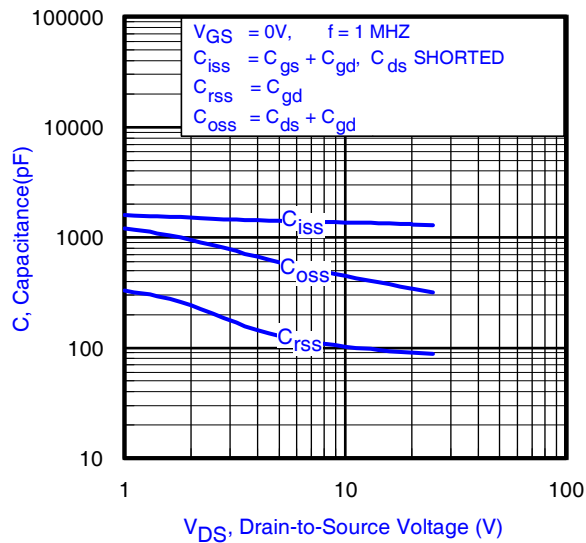
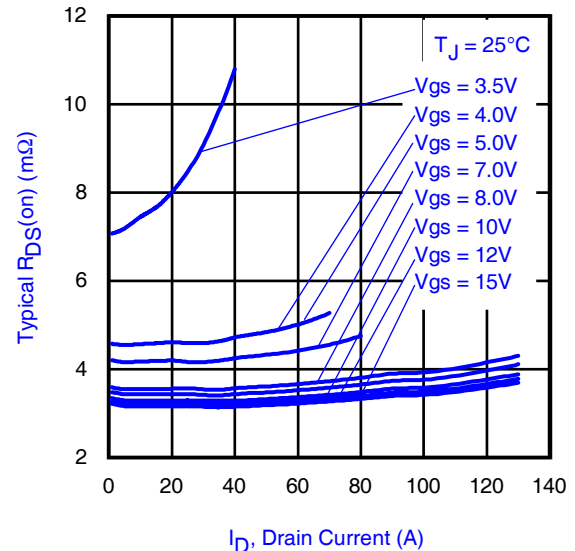
③ Surface mounted on 1 in. square Cu (still air).

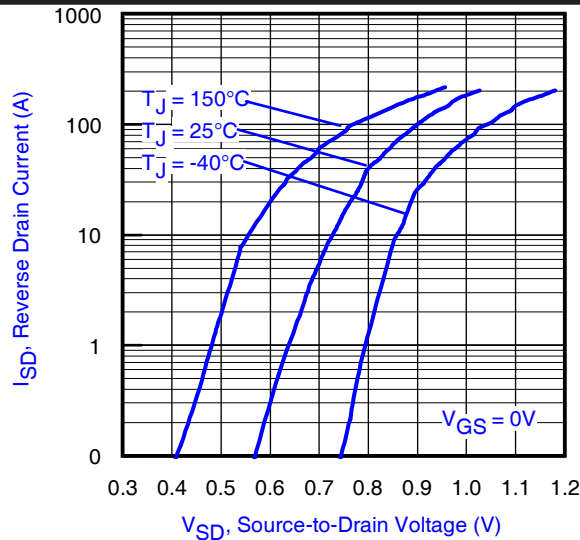
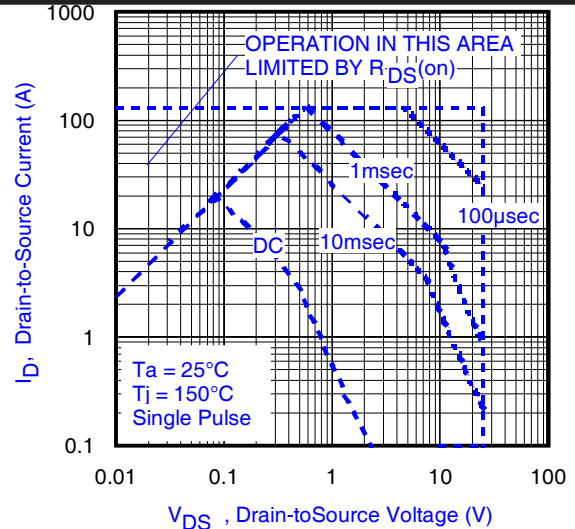
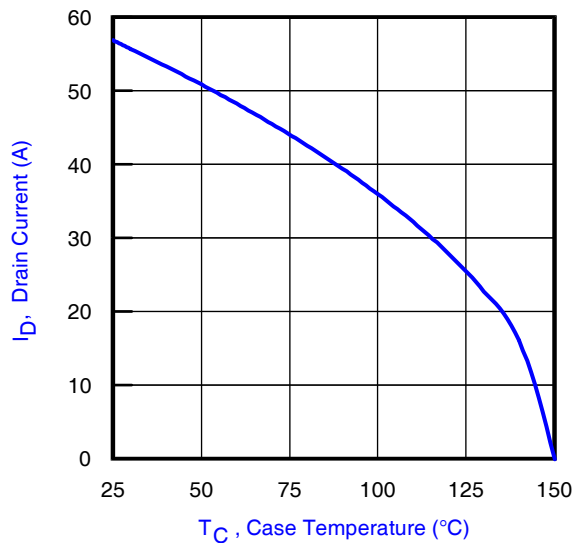
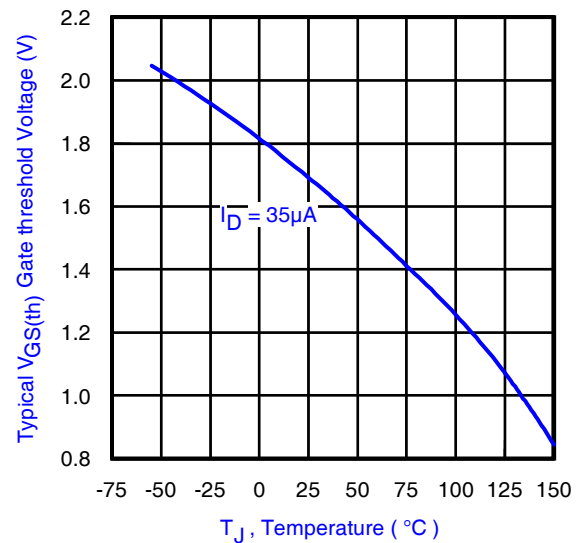
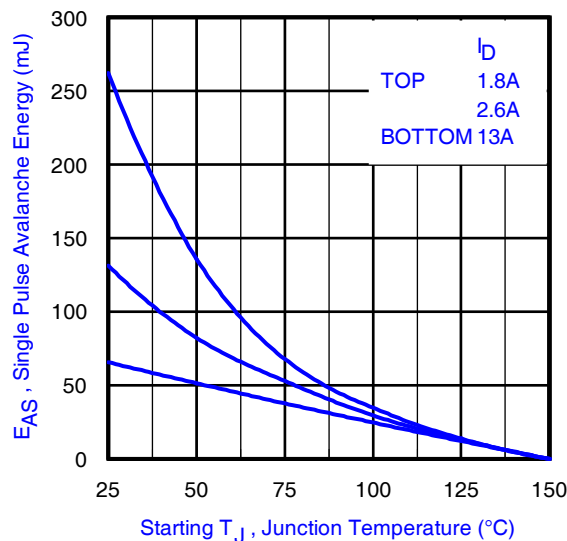


⑧ Mounted to a PCB with small clip heatsink (still air)



⑨ Mounted on minimum footprint full size board with metalized back and with small clip heatsink (still air)


Fig 4. Typical Output Characteristics

Fig 5. Typical Output Characteristics

Fig 6. Typical Transfer Characteristics

Fig 7. Normalized On-Resistance vs. Temperature

Fig 8. Typical Capacitance vs. Drain-to-Source Voltage

Fig 9. Typical On-Resistance vs. Drain Current and Gate Voltage


Fig 10. Typical Source-Drain Diode Forward Voltage

Fig 11. Maximum Safe Operating Area

Fig 12. Maximum Drain Current vs. Case Temperature

Fig 13. Typical Threshold Voltage vs. Junction Temperature

Fig 14. Maximum Avalanche Energy vs. Drain Current

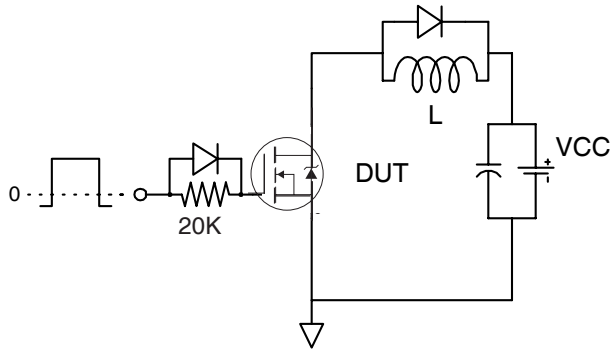


Fig 15a. Gate Charge Test Circuit

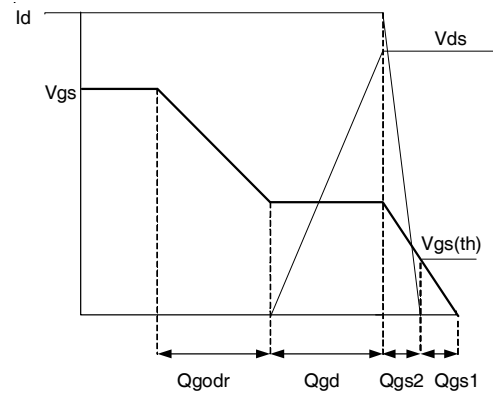


Fig 15b. Gate Charge Waveform

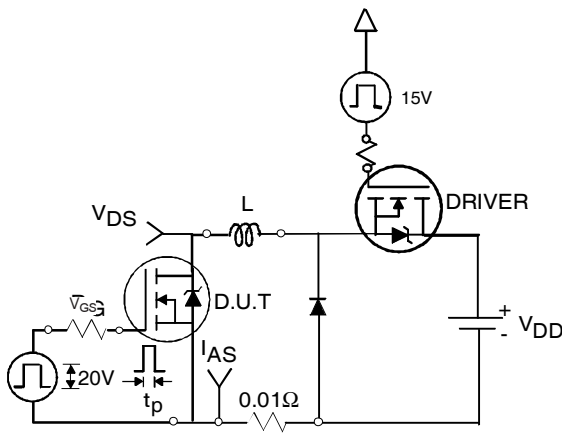


Fig 16a. Unclamped Inductive Test Circuit

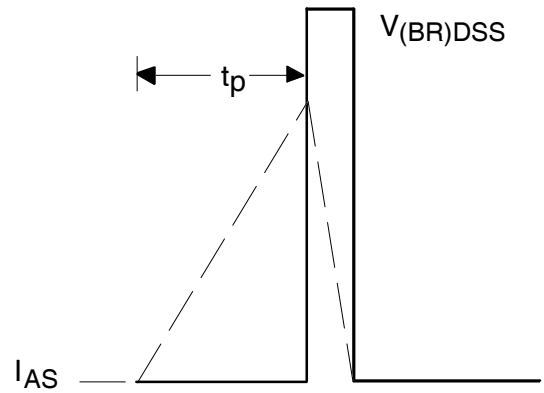


Fig 16b. Unclamped Inductive Waveforms

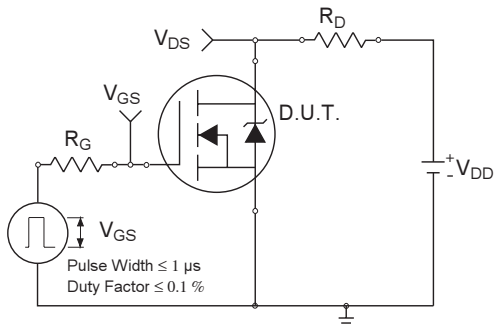


Fig 17a. Switching Time Test Circuit

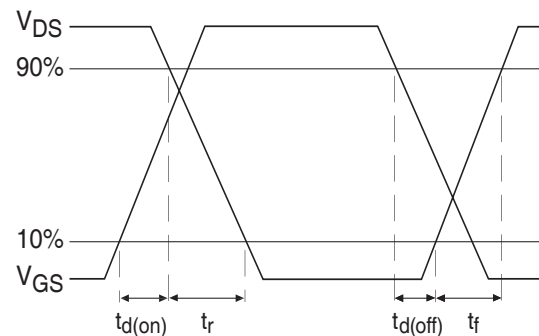


Fig 17b. Switching Time Waveforms

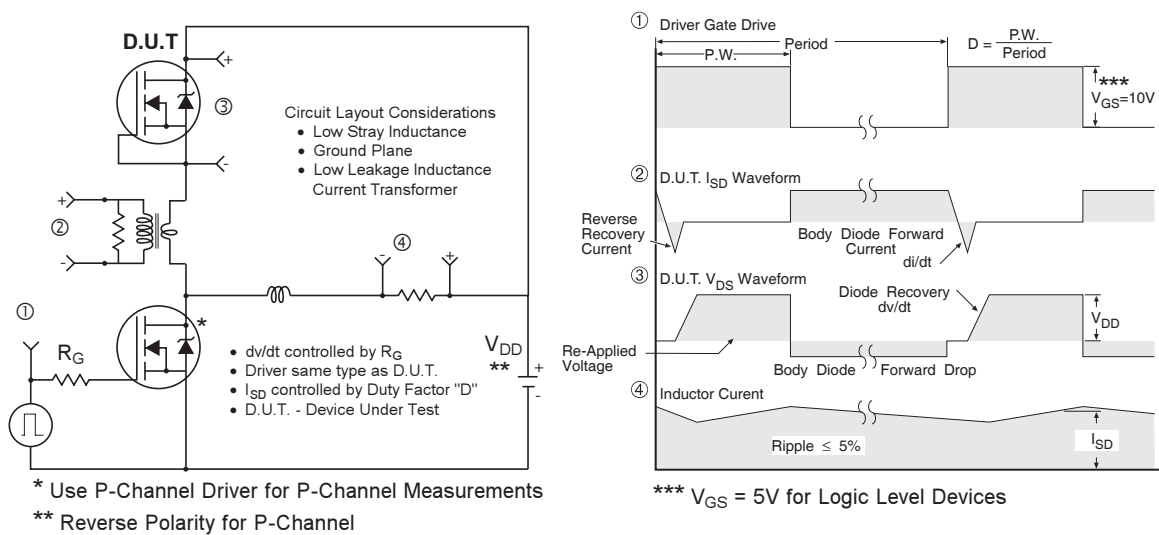
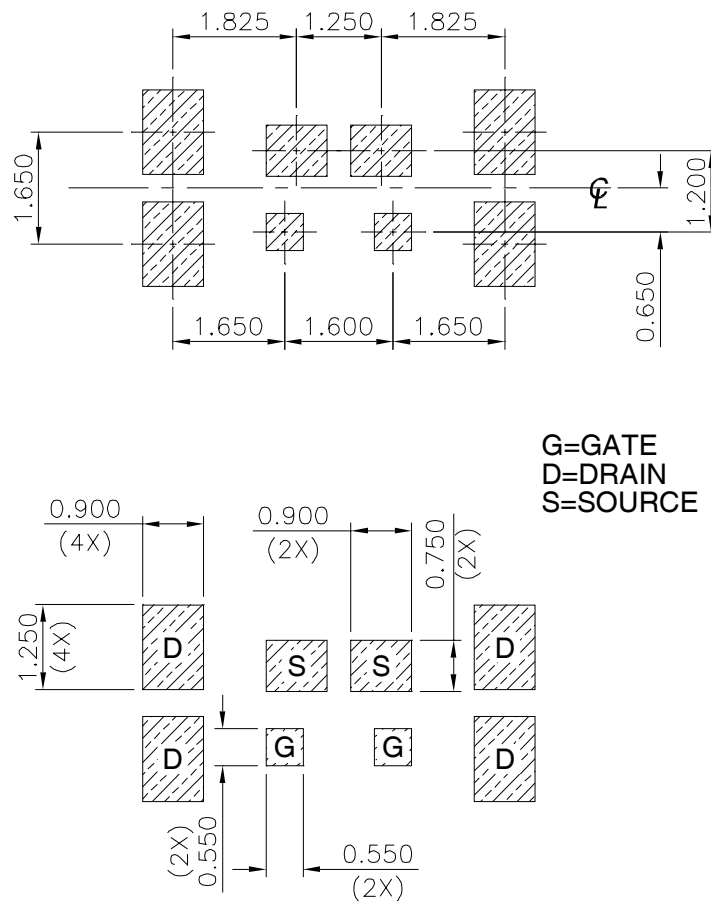


Fig 18. Diode Reverse Recovery Test Circuit for HEXFET® Power MOSFETs

DirectFET®*plus* Board Footprint, SA Outline (Small Size Can, A-Designation).

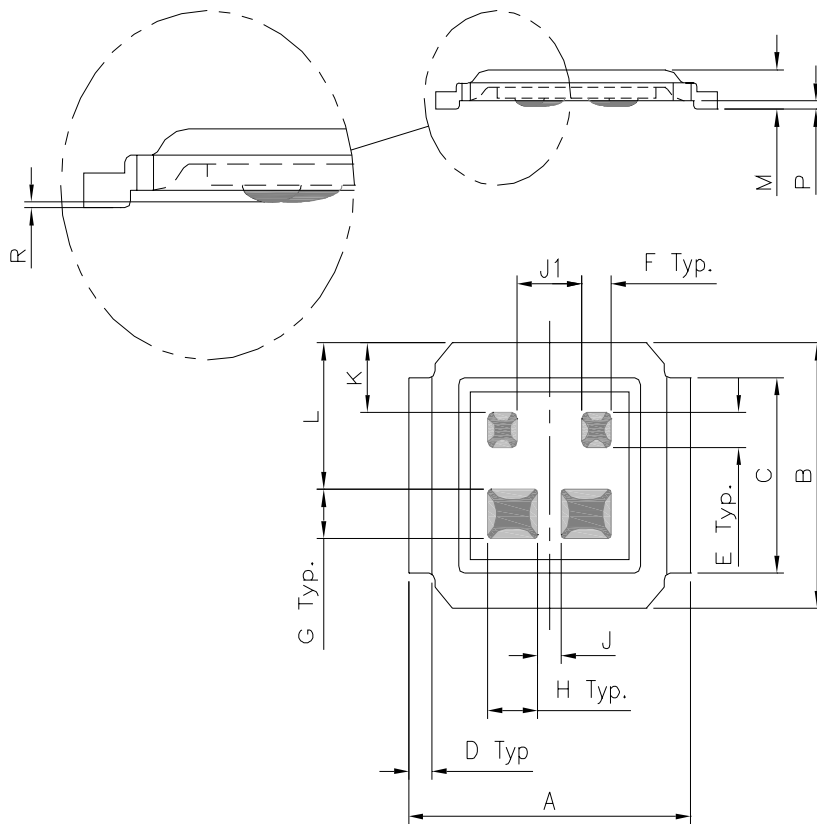
Please see application note AN-1035 for all details regarding the assembly of DirectFET®*plus*.

This includes all recommendations for stencil and substrate designs.



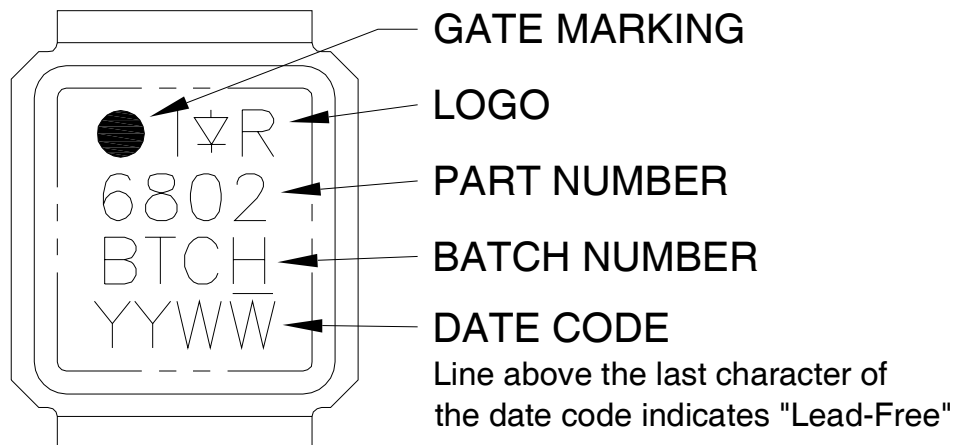
DirectFET^{®plus} Outline Dimension, SA Outline (Small Size Can, A-Designation).

Please see application note AN-1035 for all details regarding the assembly of DirectFET^{®plus}. This includes all recommendations for stencil and substrate designs.



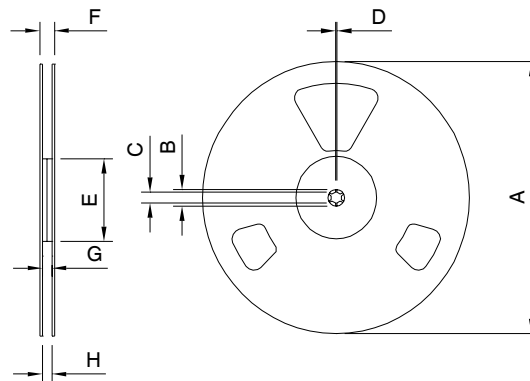
DIMENSIONS				
	METRIC		IMPERIAL	
CODE	MIN	MAX	MIN	MAX
A	4.75	4.85	0.187	0.191
B	3.70	3.95	0.146	0.156
C	2.75	2.85	0.108	0.112
D	0.35	0.45	0.014	0.018
E	0.48	0.52	0.019	0.020
F	0.48	0.52	0.019	0.020
G	0.68	0.72	0.027	0.028
H	0.83	0.87	0.033	0.034
J	0.38	0.42	0.015	0.016
J1	1.08	1.12	0.043	0.044
K	0.95	1.05	0.037	0.041
L	2.05	2.15	0.081	0.085
M	0.52	0.62	0.020	0.024
P	0.08	0.17	0.003	0.007
R	0.02	0.08	0.0008	0.0031

DirectFET^{®plus} Part Marking



Note: For the most current drawing please refer to IR website at <http://www.irf.com/package>

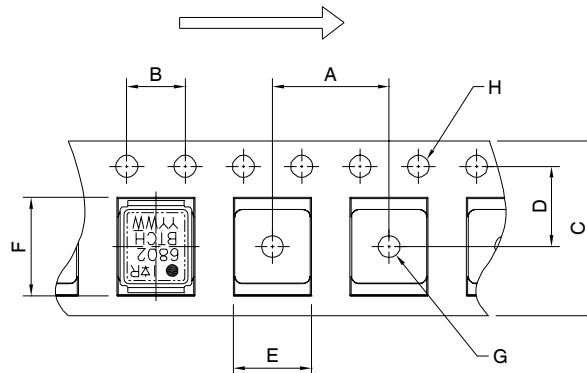
DirectFET[®]plus Tape & Reel Dimension (Showing component orientation).



NOTE: Controlling dimensions in mm
Std reel quantity is 4800 parts. (ordered as IRF6802SDTRPbF). For 1000 parts on 7" reel, order IRF6802SDTR1PbF

REEL DIMENSIONS								
STANDARD OPTION (QTY 4800)					TR1 OPTION (QTY 1000)			
	METRIC		IMPERIAL		METRIC		IMPERIAL	
CODE	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	330.0	N.C	12.992	N.C	177.77	N.C	6.9	N.C
B	20.2	N.C	0.795	N.C	19.06	N.C	0.75	N.C
C	12.8	13.2	0.504	0.520	13.5	12.8	0.53	0.50
D	1.5	N.C	0.059	N.C	1.5	N.C	0.059	N.C
E	100.0	N.C	3.937	N.C	58.72	N.C	2.31	N.C
F	N.C	18.4	N.C	0.724	N.C	13.50	N.C	0.53
G	12.4	14.4	0.488	0.567	11.9	12.01	0.47	N.C
H	11.9	15.4	0.469	0.606	11.9	12.01	0.47	N.C

LOADED TAPE FEED DIRECTION



NOTE: CONTROLLING DIMENSIONS IN MM

DIMENSIONS				
	METRIC		IMPERIAL	
CODE	MIN	MAX	MIN	MAX
A	7.90	8.10	0.311	0.319
B	3.90	4.10	0.154	0.161
C	11.90	12.30	0.469	0.484
D	5.45	5.55	0.215	0.219
E	4.00	4.20	0.158	0.165
F	5.00	5.20	0.197	0.205
G	1.50	N.C	0.059	N.C
H	1.50	1.60	0.059	0.063

Note: For the most current drawing please refer to IR website at <http://www.irf.com/package>