



Integrated Device Technology, Inc.

CMOS STATIC RAM 256K (32K x 8-BIT) IN PE PACKAGES

IDT71256SA

FEATURES:

- 32K x 8 CMOS static RAM
- Equal access and cycle times
 - Commercial: 15/20/25/35/45/70ns
- One Chip Select plus one Output Enable pin
- Bidirectional data inputs and outputs directly TTL-compatible
- Low power consumption via chip deselect
- Available in 28-pin 330 mil Plastic SOIC.

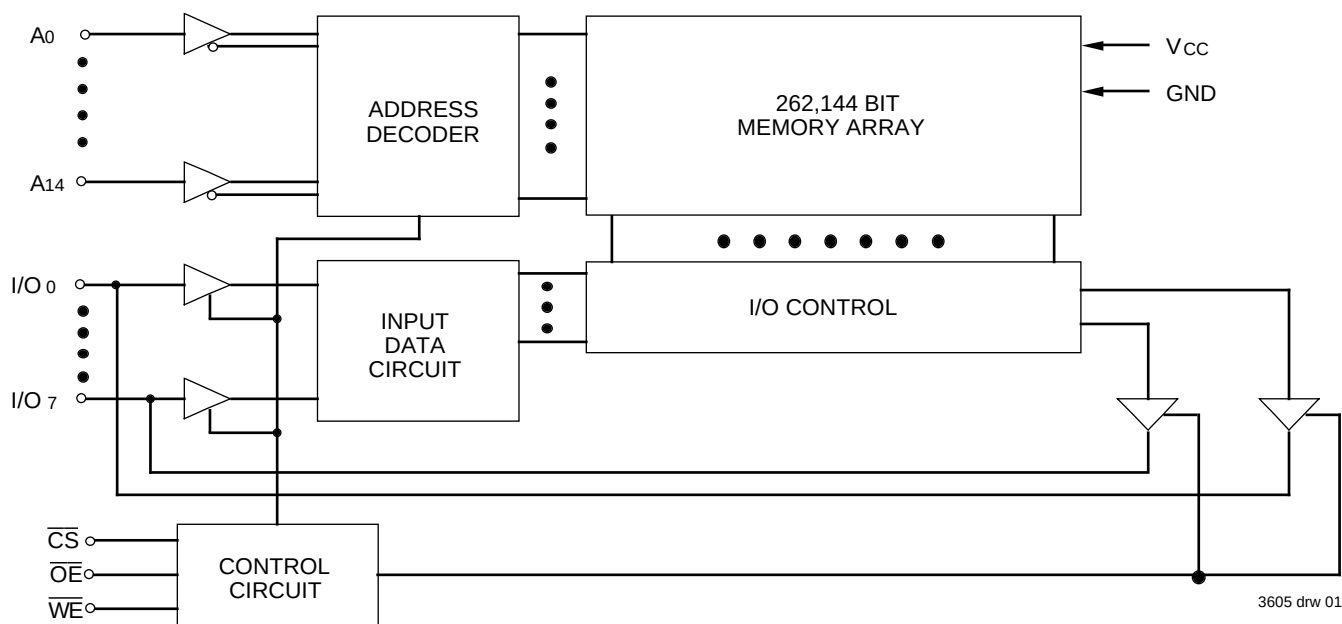
DESCRIPTION:

The ID71256SA is a 262,144-bit Static RAM organized as 32K x 8. It is fabricated using IDT's high-performance, high-reliability CMOS technology. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost-effective solution for your memory needs.

All bidirectional inputs and outputs of the IDT71256SA are TTL-compatible and operation is from a single 5V supply. Fully static asynchronous circuitry is used, requiring no clocks or refresh for operation.

The IDT71256SA is packaged in a 28-pin 330 mil Plastic SOIC.

FUNCTIONAL BLOCK DIAGRAM

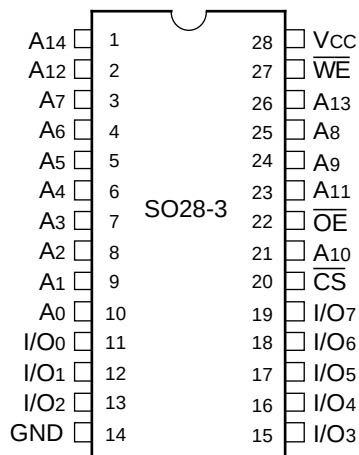


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COMMERCIAL TEMPERATURE RANGE

JULY 1996

PIN CONFIGURATIONS



3605 drw 02

SOIC
TOP VIEW

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCC	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
VIH	Input High Voltage	2.2	—	VCC+0.5	V
VIL	Input Low Voltage	-0.5 ⁽¹⁾	—	0.8	V

NOTE: 3605 tbl 01
1. VIL (min.) = -1.5V for pulse width less than 10ns, once per cycle.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Rating	Com'l.	Unit
VTERM ⁽²⁾	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
TA	Operating Temperature	0 to +70	°C
TBIAS	Temperature Under Bias	-55 to +125	°C
TSTG	Storage Temperature	-55 to +125	°C
PT	Power Dissipation	1.0	W
IOUT	DC Output Current	50	mA

NOTES: 3605 tbl 02
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. VTERM must not exceed VCC + 0.5V.

CAPACITANCE

(TA = +25°C, f = 1.0MHz, SOJ package)

Symbol	Parameter ⁽¹⁾	Conditions	Max.	Unit
CIN	Input Capacitance	VIN = 3dV	11	pF
C/I/O	I/O Capacitance	VOU = 3dV	11	pF

NOTE: 3605 tbl 03
1. This parameter is guaranteed by device characterization, but not production tested.

TRUTH TABLE^(1,2)

CS	OE	WE	I/O	Function
L	L	H	DATAOUT	Read Data
L	X	L	DATAIN	Write Data
L	H	H	High-Z	Outputs Disabled
H	X	X	High-Z	Deselected — Standby (ISB)
VHC ⁽³⁾	X	X	High-Z	Deselected — Standby (ISB1)

NOTES: 3605 tbl 04
1. H = VIH, L = VIL, x = Don't care.
2. VLC = 0.2V, VHC = VCC - 0.2V.
3. Other inputs ≥VHC or ≤VLC.

DC ELECTRICAL CHARACTERISTICS

VCC = 5.0V ± 10%

Symbol	Parameter	Test Condition	IDT71256SA		Unit
			Min.	Max.	
ILI	Input Leakage Current	VCC = Max., VIN = GND to VCC	—	5	μA
ILO	Output Leakage Current	VCC = Max., CS = VIH, VOUT = GND to VCC	—	5	μA
VOL	Output Low Voltage	IOL = 8mA, VCC = Min.	—	0.4	V
VOH	Output High Voltage	IOH = -4mA, VCC = Min.	2.4	—	V

3605 tbl 05

DC ELECTRICAL CHARACTERISTICS⁽¹⁾

(V_{CC} = 5.0V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V)

Symbol	Parameter	71256SA15	71256SA20	71256SA25	Unit
I _{CC}	Dynamic Operating Current $\overline{CS} \leq V_{IL}$, Outputs Open, V _{CC} = Max., f = f _{MAX} ⁽²⁾	150	145	145	mA
I _{SB}	Standby Power Supply Current (TTL Level) $\overline{CS} \geq V_{IH}$, Outputs Open, V _{CC} = Max., f = f _{MAX} ⁽²⁾	40	40	40	mA
I _{SB1}	Standby Power Supply Current (CMOS Level) $\overline{CS} \geq V_{HC}$, Outputs Open, V _{CC} = Max., f = 0 ⁽²⁾ V _{IN} ≤ V _{LC} or V _{IN} ≥ V _{HC}	15	15	15	mA

DC ELECTRICAL CHARACTERISTICS (CONTINUED)⁽¹⁾

(V_{CC} = 5.0V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V)

Symbol	Parameter	71256SA35	71256SA45	71256SA70	Unit
I _{CC}	Dynamic Operating Current $\overline{CS} \leq V_{IL}$, Outputs Open, V _{CC} = Max., f = f _{MAX} ⁽²⁾	140	135	130	mA
I _{SB}	Standby Power Supply Current (TTL Level) $\overline{CS} \geq V_{IH}$, Outputs Open, V _{CC} = Max., f = f _{MAX} ⁽²⁾	30	30	20	mA
I _{SB1}	Standby Power Supply Current (CMOS Level) $\overline{CS} \geq V_{HC}$, Outputs Open, V _{CC} = Max., f = 0 ⁽²⁾ V _{IN} ≤ V _{LC} or V _{IN} ≥ V _{HC}	15	15	15	mA

NOTES:

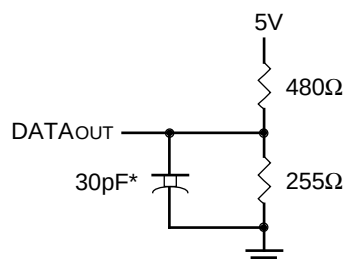
- All values are maximum guaranteed values.
- f_{MAX} = 1/t_{rc} (all address inputs are cycling at f_{MAX}); f = 0 means no address input lines are changing.

3605 tbl 06

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
AC Test Load	See Figures 1 and 2

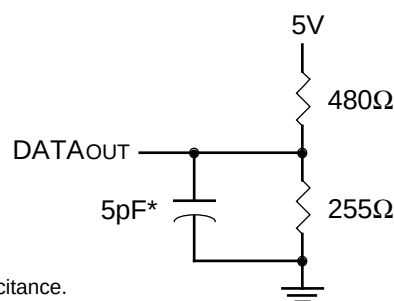
3605 tbl 07



3605 drw 03

*Including jig and scope capacitance.

Figure 1. AC Test Load



3605 drw 04

Figure 2. AC Test Load
(for t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{OW}, and t_{WHZ})

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	71256SA15		71256SA20		71256SA25		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle								
tRC	Read Cycle Time	15	—	20	—	25	—	ns
tAA	Address Access Time	—	15	—	20	—	25	ns
tACS	Chip Select Access Time	—	15	—	20	—	25	ns
tCLZ ⁽¹⁾	Chip Select to Output in Low-Z	4	—	4	—	4	—	ns
tCHZ ⁽¹⁾	Chip Deselect to Output in High-Z	0	7	0	10	0	11	ns
tOE	Output Enable to Output Valid	—	7	—	10	—	11	ns
tOLZ ⁽¹⁾	Output Enable to Output in Low-Z	0	—	0	—	0	—	ns
tOHZ ⁽¹⁾	Output Disable to Output in High-Z	0	6	0	8	0	10	ns
tOH	Output Hold from Address Change	3	—	3	—	3	—	ns
tPU ⁽¹⁾	Chip Select to Power Up Time	0	—	0	—	0	—	ns
tPD ⁽¹⁾	Chip Deselect to Power Down Time	—	15	—	20	—	25	ns
Write Cycle								
tWC	Write Cycle Time	15	—	20	—	25	—	ns
tAW	Address Valid to End of Write	10	—	15	—	20	—	ns
tCW	Chip Select to End of Write	10	—	15	—	20	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	ns
tWP	Write Pulse Width	10	—	15	—	20	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	ns
tdW	Data Valid to End of Write	7	—	11	—	13	—	ns
tdH	Data Hold Time	0	—	0	—	0	—	ns
tOW ⁽¹⁾	Output Active from End of Write	4	—	4	—	4	—	ns
tWHZ ⁽¹⁾	Write Enable to Output in High-Z	0	6	0	10	0	11	ns

NOTE:

3605 tbl 08

1. This parameter is guaranteed with the AC Load (Figure 2) by device characterization, but is not production tested.

AC ELECTRICAL CHARACTERISTICS (CONTINUED) ($V_{CC} = 5.0V \pm 10\%$)

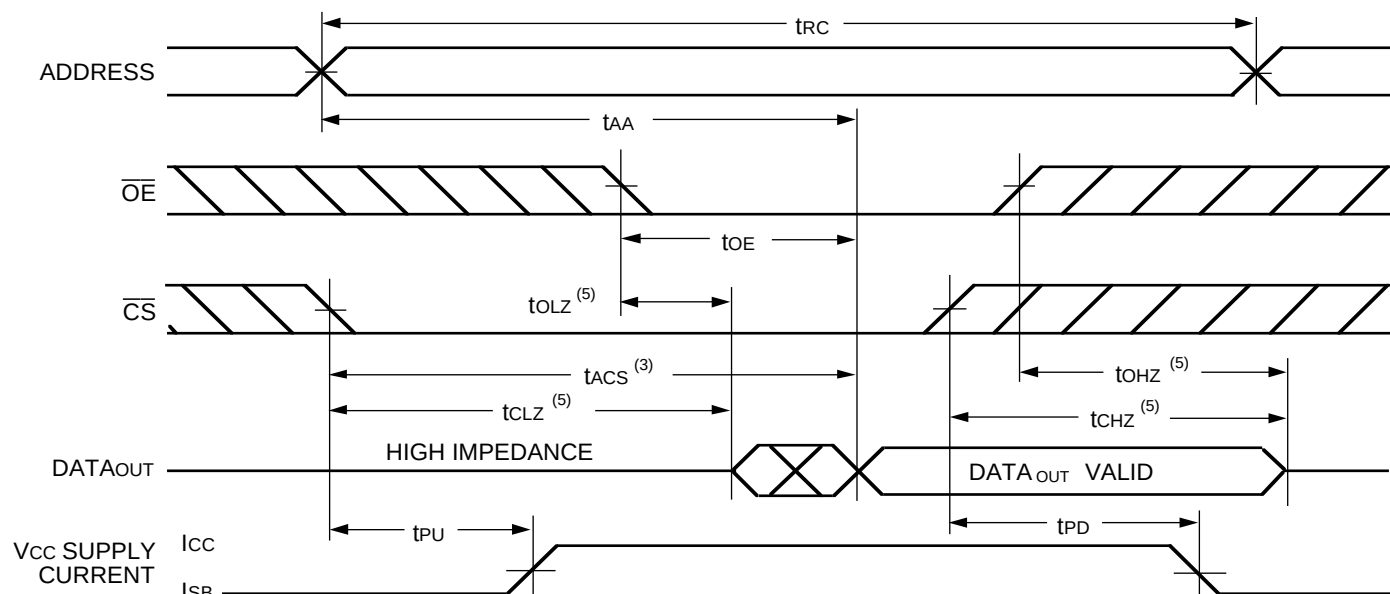
Symbol	Parameter	71256SA35		71256SA45		71256SA70		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle								
tRC	Read Cycle Time	35	—	45	—	70	—	ns
tAA	Address Access Time	—	35	—	45	—	70	ns
tACS	Chip Select Access Time	—	35	—	45	—	70	ns
tCLZ ⁽¹⁾	Chip Select to Output in Low-Z	4	—	4	—	4	—	ns
tCHZ ⁽¹⁾	Chip Deselect to Output in High-Z	0	11	0	11	0	11	ns
tOE	Output Enable to Output Valid	—	11	—	11	—	11	ns
tOLZ ⁽¹⁾	Output Enable to Output in Low-Z	0	—	0	—	0	—	ns
tOHZ ⁽¹⁾	Output Disable to Output in High-Z	0	10	0	10	0	10	ns
tOH	Output Hold from Address Change	3	—	3	—	3	—	ns
tPU ⁽¹⁾	Chip Select to Power Up Time	0	—	0	—	0	—	ns
tPD ⁽¹⁾	Chip Deselect to Power Down Time	—	25	—	25	—	25	ns
Write Cycle								
tWC	Write Cycle Time	35	—	45	—	70	—	ns
tAW	Address Valid to End of Write	20	—	20	—	20	—	ns
tCW	Chip Select to End of Write	20	—	20	—	20	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	ns
tWP	Write Pulse Width	20	—	20	—	20	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	ns
tdW	Data Valid to End of Write	13	—	13	—	13	—	ns
tdH	Data Hold Time	0	—	0	—	0	—	ns
tOW ⁽¹⁾	Output Active from End of Write	4	—	4	—	4	—	ns
tWHZ ⁽¹⁾	Write Enable to Output in High-Z	0	11	0	11	0	11	ns

NOTE:

1. This parameter is guaranteed with the AC Load (Figure 2) by device characterization, but is not production tested.

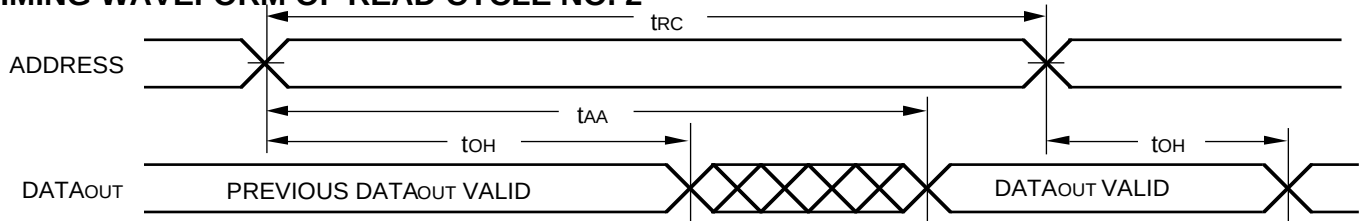
3605 tbl 08

TIMING WAVEFORM OF READ CYCLE NO. 1⁽¹⁾



3605 drw 05

TIMING WAVEFORM OF READ CYCLE NO. 2^(1,2,4)

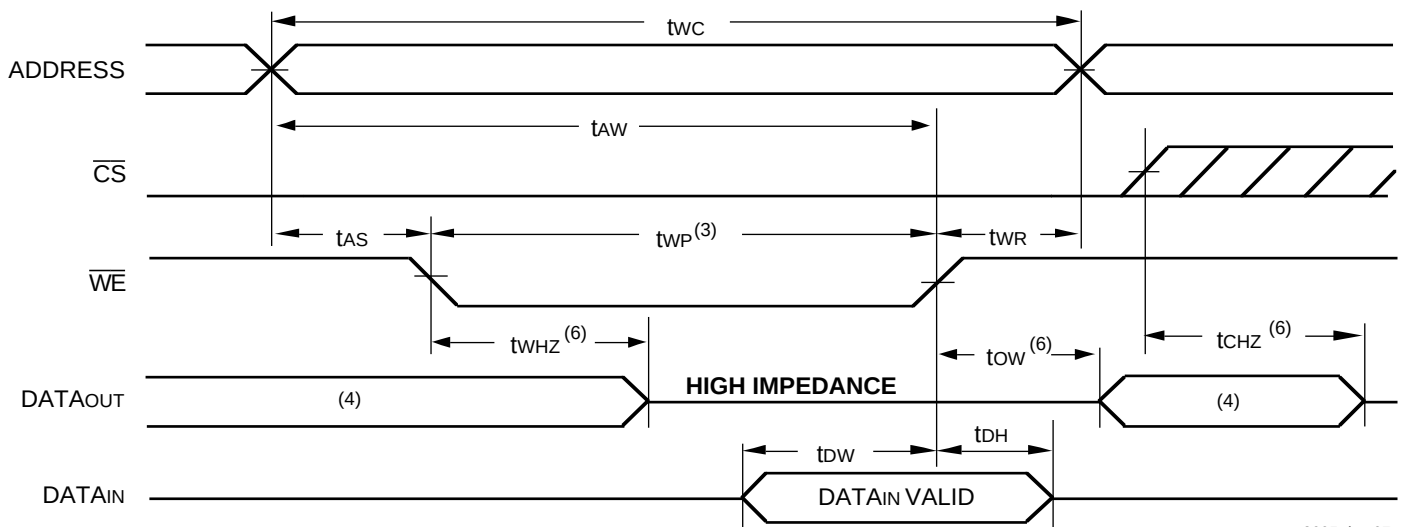


NOTES:

1. $\overline{WE}$ is HIGH for Read Cycle.
2. Device is continuously selected, $\overline{CS}$ is LOW.
3. Address must be valid prior to or coincident with the later of $\overline{CS}$ transition LOW; otherwise t_{AA} is the limiting parameter.
4. $\overline{OE}$ is LOW.
5. Transition is measured $\pm 200\text{mV}$ from steady state.

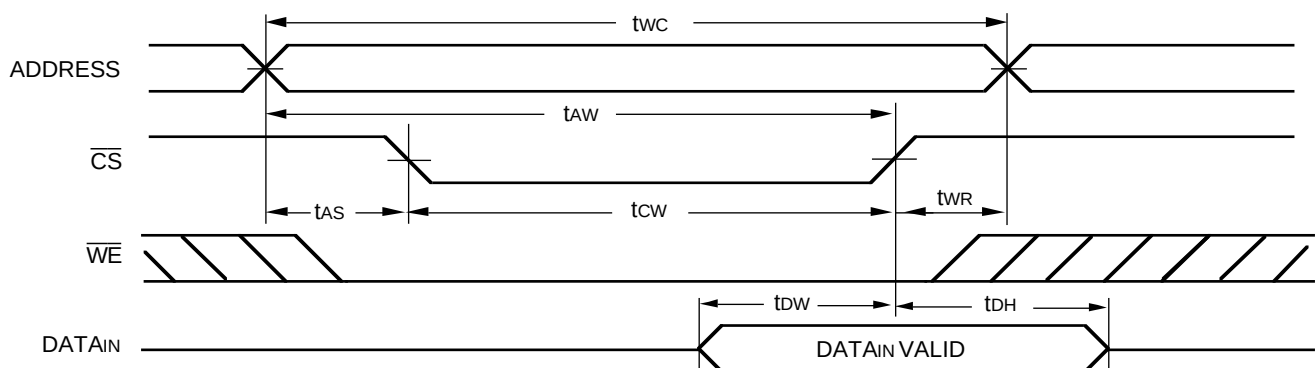
3605 drw 06

TIMING WAVEFORM OF WRITE CYCLE NO.1 ($\overline{WE}$ CONTROLLED TIMING)^(1,2,3,5)



3605 drw 07

TIMING WAVEFORM OF WRITE CYCLE NO.2 ($\overline{CS}$ CONTROLLED TIMING)^(1,2,5)



NOTES:

1. $\overline{WE}$ or $\overline{CS}$ must be HIGH during all address transitions.
2. A write occurs during the overlap of a LOW $\overline{CS}$ and a LOW $\overline{WE}$.
3. $\overline{OE}$ is continuously HIGH. If during a $\overline{WE}$ controlled write cycle $\overline{OE}$ is LOW, t_{WP} must be greater than or equal to $t_{WHZ} + t_{DW}$ to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW} . If $\overline{OE}$ is HIGH during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the minimum write pulse is as short as the specified t_{WP} .
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CS}$ LOW transition occurs simultaneously with or after the $\overline{WE}$ LOW transition, the outputs remain in a high-impedance state.
6. Transition is measured $\pm 200\text{mV}$ from steady state.

3605 drw 08

ORDERING INFORMATION

