INTEGRATED CIRCUITS

DATA SHEET

TJA1053
Fault-tolerant CAN transceiver

Product specification
Supersedes data of 1997 Oct 15
File under Integrated Circuits, IC18

2000 Dec 18

Philips Semiconductors

PHILIPS

FEATURES

Optimized for in-car low-speed communication

- Baud rate up to 125 kbaud
- Up to 32 nodes can be connected
- Supports unshielded bus wires
- Low RFI due to built-in slope control function
- Fully integrated receiver filters
- Permanent dominant monitoring of TXD.

Bus failure management

- Supports one-wire transmission modes with ground offset voltages up to 1.5 V
- Automatic switching to single-wire mode in the event of bus failure
- Automatic reset to differential mode if bus failure is removed.

Protection

- Short-circuit proof to battery and ground in 12 V powered systems
- Thermally protected
- Bus lines protected against transients in an automotive environment
- An unpowered node does not disturb the bus lines.

Support for low-power modes

- Low current sleep/standby mode with wake-up via the bus lines
- Power-on reset flag on the output.

GENERAL DESCRIPTION

The TJA1053 is the interface between the CAN protocol controller and the physical bus. It is primarily intended for low-speed applications, up to 125 kbaud, in passenger cars. The device provides differential transmit capability but will switch in error conditions to a single-wire transmitter and/or receiver. The TJA1053 is derived from the PCA82C252 giving the following advantages:

- Better equipped for networks with more than 15 nodes
- Integrated timer at the TXD input prevents a permanent dominant state
- Reduced supply current in V_{CC} standby mode
- CANH output driver is disabled in the event of a ‘CANH short-circuited to battery’ failure mode.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MIN.	UNIT
V_{CC}	supply voltage		4.75	–	5.25	V
V_{BAT}	battery voltage	no time limit	–0.3	–	+27	V
		operating	6.0	–	27	V
		load dump	–	–	40	V
$I_{BAT(sleep)}$	sleep mode current	V_{CC} = 0 V; V_{BAT} = 12 V	–	65	–	μA
V_{CANH},V_{CANL}	CANH, CANL input voltage	V_{CC} = 0 to 5.5 V; V_{BAT} ≥ 0 V; no time limit	–10	–	+27	V
		V_{CC} = 0 to 5.5 V; V_{BAT} ≥ 0 V; t < 0.1 ms; load dump	–40	–	+40	V
$V_{DROP(H)}$	CANH transmitter drop voltage	I_{CANH} = 40 mA	–	–	1.4	V
$V_{DROP(L)}$	CANL transmitter drop voltage	I_{CANL} = 40 mA	–	–	1.4	V
t_{PD}	propagation delay	TXD to RXD	–	1	–	μs
t_f	bus output fall time	90% to 10%	–	0.5	–	μs
t_r	bus output rise time	10% to 90%	–	0.5	–	μs
T_{amb}	operating ambient temperature		–40	–	+125	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TJA1053T	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1

BLOCK DIAGRAM

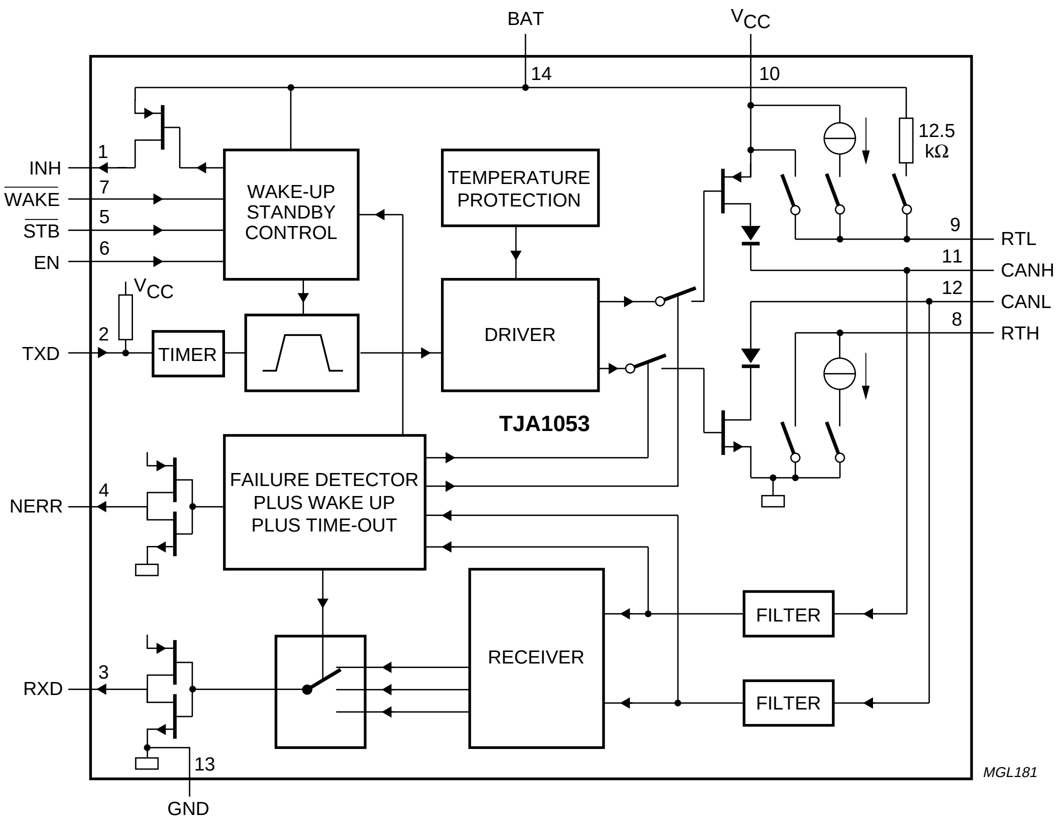


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
INH	1	inhibit output for switching external 5 V regulator
TXD	2	transmit data input, when LOW bus data will be dominant, when HIGH bus data will be recessive
RXD	3	receive data output, when LOW bus data will be dominant
NERR	4	error output pin, when LOW a bus error exists
$\overline{STB}$	5	not standby digital control input signal (active LOW)
EN	6	enable digital control input signal
$\overline{WAKE}$	7	not wake input signal, when pulled down INH becomes active for wake-up (active LOW)
RTH	8	termination resistor, CANH line will be high-impedance with certain bus errors
RTL	9	termination resistor, CANL line will be high-impedance with certain bus errors
V_{CC}	10	supply voltage (+5 V)
CANH	11	high voltage bus line, will be HIGH in dominant state
CANL	12	low voltage bus line, will be LOW in dominant state
GND	13	ground
BAT	14	battery voltage

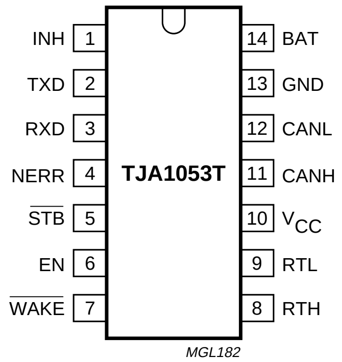


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The TJA1053 is the interface between the CAN protocol controller and the physical bus. It is primarily intended for low speed applications, up to 125 kbaud, in passenger cars. The device provides differential transmit capability to the bus and differential receive capability to the CAN controller.

To reduce RF interference the rise and fall slope are limited. This allows the use of an unshielded twisted pair or a parallel pair of wires for the bus. Moreover, it supports transmission capability on either bus wire if one of the bus wires is corrupted. The failure detection logic automatically selects a suitable transmission mode.

In normal operation (no wiring failures) the differential receiver is output to RXD. The differential receiver inputs are connected to CANH and CANL through integrated filters. The filtered input signals are also used for the single wire receivers. The CANH and CANL receivers have threshold voltages that ensure a maximum noise margin in single-wire modes.

A timer has been integrated at the TXD input. This timer prevents the TJA1053 driving the bus lines to permanent dominant state.

Failure detector

The failure detector is active in the normal operation mode and detects the following single bus failures and switches to an appropriate mode:

1. CANH wire interrupted
2. CANL wire interrupted
3. CANH short-circuited to battery
4. CANL short-circuited to ground
5. CANH short-circuited to ground
6. CANL short-circuited to battery
7. CANL mutually shorted to CANH.

The differential receiver threshold is set at –2.9 V. This ensures correct reception in the normal operating modes and, in the event of failures 1, 2 and 5 with a noise margin as high as possible. These failures, or recovery from them, do not destroy ongoing transmissions.

Failures 3 and 6 are detected by comparators connected to CANH and CANL, respectively. If the comparator threshold is exceeded for a certain period of time, the reception is switched to the single-wire mode. This time is needed to avoid false triggering by external RF fields. Recovery from these failures is detected automatically after a certain time-out (filtering) and no transmission is lost. The CANH driver and the RTH pin are switched off in the event of failure 3.

Failures 4 and 7 initially result in a permanent dominant level at RXD. After a time-out, the CANL driver and the RTL pin are switched off. Only a weak pull-up at RTL remains. Reception continues by switching to the single-wire mode via CANH. When failures 4 or 7 are removed, the recessive bus levels are restored. If the differential voltage remains below the recessive threshold level for a certain period of time, reception and transmission switch back to the differential mode.

If any of the seven wiring failures occur, the output NERR will be made LOW. On error recovery, NERR will be made HIGH again.

During all single-wire transmissions, the EMC performance (both immunity and emission) is worse than in the differential mode. Integrated receiver filters suppress any HF noise induced into the bus wires. The cut-off frequency of these filters is a compromise between propagation delay and HF suppression. In the single-wire mode, low frequency noise cannot be distinguished from the required signal.

Low power modes

The transceiver provides 3 low power modes which can be entered and exited via pins $\overline{STB}$ and EN (see Table 1).

The sleep mode is the mode with the lowest power consumption. The INH pin is switched to high-impedance for deactivation of external voltage regulators. CANL is biased to the battery voltage via the RTL output. If the supply voltage is provided the RXD and NERR will signal the wake-up interrupt

The V_{BAT} standby mode will react the same as the sleep mode with an active INH output.

The V_{CC} standby mode is the V_{BAT} standby with RTL switched to the V_{CC} voltage. In this mode the NERR output signals the V_{BAT} power-on flag and the RXD output will show the wake-up interrupt.

Wake-up requests are recognized by the transceiver when a dominant signal is detected on either bus line or if the $\overline{WAKE}$ pin is connected to ground. On a wake-up request the transceiver will set the INH output which can be used to activate the external V_{CC} voltage regulator. If V_{CC} is provided the wake-up request can be read on the NERR or RXD outputs, on which the external microcontroller can wake up the transceiver (switch to normal operating mode) via $\overline{STB}$ and EN.

To prevent false wake-up due to transients or RF fields, wake-up voltage threshold levels have to be maintained for a certain period of time. In the low power modes the failure detection circuit remains partly active to prevent increased power consumption should errors 3, 4 and 7 occur.

Power on

After power-on V_{BAT} is switched on, the INH pin will become HIGH and an internal power-on flag will be set. This flag can be read via the NERR pin ($\overline{STB}$ = 1, EN = 0) and will be reset by entering the normal operation mode.

The EN and $\overline{STB}$ pins will internally be set to LOW level, if the V_{CC} voltage is below a certain threshold level, to provide fail safe functionality.

Protections

A current limiting circuit protects the transmitter output stages against short-circuit to positive and negative battery voltage.

If the junction temperature exceeds a maximum value, the transmitter output stages are disabled. Because the transmitter is responsible for the major part of the power dissipation, this will result in a reduced power dissipation and hence a lower chip temperature. All other parts of the IC will remain operating.

The CANH and CANL inputs are protected against electrical transients which may occur in an automotive environment.

Table 1 Truth table of CAN transceiver

$\overline{STB}$	EN	MODE	INH	NERR	RXD	RTL
0	0	V_{BAT} standby(1)	HIGH	active LOW wake-up interrupt signal if V_{CC} is present		switched to V_{BAT}
0	0	sleep(2)	floating			switched to V_{BAT}
0	1	go to sleep command	floating			switched to V_{BAT}
1	0	V_{CC} standby(3)	HIGH	active LOW V_{BAT} power-on flag	active LOW wake-up interrupt	switched to V_{CC}
1	1	normal operation mode	HIGH	active LOW error flag	HIGH = receive; LOW = dominant received data	switched to V_{CC}

Notes

1. Wake-up interrupts are released when entering normal operating mode.
2. If go to sleep command was used before (EN may turn LOW as V_{CC} drops, without affecting internal functions because of fail safe functionality).
3. V_{BAT} power-on flag will be reset when entering normal operation mode.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage		–0.3	+6.0	V
V_{DD}	DC input voltage at pins 2 to 6		–0.3	V_{CC} + 0.3	V
V_{BUS}	DC input voltage at pins 11 and 12		–10	+27	V
V_{CANH}, V_{CANL}	DC input voltage at pins 11 and 12	V_{CC} = 0 to 5.5 V; $V_{BAT} \geq 0$ V; t < 0.1 ms; load dump	–40	+40	V
V_{tr}	transient voltage at pins 11 and 12	see Fig.6	–150	+100	V
V_{WAKE}	DC input voltage on pin 7		–	V_{BAT} + 0.3	V
I_{WAKE}	input current pin 7		–15	–	mA
$V_{1,8,9}$	DC input voltage on pins 1, 8 and 9		–0.3	V_{BAT} + 0.3	V
V_{BAT}	DC input voltage on pin 14		–0.3	+27	V
	voltage on pin 14	load dump; 500 ms	–	40	V
$R_{8,9}$	termination resistances pins 8 and 9		500	16000	Ω
T_{vj}	virtual junction temperature	note 1	–40	+150	°C
T_{stg}	storage temperature		–55	+150	°C
V_{esd}	electrostatic discharge voltage at any pin	note 2	–2000	+2000	V
		note 3	–200	+200	V

Notes

1. Junction temperature in accordance with IEC 60747-1. An alternative definition is: $T_{vj} = T_{amb} + PD \times R_{th\ vj-a}$. Where: $R_{th\ vj-a}$ is a fixed value to be used for the calculation of T_{vj}. The rating for T_{vj} limits the allowable combinations of power dissipation and ambient temperature.
2. Human body model: equivalent to discharging a 100 pF capacitor through a 1.5 kΩ resistor.
3. Machine model: equivalent to discharging a 200 pF capacitor through a 25 Ω resistor.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ vj-a}$	thermal resistance from junction to ambient	in free air	120	K/W

QUALITY SPECIFICATION

Quality specification in accordance with *“SNW-FQ-611-Part-E”*.

CHARACTERISTICS

V_{CC} = 4.75 to 5.25 V; $V_{\overline{STB}}$ = V_{CC}; V_{BAT} = 6 to 27 V; T_{amb} = –40 to +125 °C; all voltages are defined with respect to ground; positive currents flow into the IC; all parameters are guaranteed over the temperature range by design, but only 100% tested at 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
I_{CC}	supply current	recessive; TXD = V_{CC}; normal operating mode	–	6	10	mA
		dominant; TXD = 0 V; no load; normal operating mode	–	29	35	mA
I_{CC} + I_{BAT}	supply current	V_{CC} standby; V_{CC} = 5 V; V_{BAT} = 12 V; T_{amb} < 90 °C	–	200	500	μA
I_{BAT} + I_{CC}	supply current	V_{BAT} standby; V_{CC} = 5 V; V_{BAT} = 12 V; T_{amb} < 90 °C	–	70	95	μA
$I_{BAT(sleep)}$	supply current	sleep mode; V_{CC} = 0 V; V_{BAT} = 12 V; T_{amb} < 90 °C	–	65	90	μA
V_{BAT}	battery voltage for setting power-on flag	low power modes	–	–	1.0	V
t_{pwon}	battery voltage low time for setting power-on flag	low power modes	1	–	–	s
Pins $\overline{STB}$, EN and TXD						
V_{IH}	HIGH-level input voltage		0.7V_{CC}	–	V_{CC} + 0.3	V
V_{IL}	LOW-level input voltage		–0.3	–	0.3V_{CC}	V
I_{IH}	HIGH-level input current (pins $\overline{STB}$ and EN)	V_i = 4 V	–	9	20	μA
I_{IL}	LOW-level input current (pins $\overline{STB}$ and EN)	V_i = 1 V	4	8	–	μA
I_{IH}	HIGH-level input current (pin TXD)	V_i = 4 V	–25	–80	–200	μA
I_{IL}	LOW-level input current (pin TXD)	V_i = 1 V	–100	–320	–800	μA
V_{CC}	forced V_{BAT} standby mode (fail safe)		2.75	–	4.5	V
Pins RXD and NERR						
V_{OH}	HIGH-level output voltage (pin NERR)	I_o = –100 μA	V_{CC} – 0.9	–	V_{CC}	V
V_{OH}	HIGH-level output voltage (pin RXD)	I_o = –250 μA	V_{CC} – 0.9	–	V_{CC}	V
V_{OL}	LOW-level output voltage	I_o = 1.25 mA	0	–	0.9	V
Pin $\overline{WAKE}$						
I_{IL}	LOW-level input current	$V_{\overline{WAKE}}$ = 0 V; V_{BAT} = 27 V	–70	–40	–10	μA
$V_{wu(th)}$	wake-up threshold voltage	$V_{\overline{STB}}$ = 0 V	1.7	3.0	4.0	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Pin INH						
V_{dropH}	HIGH-level voltage drop	I_{INH} = –0.18 mA; V_{BAT} < 16 V	–	–	0.8	V
		I_{INH} = –0.18 mA; V_{BAT} > 16 V	–	–	1.0	V
I_{LI}	leakage current	sleep mode; V_{INH} = 0 V	–5.0	–	+5.0	µA
Pins CANH and CANL						
V_{drx}	differential receiver threshold voltage	no bus failures bus failures 1, 2 and 5	–3.25	–	–2.65	V
$V_{oCANHrec}$	CANH recessive output voltage	TXD = V_{CC}; R_{RTH} < 4 kΩ	–	–	0.2	V
$V_{oCANLrec}$	CANL recessive output voltage	TXD = V_{CC}; R_{RTL} < 4 kΩ	V_{CC} – 0.2	–	–	V
$V_{oCANHdom}$	CANH dominant output voltage	TXD = 0 V; V_6 = V_{CC}; I_{CANH} = –40 mA	V_{CC} – 1.4	–	–	V
$V_{oCANLdom}$	CANL dominant output voltage	TXD = 0 V; V_6 = V_{CC}; I_{CANL} = 40 mA	–	–	1.4	V
I_{oCANH}	CANH output current	V_{CANH} = 0 V; TXD = 0 V	–	–75	–100	mA
		sleep mode; V_{CANH} = 12 V	–	0	–	µA
I_{oCANL}	CANL output current	V_{CANL} = 14 V; TXD = 0 V	–	90	130	mA
		sleep mode; V_{CANL} = 0 V; V_{BAT} = 12 V	–	0	–	µA
$V_{det(th)H,L}$	voltage detection threshold for short-circuit to battery voltage on CANH and CANL	normal mode	6.5	7.3	8.0	V
$V_{det(th)H}$	voltage detection threshold for short-circuit to battery voltage on CANH	standby/sleep mode	V_{BAT} – 2.5	–	V_{BAT} – 1	V
V_{wuL}	CANL wake-up voltage threshold		2.4	3.1	3.8	V
V_{wuH}	CANH wake-up voltage threshold		1.2	1.9	2.7	V
V_{wuL}-V_{wuH}	wake-up voltage threshold difference		0.2	–	–	V
V_{CANH}	CANH single-ended receiver threshold	failures 4, 6 and 7	1.5	1.82	2.15	V
V_{CANL}	CANL single-ended receiver threshold voltage	failure 3	2.8	3.1	3.4	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Pins RTH and RTL						
R_{RTL}	RTL to V_{CC} switch-on resistance	$\lvert I_o \rvert < 10$ mA; normal operating mode	–	7	25	Ω
		$\lvert I_o \rvert < 1$ mA; V_{CC} standby mode	–	15	75	Ω
	RTL to V_{BAT} switch series resistance	V_{BAT} standby or sleep mode	8	12.5	23	kΩ
R_{RTH}	RTH to ground switch-on resistance	$\lvert I_o \rvert < 10$ mA; normal operating mode	–	43	95	Ω
V_{oRTH}	RTH output voltage	$I_o = 1$ mA; low power modes	–	0.7	1.0	V
I_{RTLpu}	RTL pull-up current	normal operating mode, failures 4, 6 and 7	–	75	–	µA
I_{RTHpd}	RTH pull-down current	normal operating mode, failure 3	–	75	–	µA
Thermal shutdown						
T_{jsd}	shutdown junction temperature		155	165	180	°C

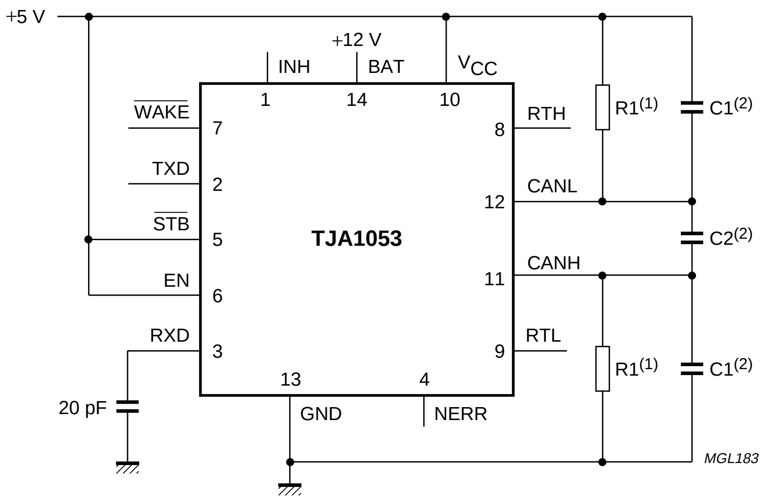
AC CHARACTERISTICS

V_{CC} = 4.75 to 5.25 V; $V_{\overline{STB}} = V_{CC}$; V_{BAT} = 6 to 27 V; T_{amb} = –40 to +125 °C; all voltages are defined with respect to ground; positive currents flow into the IC; all parameters are guaranteed over the temperature range by design, but only 100% tested at 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$t_{t(r-d)}$	CANL and CANH bus output transition time recessive-to-dominant	10% to 90%; C1 = 10 nF; C2 = 0; R1 = 100 Ω	0.6	0.85	–	µs
$t_{t(d-r)}$	CANL and CANH bus output transition time dominant-to-recessive	10% to 90%; C1 = 1 nF; C2 = 0; R1 = 100 Ω	0.3	0.4	–	µs
$t_{PD(L)}$	propagation delay TXD-to-RXD LOW	C1 = 100 pF; C2 = 0; R1 = 100 Ω; no failures and bus failures 1, 2 and 5	–	0.75	1.25	µs
		C1 = C2 = 3.3 nF; R1 = 100 Ω; no failures and bus failures 1, 2 and 5	–	1	1.5	µs
		C1 = 100 pF; C2 = 0; R1 = 100 Ω; bus failures 3, 4, 6 and 7	–	0.85	1.3	µs
		C1 = C2 = 3.3 nF; R1 = 100 Ω; bus failures 3, 4, 6 and 7	–	1.1	1.7	µs

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$t_{PD(H)}$	propagation delay TXD-to-RXD HIGH	C1 = 100 pF; C2 = 0; R1 = 100 Ω; no failures and bus failures 1, 2 and 5	–	0.95	1.5	µs
		C1 = C2 = 3.3 nF; R_l = 100 Ω; no failures and bus failures 1 and 2	–	2.2	3.0	µs
		C1 = 100 pF; C2 = 0; R1 = 100 Ω; bus failures 3, 4, 6 and 7	–	0.85	1.3	µs
		C1 = C2 = 3.3 nF; R1 = 100 Ω; bus failures 3, 4, 5, 6 and 7	–	1.4	2.1	µs
$t_{wu(min)}$	minimum dominant time for wake-up on CANL or CANH	low power modes V_{BAT} = 12 V	8	–	38	µs
$t_{\overline{WAKE}(min)}$	minimum $\overline{\text{WAKE}}$ LOW time for wake-up	low power modes V_{BAT} = 12 V	8	–	38	µs
t_{fail}	failure 3 detection time	normal mode	10	–	60	µs
	failure 6 detection time	normal mode	50	–	400	µs
	failure 3 recovery time	normal mode	10	–	60	µs
	failure 6 recovery time	normal mode	150	–	750	µs
	failures 4 and 7 detection time	normal mode	0.75	–	4.0	ms
	failures 4 and 7 recovery time	normal mode	10	–	60	µs
	failures 3, 4 and 7 detection time	low power modes; V_{BAT} = 12 V	0.8	–	8.0	ms
	failures 3, 4 and 7 recovery time	low power modes; V_{BAT} = 12 V	–	4	–	ms
t_{TXD}	TXD permanent dominant timer, disable time	normal mode and failure modes	0.75	–	4.0	ms
$t_{h(min)}$	minimum hold time to go to sleep command		5	–	50	µs
Δec	edge-count difference between CANH and CANL					
	for failures 1, 2 and 5 detection (NERR becomes LOW)	normal mode	–	3	–	
	for failures 1, 2 and 5 recovery	normal mode	–	1	–	

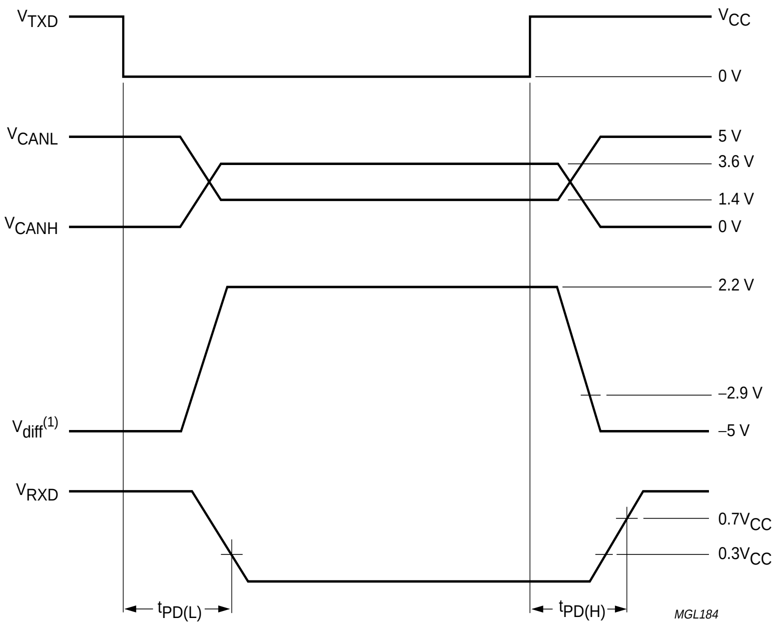
TEST AND APPLICATION INFORMATION



(1) Termination resistors R1 (100 Ω) are not connected to RTH or RTL for testing purposes because the minimum load resistance allowed on the CAN bus line is 500 Ω per transceiver.

(2) The capacitive bus load of 10 nF is split into three equal capacitors (3.3 nF) to simulate the CAN bus line.

Fig.3 Test circuit for dynamic characteristics.



(1) $V_{diff} = V_{CANH} - V_{CANL}$

Fig.4 Timing diagram for dynamic characteristics.

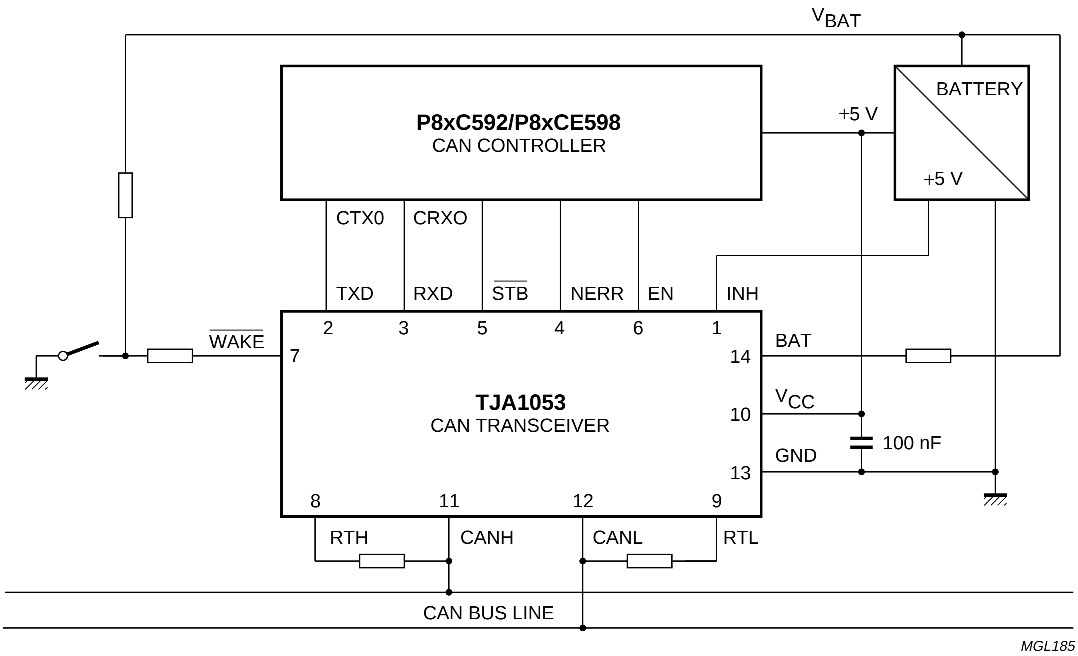
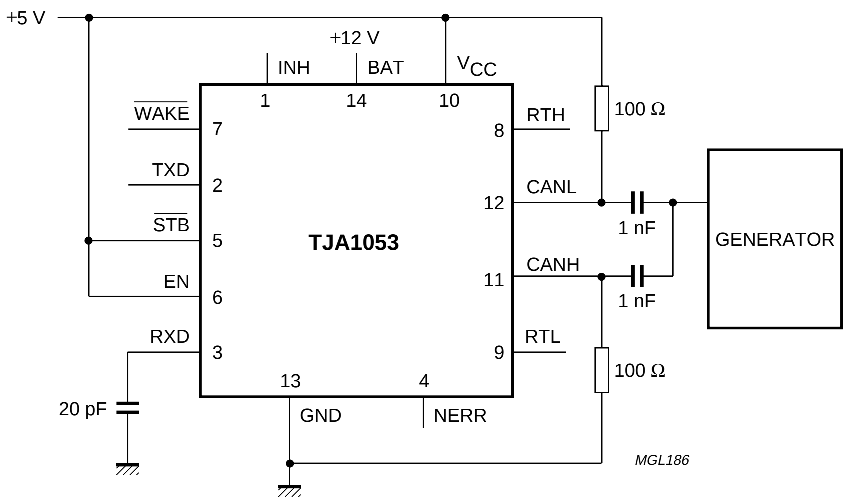


Fig.5 Application of the TJA1053.

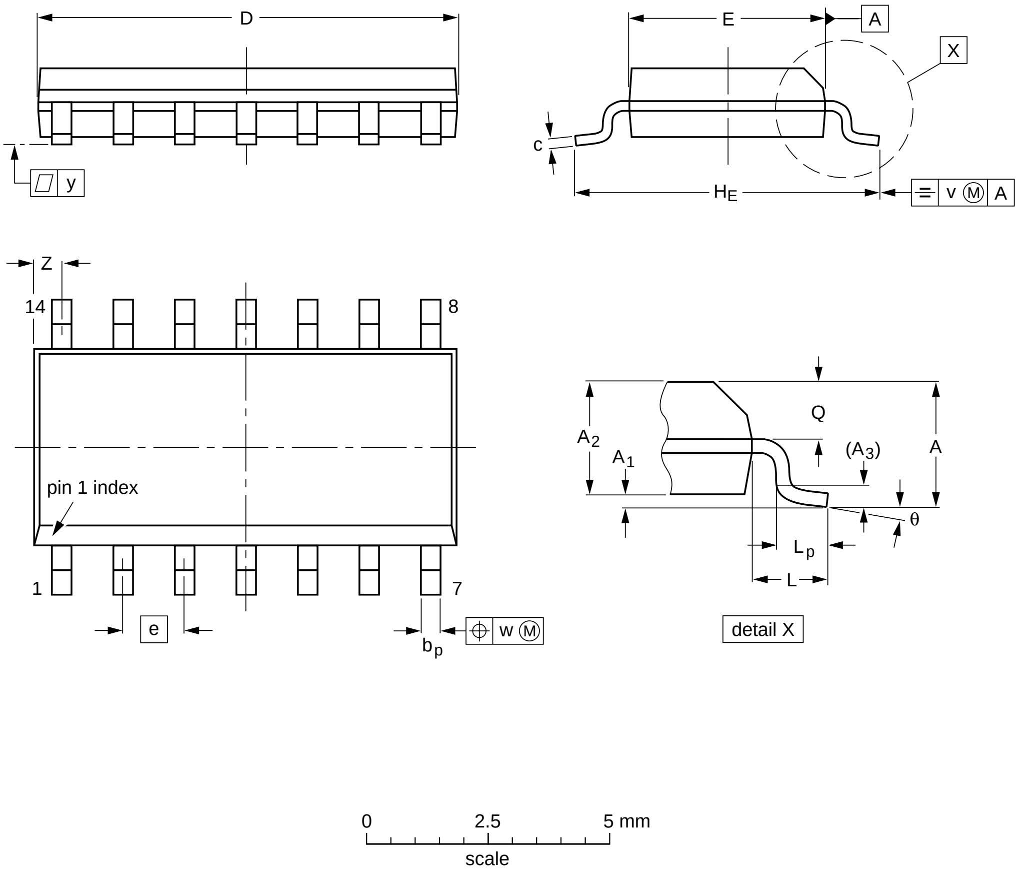


The waveforms of applied transients shall be in accordance with "*ISO7637, part 1*", test pulses 1, 2, 3a and 3b.

Fig.6 Test circuit for automotive transients.

PACKAGE OUTLINE

SO14: plastic small outline package; 14 leads; body width 3.9 mm **SOT108-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.35 0.34	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT108-1	076E06	MS-012				~~97-05-22~~ 99-12-27

SOLDERING

Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 220 °C for thick/large packages, and below 235 °C for small/thin packages.

Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	REFLOW(1)
BGA, HBGA, LFBGA, SQFP, TFBGA	not suitable	suitable
HBCC, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, HVQFN, SMS	not suitable(2)	suitable
PLCC(3), SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended(3)(4)	suitable
SSOP, TSSOP, VSO	not recommended(5)	suitable

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *“Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods”*.
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

DATA SHEET STATUS

DATA SHEET STATUS	PRODUCT STATUS	DEFINITIONS [(1)]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

Note

1. Please consult the most recently issued data sheet before initiating or completing a design.

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Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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