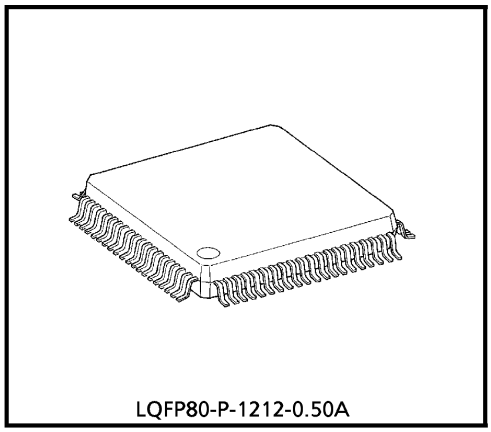
TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

# TC93P27F

## DTS MICROCONTROLLER (DTS-21)




Weight : 0.45 g (Typ.)

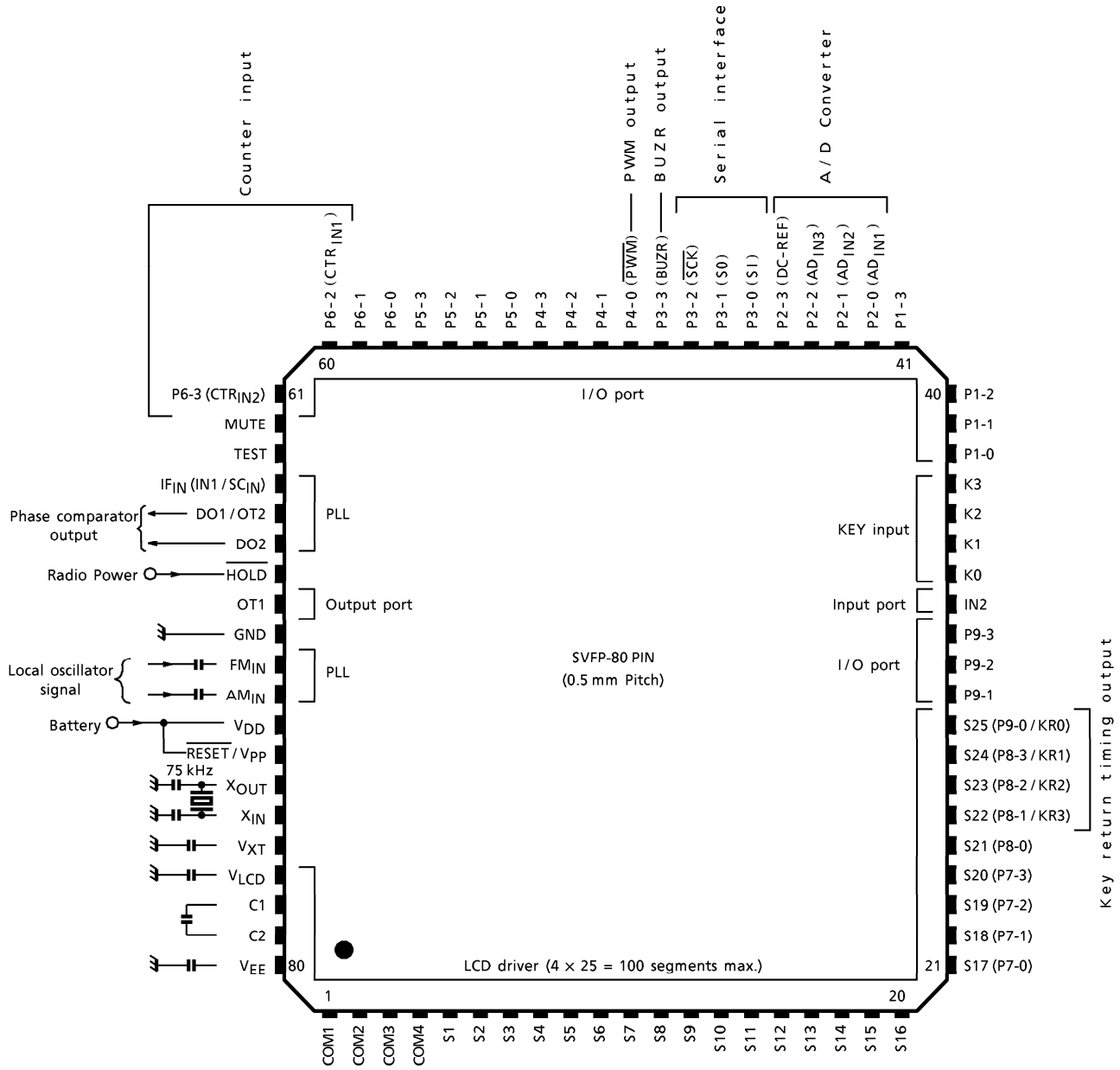
The TC93P27F is a 4-bit CMOS microcontroller for single-chip digital tuning systems, featuring a built-in 230-MHz prescaler, PLL, and LCD drivers.
The CPU has 4-bit parallel addition and subtraction instructions (e.g., AI, SI), logic operation instructions (e.g., OR, AN), composite decision and comparison instructions (e.g., TM, SL), and time-base functions.
The package is an 80-pin, 0.5 mm-pitch compact package.
In addition to various input / output ports and a dedicated key-input port, which are controlled by powerful input / output instructions (IN1 to 3, OUT1 to 3), there are many dedicated LCD pins, a PWM output port, a BUZR port, a 6-bit A / D converter, a serial interface, and an IF counter, etc.
Low-voltage and low-current consumption make this microcontroller suitable for portable DTS equipment.
TC93P27F has built-in One Time PROM that is able to be programed by EPROM writer.
TC93P27F is the same pin assignment as TC9327AF, therefore the program is written into the internal PROM of TC93P27F, and this IC operates as the same function as TC9327AF.

### FEATURES

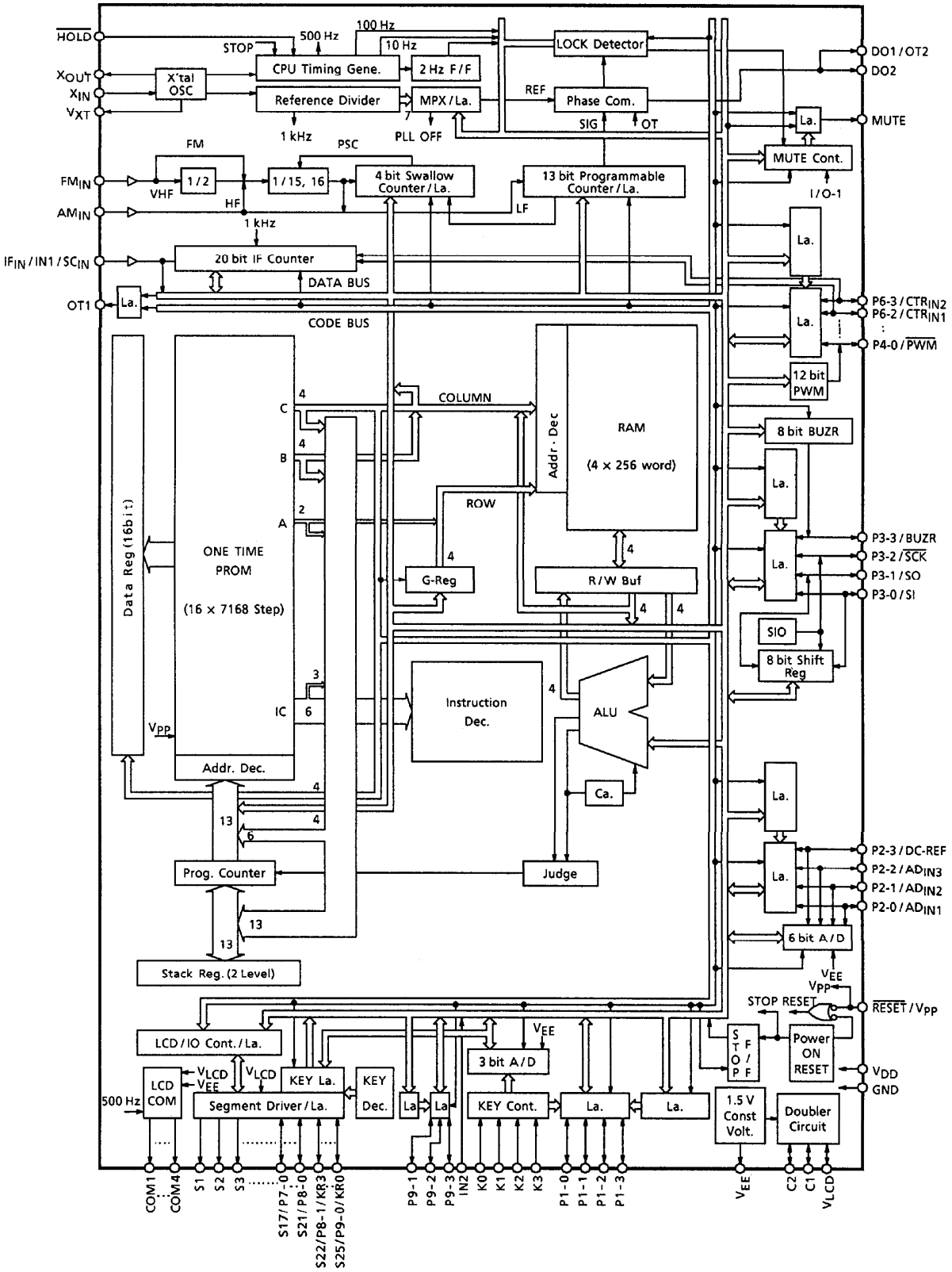
- 4-bit microcontroller for single-chip digital tuning systems.
- Operating voltage $V_{DD}$ = 1.8 to 3.6 V, with low current consumption due to CMOS circuitry (with only the CPU operating when $V_{DD}$ = 3 V, $I_{DD}$ = 130 $\mu$A Max.)
- Built-in prescaler (1 / 2 fixed divider + 2 modulus prescaler : fmax $\geqq$ 230 MHz)
- Features built-in 1 / 4-duty, 1 / 2-bias LCD drivers and a built-in 3 V booster circuit for the display.
- Data memory (RAM) and ports are easily backed up.
- Program memory (ROM) : 16 bit × 7168 steps
- Data memory (RAM) : 4 bit × 256 words

- 62-instruction set (all one-word instructions)
- Instruction execution time : 40 $\mu$s (with 75-kHz crystal) (MVGS, DAL instructions : 80 $\mu$s)
- Many addition and subtraction instructions (12 types each addition and subtraction)
- Powerful composite decision instructions (TMTR, TMFR, TMT, TMF, TMTN, TMFN)
- Data can be transmitted between addresses on the same row.
- Register indirect transfer available (MVGD, MVGS instructions).
- 16 powerful general registers (located in RAM)
- Stack levels : 2
- Free branching (JUMP instructions) is allowed in the 7168 steps of program memory (ROM) as there are no pages or fields.
- 16 bits of any address in the 1024 program memory steps (ROM) can be referenced (DAL instructions).
- Features independent frequency input pins ($FM_{IN}$ and $AM_{IN}$) and two (DO1 and DO2) phase comparator outputs for FM / VHF and AM.
- Seven kinds of reference frequencies can be selected via software.
- Powerful input / output instructions (IN1 to 3, OUT1 to 3).
- Dedicated input ports (K0 to K3) for key input, 29 LCD drive pins (100 segments maximum) available.
- 29 I / O ports : 27 input / output programmable in 1-bit units, 1 output-only port, and 1 input-only port. The 2 $IF_{IN}$, and DO1 pins can be switched by instruction to IN1 (input-only) or OT2 (output-only). In addition, 9 output LCD output pins for S17 to S25 can be switched to I / O port in 1-bit units.
- Three backup modes available by instruction : only CPU operation, crystal oscillation only, clock stop.
- Features a built-in 2-Hz timer F / F and a built-in 10 / 100 Hz interval pulse outputs (internal port for time base).
- Allows PLL lock status detection.
- Four of the LCD segment outputs (S22 to S25) can also operate as key return timing outputs (KR0 to KR3). The I / O ports are not dedicated for key return timing outputs but can have other uses as well.
- Built-in 20-bit, general-purpose IF counters can detect stations during auto-tuning by counting the intermediate frequencies of each band.
- Built-in buzzer output circuit can output 8 kinds of frequencies in 4 modes : continuous output, single-shot output, 10-Hz intermittent output, and 10-Hz intermittent 1-Hz interval output.
- Features built-in 12-bit PWM circuit usable for easy-to-use D / A converter.
- Features a built-in 3-channel, 6-bit A / D converter.
- To prevent CPU malfunction, a built-in supply voltage drop detection circuit shuts down the CPU when the voltage falls below 1.55 V.
- MASK ROM product : TC9327AF

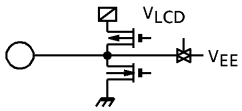
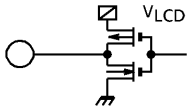
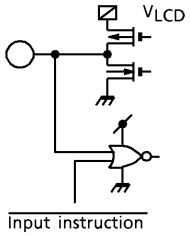
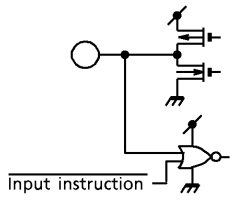
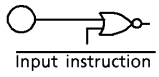
## PIN-ASSIGNMENT

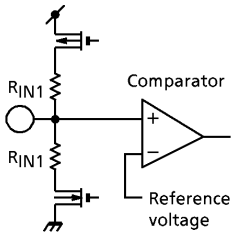
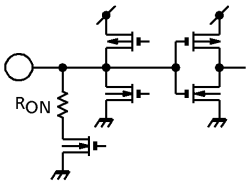


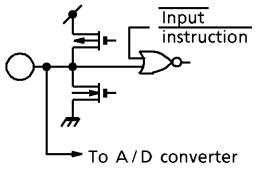
## BLOCK DIAGRAM

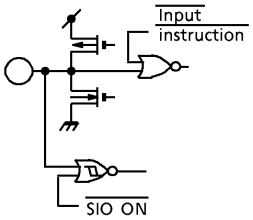
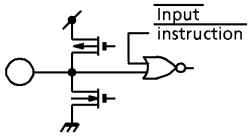
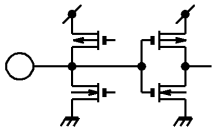


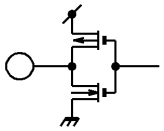
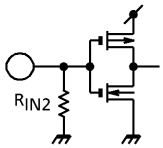
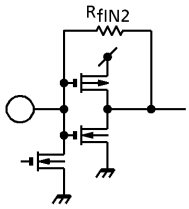
**DESCRIPTION OF PIN FUNCTION**

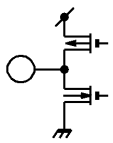
| PIN No. | SYMBOL | PIN NAME | FUNCTION AND OPERATION | REMARKS |
|---|---|---|---|---|
| 1 | COM1 | LCD common output | Output common signals to LCD panels. Through a matrix with pins S1 to S25, a maximum 100 segments can be displayed. Three levels, $V_{LCD}$, $V_{EE}$, and GND, are output at 62.5 Hz every 2 ms. $V_{EE}$ is output after system reset and CLOCK STOP are released, and a common signal is output after the DISP OFF bit is set to "0". |   |
| 2 | COM2 | | | |
| 3 | COM3 | | | |
| 4 | COM4 | | | |
| 5~20 | S1~S16 | LCD segment output | Segment signal output terminals for LCD panel. Together with COM1 to COM4, a matrix is formed that can display a maximum of 100 segments. S17 to S25 are usable as I/O port by program. Signals for key matrix and the segment signals from pins S22/KR3 to S25/KR0 are output on a time sharing basis. 4 × 4 = 16 key matrix can be created in conjunction with key inport ports K0 to K3. |   |
| 21~25 | S17/P7-0 ~ S21/P8-0 | LCD segment output/I/O port | |   |
| 26~29 | S22/P8-1/KR3 ~ S25/P9-0/KR0 | LCD segment output/I/O port/key return timing output | | |
| 30~32 | P9-1~P9-3 | I/O port 9 | 3-bit I/O port, capable of input/output setup for each bit via software. |   |
| 33 | IN2 | Input port 2 | 1-bit input port |   |

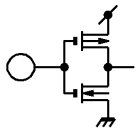
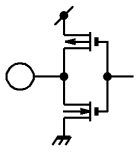
| PIN No. | SYMBOL | PIN NAME | FUNCTION AND OPERATION | REMARKS |
|---|---|---|---|---|
| 34~37 | K0~K3 | Key input port | 4-bit input port for key matrix input, capable of inputting a maximum of 4 × 4 = 16 key data in combination with the key return timing outputs (KR0 to KR3) of an LCD segment pin.<br>Comprises an A / D comparator making it possible to select high impedance with pull-down and pull-up pins for inputs, and to perform programming with a 3-bit input threshold. This allows various key matrices to be formed.<br>Also usable as a 4-channel 3-bit A / D converter with a successive comparison formula via software.<br>When an "H" level is applied in key input ports set to pull-down mode, WAIT mode is canceled. |  |
| 38~41 | P1-0~P1-3 | I / O port 1 | The input and output of these 4-bit I / O ports can be programmed in 1-bit units.<br>This pin is capable of outputting timing signals for the key matrix by program.<br>It contains load resistance in N-ch, and can form the matrix for a push-key needing no diode for the key matrix.<br>By altering the input of I / O ports set to input, the CLOCK STOP mode or the WAIT mode can be released, and the MUTE bit of the MUTE pin can be set to "1". |  |

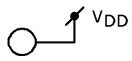
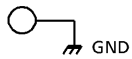
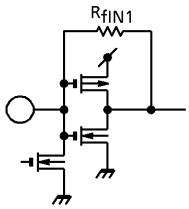
| PIN No. | SYMBOL | PIN NAME | FUNCTION AND OPERATION | REMARKS |
|---|---|---|---|---|
| 42~45 | P2-0 / $AD_{IN1}$<br>P2-1 / $AD_{IN2}$<br>P2-2 / $AD_{IN3}$<br>P2-3 / DC-REF | I/O port 2 / AD analog voltage input<br>/ AD analog voltage input<br>/ AD analog voltage input<br>/ Reference voltage input | 4-bit I/O ports, allowing input and output to be programmed in 1-bit units. Pins P2-0 to P2-2 can also be used for analog input to the built-in 6-bit, 3-channel A/D converter. The conversion time of the built-in A/D converter using the successive comparison method is 280 $\mu$s. The necessary pin can be programmed to AD analog input in 1-bit units, and P2-3 can be set to the reference voltage input. Internal power supply ($V_{DD}$) or constant voltage ($V_{EE}$) can be used as the reference voltage. So battery voltage, etc., can be easily detected. The reference voltage input, for which a built-in operational amp. is used, has high impedance. The A/D converter and all associated controls are performed via sortware. |  |

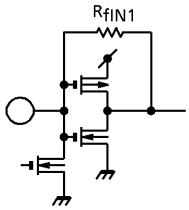
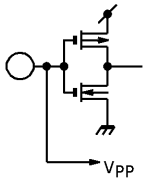
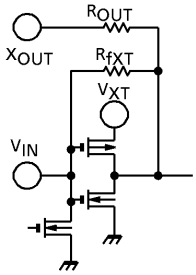
| PIN No. | SYMBOL | PIN NAME | FUNCTION AND OPERATION | REMARKS |
|---|---|---|---|---|
| 46~49 | P3-0 / SI<br>P3-1 / SO<br>P3-2 / $\overline{SCK}$<br>P3-3 / BUZR | I / O port 3<br>/ Serial data input<br>/ Serial data output<br>/ Serial clock I / O<br>/ Buzzer output | 4-bit I / O ports, allowing input and output to be programmed in 1-bit units. Pins P3-0 to P3-2 can also be used for the I / O terminals of serial interface circuits (SIO).<br>SIO functions for 4-bit or 8-bit serial data inputs from the SI pin and outputs from the SO pin at the $\overline{SCK}$ pin clock edge.<br>The clock for serial operation ($\overline{SCK}$) is capable of internal / external options and rise / fall shift options. The SO pin is also capable of switching to serial inputs (SI), facilitating the control of various LSI's and communication between controllers.<br>All SIO inputs use built-in Schmitt circuits.<br>P3-3 pins also functions as the output for a built-in buzzer. The buzzer output can select 8 kinds of 0.625 to 3 kHz frequencies with 4modes: continuous output, single-shot output, 10-Hz intermittent output, and 10-Hz intermittent 1-Hz interval output.<br>SIO, buzzer, and all associated controls can be programmed. |  <br>(excluding P3-3 pins) |
| 50~61 | P4-0 / $\overline{PWM}$<br>P4-1<br>≀<br>P6-2 / $CTR_{IN1}$<br>P6-3 / $CTR_{IN2}$ | I / O port 4<br>/ PWM output<br>I / O port 4<br>≀<br>I / O port 6<br>/ Counter input | 16-bit I / O ports, allowing input and output to be programmed in 1-bit units. The P4-0 pin is also used for built-in 12-bit PWM outputs. The PWM outputs pulse continuously at 73.26 Hz, and can change the duty of the pulses to 256 steps (8 bits), causing the added pulses to be output using 4 bits for 16 cycles (218.5 ms).<br>The P6-2 and P6-3 pins are also used for input purposes when using 20-bit IF counters as 12-bit and 8-bit binary counters.<br>The P6-2 pin can be used for 12-bit binary counter inputs, and the P6-3 pin for 8-bit binary counter inputs.<br>PWM outputs, counter inputs, and all associated controls can be programmed. |  <br>(P4-0~P6-1)<br>  <br>(P6-2, P6-3) |

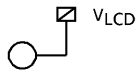
| PIN No. | SYMBOL | PIN NAME | FUNCTION AND OPERATION | REMARKS |
|---|---|---|---|---|
| 62 | MUTE | Muting output port | 1-bit output port, normally used for muting control signal output.<br>This pin can set the internal MUTE bit to "1" according to a change in the input of I/O port 1. MUTE bit output logic can be changed: PLL phase difference can also be output using this pin. |  |
| 63 | TEST | Test mode control input | Input pin used for controlling TEST mode.<br>"H" (high) level indicates TEST mode, while "L" (low) indicates normal operation.<br>The pin is normally used at low level or in NC (no connection) state. (A pull-down resistor is builtin). |  |
| 64 | $IF_{IN}$ / IN1 / $SC_{IN}$ | IF signal input / Input port<br>/ Cycle measurement input | IF signal input pin for the IF counter to count the IF signals of the FM and AM bands and to detect the automatic stop position.<br>The input frequency is between 0.35 to 12 MHz (0.2 $V_{p\text{-}pmin}$). A built-in input amp. and C coupling allow operation at low-level input.<br>The IF counter is a 20 bit counter with optional gate times of 1, 4, 16 and 64 ms. 20 bits of data can be readily stored in memory. This counter is used as a timer when the IF counter is not used.<br>The input pin can be programmed for use as an input port (IN port). CMOS input is used when the pin is set as an IN port.<br>(Note) : To set $SC_{IN}$, use the pin with DC coupling and rectangular wave input. |  |

| PIN No. | SYMBOL | PIN NAME | FUNCTION AND OPERATION | REMARKS |
|---|---|---|---|---|
| 65<br><br><br><br><br><br>66 | DO1 / OT2<br><br><br><br><br><br>DO2 | Phase comparator output / Output port<br><br><br><br><br><br>Phase comparator output | PLL phase comparator output pins. When the prescaler output of the programmable counter is higher than the reference frequency, output is at high level. When output is lower than the reference frequency, output is at low level. When output equals the reference frequency, high impedance output is obtained. Because DO1 and DO2 are output in parallel, optional filter constants can be designed for the FM / VHF and AM bands. Pin DO1 can be programmed to high impedance or programmed as an output port (OT2). Thus, the pins can be used to improve lock-up time or used as output ports. |  |

| PIN No. | SYMBOL | PIN NAME | FUNCTION AND OPERATION | REMARKS |
|---|---|---|---|---|
| 67 | $\overline{\text{HOLD}}$ | Hold mode control input | Input pin for request / release hold mode. Normally, this pin is used to input radio mode selection signals or battery detection signals.<br>Hold mode includes CLOCK STOP mode (stops crystal oscillation) and WAIT mode (halts CPU). Setting is implemented with the CKSTP instruction or the WAIT instruction. When the CKSTP instruction is executed, request / release of the hold mode depends on the internal MODE bit. If the MODE bit is "0" (MODE-0), executing the CKSTP instruction while the $\overline{\text{HOLD}}$ pin is at low level stops the generator and the CPU and changes to memory back-up mode. If the MODE bit is "1" (MODE-1), executing the CKSTP instruction enters memory back-up mode regardless of the level of the $\overline{\text{HOLD}}$ pin. Memory back-up is released when the $\overline{\text{HOLD}}$ pin goes high in MODE-0, or when the $\overline{\text{HOLD}}$ pin input changes in MODE-1.<br>When memory back-up mode is entered by executing a WAIT instruction, any change in the $\overline{\text{HOLD}}$ pin input releases the mode.<br>In memory back-up mode, current consumption is low (below 10 $\mu$A), and all the output pins (e.g., display output, output ports) are automatically set to low level. |  |
| 68 | OT1 | Output port | 1-bit output port.<br>(Note) : This output goes high after reset, and internal latch data is output as is even when CLOCK STOP is being executed. |  |

| PIN No. | SYMBOL | PIN NAME | FUNCTION AND OPERATION | REMARKS |
|---|---|---|---|---|
| 72 | $V_{DD}$ | Power-supply pins | Pins to which power is applied.<br>Normally, $V_{DD}$ = 1.8 to 3.6 V is applied.<br>In back-up mode (when CKSTP instructions are being executed), voltage can be lowered to 1.0 V. If voltage falls below 1.55 V while the CPU is operating, the CPU stops to prevent malfunction (STOP mode). When the voltage rises above 1.55 V, the CPU restarts.<br>STOP mode can be detected by checking the STOP F/F bit. If necessary, execute initialization or adjust clock by program.<br>When detecting or preventing CPU malfunctions using an external circuit, STOP mode can be invalidated and rendered non-operative by program. In that case, all four bits of the internal TEST port should be set to "0".<br>If more than 1.8 V is applied when the pin voltage is 0, the device system is reset and the program starts from address "0". (Power on reset)<br>(Note) : To operate the power on reset, the power supply should start up in 10 to 100 ms. |  |
| 69 | GND | | |  |
| 70 | $FM_{IN}$ | FM local oscillator signal input | Using programmable counter input pins for FM, VHF band.<br>The 1/2 + pulse swallow system (VHF mode) and the pulse swallow system (FM mode) are freely selectable by program.<br>At the VHF mode, local oscillation output (VCO output) of 50 to 230 MHz [0.3 $V_{p-p}$ (Min)] is input, and at the FM mode, that of 40 to 130 MHz [0.2 $V_{p-p}$ (Min)] is input.<br>A built-in input amp. and C coupling allow operation at low-level input.<br>(Note) : When in the PLL OFF mode or when set to $AM_{IN}$ input, the input is pulled down. |  |

| PIN No. | SYMBOL | PIN NAME | FUNCTION AND OPERATION | REMARKS |
|---|---|---|---|---|
| 71 | $AM_{IN}$ | AM local oscillator signal input | Programmable counter input pin for AM band.<br>The pulse swallow system (HF mode) and direct dividing system (LF mode) are freely selectable by program. At the HF mode, local oscillation output (VCO output) of 1 to 45 MHz [0.2 $V_{p-p}$ (Min)] is input, and at the LF mode, 0.9 to 10 MHz [0.2 $V_{p-p}$ (Min)] is input.<br>Built-in input amp. operates with low-level input using a C coupling.<br>(Note) : When in PLL OFF mode or when set to $FM_{IN}$ input, the input is pulled down. |  |
| 73 | $\overline{RESET}$ / $V_{PP}$ | Reset input / Program Voltage Supply | Input pin for system reset signals.<br>$\overline{RESET}$ takes place while at low level; at high level, the program starts from address "0".<br>Normally, if more than 1.8 V is supplied to $V_{DD}$ when the voltage is 0, the system is reset (power on reset).<br>Accordingly, this pin should be set to high level during operation.<br>This pin is used as program voltage supply for One Time PROM. In case of writing program into the internal PROM, 12.5 V is supplied to this pin. |  |
| 74 | $X_{OUT}$ | Crystal oscillator pin | Crystal oscillator pins.<br>A reference 75-kHz crystal resonator is connected to the $X_{IN}$ and $X_{OUT}$ pins.<br>The oscillator stops oscillating during CKSTP instruction execution.<br>The $V_{XT}$ pin is the power supply for the crystal oscillator. A stabilizing capacitor (0.47 $\mu$F typ.) is connected. |  |
| 75 | $X_{IN}$ | | | |
| 76 | $V_{XT}$ | | | |

| PIN No. | SYMBOL | PIN NAME | FUNCTION AND OPERATION | REMARKS |
|---|---|---|---|---|
| 77 | $V_{LCD}$ | Voltage doubler boosting pin | Voltage doubler boosting pin to drive the LCD.<br>A capacitor (0.1 to 3.3 $\mu$F typ.) is connected to boost the voltage.<br>The $V_{LCD}$ pin outputs voltage (3.1 V), which has been doubled from the constant voltage ($V_{EE}$ : 1.55 V) using the capacitor connected between C1 and C2. This potential is supplied to the LCD driver.<br>If the internal $V_{LCD}$ OFF bit is set to "1" by program, an external supply can be input through the $V_{LCD}$ pin to drive the LCD.<br>At this time, the $V_{LCD}$ / 2 potential, whose $V_{LCD}$ voltage divided using resisters, is output from the C2 pin. |  |
| 78 | C1 | | | |
| 79 | C2 | | | |
| 80 | $V_{EE}$ | Constant voltage supply pin | 1.55 V constant voltage supply pin to drive the LCD.<br>A stabilizing capacitor (0.47 $\mu$F Typ.) is connected. This is a reference voltage for the A / D converter, key input, and the bias potential of the LCD common output. | — |

(Note 1) : When the device is reset ($V_{DD}$ = 0 V → 1.8 V or higher or $\overline{RESET}$ = "L" → "H") I / O ports are set to input, the pins for both LCD output and I / O ports and additional functions (e.g., SIO, A / D converter) are set to I / O port input pins, while the $IF_{IN}$ / IN1 / $SC_{IN}$ pins become IF input pins.

(Note 2) : When in PLL OFF mode (when the three bits in the internal reference ports are all set to "1"), the $IF_{IN}$ / $SC_{IN}$ and $FM_{IN}$, $AM_{IN}$ pins are pulled down, and DO1 and DO2 are at high impedance.

(Note 3) : When in CLOCK STOP mode (during execution of CKSTP instruction), the output ports (excluding OT1 output) and LCD output pins are all at low level, while the constant voltage circuit ($V_{EE}$), the voltage doubler circuit ($V_{LCD}$), and the power supply for the crystal oscillator ($V_{XT}$) are at $V_{DD}$ level.

(Note 4) : When the device is being reset, the contents of the output ports and internal ports are undefined and must be initialized via software.

(Note 5) : When the pins for both LCD output and I / O ports are set to the I / O port, $V_{LCD}$ potential is used as the power supply for the output, so the $V_{LCD}$ level is output at "H" level. In addition, the input power supply is at $V_{DD}$ level, so it can be used in the same way as for the other I / O port inputs.

**MAXIMUM RATINGS** (Ta = 25°C)

| CHARACTERISTIC | SYMBOL | RATING | UNIT |
|---|---|---|---|
| Supply Voltage | $V_{DD}$ | −0.3~4.0 | V |
| Program Voltage | $V_{PP}$ | −0.3~13.0 | V |
| Input Voltage | $V_{IN}$ | −0.3~$V_{DD}$ + 0.3 | V |
| Power Dissipation | $P_D$ | 100 | mW |
| Operating Temperature | $T_{opr}$ | −10~60 | °C |
| Storage Temperature | $T_{stg}$ | −55~125 | °C |

**ELECTRICAL CHARACTERISTICS** (Unless otherwise noted, Ta = 25°C, $V_{DD}$ = 3.0 V)

| CHARACTERISTIC | SYMBOL | TEST CIR-CUIT | TEST CONDITION | | MIN | TYP. | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| Range Of Operating Supply Voltage | $V_{DD}$ | — | (*) | | 1.8 | ~ | 3.6 | V |
| Range Of Memory Retention Voltage | $V_{HD}$ | — | Crystal oscillation stopped (CKSTP instruction executed) (*) | | 1.0 | ~ | 3.6 | |
| Operating Current | $I_{DD1}$ | — | Under ordinary operation No output load $FM_{IN}$ = 230 MHz input | $V_{DD}$ = 3.0 V | — | 7.0 | 12 | mA |
| | | | Under ordinary operation No output load $FM_{IN}$ = 130 MHz input | $V_{DD}$ = 3.0 V | — | 6.0 | 10 | |
| | $I_{DD2}$ | — | Under CPU operation only (PLL off, display turned on) | $V_{DD}$ = 3.0 V | — | 65 | 130 | μA |
| | $I_{DD3}$ | — | Soft Wait mode (Crystal oscillator, display circuit operating, CPU stopped, PLL off) | | — | 45 | 90 | |
| | $I_{DD4}$ | — | Hard Wait mode (crystal oscillator operating only) | | — | 35 | 70 | |
| Memory Retention Current | $I_{HD}$ | — | Crystal oscillation stopped (CKSTP instruction executed) | | — | 0.1 | 10 | |
| Crystal Oscillation Frequency | $f_{XT}$ | — | (*) | | — | 75 | — | kHz |
| Crystal oscillation Start-up Time | $t_{ST}$ | — | Crystal oscillation $f_{XT}$ = 75 kHz | | — | — | 1.0 | s |

VOLTAGE DOUBLER CIRCUIT

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| Voltage Doubler Reference Voltage | $V_{EE}$ | — | GND reference ($V_{EE}$) | 1.35 | 1.55 | 1.75 | V |
| Constant Voltage Temperature Characteristics | $D_V$ | — | GND reference ($V_{EE}$) | — | −5 | — | mV/°C |
| Voltage Doubler Boosting Voltage | $V_{LCD}$ | — | GND reference ($V_{LCD}$) | 2.7 | 3.1 | 3.5 | V |

For conditions marked by an asterisk (*), guaranteed when $V_{DD}$ = 1.8 to 3.6 V, Ta = −10 to 60°C

| CHARACTERISTIC | SYMBOL | TEST CIR-CUIT | TEST CONDITION | MIN | TYP. | MAX | UNIT |
|---|---|---|---|---|---|---|---|

OPERATING FREQUENCY RANGES FOR PROGRAMMABLE COUNTER AND LF COUNTER

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| $FM_{IN}$ (VHF Mode) | $f_{VHF}$ | — | Sine wave input when $V_{IN}$ = 0.3 $V_{p-p}$(*) | 50 | ~ | 230 | MHz |
| | | | Sine wave input when $V_{IN}$ = 0.2 $V_{p-p}$, $V_{DD}$ = 1.8~3.0 V, Ta = −10~60°C | | | | |
| $FM_{IN}$ (FM Mode) | $f_{FM}$ | — | Sine wave input when $V_{IN}$ = 0.2 $_{p-p}$ (*) | 40 | ~ | 130 | |
| $AM_{IN}$ (HF Mode) | $f_{HF}$ | — | Sine wave input when $V_{IN}$ = 0.2 $_{p-p}$ (*) | 1 | ~ | 45 | |
| $AM_{IN}$ (LF Mode) | $f_{LF}$ | — | Sine wave input when $V_{IN}$ = 0.2 $_{p-p}$ (*) | 0.9 | ~ | 10 | |
| $IF_{IN}$ | $f_{IF}$ | — | Sine wave input when $V_{IN}$ = 0.2 $_{p-p}$ (*) | 0.35 | ~ | 12 | |
| Input Amplitude | $V_{IN}$ | — | $FM_{IN}$ input (VHF mode) (*) | 0.3 | ~ | $V_{DD}$ − 0.8 | $V_{p-p}$ |
| | | | $FM_{IN}$ input (VHF mode) $V_{DD}$ = 1.8~3.0 V, Ta = −10 to 60°C | 0.2 | ~ | $V_{DD}$ − 0.8 | |
| | | | $FM_{IN}$ (FM mode), $AM_{IN}$, $IF_{IN}$ input (*) | 0.2 | ~ | $V_{DD}$ − 0.8 | |

LCD COMMON OUTPUT / SEGMENT OUTPUT, GENERAL-PURPOSE I / O PORTS
(COM 1 to COM4, S1 to S16, S17 / P7-0 to S25 / P9-0, P9-1 to 3, IN2)

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Output Current | "H" Level | $I_{OH1}$ | — | $V_{LCD}$ = 3 V, $V_{OH}$ = 2.7 V | −0.4 | −0.8 | — | mA |
| | "L" Level | $I_{OL1}$ | — | $V_{LCD}$ = 3 V, $V_{OL}$ = 0.3 V | 0.4 | 0.8 | — | mA |
| Output Voltage 1 / 2 Level | | $V_{BS}$ | — | No load | 1.35 | 1.55 | 1.75 | V |
| Input Leak Current | | $I_{LI}$ | — | $V_{IH}$ = $V_{DD}$, $V_{IL}$ = 0 V (when using I / O port, IN port) | — | — | ±1.0 | μA |
| Input Voltage | "H" Level | $V_{IH1}$ | — | (when using I / O port, IN port) | $V_{DD}$ × 0.6 | ~ | $V_{DD}$ | V |
| | "L" Level | $V_{IL1}$ | — | (when using I / O port, IN port) | 0 | ~ | $V_{DD}$ × 0.1 | |

I / O PORT (P1-0 to P1-3)

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Output Current | "H" Level | $I_{OH1}$ | — | $V_{OH}$ = 2.7 V | −0.4 | −0.8 | — | mA |
| | "L" Level | $I_{OL1}$ | — | $V_{OL}$ = 0.3 V | 0.4 | 0.8 | — | mA |
| Input Leak Current | | $I_{LI}$ | — | $V_{IH}$ = 3.0 V, $V_{IL}$ = 0 V (when using I / O port) | — | — | ±1.0 | μA |
| Input Voltage | "H" Level | $V_{IH2}$ | — | (When using I / O port) | 2.4 | ~ | 3.0 | V |
| | "L" Level | $V_{IL2}$ | — | (When using I / O port) | 0 | ~ | 0.6 | |
| N-ch Load Resistance | | $R_{ON}$ | — | $V_{OL}$ = 3.0 V (When connected to load resistance) | 50 | 100 | 200 | kΩ |

For conditions marked by an asterisk (*), guaranteed when $V_{DD}$ = 1.8 to 3.6 V, Ta = −10 to 60°C

| CHARACTERISTIC | | SYMBOL | TEST CIR-CUIT | TEST CONDITION | MIN | TYP. | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $\overline{HOLD}$ INPUT PORT | | | | | | | | |
| Input Leak Current | | $I_{LI}$ | — | $V_{IH}$ = 3.0 V, $V_{IL}$ = 0 V | — | — | ± 1.0 | μA |
| Input Voltage | "H" Level | $V_{IH3}$ | — | — | 2.4 | ~ | 3.0 | V |
| | "L" Level | $V_{IL3}$ | — | — | 0 | ~ | 1.2 | |
| A / D CONVERTER ($AD_{IN1}$ to $AD_{IN3}$, DC-REF) | | | | | | | | |
| Analog Input Voltage Range | | $V_{AD}$ | — | $AD_{IN1}$~$AD_{IN3}$ | 0 | ~ | $V_{DD}$ | V |
| Analog Reference Voltage Range | | $V_{REF}$ | — | DC-REF, $V_{DD}$ = 2.0~3.6 V | 1.0 | ~ | $V_{DD}$ × 0.9 | V |
| Resolution | | $V_{RES}$ | — | — | — | 6 | — | bit |
| Conversion Total Error | | — | — | $V_{DD}$ = 2.0~3.6 V | — | ± 1.0 | ± 4.0 | LSB |
| Analog Input Leak | | $I_{LI}$ | — | $V_{IH}$ = 3.0 V, $V_{IL}$ = 0 V ($AD_{IN1}$~$AD_{IN3}$, DC-REF) | — | — | ± 1.0 | μA |
| KEY INPUT PORT (K0 to K3) | | | | | | | | |
| Key Input Voltage Range | | $V_{KI}$ | — | — | 0 | ~ | $V_{DD}$ | V |
| A / D Conversion Resolution | | $V_{RES}$ | — | — | — | 3 | — | bit |
| A / D Conversion Total Error | | — | — | $V_{DD}$ = 1.8~2.0 V | — | — | ± 1.5 | LSB |
| | | | | $V_{DD}$ = 2.0~3.6 V | — | — | ± 0.5 | |
| N-ch / P-ch Input Resistance | | $R_{IN1}$ | — | — | 50 | 100 | 200 | kΩ |
| Input Voltage | "H" Level | $V_{IH4}$ | — | When releasing WAIT instruction | 1.8 | ~ | 3.0 | V |
| | "L" Level | $V_{IL4}$ | — | When releasing WAIT instruction | 0 | ~ | 0.3 | V |
| Input Leak Current | | $I_{LI}$ | — | When input resistance is off, $V_{IH}$ = 3.0 V, $V_{IL}$ = 0 V | — | — | ± 1.0 | μA |
| DO1 / OT2, DO2 OUTPUT, MUTE, OT1 OUTPUT | | | | | | | | |
| Output Current | "H" Level | $I_{OH1}$ | — | $V_{OH}$ = 2.7 V | − 0.4 | − 0.8 | — | mA |
| | "L" Level | $I_{OL1}$ | — | $V_{OL}$ = 0.3 V | 0.4 | 0.8 | — | |
| Output Off Leak Current | | $I_{TL}$ | — | $V_{TLH}$ = 3.0 V, $V_{TLL}$ = 0 V (DO1, DO2) | — | — | ± 100 | nA |

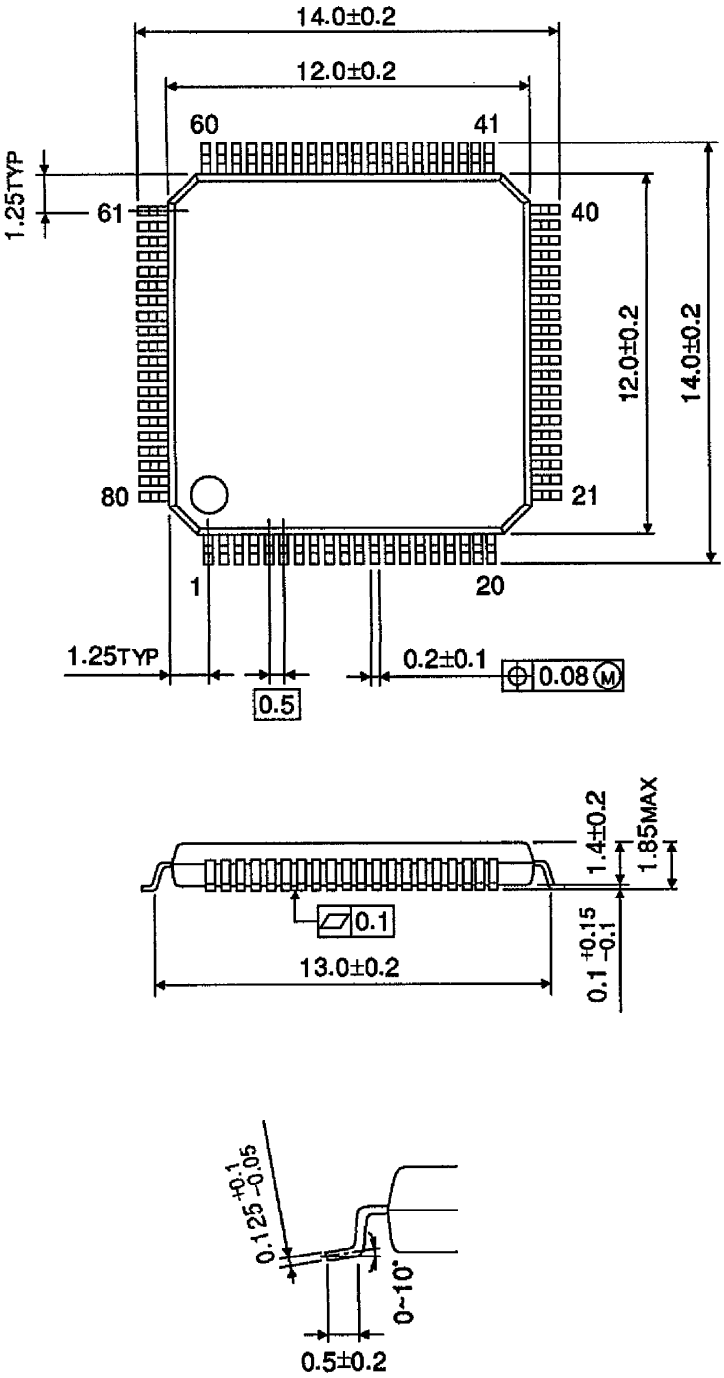
For conditions marked by an asterisk (*), guaranteed when $V_{DD}$ = 1.8 to 3.6 V, Ta = − 10 to 60°C

| CHARACTERISTIC | | SYMBOL | TEST CIR-CUIT | TEST CONDITION | MIN | TYP. | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| GENERAL-PURPOSE I/O PORT (P2-0 to P6-3) | | | | | | | | |
| Output Current | "H" Level | $I_{OH1}$ | — | $V_{OH}$ = 2.7 V | −0.4 | −0.8 | — | mA |
| | "L" Level | $I_{OL1}$ | — | $V_{OL}$ = 0.3 V | 0.4 | 0.8 | — | |
| Input Leak Current | | $I_{LI}$ | — | $V_{IH}$ = 3.0 V, $V_{IL}$ = 0 V | — | — | ±1.0 | μA |
| Input Voltage | "H" Level | $V_{IH2}$ | — | — | 2.4 | ~ | 3.0 | V |
| | "L" Level | $V_{IL2}$ | — | — | 0 | ~ | 0.6 | |
| IN1/$SC_{IN}$, $\overline{RESET}$ INPUT PORT | | | | | | | | |
| Input Leak Current | | $I_{LI}$ | — | $V_{IH}$ = 3.0 V, $V_{IL}$ = 0 V (excluding $SC_{IN}$ input) | — | — | ±1.0 | μA |
| Input Voltage | "H" Level | $V_{IH2}$ | — | — | 2.4 | ~ | 3.0 | V |
| | "L" Level | $V_{IL2}$ | — | — | 0 | ~ | 0.6 | |
| OTHERS | | | | | | | | |
| Input Pull-down Resistance | | $R_{IN2}$ | — | (TEST) | 15 | 30 | 60 | kΩ |
| $X_{IN}$ Amp. Feedback Resistance | | $R_{fXT}$ | — | ($X_{IN}$-$X_{OUT}$) | — | 20 | — | MΩ |
| $X_{OUT}$ Output Resistance | | $R_{OUT}$ | — | ($X_{OUT}$) | — | 4 | — | kΩ |
| Input Amp. Feedback Resistance | | $R_{fIN1}$ | — | ($FM_{IN}$, $AM_{IN}$) | 150 | 300 | 600 | kΩ |
| | | $R_{fIN2}$ | — | ($IF_{IN}$/$SC_{IN}$) | 500 | 1000 | 2000 | |
| Voltage Drop Detection Voltage | | $V_{STP}$ | — | ($V_{DD}$) | 1.35 | 1.55 | 1.75 | V |
| Voltage Drop Detection Temperature Property | | $D_S$ | — | ($V_{DD}$) | — | −3 | — | mV/°C |

For conditions marked by an asterisk (*), guaranteed when $V_{DD}$ = 1.8 to 3.6 V, Ta = −10 to 60°C

**PACKAGE DIMENSIONS**

LQFP80-P-1212-0.50A




Weight : 0.45 g (Typ.)

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