BLL6H1214-500

LDMOS L-band radar power transistor

Rev. 02 — 1 April 2010 Product data sheet

1. Product profile

1.1 General description

500 W LDMOS power transistor intended for L-band radar applications in the 1.2 GHz to 1.4 GHz range.

Table 1. Test information

Typical RF performance at T_{case} = 25 °C; t_p = 300 µs; δ = 10 %; I_{Dq} = 150 mA; in a class-AB production test circuit.

Mode of operation	f (GHz)	V_{DS} (V)	P_L (W)	G_p (dB)	η_D (%)	t_r (ns)	t_f (ns)
pulsed RF	1.2 to 1.4	50	500	17	50	20	6

CAUTION

This device is sensitive to ElectroStatic Discharge (ESD). Therefore care should be taken during transport and handling.

1.2 Features and benefits

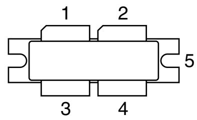
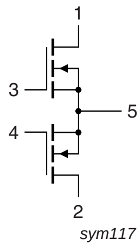
- Typical pulsed RF performance at a frequency of 1.2 GHz to 1.4 GHz, a supply voltage of 50 V, an I_{Dq} of 150 mA, a t_p of 300 µs with δ of 10 %:
  - Output power = 500 W
  - Power gain = 17 dB
  - Efficiency = 50 %
- Easy power control
- Integrated ESD protection
- High flexibility with respect to pulse formats
- Excellent ruggedness
- High efficiency
- Excellent thermal stability
- Designed for broadband operation (1.2 GHz to 1.4 GHz)
- Internally matched for ease of use
- Compliant to Directive 2002/95/EC, regarding restriction of hazardous substances (RoHS)

1.3 Applications

- L-band power amplifiers for radar applications in the 1.2 GHz to 1.4 GHz frequency range

2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
1	drain1		
2	drain2		
3	gate1		
4	gate2		
5	source [1]		

[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLL6H1214-500	-	flanged balanced LDMOST ceramic package; 2 mounting holes; 4 leads	SOT539A

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	100	V
V_{GS}	gate-source voltage		–0.5	+13	V
I_D	drain current		-	45	A
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature		-	200	°C

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$Z_{th(j-c)}$	transient thermal impedance from junction to case	T_{case} = 85 °C; P_L = 500 W		
		t_p = 100 µs; δ = 10 %	0.07	K/W
		t_p = 200 µs; δ = 10 %	0.08	K/W
		t_p = 300 µs; δ = 10 %	0.1	K/W
		t_p = 100 µs; δ = 20 %	0.1	K/W

6. Characteristics

Table 6. DC characteristics

T_j = 25 °C; per section unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 V; I_D = 2.7 mA	100	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 10 V; I_D = 270 mA	1.3	1.8	2.2	V
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 50 V	-	-	1.4	µA
I_{DSX}	drain cut-off current	V_{GS} = $V_{GS(th)}$ + 3.75 V; V_{DS} = 10 V	32	42	-	A
I_{GSS}	gate leakage current	V_{GS} = 11 V; V_{DS} = 0 V	-	-	140	nA
g_{fs}	forward transconductance	V_{DS} = 10 V; I_D = 270 mA	1.7	3	-	S
$R_{DS(on)}$	drain-source on-state resistance	V_{GS} = $V_{GS(th)}$ + 3.75 V; I_D = 9.5 A	-	100	164	mΩ

Table 7. RF characteristics

Mode of operation: pulsed RF; t_p = 300 µs; δ = 10 %; RF performance at V_{DS} = 50 V; I_{Dq} = 150 mA; T_{case} = 25 °C; unless otherwise specified, in a class-AB production test circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
P_L	output power		500	-	-	W
V_{DS}	drain-source voltage	P_L = 500 W	-	-	50	V
G_p	power gain	P_L = 500 W	15	17	-	dB
RL_{in}	input return loss	P_L = 500 W	-	10	-	dB
$P_{L(1dB)}$	output power at 1 dB gain compression		-	600	-	W
η_D	drain efficiency	P_L = 500 W	45	50	-	%
$P_{droop(pulse)}$	pulse droop power	P_L = 500 W	-	0	0.3	dB
t_r	rise time	P_L = 500 W	-	20	50	ns
t_f	fall time	P_L = 500 W	-	6	50	ns

6.1 Ruggedness in class-AB operation

The BLL6H1214-500 is capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions: V_{DS} = 50 V; I_{Dq} = 150 mA; P_L = 500 W; t_p = 300 µs; δ = 10 %.

7. Application information

7.1 Impedance information

Table 8. Typical impedance

Typical values per section unless otherwise specified.

f GHz	Z_S Ω	Z_L Ω
1.2	1.268 – j2.623	2.987 – j1.664
1.3	2.193 – j2.457	2.162 – j1.326
1.4	2.359 – j2.052	1.604 – j1.887

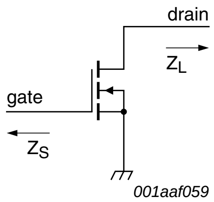
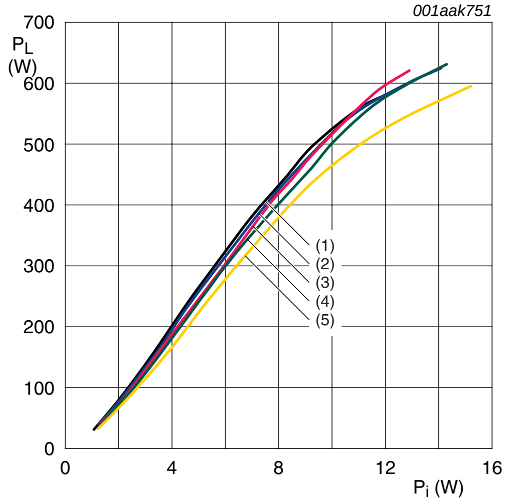


Fig 1. Definition of transistor impedance

7.2 RF performance

7.2.1 Performance curves measured with δ = 10 %, t_p = 300 μs and T_{hs} = 25 °C



V_{DS} = 50 V; t_p = 300 µs; δ = 10 %; I_{Dq} = 150 mA.

(1) f = 1200 MHz

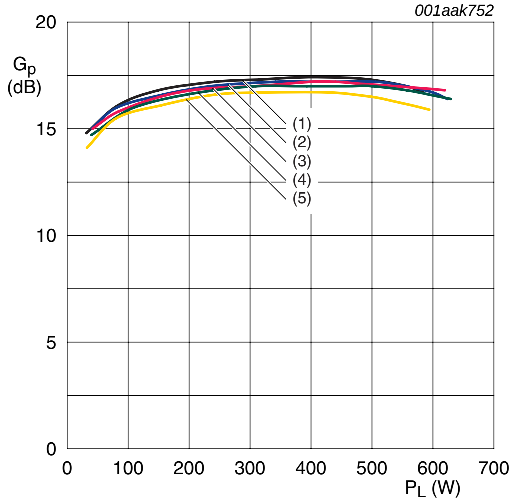
(2) f = 1250 MHz

(3) f = 1300 MHz

(4) f = 1350 MHz

(5) f = 1400 MHz

Fig 2. Output power as a function of input power; typical values



V_{DS} = 50 V; t_p = 300 µs; δ = 10 %; I_{Dq} = 150 mA.

(1) f = 1200 MHz

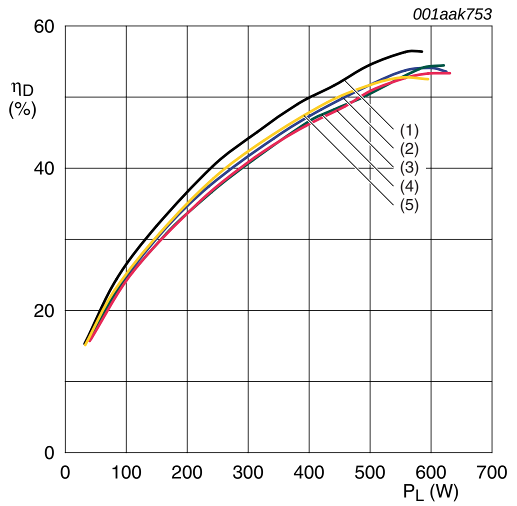
(2) f = 1250 MHz

(3) f = 1300 MHz

(4) f = 1350 MHz

(5) f = 1400 MHz

Fig 3. Power gain as a function of load power; typical values



V_{DS} = 50 V; t_p = 300 μs; δ = 10 %; I_{Dq} = 150 mA.

(1) f = 1200 MHz

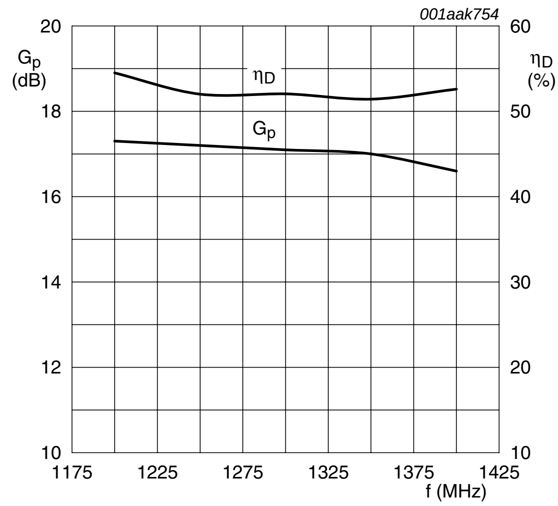
(2) f = 1250 MHz

(3) f = 1300 MHz

(4) f = 1350 MHz

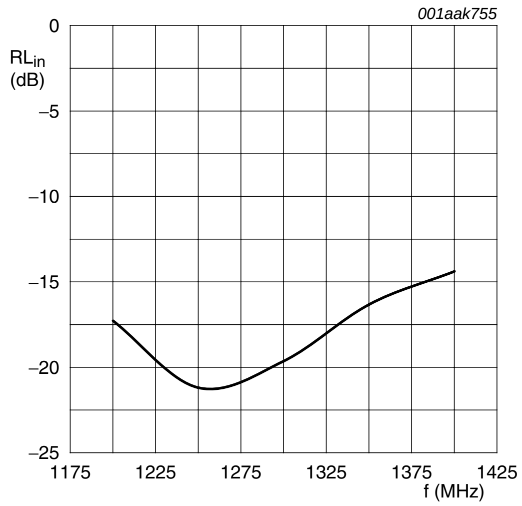
(5) f = 1400 MHz

Fig 4. Drain efficiency as a function of load power; typical values



V_{DS} = 50 V; t_p = 300 μs; δ = 10 %; I_{Dq} = 150 mA.

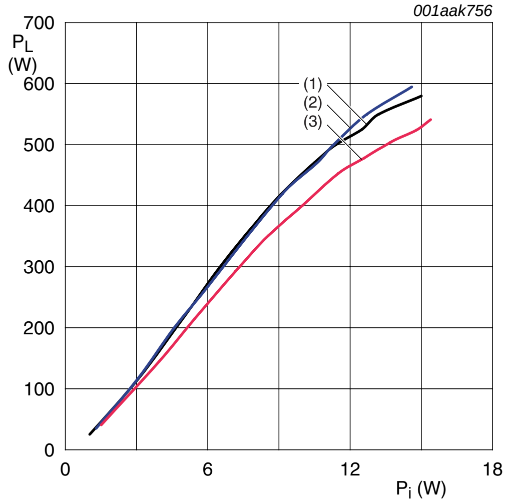
Fig 5. Power gain and drain efficiency as function of frequency; typical values



P_L = 500 W; V_{DS} = 50 V; t_p = 300 μs; δ = 10 %; I_{Dq} = 150 mA.

Fig 6. Input return loss as a function of frequency; typical value

7.2.2 Performance curves measured with δ = 10 %, t_p = 300 μs and T_{hs} = 65 °C



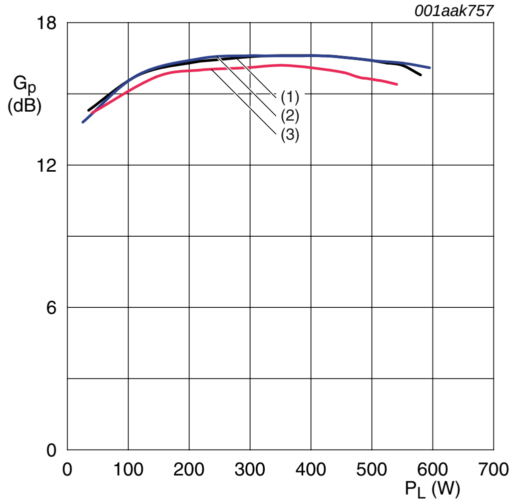
V_{DS} = 50 V; t_p = 300 µs; δ = 10 %; I_{Dq} = 100 mA.

(1) f = 1200 MHz

(2) f = 1300 MHz

(3) f = 1400 MHz

Fig 7. Output power as a function of input power; typical values



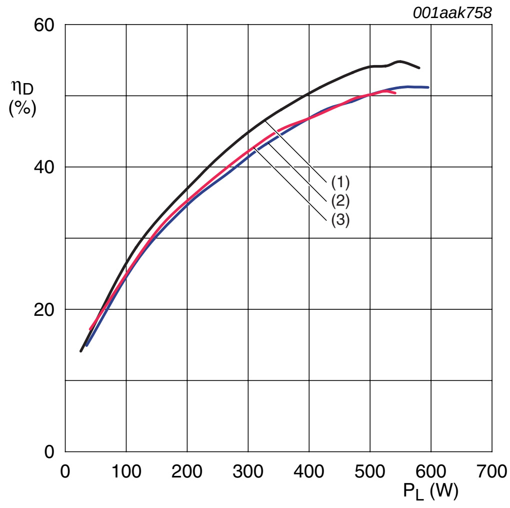
V_{DS} = 50 V; t_p = 300 µs; δ = 10 %; I_{Dq} = 100 mA.

(1) f = 1200 MHz

(2) f = 1300 MHz

(3) f = 1400 MHz

Fig 8. Power gain as a function of load power; typical values



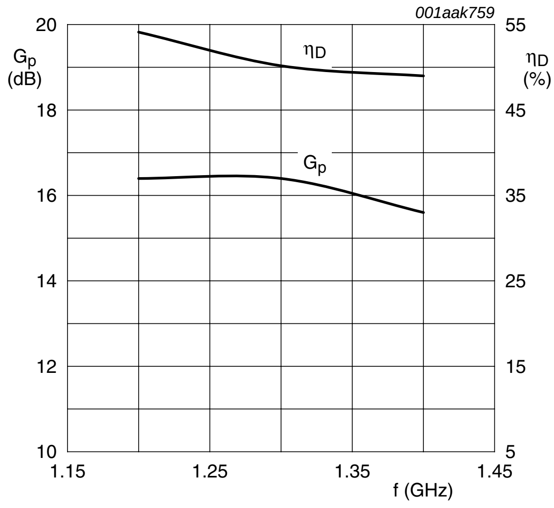
V_{DS} = 50 V; t_p = 300 µs; δ = 10 %; I_{Dq} = 100 mA.

(1) f = 1200 MHz

(2) f = 1300 MHz

(3) f = 1400 MHz

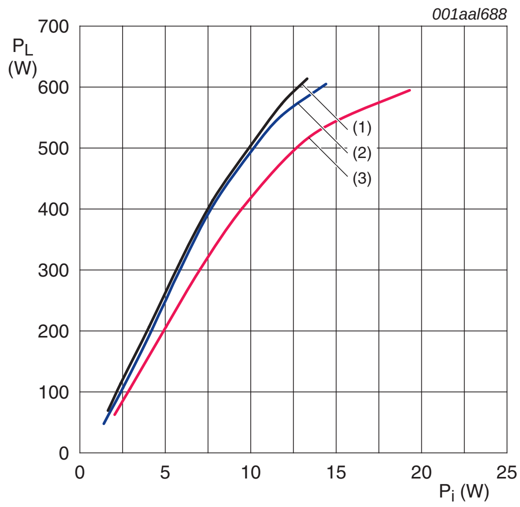
Fig 9. Drain efficiency as a function of load power; typical values



P_L = 250 W; V_{DS} = 50 V; t_p = 300 µs; δ = 10 %; I_{Dq} = 100 mA.

Fig 10. Power gain and drain efficiency as function of frequency; typical values

7.2.3 Performance curves measured with δ = 10 %, t_p = 300 μs and f = 1300 MHz



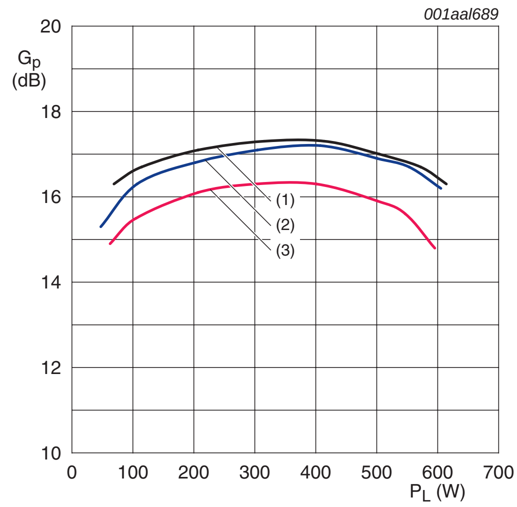
V_{DS} = 50 V; t_p = 300 µs; δ = 10 %; I_{Dq} = 150 mA; f = 1300 MHz.

(1) T_{hs} = –40 °C

(2) T_{hs} = 25 °C

(3) T_{hs} = 65°C

Fig 11. Output power as a function of input power; typical values



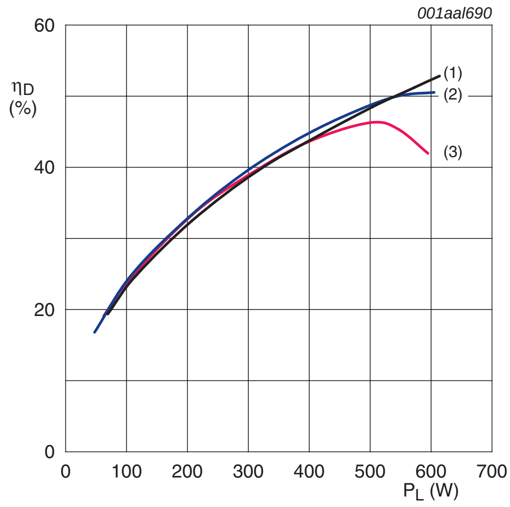
V_{DS} = 50 V; t_p = 300 µs; δ = 10 %; I_{Dq} = 150 mA; f = 1300 MHz.

(1) T_{hs} = –40 °C

(2) T_{hs} = 25 °C

(3) T_{hs} = 65°C

Fig 12. Power gain as a function of load power; typical values



V_{DS} = 50 V; t_p = 300 µs; δ = 10 %; I_{Dq} = 150 mA; f = 1300 MHz.

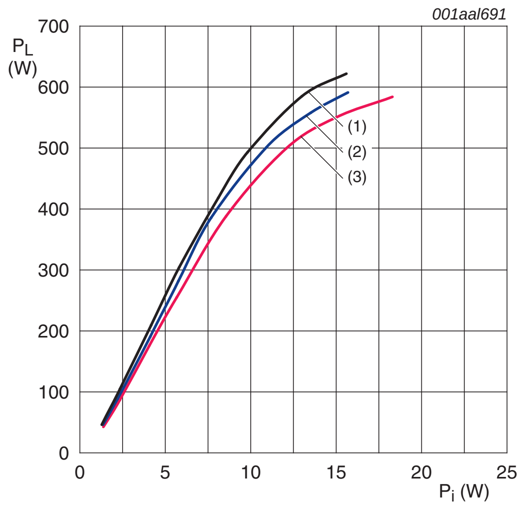
(1) T_{hs} = –40 °C

(2) T_{hs} = 25 °C

(3) T_{hs} = 65°C

Fig 13. Drain efficiency as a function of load power; typical values

7.2.4 Performance curves measured with δ = 20 %, t_p = 500 μs and T_{hs} = 25 °C



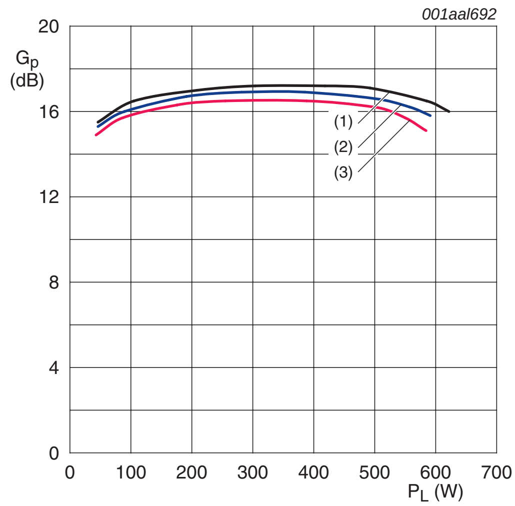
V_{DS} = 50 V; t_p = 500 µs; δ = 20 %; I_{Dq} = 150 mA.

(1) f = 1200 MHz

(2) f = 1300 MHz

(3) f = 1400 MHz

Fig 14. Output power as a function of input power; typical values



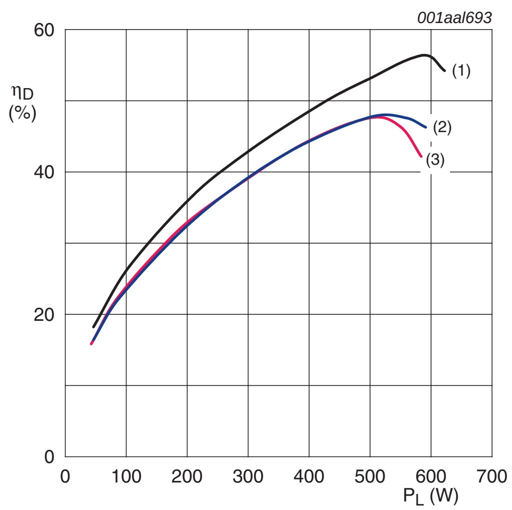
V_{DS} = 50 V; t_p = 500 µs; δ = 20 %; I_{Dq} = 150 mA.

(1) f = 1200 MHz

(2) f = 1300 MHz

(3) f = 1400 MHz

Fig 15. Power gain as a function of load power; typical values



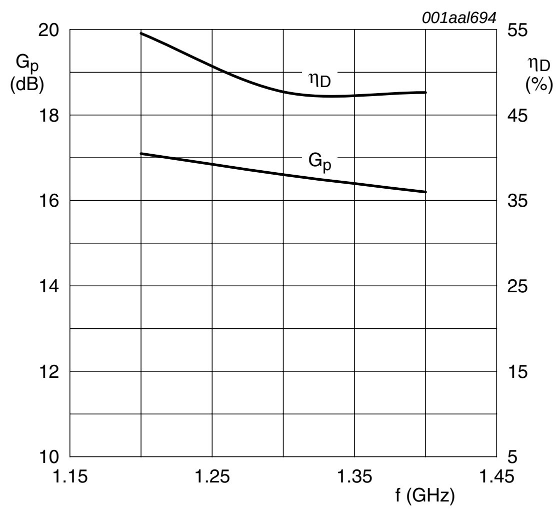
V_{DS} = 50 V; t_p = 500 µs; δ = 20 %; I_{Dq} = 150 mA.

(1) f = 1200 MHz

(2) f = 1300 MHz

(3) f = 1400 MHz

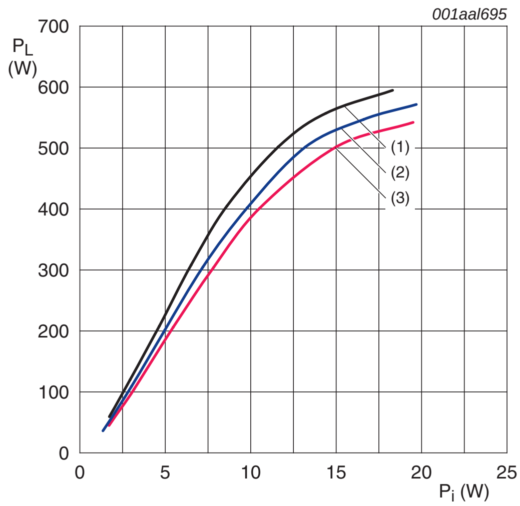
Fig 16. Drain efficiency as a function of load power; typical values



V_{DS} = 50 V; t_p = 500 µs; δ = 20 %; I_{Dq} = 150 mA.

Fig 17. Power gain and drain efficiency as function of frequency; typical values

7.2.5 Performance curves measured with δ = 20 %, t_p = 500 μs and T_{hs} = 65 °C



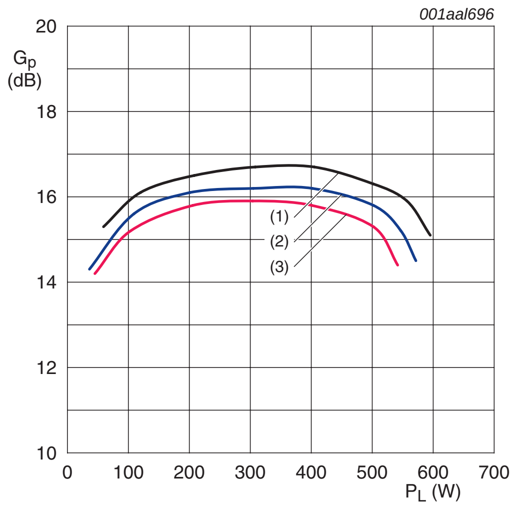
V_{DS} = 50 V; t_p = 500 µs; δ = 20 %; I_{Dq} = 150 mA.

(1) f = 1200 MHz

(2) f = 1300 MHz

(3) f = 1400 MHz

Fig 18. Output power as a function of input power; typical values



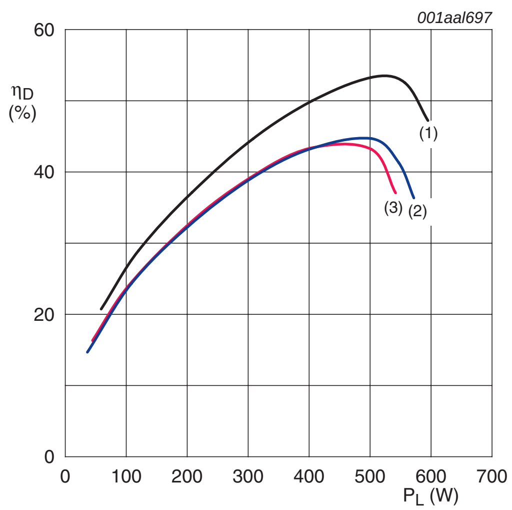
V_{DS} = 50 V; t_p = 500 µs; δ = 20 %; I_{Dq} = 150 mA.

(1) f = 1200 MHz

(2) f = 1300 MHz

(3) f = 1400 MHz

Fig 19. Power gain as a function of load power; typical values



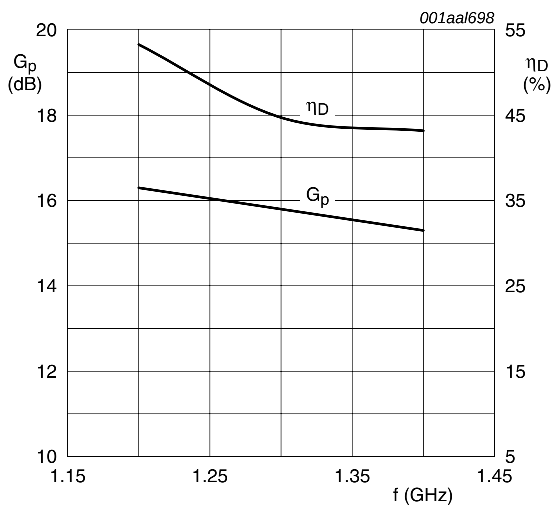
V_{DS} = 50 V; t_p = 500 µs; δ = 20 %; I_{Dq} = 150 mA.

(1) f = 1200 MHz

(2) f = 1300 MHz

(3) f = 1400 MHz

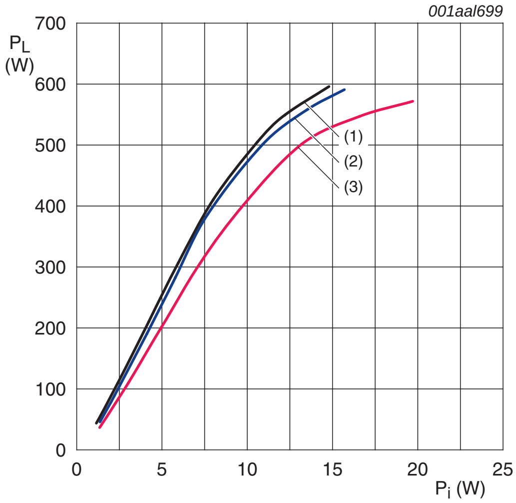
Fig 20. Drain efficiency as a function of load power; typical values



V_{DS} = 50 V; t_p = 500 µs; δ = 20 %; I_{Dq} = 150 mA.

Fig 21. Power gain and drain efficiency as function of frequency; typical values

7.2.6 Performance curves measured with δ = 20 %, t_p = 500 μs and f = 1300 MHz



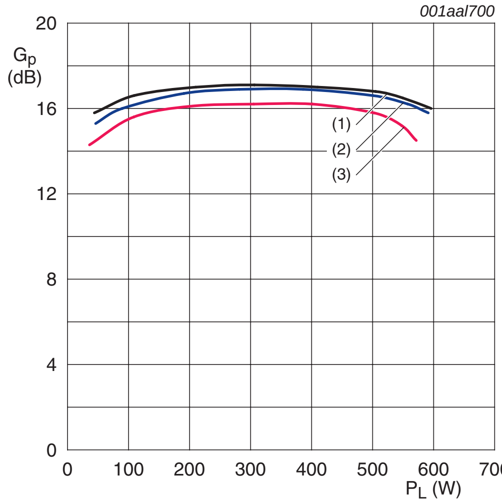
V_{DS} = 50 V; t_p = 500 µs; δ = 20 %; I_{Dq} = 150 mA; f = 1300 MHz.

(1) T_{hs} = –40 °C

(2) T_{hs} = 25 °C

(3) T_{hs} = 65°C

Fig 22. Output power as a function of input power; typical values



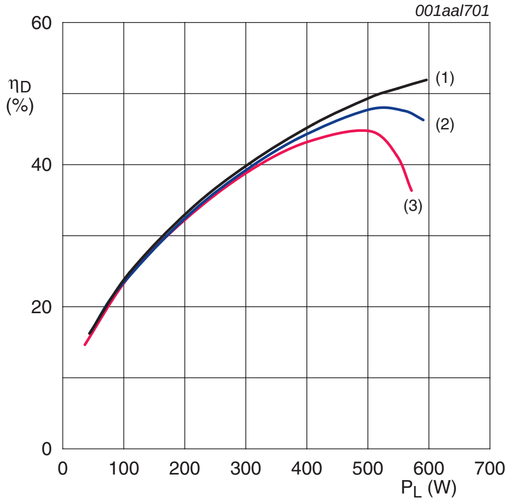
V_{DS} = 50 V; t_p = 500 µs; δ = 20 %; I_{Dq} = 150 mA; f = 1300 MHz.

(1) T_{hs} = –40 °C

(2) T_{hs} = 25 °C

(3) T_{hs} = 65°C

Fig 23. Power gain as a function of load power; typical values



V_{DS} = 50 V; t_p = 500 µs; δ = 20 %; I_{Dq} = 150 mA; f = 1300 MHz.

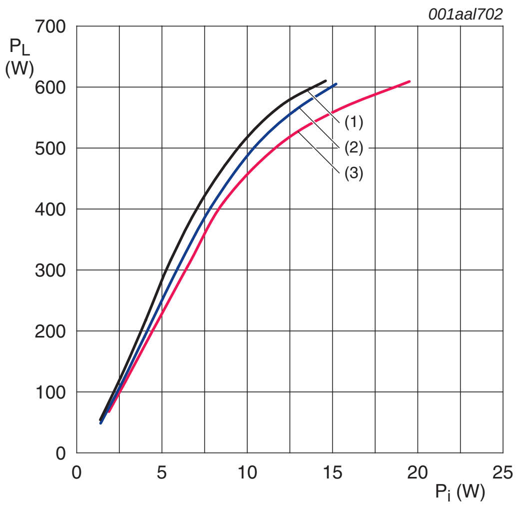
(1) T_{hs} = –40 °C

(2) T_{hs} = 25 °C

(3) T_{hs} = 65°C

Fig 24. Drain efficiency as a function of load power; typical values

7.2.7 Performance curves measured with δ = 10 %, t_p = 1 ms and T_{hs} = 25 °C



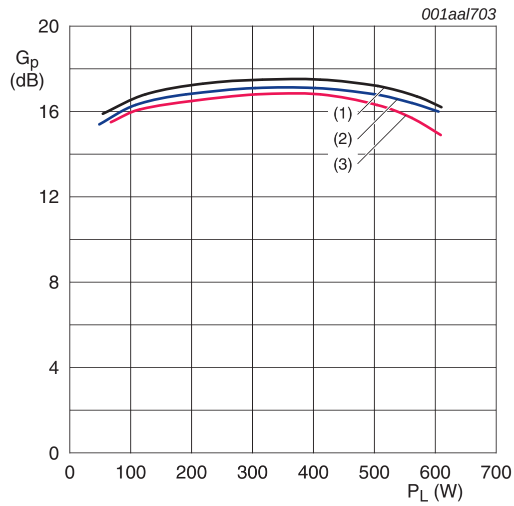
V_{DS} = 50 V; t_p = 500 μs; δ = 20 %; I_{Dq} = 150 mA.

(1) f = 1200 MHz

(2) f = 1300 MHz

(3) f = 1400 MHz

Fig 25. Output power as a function of input power; typical values



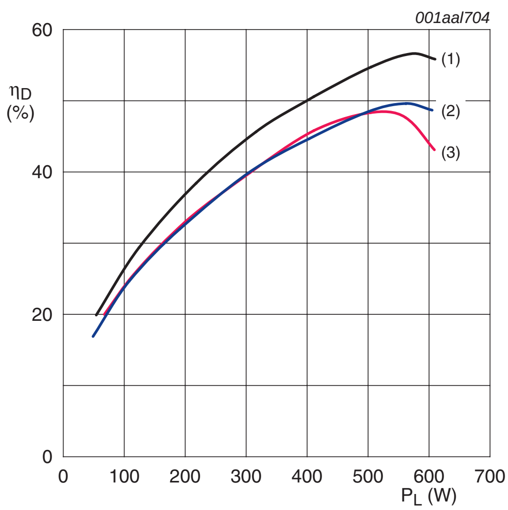
V_{DS} = 50 V; t_p = 500 μs; δ = 20 %; I_{Dq} = 150 mA.

(1) f = 1200 MHz

(2) f = 1300 MHz

(3) f = 1400 MHz

Fig 26. Power gain as a function of load power; typical values



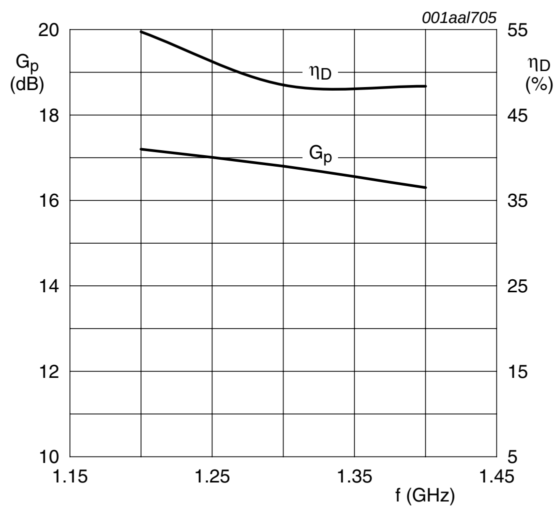
V_{DS} = 50 V; t_p = 500 μs; δ = 20 %; I_{Dq} = 150 mA.

(1) f = 1200 MHz

(2) f = 1300 MHz

(3) f = 1400 MHz

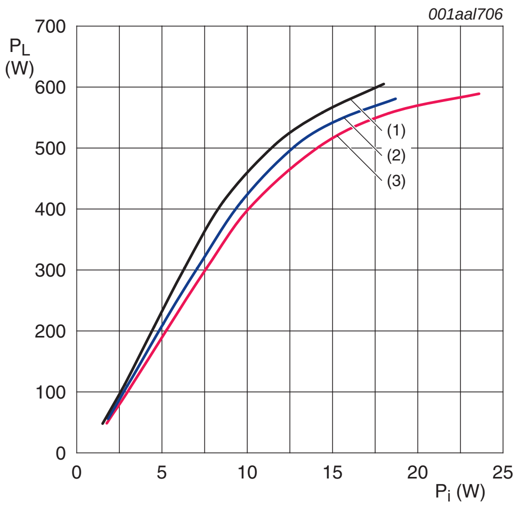
Fig 27. Drain efficiency as a function of load power; typical values



V_{DS} = 50 V; t_p = 500 μs; δ = 20 %; I_{Dq} = 150 mA.

Fig 28. Power gain and drain efficiency as function of frequency; typical values

7.2.8 Performance curves measured with δ = 10 %, t_p = 1 ms and T_{hs} = 65 °C



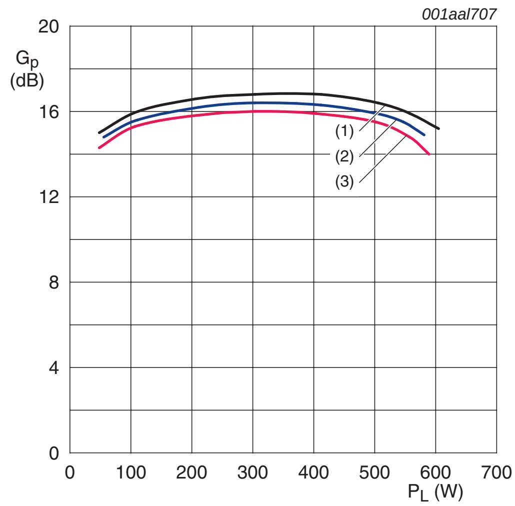
V_{DS} = 50 V; t_p = 500 µs; δ = 20 %; I_{Dq} = 150 mA.

(1) f = 1200 MHz

(2) f = 1300 MHz

(3) f = 1400 MHz

Fig 29. Output power as a function of input power; typical values



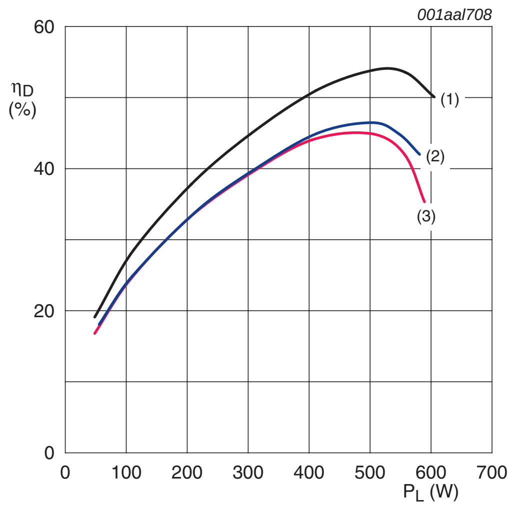
V_{DS} = 50 V; t_p = 500 µs; δ = 20 %; I_{Dq} = 150 mA.

(1) f = 1200 MHz

(2) f = 1300 MHz

(3) f = 1400 MHz

Fig 30. Power gain as a function of load power; typical values



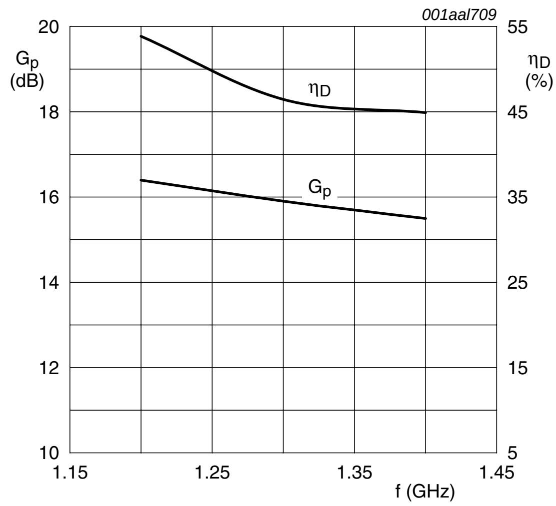
V_{DS} = 50 V; t_p = 500 µs; δ = 20 %; I_{Dq} = 150 mA.

(1) f = 1200 MHz

(2) f = 1300 MHz

(3) f = 1400 MHz

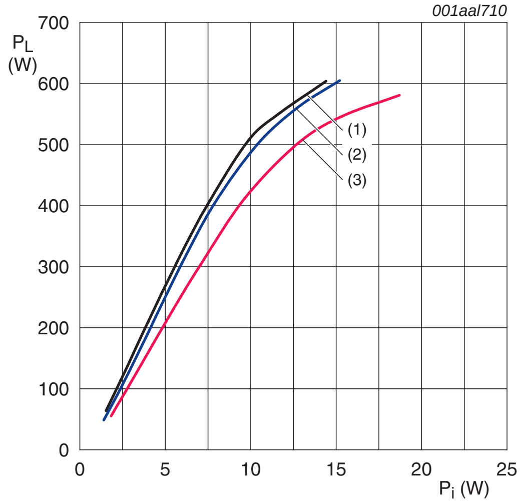
Fig 31. Drain efficiency as a function of load power; typical values



V_{DS} = 50 V; t_p = 500 µs; δ = 20 %; I_{Dq} = 150 mA.

Fig 32. Power gain and drain efficiency as function of frequency; typical values

7.2.9 Performance curves measured with δ = 10 %, t_p = 1 ms and f = 1300 MHz



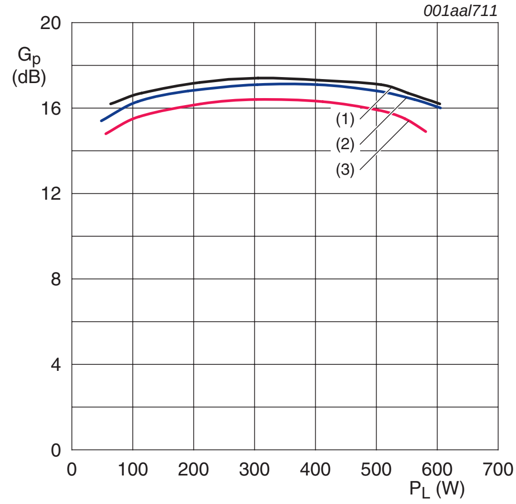
V_{DS} = 50 V; t_p = 500 μs; δ = 20 %; I_{Dq} = 150 mA; f = 1300 MHz.

(1) T_{hs} = –40 °C

(2) T_{hs} = 25 °C

(3) T_{hs} = 65°C

Fig 33. Output power as a function of input power; typical values



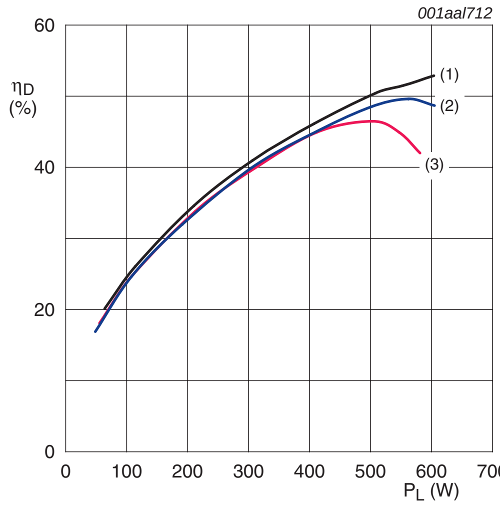
V_{DS} = 50 V; t_p = 500 μs; δ = 20 %; I_{Dq} = 150 mA; f = 1300 MHz.

(1) T_{hs} = –40 °C

(2) T_{hs} = 25 °C

(3) T_{hs} = 65°C

Fig 34. Power gain as a function of load power; typical values



V_{DS} = 50 V; t_p = 500 μs; δ = 20 %; I_{Dq} = 150 mA; f = 1300 MHz.

(1) T_{hs} = –40 °C

(2) T_{hs} = 25 °C

(3) T_{hs} = 65°C

Fig 35. Drain efficiency as a function of load power; typical values

8. Test information

Table 9. List of components

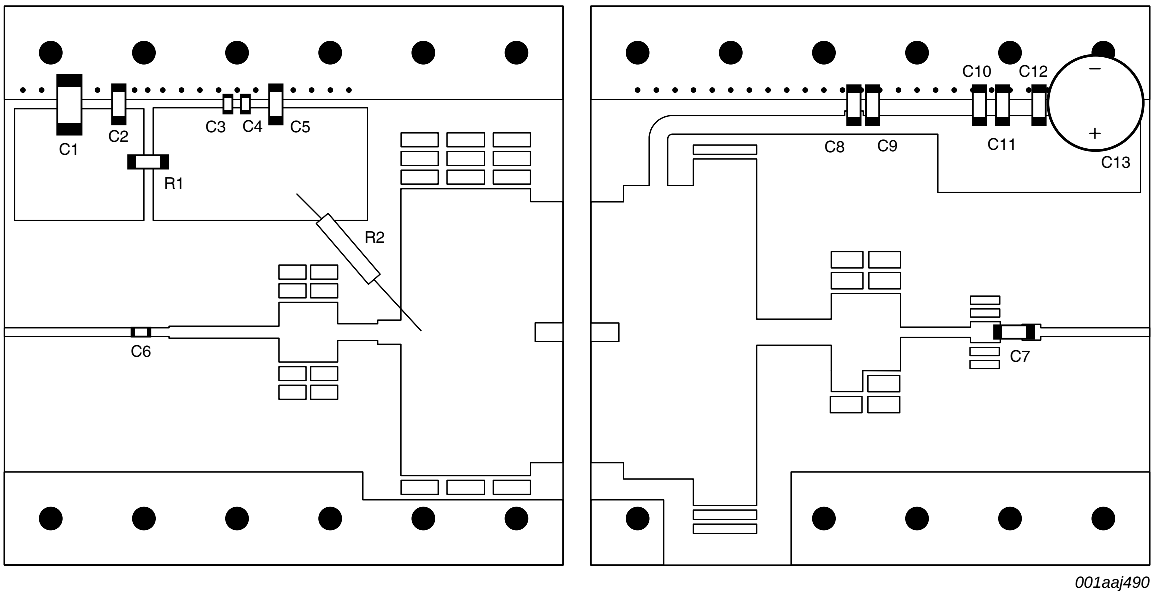
For test circuit see Figure 36.

Component	Description	Value		Remarks
C1	multilayer ceramic chip capacitor	22 μF; 35 V		
C2	multilayer ceramic chip capacitor	51 pF	[1]	
C3, C4	multilayer ceramic chip capacitor	100 pF	[1]	
C5, C11, C12	multilayer ceramic chip capacitor	1 nf	[2]	
C6	multilayer ceramic chip capacitor	47 pF	[1]	
C7, C8, C10	multilayer ceramic chip capacitor	51 pF	[3]	
C9	multilayer ceramic chip capacitor	100 pF	[3]	
C13	electrolytic capacitor	10 μF; 63 V		
R1	SMD resistor	56 Ω		0603
R2	metal film resistor	51 Ω		

[1] American Technical Ceramics type 100A or capacitor of same quality.

[2] American Technical Ceramics type 100B or capacitor of same quality.

[3] American Technical Ceramics type 800B or capacitor of same quality.



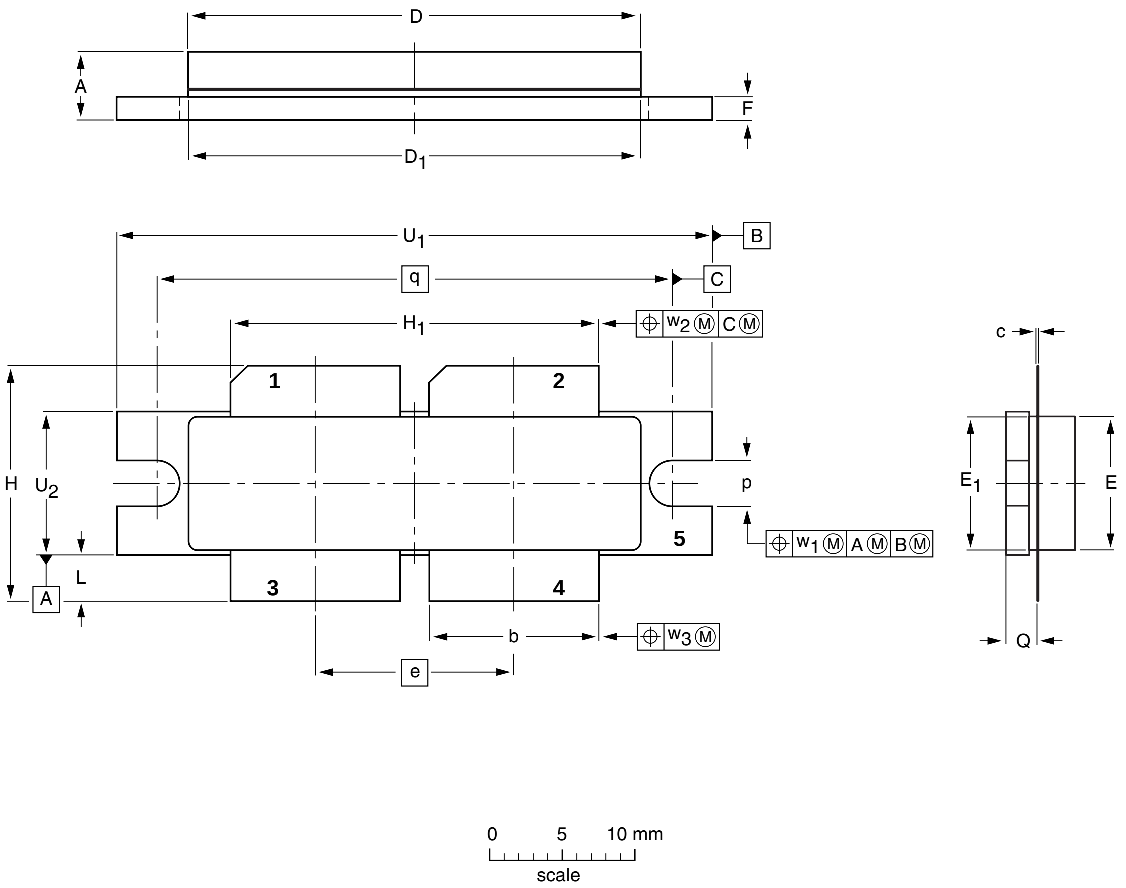
Printed-Circuit Board (PCB): Duroid 6006; ε_r = 6.15 F/m; thickness = 0.64 mm; thickness copper plating = 35 μm.

See Table 9 for a list of components.

Fig 36. Component layout for class-AB production test circuit

9. Package outline

Flanged balanced LDMOST ceramic package; 2 mounting holes; 4 leads **SOT539A**



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D_1	e	E	E_1	F	H	H_1	L	p	Q	q	U_1	U_2	w_1	w_2	w_3
mm	4.7 4.2	11.81 11.56	0.18 0.10	31.55 30.94	31.52 30.96	13.72	9.50 9.30	9.53 9.27	1.75 1.50	17.12 16.10	25.53 25.27	3.48 2.97	3.30 3.05	2.26 2.01	35.56	41.28 41.02	10.29 10.03	0.25	0.51	0.25
inches	0.185 0.165	0.465 0.455	0.007 0.004	1.242 1.218	1.241 1.219	0.540	0.374 0.366	0.375 0.365	0.069 0.059	0.674 0.634	1.005 0.995	0.137 0.117	0.130 0.120	0.089 0.079	1.400	1.625 1.615	0.405 0.395	0.010	0.020	0.010

Note
1. millimeter dimensions are derived from the original inch dimensions.
2. recommended screw pitch dimension of 1.52 inch (38.6 mm) based on M3 screw.

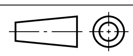
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT539A						~~00-03-03~~ 10-02-02

Fig 37. Package outline SOT539A

10. Abbreviations

Table 10. Abbreviations

Acronym	Description
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
LDMOST	Laterally Diffused Metal-Oxide Semiconductor Transistor
RF	Radio Frequency
SMD	Surface Mounted Device
L-band	Long wave Band
VSWR	Voltage Standing-Wave Ratio

11. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLL6H1214-500_2	20100401	Product data sheet	-	BLL6H1214-500_1
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • The status of this data sheet has been changed to “Product data sheet” • Added Section 7.2.3 on page 8. • Added Section 7.2.4 on page 9. • Added Section 7.2.5 on page 10. • Added Section 7.2.6 on page 11. • Added Section 7.2.7 on page 12. • Added Section 7.2.8 on page 13. • Added Section 7.2.9 on page 14.			
BLL6H1214-500_1	20090120	Objective data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term ‘short data sheet’ is explained in section “Definitions”.

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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14. Contents

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