



1:5 Clock Driver with Selectable LVPECL Inputs and LVDS Outputs

General Description

The MAX9310 is a fast, low-skew 1:5 differential driver with selectable LVPECL/HSTL inputs and LVDS outputs, designed for clock distribution applications. This device features an ultra-low propagation delay of 345ps with 45.5mA of supply current.

The MAX9310 operates from a 2.375V to 2.625V power supply for use in 2.5V systems. A 2:1 input multiplexer is used to select one of two differential inputs. The input selection is controlled through the CLKSEL pin. This device also features a synchronous enable function.

The MAX9310 is offered in a space-saving 20-pin TSSOP package and operates over the extended temperature range from -40°C to +85°C.

Applications

Data and Clock Drivers and Buffers
Central-Office Backplane Clock Distribution
DSLAM
Base Stations
ATE

Features

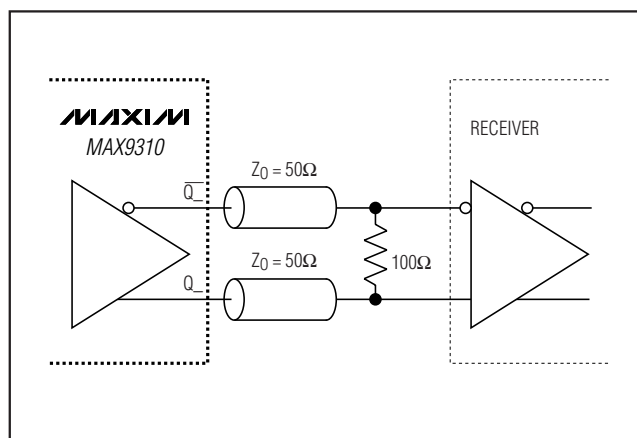
- ◆ Guaranteed 1.0GHz Operating Frequency
- ◆ 8ps Output-to-Output Skew
- ◆ 345ps Propagation Delay
- ◆ Accepts LVPECL and Differential HSTL Inputs
- ◆ Synchronous Output Enable/Disable
- ◆ Two Selectable Differential Inputs
- ◆ 2.375V to 2.625V Supply Voltage
- ◆ ESD Protection: $\pm 2\text{kV}$ (Human Body Model)
- ◆ Input Bias Resistors Drive Output Low for Open Inputs

Ordering Information

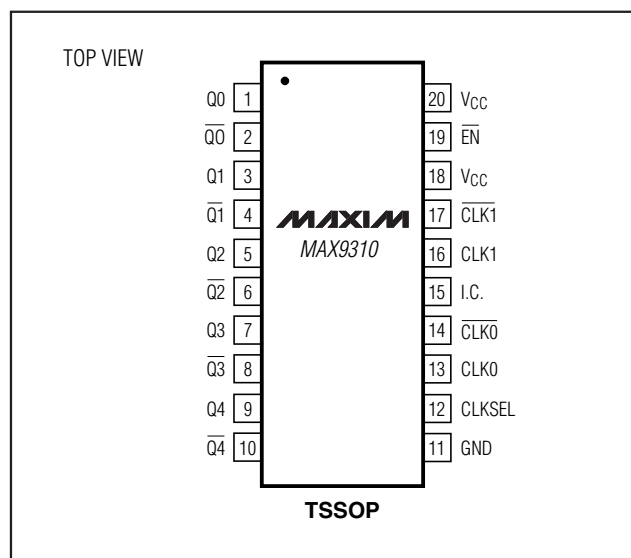
PART	TEMP RANGE	PIN-PACKAGE
MAX9310EUP	-40°C to +85°C	20 TSSOP

Functional diagram appears at end of data sheet.

Typical Application Circuit



Pin Configuration



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ABSOLUTE MAXIMUM RATINGS

V_{CC} to GND	-0.3V to +4.1V
$\overline{EN}$, CLKSEL, CLK_, $\overline{CLK}_-$ to GND	-0.3V to ($V_{CC} + 0.3V$)
CLK_ to $\overline{CLK}_-$	$V_{CC} - GND$
Continuous Output Current	24mA
Surge Output Current	50mA
Continuous Power Dissipation ($T_A = +70^\circ C$)	
Single-Layer PC Board	
20-Pin TSSOP (derate 7.69mW/ $^\circ C$ above $+70^\circ C$)	615mW
Multilayer PC Board	
20-Pin TSSOP (derate 11mW/ $^\circ C$ above $+70^\circ C$)	879mW
Junction-to-Ambient Thermal Resistance in Still Air	
Single-Layer PC Board	
20-Pin TSSOP	+130 $^\circ C/W$

Multilayer PC Board	
20-Pin TSSOP	+91 $^\circ C/W$
Junction-to-Ambient Thermal Resistance with 500LFPM	
Airflow Single-Layer PC board	
20-Pin TSSOP	+96 $^\circ C/W$
Junction-to-Case Thermal Resistance	
20-Pin TSSOP	+20 $^\circ C/W$
Operating Temperature Range	-40 $^\circ C$ to +85 $^\circ C$
Junction Temperature	+150 $^\circ C$
Storage Temperature Range	-65 $^\circ C$ to +150 $^\circ C$
ESD Protection	
Human Body Model (inputs and outputs)	$\pm 2kV$
Lead Temperature (soldering, 10s)	+300 $^\circ C$

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

($V_{CC} - GND = 2.375V$ to $2.625V$, outputs terminated with $100\Omega \pm 1\%$, unless otherwise noted. Typical values are at $V_{CC} - GND = 2.5V$, $V_{IHD} = V_{CC} - 1.0V$, $V_{ILD} = V_{CC} - 1.5V$, unless otherwise noted.) (Notes 1, 2, and 3)

PARAMETER	SYMBOL	CONDITIONS	-40°C			+25°C			+85°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
SINGLE-ENDED INPUTS (CLKSEL, $\overline{EN}$)												
Input High Voltage	V _{IH}		V _{CC} - 1.165		V _{CC} - 0.88	V _{CC} - 1.165		V _{CC} - 0.88	V _{CC} - 1.165		V _{CC} - 0.88	V
Input Low Voltage	V _{IL}		V _{CC} - 1.81		V _{CC} - 1.475	V _{CC} - 1.81		V _{CC} - 1.475	V _{CC} - 1.81		V _{CC} - 1.475	V
Input Current	I _{IN}	V _{IH} (MAX), V _{IL} (MAX)	-150		+50	-150		+50	-150		+50	μA
DIFFERENTIAL INPUTS (CLK ₋ , $\overline{CLK}_-$)												
Differential Input High Voltage	V _{IHD}	Figure 1	1.2		V _{CC}	1.2		V _{CC}	1.2		V _{CC}	V
Differential Input Low Voltage	V _{ILD}	Figure 1	GND		V _{CC} - 0.095	GND		V _{CC} - 0.095	GND		V _{CC} - 0.095	V
Differential Input Voltage	V _{ID}	V _{IHD} - V _{ILD}	0.095		V _{CC}	0.095		V _{CC}	0.095		V _{CC}	V
Input Current	I _{IH} , I _{IL}	CLK ₋ , or $\overline{CLK}_-$ = V _{IHD} or V _{ILD}	-60		+50	-60		+50	-60		+60	μA
OUTPUTS (Q ₋ , $\overline{Q}_-$)												
Output High Voltage	V _{OH}	Figure 1			1.6			1.6			1.6	V
Output Low Voltage	V _{OL}	Figure 1	0.9			0.9			0.9			V
Differential Output Voltage	V _{OD}	V _{OH} - V _{OL} , Figure 1	250	350	450	250	350	450	250	350	450	mV

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MAX9310

DC ELECTRICAL CHARACTERISTICS (continued)

($V_{CC} - GND = 2.375V$ to $2.625V$, outputs terminated with $100\Omega \pm 1\%$, unless otherwise noted. Typical values are at $V_{CC} - GND = 2.5V$, $V_{IHD} = V_{CC} - 1.0V$, $V_{ILD} = V_{CC} - 1.5V$, unless otherwise noted.) (Notes 1, 2, and 3)

PARAMETER	SYMBOL	CONDITIONS	-40°C			+25°C			+85°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Change in V _{OD} Between Complementary Output States	ΔV _{OD}				40			40			40	mV
Output Offset Voltage	V _{OS}		1.125	1.25	1.375	1.125	1.25	1.375	1.125	1.25	1.375	mV
Change in V _{OS} Between Complementary Output States	ΔV _{OCM}				25			25			25	mV
Output Short-Circuit Current	I _{OSC}	Q ₋ shorted to $\overline{Q_-}$			12			12			12	mA
		Q ₋ or $\overline{Q_-}$ shorted to GND			28			28			28	
POWER SUPPLY												
Power-Supply Current	I _{CC}	(Note 4)		42	75		45.5	75		48.5	75	mA

AC ELECTRICAL CHARACTERISTICS

($V_{CC} - GND = 2.375V$ to $2.625V$, outputs terminated with $100\Omega \pm 1\%$, $f_{IN} \leq 1.0GHz$, input transition time = 125ps (20% to 80%), $V_{IHD} - V_{ILD} = 0.15V$ to V_{CC} , unless otherwise noted. Typical values are at $V_{CC} - GND = 2.5V$, $V_{IHD} = V_{CC} - 1.0V$, $V_{ILD} = V_{CC} - 1.5V$, unless otherwise noted.) (Notes 1 and 5)

PARAMETER	SYMBOL	CONDITIONS	-40°C			+25°C			+85°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Propagation Delay CLK_- , $\overline{CLK_-}$ to Q_- , $\overline{Q_-}$	t_{PHL} , t_{PLH}	Figure 1	250	335	600	250	345	600	250	345	600	ps
Output-to-Output Skew	t_{SKOO}	(Note 6)		10	25		8	25		5	25	ps
Part-to-Part Skew	t_{SKPP}	(Note 7)			145			145			145	ps
Added Random Jitter	t_{RJ}	$f_{IN} = 1.0GHz$, clock pattern (Note 8)		0.4	1.0		0.4	1.0		0.4	1.0	ps (RMS)
Added Deterministic Jitter	t_{DJ}	$f_{IN} = 1.0Gbps$, $2^{23} - 1$ PRBS pattern (Note 8)		41	52		41	52		41	52	ps (P-P)

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AC ELECTRICAL CHARACTERISTICS (continued)

($V_{CC} - GND = 2.375V$ to $2.625V$, outputs terminated with $100\Omega \pm 1\%$, $f_{IN} \leq 1.0GHz$, input transition time = $125ps$ (20% to 80%), $V_{IHD} - V_{ILD} = 0.15V$ to V_{CC} , unless otherwise noted. Typical values are at $V_{CC} - GND = 2.5V$, $V_{IHD} = V_{CC} - 1.0V$, $V_{ILD} = V_{CC} - 1.5V$, unless otherwise noted.) (Notes 1 and 5)

PARAMETER	SYMBOL	CONDITIONS	-40°C			+25°C			+85°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Operating Frequency	f_{MAX}	$V_{OD} \geq 250mV$	1.0			1.0			1.0			GHz
Differential Output Rise/Fall Time	t_R/t_F	20% to 80%, Figure 1	140	205	300	140	205	300	140	205	300	ps

Note 1: Measurements are made with the device in thermal equilibrium.

Note 2: Current into a pin is defined as positive. Current out of a pin is defined as negative.

Note 3: DC parameters are production tested at +25°C. DC limits are guaranteed by design and characterized over the full operating temperature range.

Note 4: All pins are open except V_{CC} and GND, all outputs are loaded with 100Ω differentially.

Note 5: Guaranteed by design and characterization. Limits are set to ± 6 sigma.

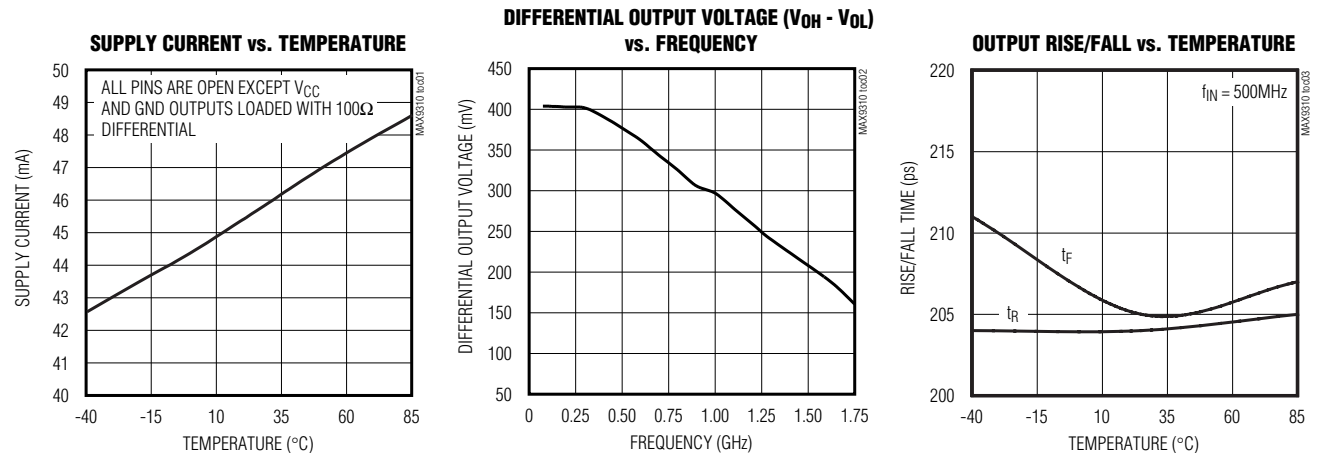
Note 6: Measured between outputs of the same part at the signal crossing points for a same-edge transition.

Note 7: Measured between outputs of different parts at the signal crossing points under identical conditions for a same-edge transition.

Note 8: Device jitter added to the input signal.

Typical Operating Characteristics

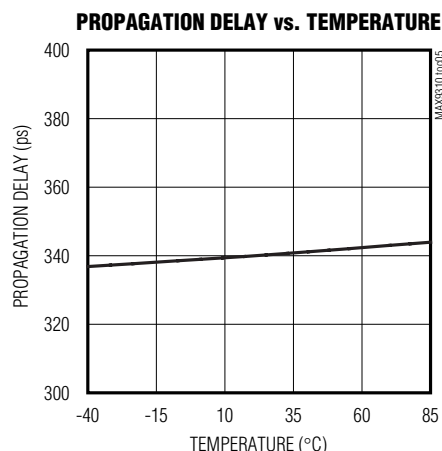
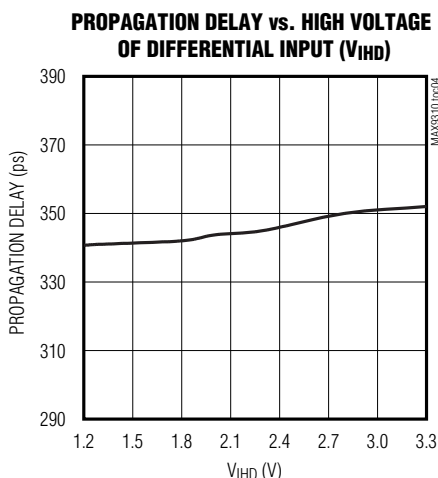
($V_{CC} - GND = 2.5V$, outputs terminated with $100\Omega \pm 1\%$, $f_{IN} = 1.0GHz$, input transition time = $125ps$ (20% to 80%), $V_{IHD} = V_{CC} - 1.0V$, $V_{ILD} = V_{CC} - 1.5V$, unless otherwise noted.)



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Typical Operating Characteristics (continued)

($V_{CC} - GND = 2.5V$, outputs terminated with $100\Omega \pm 1\%$, $f_{IN} = 1.0GHz$, input transition time = 125ps (20% to 80%), $V_{IHD} = V_{CC} - 1.0V$, $V_{ILD} = V_{CC} - 1.5V$, unless otherwise noted.)



Pin Description

PIN	NAME	FUNCTION
1	Q0	Noninverting Differential Output 0. Typically terminated with 100Ω to $\overline{Q0}$.
2	$\overline{Q0}$	Inverting Differential Output 0. Typically terminated with 100Ω to Q0.
3	Q1	Noninverting Differential Output 1. Typically terminated with 100Ω to $\overline{Q1}$.
4	$\overline{Q1}$	Inverting Differential Output 1. Typically terminated with 100Ω to Q1.
5	Q2	Noninverting Differential Output 2. Typically terminated with 100Ω to $\overline{Q2}$.
6	$\overline{Q2}$	Inverting Differential Output 2. Typically terminated with 100Ω to Q2.
7	Q3	Noninverting Differential Output 3. Typically terminated with 100Ω to $\overline{Q3}$.
8	$\overline{Q3}$	Inverting Differential Output 3. Typically terminated with 100Ω to Q3.
9	Q4	Noninverting Differential Output 4. Typically terminated with 100Ω to $\overline{Q4}$.
10	$\overline{Q4}$	Inverting Differential Output 4. Typically terminated with 100Ω to Q4.
11	GND	Ground
12	CLKSEL	Clock Select Input. Drive low to select the CLK0, $\overline{CLK0}$ input. Drive high to select the CLK1, $\overline{CLK1}$ input. Internal $60k\Omega$ pulldown to GND.
13	CLK0	Noninverting Differential Clock Input 0. Internal $75k\Omega$ pulldown to GND.
14	$\overline{CLK0}$	Inverting Differential Clock Input 0. Internal $75k\Omega$ pullup to V_{CC} and $75k\Omega$ pulldown to GND.
15	I.C.	Internally Connect. Do not connect externally.
16	CLK1	Noninverting Differential Input 1. Internal $75k\Omega$ pulldown to GND.
17	$\overline{CLK1}$	Inverting Differential Input 1. Internal $75k\Omega$ pullup to V_{CC} and $75k\Omega$ pulldown to GND.

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Pin Description (continued)

PIN	NAME	FUNCTION
18, 20	VCC	Positive Supply Voltage. Bypass each VCC to GND with 0.1µF and 0.01µF ceramic capacitors. Place the capacitors as close to the device as possible with the smaller value capacitor closest to the device.
19	$\overline{\text{EN}}$	Output Enable Input. Outputs are synchronously enabled on the falling edge of the selected clock input when $\overline{\text{EN}}$ is low. Outputs are synchronously driven to a differential low state on the falling edge of the selected clock input when $\overline{\text{EN}}$ is high. Internal 60kΩ pulldown to GND (Figure 2).

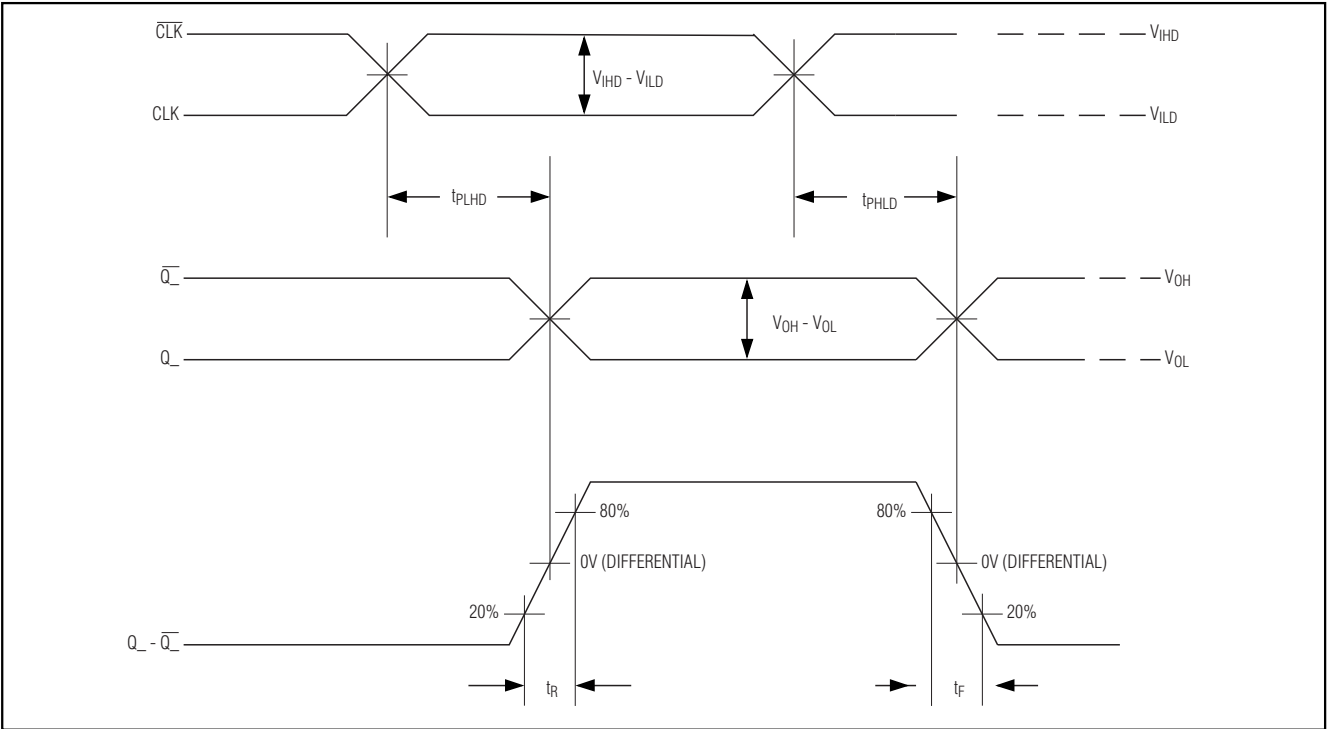


Figure 1. MAX9310 Timing Diagram

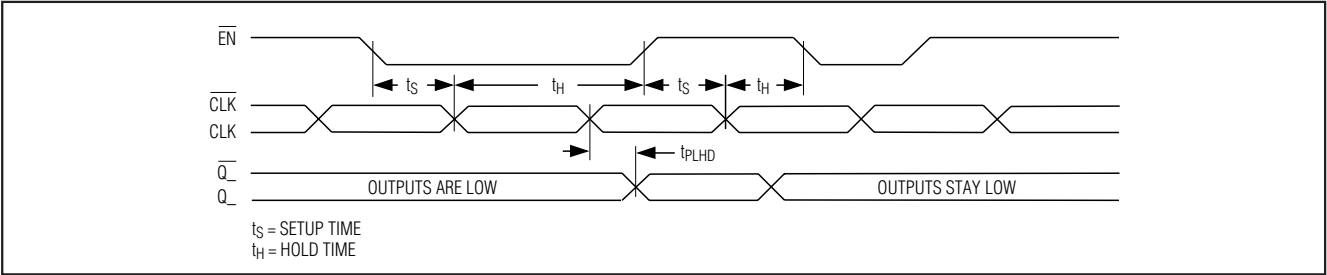


Figure 2. MAX9310 $\overline{\text{EN}}$ Timing Diagram

1:5 Clock Driver with Selectable LVPECL Inputs and LVDS Outputs

Detailed Description

The MAX9310 is a low-skew 1:5 differential driver with two selectable LVPECL inputs and LVDS outputs, designed for clock distribution applications. The selected clock accepts a differential input signal and reproduces it on five separate differential LVDS outputs. The inputs are biased with internal resistors such that the output is differential low when inputs are open. The output drivers are guaranteed to operate at frequencies up to 1.0GHz with LVDS output levels conforming to the EIA/TIA-644 standard.

The MAX9310 is designed for 2.375V to 2.625V operation in systems with a nominal 2.5V supply.

Differential LVPECL Input

The MAX9310 has two input differential pairs that accept differential LVPECL/HSTL inputs. Each differential input pair has to be independently terminated. A select pin (CLKSEL) is used to activate the desired input. The maximum magnitude of the differential signal applied to the input is V_{CC} . Specifications for the high and low voltages of a differential input (V_{IHD} and V_{ILD}) and the differential input voltage ($V_{IHD} - V_{ILD}$) apply simultaneously.

Synchronous Enable

The MAX9310 is synchronously enabled and disabled with outputs in a differential low state to eliminate shortened clock pulses. $\overline{EN}$ is connected to the input of an edge-triggered D flip-flop. After power-up, drive $\overline{EN}$ low and toggle the selected clock input to enable the outputs. The outputs are enabled on the falling edge of the selected clock input after $\overline{EN}$ goes low. The outputs are set to a differential low state on the falling edge of the selected clock input after $\overline{EN}$ goes high (Figure 2).

Input Bias Resistors

Internal biasing resistors ensure a (differential) output low condition in the event that the inputs are not connected. The inverting input ($\overline{CLK_}$) is biased with a 75k Ω pulldown to GND and a 75k Ω pullup to V_{CC} . The noninverting input ($CLK_$) is biased with a 75k Ω pulldown to GND.

Differential LVDS Output

The LVDS outputs must be terminated with 100 Ω across $Q_$ and $\overline{Q_}$, as shown in the *Typical Application Circuit*. The outputs are short-circuit protected.

Applications Information

Supply Bypassing

Bypass each V_{CC} to GND with high-frequency surface-mount ceramic 0.1 μ F and 0.01 μ F capacitors in parallel as close to the device as possible, with the 0.01 μ F capacitor closest to the device. Use multiple parallel vias to minimize parasitic inductance and reduce power-supply bounce with high-current transients.

Controlled-Impedance Traces

Input and output trace characteristics affect the performance of the MAX9310. Connect high-frequency input and output signals to 50 Ω characteristic impedance traces. Minimize the number of vias to prevent impedance discontinuities. Reduce reflections by maintaining the 50 Ω characteristic impedance through cables and connectors. Reduce skew within a differential pair by matching the electrical length of the traces.

Output Termination

Terminate the outputs with 100 Ω across $Q_$ and $\overline{Q_}$, as shown in the *Typical Application Circuit*.

Chip Information

TRANSISTOR COUNT: 716

PROCESS: Bipolar

Functional Diagram



MAX9310

-SSOP,NO PADS.EPS

COMMON DIMENSIONS

	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	—	1.10	—	.043
A ₁	0.05	0.15	.002	.006
A ₂	0.85	0.95	.033	.037
b	0.19	0.30	.007	.012
b ₁	0.19	0.25	.007	.010
c	0.090	0.20	.0035	.008
c ₁	0.090	0.135	.0035	.0053
D	SEE VARIATIONS		SEE VARIATIONS	
E	4.30	4.50	.169	.177
e	0.65 BSC		.026 BSC	
H	6.25	6.50	.246	.256
L	0.50	0.70	.020	.028
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°

JEDEC		VARIATIONS			
MO-153	N	MILLIMETERS		INCHES	
		MIN.	MAX.	MIN.	MAX.
AB-1	14 D	4.90	5.10	.193	.201
AB	16 D	4.90	5.10	.193	.201
AC	20 D	6.40	6.60	.252	.260
AD	24 D	7.70	7.90	.303	.311
AE	28 D	9.60	9.80	.378	.386

NOTES:

- DIMENSIONS D AND E DO NOT INCLUDE FLASH
- MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm PER SIDE
- CONTROLLING DIMENSION: MILLIMETER
- MEETS JEDEC OUTLINE MO-153. SEE JEDEC VARIATIONS TABLE.
- "N" REFERS TO NUMBER OF LEADS
- THE LEAD TIPS MUST LIE WITHIN A SPECIFIED ZONE. THIS TOLERANCE ZONE IS DEFINED BY TWO PARALLEL PLANES. ONE PLANE IS THE SEATING PLANE, DATUM [-C-]; THE OTHER PLANE IS AT THE SPECIFIED DISTANCE FROM [-C-] IN THE DIRECTION INDICATED.

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