MC68HC05B6/D
Rev. 3

MC68HC05B6

HC05

MC68HC05B4
MC68HC705B5
MC68HC05B6
MC68HC05B8
MC68HC05B16
MC68HC705B16
MC68HC05B32
MC68HC705B32

TECHNICAL DATA

TECHNICAL
DATA

MOTOROLA

MC68HC05B6

High-density Complementary Metal Oxide Semiconductor (HCMOS) Microcomputer Unit

CAUTION

This document includes descriptions of the various self-check and bootstrap mechanisms that are currently implemented as firmware in the non-user ROM areas of the MC68HC05B6 and related devices.

As these firmware routines are intended primarily to help Motorola's engineers test the devices, they may be changed or removed at any time.

For this reason, Motorola recommends that the self-check and bootstrap routines are not called from from the user software. Customers who do call these routines from the user software do so at their own risk.

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1
INTRODUCTION

The MC68HC05B6 microcomputer (MCU) is a member of Motorola's MC68HC05 family of low-cost single chip microcomputers. This 8-bit MCU contains an on-chip oscillator, CPU, RAM, ROM, EEPROM, A/D converter, pulse length modulated outputs, I/O, serial communications interface, programmable timer system and watchdog. The fully static design allows operation at frequencies down to dc to further reduce the already low power consumption to a few micro-amps.

This data sheet is structured such that devices similar to the MC68HC05B6 are described in a set of appendices (see Table 1-1).

Table 1-1 Data sheet appendices

Device	Appendix	Differences from MC68HC05B6
MC68HC05B4	A	4K bytes ROM; no EEPROM
MC68HC05B8	B	7.25K bytes ROM
MC68HC705B5	C	6K bytes EPROM; self-check replaced by bootstrap firmware; no EEPROM
MC68HC05B16	D	16K bytes ROM; increased RAM and self-check ROM
MC68HC705B16	E	16K bytes EPROM; increased RAM; self-check replaced by bootstrap firmware; modified power-on reset routine
MC68HC05B32	F	32K bytes ROM; no page zero ROM; increased RAM
MC68HC705B32	G	32K bytes EPROM; no page zero ROM; increased RAM; self-check mode replaced by bootstrap firmware

1

1.1 Features

Hardware features

- Fully static design featuring the industry standard M68HC05 family CPU core
- On chip crystal oscillator with divide by 2 or a software selectable divide by 32 option (SLOW mode)
- 2.1 MHz internal operating frequency at 5V; 1.0 MHz at 3V
- 176 bytes of RAM
- 5936 bytes of user ROM plus 14 bytes of user vectors
- 256 bytes of byte erasable EEPROM with internal charge pump and security bit
- Write/erase protect bit for 224 of the 256 bytes EEPROM
- Self test/bootstrap mode
- Power saving STOP, WAIT and SLOW modes
- Three 8-bit parallel I/O ports and one 8-bit input-only port
- Software option available to output the internal E-clock to port pin PC2
- 16-bit timer with 2 input captures and 2 output compares
- Computer operating properly (COP) watchdog timer
- Serial communications interface system (SCI) with independent transmitter/receiver baud rate selection; receiver wake-up function for use in multi-receiver systems
- 8 channel A/D converter
- 2 pulse length modulation systems which can be used as D/A converters
- One interrupt request input plus 4 on-board hardware interrupt sources
- Available in 52-pin plastic leaded chip carrier (PLCC), 64-pin quad flat pack (QFP) and 56-pin shrink dual in line (SDIP) packages
- Complete development system support available using the MMDS05 development station with the M68HC05BEM emulation module or the M68HC05BEVS evaluation system

1.2 Mask options for the MC68HC05B6

The MC68HC05B6 has three mask options that are programmed during manufacture and must be specified on the order form.

- Power-on-reset delay (t_{PORL}) = 16 or 4064 cycles

- Automatic watchdog enable/disable following a power-on or external reset
- Watchdog enable/disable during WAIT mode

Warning: It is recommended that an external clock is always used if t_{PORL} is set to 16 cycles. This will prevent any problems arising with oscillator stability when the device is put into STOP mode.

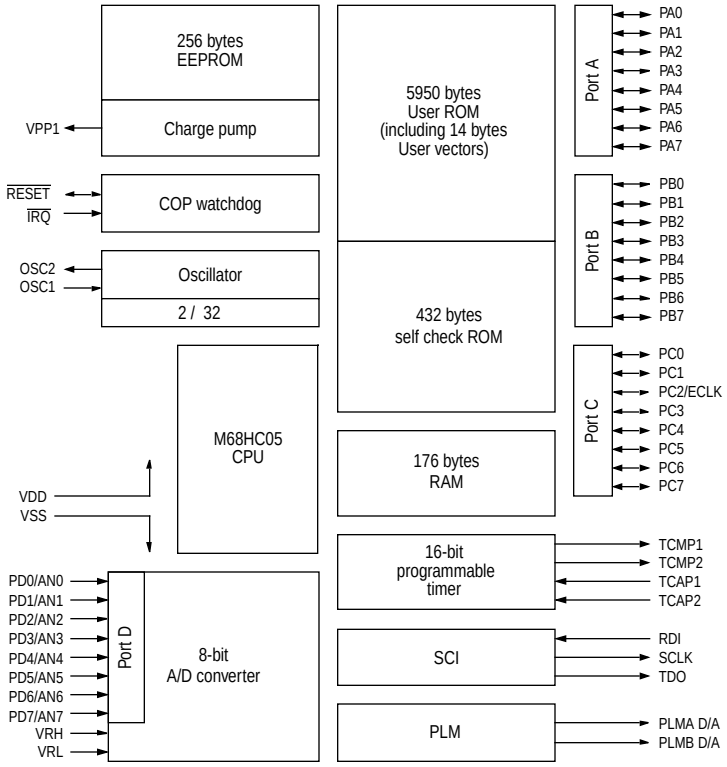

Figure 1-1 MC68HC05B6 block diagram

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2
MODES OF OPERATION AND PIN DESCRIPTIONS

2.1 Modes of operation

The MC68HC05B6 MCU has two modes of operation, namely single chip and self check modes. Table 2-1 shows the conditions required to enter each mode on the rising edge of $\overline{\text{RESET}}$.

Table 2-1 Mode of operation selection

$\overline{\text{IRQ}}$ pin	TCAP1 pin	PD3	PD4	Mode
V_{SS} to V_{DD}	V_{SS} to V_{DD}	X	X	Single chip
$2V_{DD}$	V_{DD}	0	X	Self-check
$2V_{DD}$	V_{DD}	1	0	Serial RAM loader
$2V_{DD}$	V_{DD}	1	1	Jump to any address

2.1.1 Single chip mode

This is the normal operating mode of the MC68HC05B6. In this mode the device functions as a self-contained microcomputer (MCU) with all on-board peripherals, including the three 8-bit I/O ports and the 8-bit input-only port, available to the user. All address and data activity occurs within the MCU.

2.1.2 Self-check mode

The self-check function available on the MC68HC05B6 provides an internal capability to determine if the device is functional. Self-check is performed using the circuit shown in Figure 2-1. Port C pins PC0–PC3 are monitored for the self-check results (light emitting diodes are shown but other devices could be used), and are interpreted as described in Table 2-2. The self-check mode

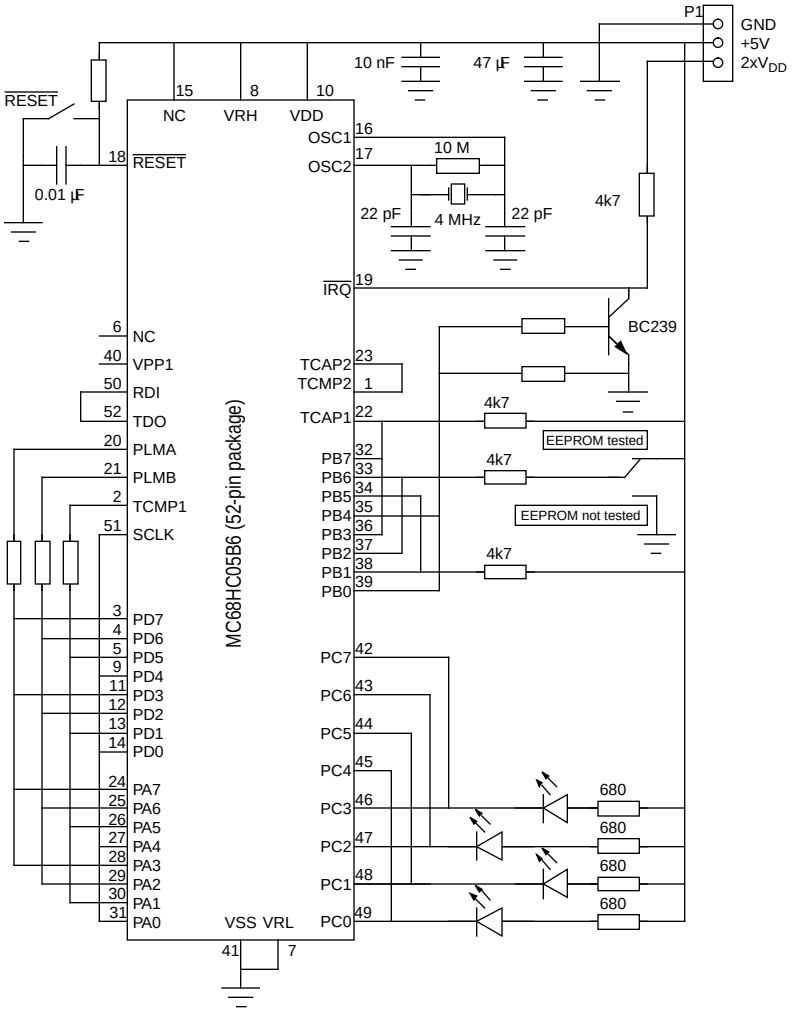
is entered by applying 2 x V_{DD} dc (via a 4.7k resistor) to the $\overline{IRQ}$ pin and 5V dc input (via a 4.7k resistor) to the TCAP1 pin and then depressing the reset switch to execute a reset. After reset, the following tests are performed automatically and once completed they continually repeat. A good device will exhibit flashing LEDs; a bad device will be indicated by the LEDs holding at one value.

I/0	—	Functionally exercises ports A, B, C and D
RAM	—	Counter test for each RAM byte
ROM	—	Exclusive OR with odd ones parity result
Timer	—	Tracks counter registers and checks ICF1, ICF2, OCF1, OCF2 and TOF flags
SCI	—	Transmission test; check for RDRF, TDRE, TC and FE flags
A/D	—	Check A/D functionality on internal channels: VRL, VRH and (VRL + VRH)/2
EEPROM	—	This test is optional; it executes a write/erase test of the 256 bytes EEPROM (available only for the MC68HC05B6 version), and then deactivates the security bit.
PLM	—	Checks the PLM basic functionality
Interrupts	—	Tests external timer and SCI interrupts
Watchdog	—	Tests the watchdog

Table 2-2 MC68HC05B6 self-check results

PC3	PC2	PC1	PC0	Remarks
1	0	0	1	Bad port
0	1	1	0	Bad port
1	0	1	0	Bad RAM
1	0	1	1	Bad ROM
1	1	0	0	Bad Timer
1	1	0	1	Bad SCI
1	1	1	0	Bad A/D
0	0	0	0	Bad EEPROM (or other if B4)
0	0	0	1	Bad PLM
0	0	1	0	Bad interrupts
0	0	1	1	Bad watchdog
Flashing				Good device
All others				Bad device, bad port etc.

'0' indicates LED on; '1' indicates LED off



Note: For the MC68HC05B4, switches on PB5 and PB6 have no effect
All resistors are 10 k , unless otherwise stated.

Figure 2-1 MC68HC05B6 self-check schematic diagram

2.2 Serial RAM loader

The ‘load program in RAM and execute’ mode is entered if the following conditions are satisfied when the reset pin is released to V_{DD}. The format used is identical to the format used for the MC68HC805C4. The SEC bit in the options register must be inactive, i.e. set to ‘1’.

- $\overline{IRQ}$ at 2xV_{DD}
- TCAP1 at V_{DD}
- PD3 at V_{DD} for at least 30 machine cycles after reset
- PD4 at V_{SS} for at least 30 machine cycles after reset

In the ‘load program in RAM and execute’ routine, user programs are loaded into MCU RAM via the SCI port and then executed. Data is loaded sequentially, starting at RAM location $0050, until the last byte is loaded. Program control is then transferred to the RAM program starting at location $0051. The first byte loaded is the count of the total number of bytes in the program plus the count byte. The program starts at the second byte in RAM. During the firmware initialization stage, the SCI is configured for the NRZ data format (idle line, start bit, eight data bits and stop bit). The baud rate is 9600 with a 4 MHz crystal. A program to convert ASCII S-records to the format required by the RAM loader is available from Motorola.

If immediate execution is not desired after loading the RAM program, it is possible to hold off execution. This is accomplished by setting the byte count to a value that is greater than the overall length of the loaded data. When the last byte is loaded, the firmware will halt operation expecting additional data to arrive. At this point, the reset switch is placed in the reset position which will reset the MCU, but keep the RAM program intact. All routines can now be entered from this state, including the one which will execute the program in RAM (see Section 2.3).

To load a program in the EEPROM, the ‘load program in RAM and execute’ function is also used. In this instance the process involves two distinct steps. Firstly, the RAM is loaded with a program which will control the loading of the EEPROM, and when the RAM contents are executed, the MCU is instructed to load the EEPROM.

The erased state of the EEPROM is $FF.

Figure 2-2 shows the schematic diagram of the circuit required for the serial RAM loader.

2.3 ‘Jump to any address’

The ‘jump to any address’ mode is entered when the reset pin is released to V_{DD}, if the following conditions are satisfied:

- $\overline{IRQ}$ at 2xV_{DD}
- TCAP1 at V_{DD}
- PD3 at V_{DD} for at least 30 machine cycles after reset
- PD4 at V_{DD} for at least 30 machine cycles after reset

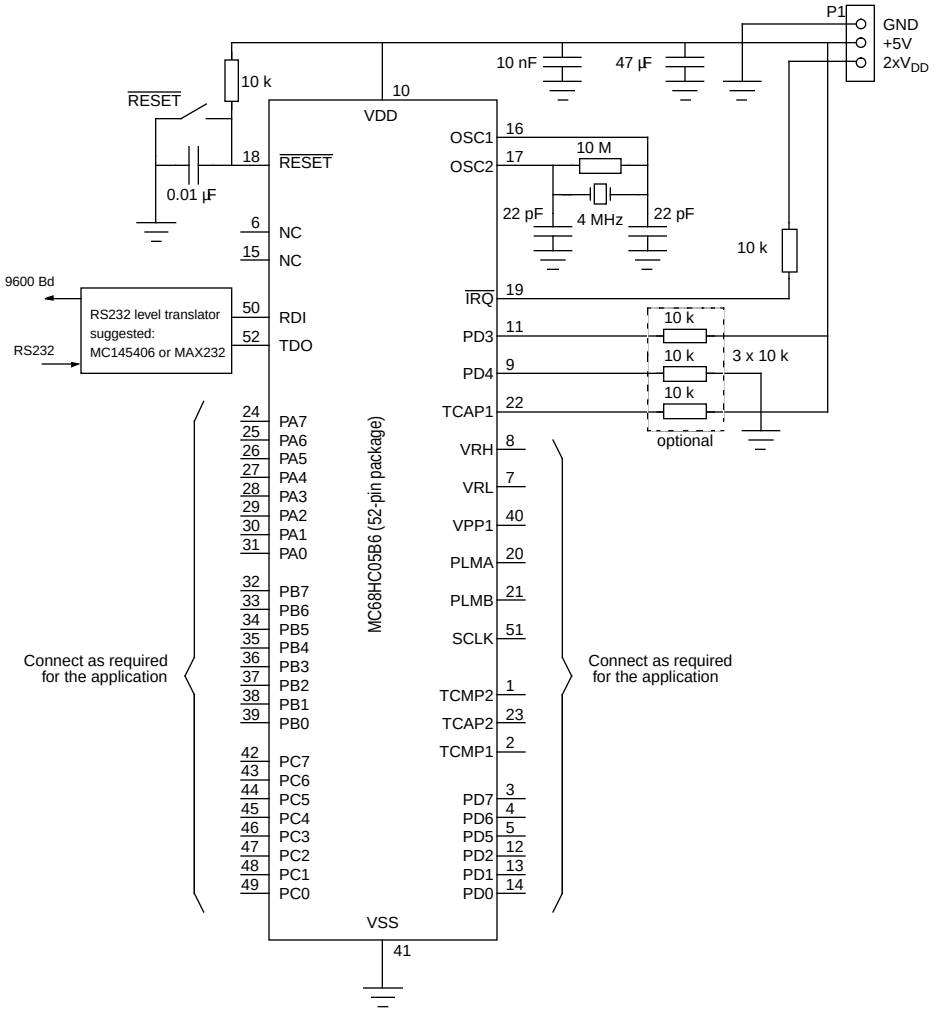
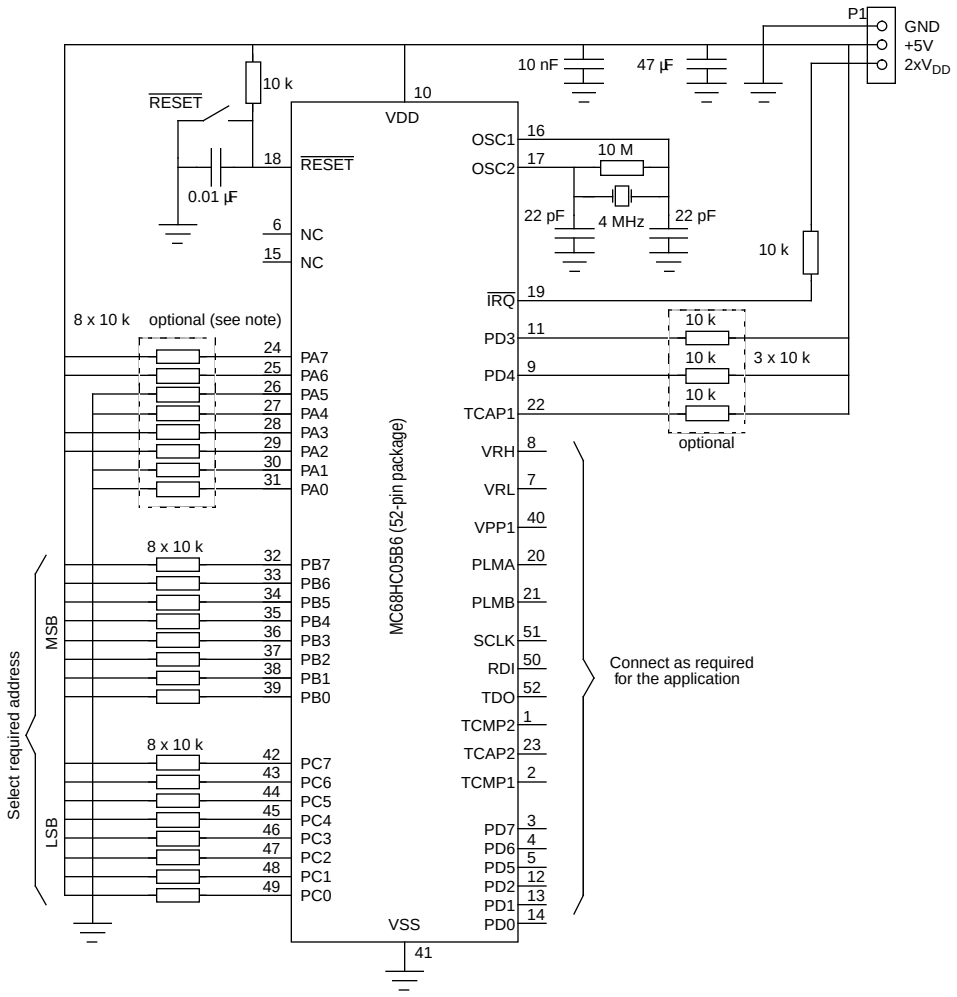


Figure 2-2 MC68HC05B6 ‘load program in RAM and execute’ schematic diagram

This function allows execution of programs previously loaded in RAM or EEPROM using the methods outlined in Section 2.2.

To execute the ‘jump to any address’ function, data input at port A has to be $CC and data input at port B and port C should represent the MSB and LSB respectively, of the address to jump to for execution of the user program. A schematic diagram of the circuit required is shown in Figure 2-3.



Note: These eight resistors are optional; direct connection is possible if pins PA0-PA7, PB0-PB7 and PC0-PC7 are kept in input mode during application.

Figure 2-3 MC68HC05B6 ‘jump to any address’ schematic diagram

2.4 Low power modes

The STOP and WAIT instructions have different effects on the programmable timer, the serial communications interface, the watchdog system, the EEPROM and the A/D converter. These different effects are described in the following sections.

2.4.1 STOP

The STOP instruction places the MCU in its lowest power consumption mode. In STOP mode, the internal oscillator is turned off, halting all internal processing including timer, serial communications interface and the A/D converter (see flowchart in Figure 2-4). The only way for the MCU to wake-up from the STOP mode is by receipt of an external interrupt or by the detection of a reset (logic low on $\overline{\text{RESET}}$ pin or a power-on reset).

During STOP mode, the I-bit in the CCR is cleared to enable external interrupts (see Section 10.1.5). The SM bit is cleared to allow nominal speed operation for the 4064 cycles count while exiting STOP mode (see Section 2.4.3).

All other registers and memory remain unaltered and all input/output lines remain unchanged. This continues until an external interrupt ($\overline{\text{IRQ}}$) or reset is sensed, at which time the internal oscillator is turned on. The external interrupt or reset causes the program counter to vector to the corresponding locations ($1FFA, B and $1FFE, F respectively).

When leaving STOP mode, a t_{PORL} internal cycles delay is provided to give the oscillator time to stabilise before releasing CPU operation. This delay is selectable via a mask option to be either 16 or 4064 cycles. The CPU will resume operation by servicing the interrupt that wakes it up, or by fetching the reset vector, if reset wakes it up.

Warning: If t_{PORL} is selected to be 16 cycles, it is recommended that an external clock signal is used to avoid problems with oscillator stability while the device is in STOP mode.

Note: The stacking corresponding to an eventual interrupt to go out of STOP mode will only be executed when going out of STOP mode.

The following list summarizes the effect of STOP mode on the individual modules of the MC68HC05B6.

- The watchdog timer is reset; refer to Section 9.1.4.1
- The EEPROM acts as read-only memory (ROM); refer to Section 3.6
- All SCI activity stopped; refer to Section 6.13
- The timer stops counting; refer to Section 5.6
- The PLM outputs remain at current level; refer to Section 7.2
- The A/D converter is disabled; refer to Section 8.3
- The I-bit in the CCR is cleared

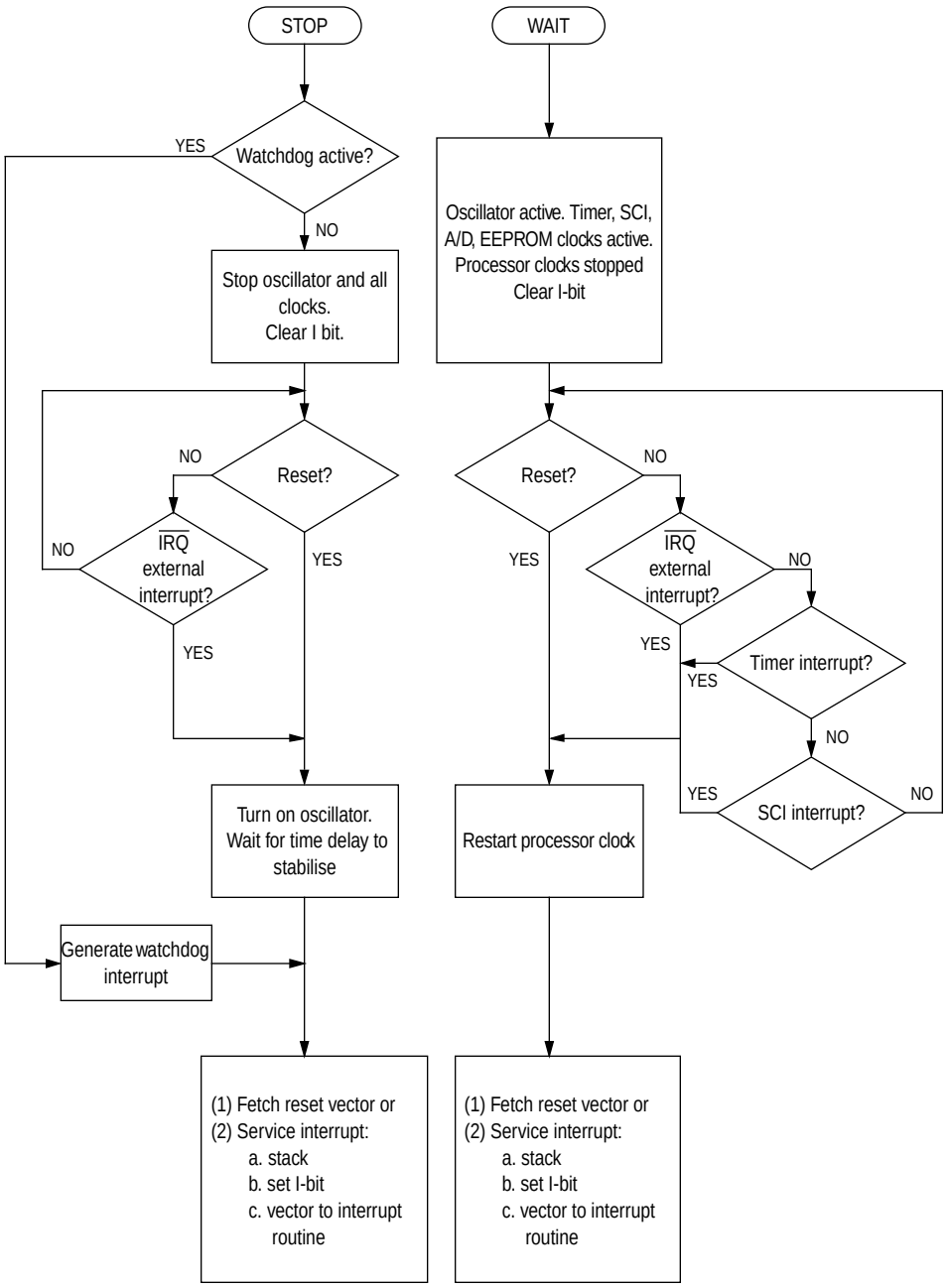


Figure 2-4 STOP and WAIT flowcharts

2.4.2 WAIT

The WAIT instruction places the MCU in a low power consumption mode, but WAIT mode consumes more power than STOP mode. All CPU action is suspended and the watchdog is disabled, but the timer, A/D and SCI systems remain active and operate as normal (see flowchart in Figure 2-4). All other memory and registers remain unaltered and all parallel input/output lines remain unchanged. The programming or erase mechanism of the EEPROM is also unaffected, as well as the charge pump high voltage generator.

During WAIT mode the I-bit in the CCR is cleared to enable all interrupts. The INTE bit in the miscellaneous register (Section 2.5) is not affected by WAIT mode. When any interrupt or reset is sensed, the program counter vectors to the locations containing the start address of the interrupt or reset service routine.

Any $\overline{\text{IRQ}}$, timer (overflow, input capture or output compare) or SCI interrupt (in addition to a logic low on the $\overline{\text{RESET}}$ pin) causes the processor to exit WAIT mode.

If a non-reset exit from WAIT mode is performed (i.e. timer overflow interrupt exit), the state of the remaining systems will be unchanged.

If a reset exit from WAIT mode is performed the entire system reverts to the disabled reset state.

Note: The stacking corresponding to an eventual interrupt to leave WAIT mode will only be executed when leaving WAIT mode.

The following list summarizes the effect of WAIT mode on the modules of the MC68HC05B6.

- The watchdog timer functions according to the mask option selected; refer to Section 9.1.4.2
- The EEPROM is not affected; refer to Section 3.7
- The SCI is not affected; refer to Section 6.14
- The timer is not affected; refer to Section 5.7
- The PLM is not affected; refer to Section 7.4
- The A/D converter is not affected; refer to Section 8.4
- The I-bit in the CCR is cleared

2.4.2.1 Power consumption during WAIT mode

Power consumption during WAIT mode depends on how many systems are active. The power consumption will be highest when all the systems (A/D, timer, EEPROM and SCI) are active, and lowest when the EEPROM erase and programming mechanism, SCI and A/D are disabled. The timer cannot be disabled in WAIT mode. It is important that before entering WAIT mode, the programmer sets the relevant control bits for the individual modules to reflect the desired functionality during WAIT mode.

Power consumption may be further reduced by the use of SLOW mode.

2.4.3 SLOW mode

The SLOW mode function is controlled by the SM bit in the miscellaneous register at location $000C. It allows the user to insert, under software control, an extra divide-by-16 between the oscillator and the internal clock driver (see Figure 2-5). This feature permits a slow down of all the internal operations and thus reduces power consumption. The SLOW mode function should not be enabled while using the A/D converter or while erasing/programming the EEPROM unless the internal A/D RC oscillator is turned on.

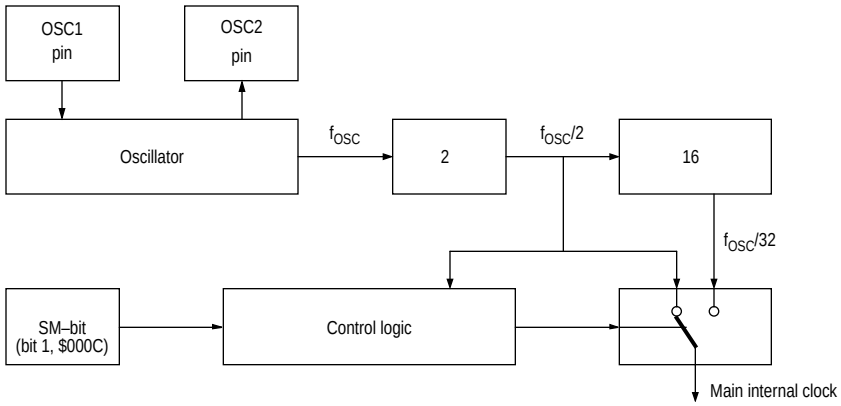


Figure 2-5 Slow mode divider block diagram

2.4.3.1 Miscellaneous register

	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
Miscellaneous	$000C	POR	INTP	INTN	INTE	SFA	SFB	SM	WDOG	?001 000?

SM — Slow mode

1 (set) – The system runs at a bus speed 16 times lower than normal (f_{OSC}/32). SLOW mode affects all sections of the device, including SCI, A/D and timer.

0 (clear) – The system runs at normal bus speed (f_{OSC}/2).

The SM bit is cleared by external or power-on reset. The SM bit is automatically cleared when entering STOP mode.

Note: The bits shown shaded in the above representation are explained individually in the relevant sections of this manual. The complete register plus an explanation of each bit can be found in Section 3.8.

2.5 Pin descriptions

2.5.1 VDD and VSS

Power is supplied to the microcontroller using these two pins. VDD is the positive supply and VSS is ground.

It is in the nature of CMOS designs that very fast signal transitions occur on the MCU pins. These short rise and fall times place very high short-duration current demands on the power supply. To prevent noise problems, special care must be taken to provide good power supply by-passing at the MCU. By-pass capacitors should have good high-frequency characteristics and be as close to the MCU as possible. Bypassing requirements vary, depending on how heavily the MCU pins are loaded.

2.5.2 $\overline{\text{IRQ}}$

This is an input-only pin for external interrupt sources. Interrupt triggering is selected using the INTP and INTN bits in the miscellaneous register, to be one of four options detailed in Table 9-3. In addition, the external interrupt facility ($\overline{\text{IRQ}}$) can be disabled using the INTE bit in the miscellaneous register (see Section 3.8). It is only possible to change the interrupt option bits in the miscellaneous register while the I-bit is set. Selecting a different interrupt option will automatically clear any pending interrupts. Further details of the external interrupt procedure can be found in Section 9.2.3.1.

The $\overline{\text{IRQ}}$ pin contains an internal Schmitt trigger as part of its input to improve noise immunity.

2.5.3 $\overline{\text{RESET}}$

This active low I/O pin is used to reset the MCU. Applying a logic zero to this pin forces the device to a known start-up state. An external RC-circuit can be connected to this pin to generate a power-on-reset (POR) if required. In this case, the time constant must be great enough (at least 100ms) to allow the oscillator circuit to stabilise. This input has an internal Schmitt trigger to improve noise immunity. When a reset condition occurs internally, i.e. from the COP watchdog, the $\overline{\text{RESET}}$ pin provides an active-low open drain output signal that may be used to reset external hardware.

2.5.4 TCAP1

The TCAP1 input controls the input capture 1 function of the on-chip programmable timer system.

2.5.5 TCAP2

The TCAP2 input controls the input capture 2 function of the on-chip programmable timer system.

2.5.6 TCMP1

The TCMP1 pin is the output of the output compare 1 function of the timer system.

2.5.7 TCMP2

The TCMP2 pin is the output of the output compare 2 function of the timer system.

2.5.8 OSC1, OSC2

These pins provide control input for an on-chip oscillator circuit. A crystal, ceramic resonator or external clock signal connected to these pins supplies the oscillator clock. The oscillator frequency (f_{OSC}) is divided by two to give the internal bus frequency (f_{OP}). There is also a software option which introduces an additional divide by 16 into the oscillator clock, giving an internal bus frequency of $f_{OSC}/32$.

2.5.8.1 Crystal

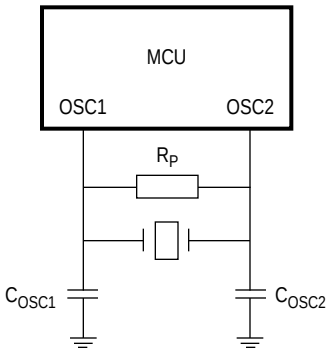
The circuit shown in Figure 2-6(a) is recommended when using either a crystal or a ceramic resonator. Figure 2-6(d) lists the recommended capacitance and feedback resistance values. The internal oscillator is designed to interface with an AT-cut parallel-resonant quartz crystal resonator in the frequency range specified for f_{OSC} (see Section 11.5). Use of an external CMOS oscillator is recommended when crystals outside the specified ranges are to be used. The crystal and associated components should be mounted as close as possible to the input pins to minimise output distortion and start-up stabilisation time. The manufacturer of the particular crystal being considered should be consulted for specific information.

2.5.8.2 Ceramic resonator

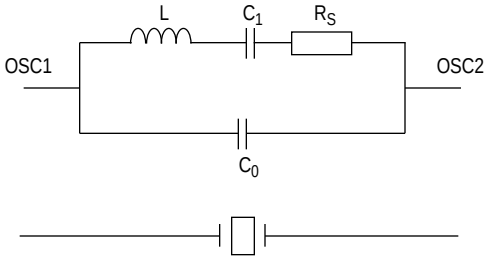
A ceramic resonator may be used instead of a crystal in cost sensitive applications. The circuit shown in Figure 2-6(a) is recommended when using either a crystal or a ceramic resonator. Figure 2-6(d) lists the recommended capacitance and feedback resistance values. The manufacturer of the particular ceramic resonator being considered should be consulted for specific information.

2.5.8.3 External clock

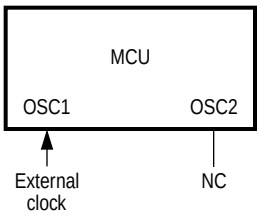
An external clock should be applied to the OSC1 input, with the OSC2 pin left unconnected, as shown in Figure 2-6(c). The t_{OXOV} or t_{ILCH} specifications (see Section 11.5) do not apply when using an external clock input. The equivalent specification of the external clock source should be used in lieu of t_{OXOV} or t_{ILCH}.



(a) Crystal/ceramic resonator oscillator connections



(b) Crystal equivalent circuit



(c) External clock source connections

Crystal

	2MHz	4MHz	Unit
R_S(max)	400	75	
C_0	5	7	pF
C_1	8	12	nF
C_{OSC1}	15 – 40	15 – 30	pF
C_{OSC2}	15 – 30	15 – 25	pF
R_P	10	10	M
Q	30 000	40 000	—

Ceramic resonator

	2 – 4MHz	Unit
R_S(typ)	10	
C_0	40	pF
C_1	4.3	pF
C_{OSC1}	30	pF
C_{OSC2}	30	pF
R_P	1 – 10	M
Q	1250	—

(d) Typical crystal and ceramic resonator parameters

Figure 2-6 Oscillator connections

2.5.9 RDI (Receive data in)

The RDI pin is the input pin of the SCI receiver.

2.5.10 TDO (Transmit data out)

The TDO pin is the output pin of the SCI transmitter.

2.5.11 SCLK

The SCLK pin is the clock output pin of the SCI transmitter.

2.5.12 PLMA

The PLMA pin is the output of pulse length modulation converter A.

2.5.13 PLMB

The PLMB pin is the output of pulse length modulation converter B.

2.5.14 VPP1

The VPP1 pin is the output of the charge pump for the EEPROM1 array.

2.5.15 VRH

The VRH pin is the positive reference voltage for the A/D converter.

2.5.16 VRL

The VRL pin is the negative reference voltage for the A/D converter.

2.5.17 PA0 – PA7/PB0 – PB7/PC0 – PC7

These 24 I/O lines comprise ports A, B and C. The state of any pin is software programmable, and all the pins are configured as inputs during power-on or reset.

Under software control the PC2 pin can output the internal E-clock (see Section 4.2).

2.5.18 PD0/AN0–PD7/AN7

This 8-bit input only port (D) shares its pins with the A/D converter. When enabled, the A/D converter uses pins PD0/AN0 – PD7/AN7 as its analog inputs. On reset, the A/D converter is disabled which forces the port D pins to be input only port pins (see Section 8.5).

3
MEMORY AND REGISTERS

The MC68HC05B6 MCU is capable of addressing 8192 bytes of memory and registers with its program counter. The memory map includes 5950 bytes of User ROM (including User vectors), 432 bytes of self check ROM, 176 bytes of RAM and 256 bytes of EEPROM.

3.1 Registers

All the I/O, control and status registers of the MC68HC05B6 are contained within the first 32-byte block of the memory map, as shown in Figure 3-1. The miscellaneous register is shown in Section 3.8 as this register contains bits which are relevant to several modules.

3.2 RAM

The user RAM comprises 176 bytes of memory, from $0050 to $00FF. This is shared with a 64 byte stack area. The stack begins at $00FF and may extend down to $00C0.

Note: Using the stack area for data storage or temporary work locations requires care to prevent the data from being overwritten due to stacking from an interrupt or subroutine call.

3.3 ROM

The User ROM consists of 5950 bytes of ROM mapped as follows:

- 48 bytes of page zero ROM from $0020 to $004F
- 5888 bytes of User ROM from $0800 to $1EFF
- 14 bytes of User vectors from $1FF2 to $1FFF

3.4 Self-check ROM

There are two areas of self-check ROM (ROMI and ROMII) located from $0200 to $02BF (192 bytes) and $1F00 to $1FEF (240 bytes) respectively.

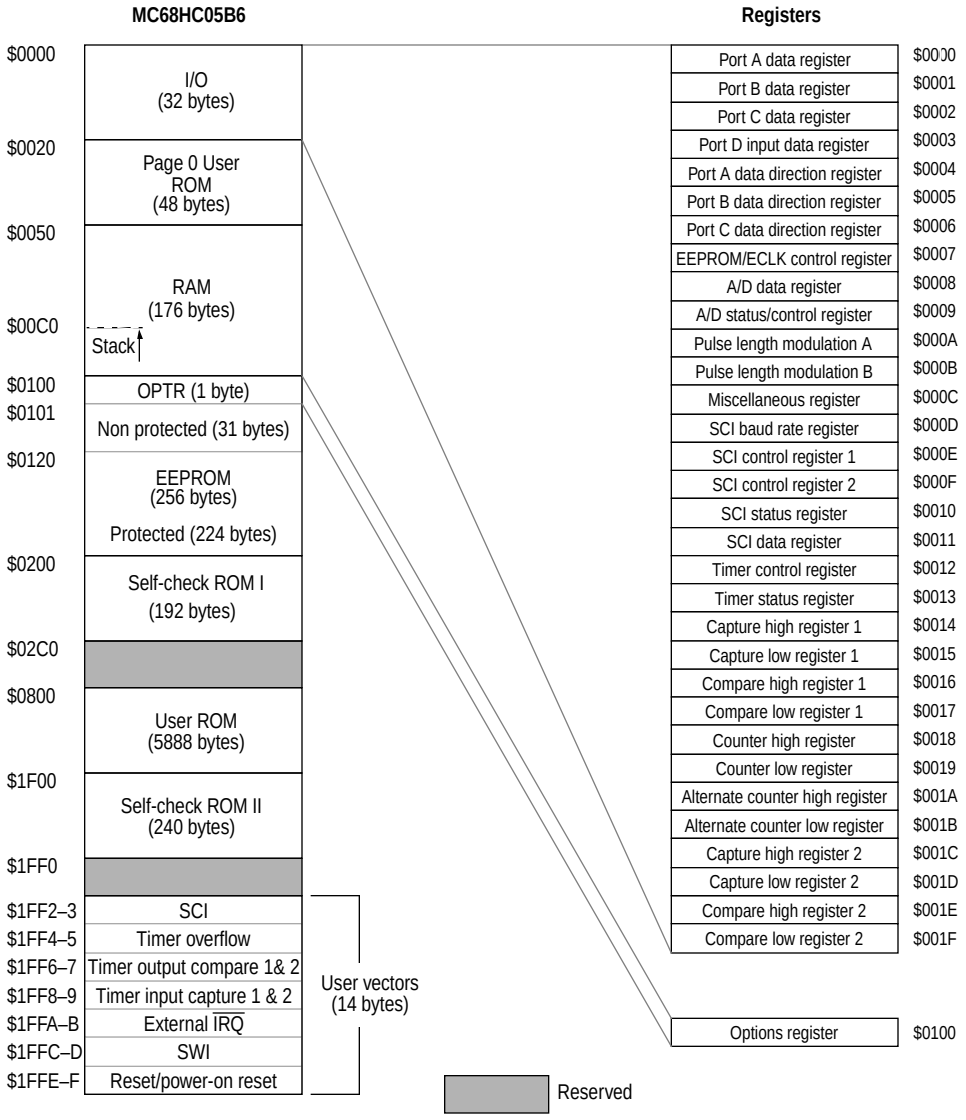


Figure 3-1 Memory map of the MC68HC05B6

3.5 EEPROM

The user EEPROM consists of 256 bytes of memory located from address $0100 to $01FF. 255 bytes are general purpose and 1 byte is used by the option register. The non-volatile EEPROM is byte erasable.

An internal charge pump provides the EEPROM voltage (V_{PP1}), which removes the need to supply a high voltage for erase and programming functions. The charge pump is a capacitor/diode ladder network which will give a very high impedance output of around 20-30 M . The voltage of the charge pump is visible at the VPP1 pin. During normal operation of the device, where programming/erasing of the EEPROM array will occur, VPP1 should never be connected to either VDD or VSS as this could prevent the charge pump reaching the necessary programming voltage. Where it is considered dangerous to leave VPP1 unconnected for reasons of excessive noise in a system, it may be tied to V_{DD}; this will protect the EEPROM data but will also increase power consumption, and therefore it is recommended that the protect bit function is used for regular protection of EEPROM data (see Section 3.5.5).

In order to achieve a higher degree of security for stored data, there is no capability for bulk or row erase operations.

The EEPROM control register ($0007) provides control of the EEPROM programming and erase operations.

Warning: The VPP1 pin should never be connected to VSS, as this could cause permanent damage to the device.

3.5.1 EEPROM control register

	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
EEPROM/ECLK control	$0007	0	0	0	0	ECLK	E1ERA	E1LAT	E1PGM	0000 0000

ECLK

See Section 4.3 for a description of this bit.

E1ERA — EEPROM erase/programming bit

Providing the E1LAT and E1PGM bits are at logic one, this bit indicates whether the access to the EEPROM is for erasing or programming purposes.

1 (set) – An erase operation will take place.

0 (clear) – A programming operation will take place.

Once the program/erase EEPROM address has been selected, E1ERA cannot be changed.

E1LAT — EEPROM programming latch enable bit

1 (set) – Address and data can be latched into the EEPROM for further program or erase operations, providing the E1PGM bit is cleared.

0 (clear) – Data can be read from the EEPROM. The E1ERA bit and the E1PGM bit are reset to zero when E1LAT is '0'.

STOP, power-on and external reset clear the E1LAT bit.

Note: After the t_{ERA1} erase time or t_{PROG1} programming time, the E1LAT bit has to be reset to zero in order to clear the E1ERA bit and the E1PGM bit.

E1PGM — EEPROM charge pump enable/disable

1 (set) – Internal charge pump generator switched on.

0 (clear) – Internal charge pump generator switched off.

When the charge pump generator is on, the resulting high voltage is applied to the EEPROM array. This bit cannot be set before the data is selected, and once this bit has been set it can only be cleared by clearing the E1LAT bit.

A summary of the effects of setting/clearing bits 0, 1 and 2 of the control register are give in Table 3-1.

Table 3-1 EEPROM control bits description

E1ERA	E1LAT	E1PGM	Description
0	0	0	Read condition
0	1	0	Ready to load address/data for program/erase
0	1	1	Byte programming in progress
1	1	0	Ready for byte erase (load address)
1	1	1	Byte erase in progress

Note: All combinations are not shown in the above table, since the E1PGM and E1ERA bits are cleared when the E1LAT bit is at zero, and will result in a read condition.

3.5.2 EEPROM read operation

To be able to read from EEPROM, the E1LAT bit has to be at logic zero, as shown in Table 3-1. While this bit is at logic zero, the E1PGM bit and the E1ERA bit are permanently reset to zero and the 256 bytes of EEPROM may be read as if it were a normal ROM area. The internal charge pump generator is automatically switched off since the E1PGM bit is reset.

If a read operation is executed while the E1LAT bit is set (erase or programming sequence), data resulting from the operation will be $FF.

Note: When not performing any programming or erase operation, it is recommended that EEPROM should remain in the read mode (E1LAT = 0)

3.5.3 EEPROM erase operation

To erase the contents of a byte of the EEPROM, the following steps should be taken:

1. Set the E1LAT bit.
2. Set the E1ERA bit (1& 2 may be done simultaneously with the same instruction).
3. Write address/data to the EEPROM address to be erased.
4. Set the E1PGM bit.
5. Wait for a time t_{ERA1}.
6. Reset the E1LAT bit (to logic zero).

While an erase operation is being performed, any access of the EEPROM array will not be successful.

The erased state of the EEPROM is $FF and the programmed state is $00.

Note: Data written to the address to be erased is not used, therefore its value is not significant.

If a second word is to be erased, it is important that the E1LAT bit be reset before restarting the erasing sequence otherwise any write to a new address will have no effect. This condition provides a higher degree of security for the stored data.

User programs must be running from the RAM or ROM as the EEPROM will have its address and data buses latched.

3.5.4 EEPROM programming operation

To program a byte of EEPROM, the following steps should be taken:

1. Set the E1LAT bit.
2. Write address/data to the EEPROM address to be programmed.
3. Set the E1PGM bit.
4. Wait for time t_{PROG1}.
5. Reset the E1LAT bit (to logic zero).

While a programming operation is being performed, any access of the EEPROM array will not be successful.

Warning: To program a byte correctly, it has to have been previously erased.

If a second word is to be programmed, it is important that the E1LAT bit be reset before restarting the programming sequence otherwise any write to a new address will have no effect. This condition provides a higher degree of security for the stored data.

User programs must be running from the RAM or ROM as the EEPROM will have its address and data buses latched.

Note: 224 bytes of EEPROM (address $0120 to $01FF) can be program and erase protected under the control of bit 1 of the OPTR register detailed in Section 3.5.5.

3.5.5 Options register (OPTR)

This register (OPTR), located at $0010, contains the secure and protect functions for the EEPROM and allows the user to select options in a non-volatile manner. The contents of the OPTR register are loaded into data latches with each power-on or external reset.

	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
Options (OPTR)(1)	$0100							EE1P	SEC	Not affected

(1) This register is implemented in EEPROM; therefore reset has no effect on the individual bits.

EE1P – EEPROM protect bit

In order to achieve a higher degree of protection, the EEPROM is effectively split into two parts, both working from the VPP1 charge pump. Part 1 of the EEPROM array (32 bytes from $0100 to $011F) cannot be protected; part 2 (224 bytes from $0120 to $01FF) is protected by the EE1P bit of the options register.

1 (set) – Part 2 of the EEPROM array is not protected; all 256 bytes of EEPROM can be accessed for any read, erase or programming operations

0 (clear) – Part 2 of the EEPROM array is protected; any attempt to erase or program a location will be unsuccessful

When this bit is set to 1 (erased), the protection will remain until the next power-on or external reset. EE1P can only be written to ‘0’ when the ELAT bit in the EEPROM control register is set.

SEC – Security bit

This high security bit allows the user to secure the EEPROM data from external accesses. When the SEC bit is at ‘0’, the EEPROM contents are secured by preventing any entry to test mode. The only way to erase the SEC bit to ‘1’ externally is to enter self-check mode, at which time the entire EEPROM contents will be erased. When the SEC bit is changed, its new value will have no effect until the next external or power-on reset.

3.6 EEPROM during STOP mode

When entering STOP mode, the EEPROM is automatically set to the read mode and the VPP1 high voltage charge pump generator is automatically disabled.

3.7 EEPROM during WAIT mode

The EEPROM is not affected by WAIT mode. Any program/erase operation will continue as in normal operating mode. The charge pump is not affected by WAIT mode, therefore it is possible to wait the t_{ERA1} erase time or t_{PROG1} programming time in WAIT mode.

Under normal operating conditions, the charge pump generator is driven by the internal CPU clocks. When the operating frequency is low, e.g. during WAIT mode, the clocking should be done by the internal A/D RC oscillator. The RC oscillator is enabled by setting the ADRC bit of the A/D status/control register at $0009.

Table 3-2 Register outline

Register name	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
Port A data (PORTA)	$0000									Undefined
Port B data (PORTB)	$0001									Undefined
Port C data (PORTC)	$0002						PC2/ ECLK			Undefined
Port D data (PORTD)	$0003	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0	Undefined
Port A data direction (DDRA)	$0004									0000 0000
Port B data direction (DDRB)	$0005									0000 0000
Port C data direction (DDRC)	$0006									0000 0000
EEPROM/ECLK control	$0007	0	0	0	0	ECLK	E1ERA	E1LAT	E1PGM	0000 0000
A/D data (ADDATA)	$0008									0000 0000
A/D status/control (ADSTAT)	$0009	COCO	ADRC	ADON	0	CH3	CH2	CH1	CH0	0000 0000
Pulse length modulation A (PLMA)	$000A									0000 0000
Pulse length modulation B (PLMB)	$000B									0000 0000
Miscellaneous	$000C	POR(1)	INTP	INTN	INTE	SFA	SFB	SM	WDOG(2)	?001 000?
SCI baud rate (BAUD)	$000D	SPC1	SPC0	SCT1	SCT0	SCT0	SCR2	SCR1	SCR0	00uu uuuu
SCI control 1 (SCCR1)	$000E	R8	T8		M	WAKE	CPOL	CPHA	LBCL	Undefined
SCI control 2 (SCCR2)	$000F	TIE	TCIE	RIE	ILIE	TE	RE	RWU	SBK	0000 0000
SCI status (SCSR)	$0010	TDRE	TC	RDRF	IDLE	OR	NF	FE		1100 000u
SCI data (SCDR)	$0011									0000 0000
Timer control (TCR)	$0012	ICIE	OCIE	TOIE	FOLV2	FOLV1	OLV2	IEDG1	OLVL1	0000 00u0
Timer status (TSR)	$0013	ICF1	OCF1	TOF	ICF2	OCF2				Undefined
Input capture high 1	$0014									Undefined
Input capture low 1	$0015									Undefined
Output compare high 1	$0016									Undefined
Output compare low 1	$0017									Undefined
Timer counter high	$0018									1111 1111
Timer counter low	$0019									1111 1100
Alternate counter high	$001A									1111 1111
Alternate counter low	$001B									1111 1100
Input capture high 2	$001C									Undefined
Input capture low 2	$001D									Undefined
Output compare high 2	$001E									Undefined
Output compare low 2	$001F									Undefined
Options (OPTR)(3)	$0100							EE1P	SEC	Not affected

(1) The POR bit is set each time there is a power-on reset.

(2) The state of the WDOG bit after reset is dependent on the mask option selected; 1=watchdog enabled, 0=watchdog disabled.

(3) This register is implemented in EEPROM; therefore reset has no effect on the individual bits.

3.8 Miscellaneous register

	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
Miscellaneous	$000C	POR(1)	INTP	INTN	INTE	SFA	SFB	SM	WDOG(2)	?001 000?

(1) The POR bit is set each time there is a power-on reset.

(2) The state of the WDOG bit after reset is dependent on the mask option selected; 1=watchdog enabled, 0=watchdog disabled.

POR — Power-on reset bit (see Section 9.1)

This bit is set each time the device is powered on. Therefore, the state of the POR bit allows the user to make a software distinction between a power-on and an external reset. This bit cannot be set by software and is cleared by writing it to zero.

1 (set) – A power-on reset has occurred.

0 (clear) – No power-on reset has occurred.

INTP, INTN — External interrupt sensitivity options (see Section 9.2)

These two bits allow the user to select which edge the $\overline{IRQ}$ pin will be sensitive to (see Table 3-3). Both bits can be written to only while the I-bit is set, and are cleared by power-on or external reset, thus the device is initialised with negative edge and low level sensitivity.

Table 3-3 $\overline{IRQ}$ sensitivity

INTP	INTN	$\overline{IRQ}$ sensitivity
0	0	Negative edge and low level sensitive
0	1	Negative edge only
1	0	Positive edge only
1	1	Positive and negative edge sensitive

INTE — External interrupt enable (see Section 9.2)

1 (set) – External interrupt function ($\overline{IRQ}$) enabled.

0 (clear) – External interrupt function ($\overline{IRQ}$) disabled.

The INTE bit can be written to only while the I-bit is set, and is set by power-on or external reset, thus enabling the external interrupt function.

SFA — Slow or fast mode selection for PLMA (see Section 7.1)

This bit allows the user to select the slow or fast mode of the PLMA pulse length modulation output.

1 (set) – Slow mode PLMA (4096 x timer clock period).

0 (clear) – Fast mode PLMA (256 x timer clock period).

SFB — Slow or fast mode selection for PLMB (see Section 7.1)

This bit allows the user to select the slow or fast mode of the PLMB pulse length modulation output.

1 (set) – Slow mode PLMB (4096 x timer clock period).

0 (clear) – Fast mode PLMB (256 x timer clock period).

Note: The highest speed of the PLM system corresponds to the frequency of the TOF bit being set, multiplied by 256. The lowest speed of the PLM system corresponds to the frequency of the TOF bit being set, multiplied by 16.

Warning: Because the SFA bit and SFB bit are not double buffered, it is mandatory to set the SFA bit and SFB bit to the desired values before writing to the PLM registers; not doing so could temporarily give incorrect values at the PLM outputs.

SM — Slow mode (see Section 2.4.3)

1 (set) – The system runs at a bus speed 16 times lower than normal ($f_{OSC}/32$). SLOW mode affects all sections of the device, including SCI, A/D and timer.

0 (clear) – The system runs at normal bus speed ($f_{OSC}/2$).

The SM bit is cleared by external or power-on reset. The SM bit is automatically cleared when entering STOP mode.

WDOG — Watchdog enable/disable (see Section 9.1.4)

The WDOG bit can be used to enable the watchdog timer previously disabled by a mask option. Following a watchdog reset the state of the WDOG bit is as defined by the mask option specified.

1 (set) – Watchdog counter cleared and enabled.

0 (clear) – The watchdog cannot be disabled by software; writing a zero to this bit has no effect.

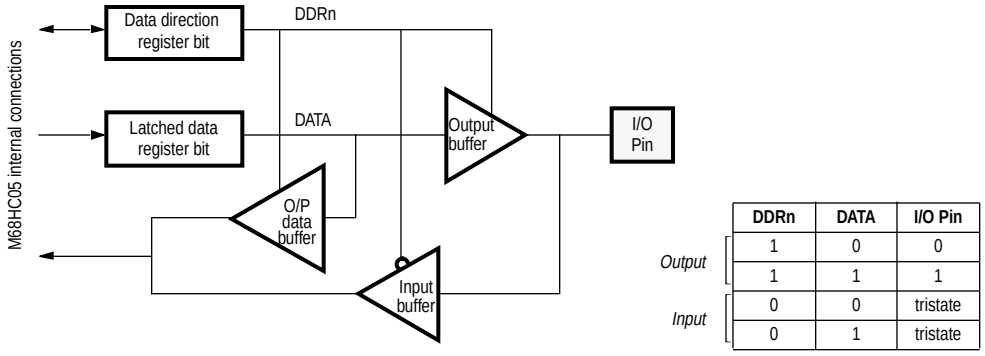
4
INPUT/OUTPUT PORTS

In single-chip mode, the MC68HC05B6 has a total of 24 I/O lines, arranged as three 8-bit ports (A, B and C), and eight input-only lines, arranged as one 8-bit port (D). Each I/O line is individually programmable as either input or output, under the software control of the data direction registers. The 8-bit input-only port (D) shares its pins with the A/D converter, when the A/D converter is enabled. To avoid glitches on the output pins, data should be written to the I/O port data register before writing ones to the corresponding data direction register bits to set the pins to output mode.

4.1 Input/output programming

The bidirectional port lines may be programmed as inputs or outputs under software control. The direction of each pin is determined by the state of the corresponding bit in the port data direction register (DDR). Each port has an associated DDR. Any I/O port pin is configured as an output if its corresponding DDR bit is set to a logic one. A pin is configured as an input if its corresponding DDR bit is cleared to a logic zero.

At power-on or reset, all DDRs are cleared, thus configuring all port pins as inputs. The data direction registers can be written to or read by the MCU. During the programmed output state, a read of the data register actually reads the value of the output data latch and not the I/O pin. The operation of the standard port hardware is shown schematically in Figure 4-1.



DDRn	DATA	I/O Pin
1	0	0
1	1	1
0	0	tristate
0	1	tristate

Figure 4-1 Standard I/O port structure

Table 4-1 shows the effect of reading from or writing to an I/O pin in various circumstances. Note that the read/write signal shown is internal and not available to the user.

Table 4-1 I/O pin states

R/$\overline{W}$	DDRn	Action of MCU write to/read of data bit
0	0	The I/O pin is in input mode. Data is written into the output data latch.
0	1	Data is written into the output data latch, and output to the I/O pin.
1	0	The state of the I/O pin is read.
1	1	The I/O pin is in output mode. The output data latch is read.

4.2 Ports A and B

These ports are standard M68HC05 bidirectional I/O ports, each comprising a data register and a data direction register.

Reset does not affect the state of the data register, but clears the data direction register, thereby returning all port pins to input mode. Writing a ‘1’ to any DDR bit sets the corresponding port pin to output mode.

4.3 Port C

In addition to the standard port functions described for port A and B, port C pin 2 can be configured, using the ECLK bit of the EEPROM/ECLK control register, to output the CPU clock. If this is selected the corresponding DDR bit is automatically set and bit 2 of port C will always read the output data latch. The other port C pins are not affected by this feature.

	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
EEPROM/ECLK control	$0007	0	0	0	0	ECLK	E1ERA	E1LAT	E1PGM	0000 0000

ECLK — External clock output bit

1 (set) – ECLK CPU clock is output on PC2.

0 (clear) – ECLK CPU clock is not output on PC2; port C acts as a normal I/O port.

The ECLK bit is cleared by power-on or external reset. It is not affected by the execution of a STOP or WAIT instruction.

The timing diagram of the clock output is shown in Figure 4-2.

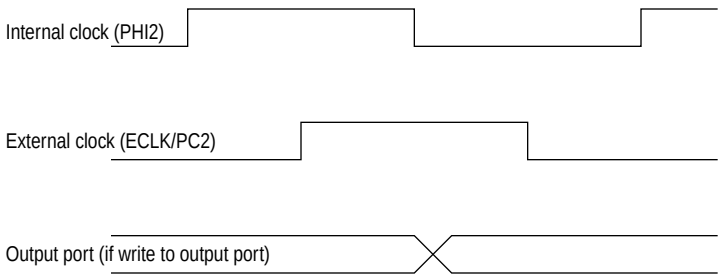


Figure 4-2 ECLK timing diagram

4.4 Port D

This 8-bit input-only port shares its pins with the A/D converter subsystem. When the A/D converter is enabled, pins PD0-PD7 read the eight analog inputs to the A/D converter. Port D can be read at any time, however, if it is read during an A/D conversion sequence noise, may be injected on the analog inputs, resulting in reduced accuracy of the A/D. Furthermore, performing

a digital read of port D with levels other than V_{DD} or V_{SS} on the port D pins will result in greater power dissipation during the read cycle.

As port D is an input-only port there is no DDR associated with it. Also, at power up or external reset, the A/D converter is disabled, thus the port is configured as a standard input-only port.

Note: It is recommended that all unused input ports and I/O ports be tied to an appropriate logic level (i.e. either V_{DD} or V_{SS}).

4.5 Port registers

The following sections explain in detail the individual bits in the data and control registers associated with the ports.

4.5.1 Port data registers A and B (PORTA and PORTB)

	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
Port A data (PORTA)	$0000									Undefined
Port B data (PORTB)	$0001									Undefined

Each bit can be configured as input or output via the corresponding data direction bit in the port data direction register (DDRx).

The state of the port data registers following reset is not defined.

4.5.2 Port data register C (PORTC)

	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
Port C data (PORTC)	$0002						PC2/ ECLK			Undefined

Each bit can be configured as input or output via the corresponding data direction bit in the port data direction register (DDRx).

In addition, bit 2 of port C is used to output the CPU clock if the ECLK bit in the EEPROM CTL/ECLK register is set (see Section 4.3).

The state of the port data registers following reset is not defined.

4.5.3 Port data register D (PORTD)

	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
Port D data (PORTD)	$0003	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0	Undefined

All the port D bits are input-only and are shared with the A/D converter. The function of each bit is determined by the ADON bit in the A/D status/control register.

The state of the port data registers following reset is not defined.

4.5.3.1 A/D status/control register

	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
A/D status/control	$0009	COCO	ADRC	ADON	0	CH3	CH2	CH1	CH0	0000 0000

ADON — A/D converter on

1 (set) – A/D converter is switched on; all port D pins act as analog inputs for the A/D converter.

0 (clear) – A/D converter is switched off; all port D pins act as input only pins.

Reset clears the ADON bit, thus configuring port D as an input only port.

4.5.4 Data direction registers (DDRA, DDRB and DDRC)

	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
Port A data direction (DDRA)	$0004									0000 0000
Port B data direction (DDRB)	$0005									0000 0000
Port C data direction (DDRC)	$0006									0000 0000

Writing a ‘1’ to any bit configures the corresponding port pin as an output; conversely, writing any bit to ‘0’ configures the corresponding port pin as an input.

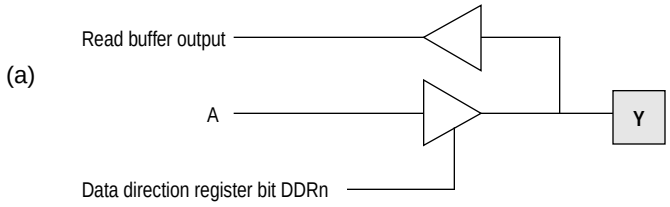
Reset clears these registers, thus configuring all ports as inputs.

4.6 Other port considerations

All output ports can emulate ‘open-drain’ outputs. This is achieved by writing a zero to the relevant output port latch. By toggling the corresponding data direction bit, the port pin will either be an output zero or tri-state (an input). This is shown diagrammatically in Figure 4-3.

When using a port pin as an ‘open-drain’ output, certain precautions must be taken in the user software. If a read-modify-write instruction is used on a port where the ‘open-drain’ is assigned and the pin at this time is programmed as an input, it will read it as a ‘one’. The read-modify-write instruction will then write this ‘one’ into the output data latch on the next cycle. This would cause the ‘open-drain’ pin not to output a ‘zero’ when desired.

Note: ‘Open-drain’ outputs should not be pulled above V_{DD}.



(b)

DDRn	A	Y	
1	0	0	Normal operation – tri state
1	1	1	
0	0	tri state	
0	1	tri state	
1	0	low	‘Open-drain’
1	1	—	
0	0	high	
0	1	high	

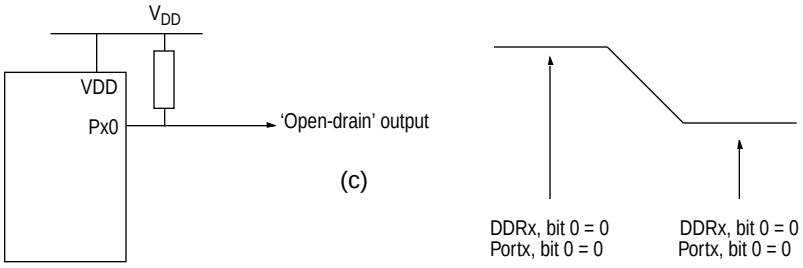


Figure 4-3 Port logic levels

5
PROGRAMMABLE TIMER

The programmable timer on the MC68HC05B6 consists of a 16-bit read-only free-running counter, with a fixed divide-by-four prescaler, plus the input capture/output compare circuitry. The timer can be used for many purposes including measuring pulse length of two input signals and generating two output signals. Pulse lengths for both input and output signals can vary from several microseconds to many seconds. In addition, it works in conjunction with the pulse width modulation (PLM) system to execute two 8-bit D/A PLM (pulse length modulation) conversions, with a choice of two repetition rates. The timer is also capable of generating periodic interrupts or indicating passage of an arbitrary multiple of four CPU cycles. A block diagram is shown in Figure 5-1, and timing diagrams are shown in Figure 5-2, Figure 5-3, Figure 5-4 and Figure 5-5.

The timer has a 16-bit architecture, hence each specific functional segment is represented by two 8-bit registers (except the PLMA and PLMB which use one 8-bit register for each). These registers contain the high and low byte of that functional segment. Accessing the low byte of a specific timer function allows full control of that function; however, an access of the high byte inhibits that specific timer function until the low byte is also accessed.

The 16-bit programmable timer is monitored and controlled by a group of sixteen registers, full details of which are contained in this section.

Note: A problem may arise if an interrupt occurs in the time between the high and low bytes being accessed. To prevent this, the I-bit in the condition code register (CCR) should be set while manipulating both the high and low byte register of a specific timer function, ensuring that an interrupt does not occur.

5.1 Counter

The key element in the programmable timer is a 16-bit, free-running counter or counter register, preceded by a prescaler that divides the internal processor clock by four. The prescaler gives the timer a resolution of 2µs if the internal bus clock is 2 MHz. The counter is incremented during the low portion of the internal bus clock. Software can read the counter at any time without affecting its value.

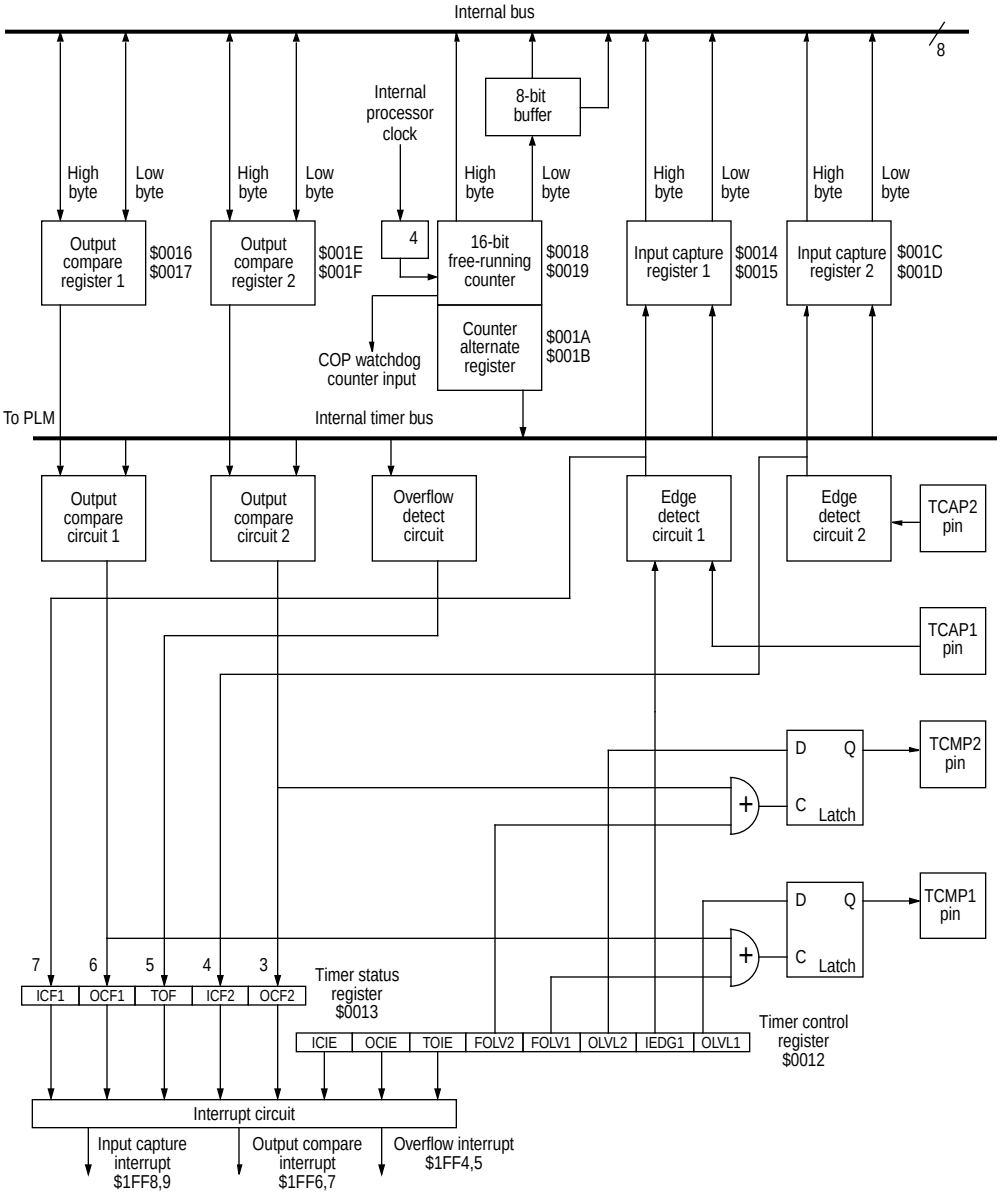


Figure 5-1 16-bit programmable timer block diagram

5.1.1 Counter register and alternate counter register

	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
Timer counter high	$0018									1111 1111
Timer counter low	$0019									1111 1100

	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
Alternate counter high	$001A									1111 1111
Alternate counter low	$001B									1111 1100

The double-byte, free-running counter can be read from either of two locations, $18-$19 (counter register) or $1A-$1B (alternate counter register). A read from only the less significant byte (LSB) of the free-running counter ($19 or $1B) receives the count value at the time of the read. If a read of the free-running counter or alternate counter register first addresses the more significant byte (MSB) ($18 or $1A), the LSB is transferred to a buffer. This buffer value remains fixed after the first MSB read, even if the user reads the MSB several times. This buffer is accessed when reading the free-running counter or alternate counter register LSB and thus completes a read sequence of the total counter value. In reading either the free-running counter or alternate counter register, if the MSB is read, the LSB must also be read to complete the sequence. If the timer overflow flag (TOF) is set when the counter register LSB is read then a read of the timer status register (TSR) will clear the flag.

The alternate counter register differs from the counter register only in that a read of the LSB does not clear TOF. Therefore, where it is critical to avoid the possibility of missing timer overflow interrupts due to clearing of TOF, the alternate counter register should be used.

The free-running counter is set to $FFFC during power-on and external reset and is always a read-only register. During a power-on reset, the counter begins running after the oscillator start-up delay. Because the free-running counter is 16 bits preceded by a fixed divide-by-4 prescaler, the value in the free-running counter repeats every 262,144 internal bus clock cycles. TOF is set when the counter overflows (from $FFFF to $0000); this will cause an interrupt if TOIE is set.

In some particular timing control applications it may be desirable to reset the 16-bit free running counter under software control. When the low byte of the counter ($19 or $1B) is written to, the counter is configured to its reset value ($FFFC).

The divide-by-4 prescaler is also reset and the counter resumes normal counting operation. All of the flags and enable bits remain unaltered by this operation. If access has previously been made to the high byte of the free-running counter ($18 or $1A), then the reset counter operation terminates the access sequence.

Warning: This operation may affect the function of the watchdog system (see Section 9.1.4). The PLM results will also be affected while resetting the counter.

5.2 Timer control and status

The various functions of the timer are monitored and controlled using the timer control and status registers described below.

5.2.1 Timer control register (TCR)

The timer control register ($0012) is used to enable the input captures (ICIE), output compares (OCIE), and timer overflow (TOIE) functions as well as forcing output compares (FOLV1 and FOLV2), selecting input edge sensitivity (IEDG1) and levels of output polarity (OLV1 and OLV2).

	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
Timer control (TCR)	$0012	ICIE	OCIE	TOIE	FOLV2	FOLV1	OLV2	IEDG1	OLVL1	0000 00u0

ICIE — Input captures interrupt enable

If this bit is set, a timer interrupt is enabled whenever the ICF1 or ICF2 status flag (in the timer status register) is set.

1 (set) – Interrupt enabled.

0 (clear) – Interrupt disabled.

OCIE — Output compares interrupt enable

If this bit is set, a timer interrupt is enabled whenever the OCF1 or OCF2 status flag (in the timer status register) is set.

1 (set) – Interrupt enabled.

0 (clear) – Interrupt disabled.

TOIE — Timer overflow interrupt enable

If this bit is set, a timer interrupt is enabled whenever the TOF status flag (in the timer status register) is set.

1 (set) – Interrupt enabled.

0 (clear) – Interrupt disabled.

FOLV2 — Force output compare 2

This bit always reads as zero, hence writing a zero to this bit has no effect. Writing a one at this position will force the OLV2 bit to the corresponding output level latch, thus appearing at the TCMP2 pin. Note that this bit does not affect the OCF2 bit of the status register (see Section 5.4.3).

1 (set) – OLV2 bit forced to output level latch.

0 (clear) – No effect.

FOLV1 — Force output compare 1

This bit always reads as zero, hence writing a zero to this bit has no effect. Writing a one at this position will force the OLV1 bit to the corresponding output level latch, thus appearing at the TCMP1 pin. Note that this bit does not affect the OCF1 bit of the status register (see Section 5.4.3).

1 (set) – OLV1 bit forced to output level latch.

0 (clear) – No effect.

OLV2 — Output level 2

When OLV2 is set a high output level will be clocked into the output level register by the next successful output compare, and will appear on the TCMP2 pin. When clear, it will be a low level which will appear on the TCMP2 pin.

1 (set) – A high output level will appear on the TCMP2 pin.

0 (clear) – A low output level will appear on the TCMP2 pin.

IEDG1 — Input edge 1

When IEDG1 is set, a positive-going edge on the TCAP1 pin will trigger a transfer of the free-running counter value to the input capture register 1. When clear, a negative-going edge triggers the transfer.

1 (set) – TCAP1 is positive-going edge sensitive.

0 (clear) – TCAP1 is negative-going edge sensitive.

Note: There is no need for an equivalent bit for the input capture register 2 as TCAP2 is negative-going edge sensitive only.

OLV1 — Output level 1

When OLV1 is set a high output level will be clocked into the output level register by the next successful output compare, and will appear on the TCMP1 pin. When clear, it will be a low level which will appear on the TCMP1 pin.

1 (set) – A high output level will appear on the TCMP1 pin.

0 (clear) – A low output level will appear on the TCMP1 pin.

5.2.2 Timer status register (TSR)

The timer status register ($13) contains the status bits corresponding to the four timer interrupt conditions – ICF1,OCF1, TOF, ICF2 and OCF2.

Accessing the timer status register satisfies the first condition required to clear the status bits. The remaining step is to access the register corresponding to the status bit.

	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
Timer status (TSR)	$0013	ICF1	OCF1	TOF	ICF2	OCF2				Undefined

ICF1 — Input capture flag 1

This bit is set when the selected polarity of edge is detected by the input capture edge detector 1 at TCAP1; an input capture interrupt will be generated, if ICIE is set. ICF1 is cleared by reading the TSR and then the input capture low register 1 ($15).

1 (set) – A valid input capture has occurred.

0 (clear) – No input capture has occurred.

OCF1 — Output compare flag 1

This bit is set when the output compare 1 register contents match those of the free-running counter; an output compare interrupt will be generated if OCIE is set. OCF1 is cleared by reading the TSR and then the output compare 1 low register ($17).

1 (set) – A valid output compare has occurred.

0 (clear) – No output compare has occurred.

TOF — Timer overflow status flag

This bit is set when the free-running counter overflows from $FFFF to $0000; a timer overflow interrupt will occur if TOIE is set. TOF is cleared by reading the TSR and the counter low register ($19).

1 (set) – Timer overflow has occurred.

0 (clear) – No timer overflow has occurred.

When using the timer overflow function and reading the free-running counter at random times to measure an elapsed time, a problem may occur whereby the timer overflow flag is unintentionally cleared if:

1 The timer status register is read or written when TOF is set, and

2 The LSB of the free-running counter is read, but not for the purpose of servicing the flag.

Reading the alternate counter register instead of the counter register will avoid this potential problem.

ICF2 — Input capture flag 2

This bit is set when a negative edge is detected by the input capture edge detector 2 at TCAP2; an input capture interrupt will be generated if ICIE is set. ICF2 is cleared by reading the TSR and then the input capture low register 2 ($1D).

1 (set) – A valid (negative) input capture has occurred.

0 (clear) – No input capture has occurred.

OCF2 — Output compare flag 2

This bit is set when the output compare 2 register contents match those of the free-running counter; an output compare interrupt will be generated if OCIE is set. OCF2 is cleared by reading the TSR and then the output compare 2 low register ($1F).

1 (set) – A valid output compare has occurred.

0 (clear) – No output compare has occurred.

5.3 Input capture

'Input capture' is a technique whereby an external signal is used to trigger a read of the free running counter. In this way it is possible to relate the timing of an external signal to the internal counter value, and hence to elapsed time.

There are two input capture registers: input capture register 1 (ICR1) and input capture register 2 (ICR2).

The same input capture interrupt enable bit (ICIE) is used for the two input captures.

5.3.1 Input capture register 1 (ICR1)

	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
Input capture high 1	$0014									Undefined
Input capture low 1	$0015									Undefined

The two 8-bit registers that make up the 16-bit input capture register 1 are read-only, and are used to latch the value of the free-running counter after the input capture edge detector circuit 1 senses a valid transition at TCAP1. The level transition that triggers the counter transfer is defined by the input edge bit (IEDG1). When an input capture 1 occurs, the corresponding flag ICF1 in TSR is set. An interrupt can also accompany an input capture 1 provided the ICIE bit in TCR is set. The 8 most significant bits are stored in the input capture high 1 register at $14, the 8 least significant bits in the input capture low 1 register at $15.

The result obtained from an input capture will be one greater than the value of the free-running counter on the rising edge of the internal bus clock preceding the external transition. This delay is required for internal synchronization. Resolution is one count of the free-running counter, which is four internal bus clock cycles. The free-running counter contents are transferred to the input capture register 1 on each valid signal transition whether the input capture 1 flag (ICF1) is set or clear. The input capture register 1 always contains the free-running counter value that corresponds to the most recent input capture 1. After a read of the input capture 1 register MSB ($14), the counter transfer is inhibited until the LSB ($15) is also read. This characteristic causes the time used in the input capture software routine and its interaction with the main program to determine the minimum pulse period. A read of the input capture 1 register LSB ($15) does not inhibit the free-running counter transfer since the two actions occur on opposite edges of the internal bus clock.

Reset does not affect the contents of the input capture 1 register, except when exiting STOP mode (see Section 5.6).

5.3.2 Input capture register 2 (ICR2)

	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
Input capture high 2	$001C									Undefined
Input capture low 2	$001D									Undefined

The two 8-bit registers that make up the 16-bit input capture register 2 are read-only, and are used to latch the value of the free-running counter after the input capture edge detector circuit 2 senses a negative transition at pin TCAP2. When an input capture 2 occurs, the corresponding flag ICF2 in TSR is set. An interrupt can also accompany an input capture 2 provided the ICIE bit in TCR is set.The 8 most significant bits are stored in the input capture 2 high register at $1C, the 8 least significant bits in the input capture 2 low register at $1D.

The result obtained from an input capture will be one greater than the value of the free-running counter on the rising edge of the internal bus clock preceding the external transition. This delay is required for internal synchronization. Resolution is one count of the free-running counter, which is four internal bus clock cycles. The free-running counter contents are transferred to the input capture register 2 on each negative signal transition whether the input capture 2 flag (IC2F) is set or clear. The input capture register 2 always contains the free-running counter value that corresponds to the most recent input capture 2. After a read of the input capture register 2 MSB ($1C), the counter transfer is inhibited until the LSB ($1D) is also read. This characteristic causes the time used in the input capture software routine and its interaction with the main program to determine the minimum pulse period. A read of the input capture register 2 LSB ($1C) does not inhibit the free-running counter transfer since the two actions occur on opposite edges of the internal bus clock.

Reset does not affect the contents of the input capture 2 register, except when exiting STOP mode (see Section 5.6).

5.4 Output compare

'Output compare' is a technique which may be used, for example, to generate an output waveform, or to signal when a specific time period has elapsed, by presetting the output compare register to the appropriate value.

There are two output compare registers: output compare register 1 (OCR1) and output compare register 2 (OCR2).

Note: The same output compare interrupt enable bit (OCIE) is used for the two output compares.

5.4.1 Output compare register 1 (OCR1)

	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
Output compare high 1	$0016									Undefined
Output compare low 1	$0017									Undefined

The 16-bit output compare register 1 is made up of two 8-bit registers at locations $16 (MSB) and $17 (LSB). The contents of the output compare register 1 are compared with the contents of the free-running counter continually and, if a match is found, the corresponding output compare flag (OCF1) in the timer status register is set and the output level (OLVL1) is transferred to pin TCMP1. The output compare register 1 values and the output level bit should be changed after each successful comparison to establish a new elapsed timeout. An interrupt can also accompany a successful output compare provided the corresponding interrupt enable bit (OCIE) is set. (The free-running counter is updated every four internal bus clock cycles.)

After a processor write cycle to the output compare register 1 containing the MSB ($16), the output compare function is inhibited until the LSB ($17) is also written. The user must write both bytes (locations) if the MSB is written first. A write made only to the LSB ($17) will not inhibit the compare 1 function. The processor can write to either byte of the output compare register 1 without affecting the other byte. The output level (OLVL1) bit is clocked to the output level register and hence to the TCMP1 pin whether the output compare flag 1 (OCF1) is set or clear. The minimum time required to update the output compare register 1 is a function of the program rather than the internal hardware. Because the output compare flag 1 and the output compare register 1 are not defined at power on, and not affected by reset, care must be taken when initializing output compare functions with software. The following procedure is recommended:

- Write to output compare high 1 to inhibit further compares;
- Read the timer status register to clear OCF1 (if set);
- Write to output compare low 1 to enable the output compare 1 function.

The purpose of this procedure is to prevent the OCF1 bit from being set between the time it is read and the write to the corresponding output compare register.

All bits of the output compare register are readable and writable and are not altered by the timer hardware or reset. If the compare function is not needed, the two bytes of the output compare register can be used as storage locations.

5.4.2 Output compare register 2 (OCR2)

	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
Output compare high 2	$001E									Undefined
Output compare low 2	$001F									Undefined

The 16-bit output compare register 2 is made up of two 8-bit registers at locations $1E (MSB) and $1F (LSB). The contents of the output compare register 2 are compared with the contents of the free-running counter continually and, if a match is found, the corresponding output compare flag (OCF2) in the timer status register is set and the output level (OLVL2) is transferred to pin TCMP2. The output compare register 2 values and the output level bit should be changed after each successful comparison to establish a new elapsed timeout. An interrupt can also accompany a successful output compare provided the corresponding interrupt enable bit (OCIE) is set. (The free-running counter is updated every four internal bus clock cycles.)

After a processor write cycle to the output compare register 2 containing the MSB ($1E), the output compare function is inhibited until the LSB ($1F) is also written. The user must write both bytes (locations) if the MSB is written first. A write made only to the LSB ($1F) will not inhibit the compare 2 function. The processor can write to either byte of the output compare register 2 without affecting the other byte. The output level (OLVL2) bit is clocked to the output level register and hence to the TCMP2 pin whether the output compare flag 2 (OCF2) is set or clear. The minimum time required to update the output compare register 2 is a function of the program rather than the internal hardware. Because the output compare flag 2 and the output compare register 2 are not defined at power on, and not affected by reset, care must be taken when initializing output compare functions with software. The following procedure is recommended:

- Write to output compare high 2 to inhibit further compares;
- Read the timer status register to clear OCF2 (if set);
- Write to output compare low 2 to enable the output compare 2 function.

The purpose of this procedure is to prevent the OCF1 bit from being set between the time it is read and the write to the corresponding output compare register.

All bits of the output compare register are readable and writable and are not altered by the timer hardware or reset. If the compare function is not needed, the two bytes of the output compare register can be used as storage locations.

5.4.3 Software force compare

A software force compare is required in many applications. To achieve this, bit 3 (FOLV1 for OCR1) and bit 4 (FOLV2 for OCR2) in the timer control register are used. These bits always read as 'zero', but a write to 'one' causes the respective OLVL1 or OLVL2 values to be copied to the respective output level (TCMP1 and TCMP2 pins).

Internal logic is arranged such that in a single instruction, one can change OLVL1 and/or OLVL2, at the same time causing a forced output compare with the new values of OLVL1 and OLVL2. In conjunction with normal compare, this function allows a wide range of applications including fixed frequency generation.

Note: A software force compare will affect the corresponding output pin TCMP1 and/or TCMP2, but will not affect the compare flag, thus it will not generate an interrupt.

5.5 Pulse Length Modulation (PLM)

The programmable timer works in conjunction with the PLM system to execute two 8-bit D/A PLM conversions, with a choice of two repetition rates (see Section 7).

5.5.1 Pulse length modulation registers A and B (PLMA/PLMB)

	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
Pulse length modulation A (PLMA)	$000A									0000 0000

	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
Pulse length modulation B (PLMB)	$000B									0000 0000

5.6 Timer during STOP mode

When the MCU enters STOP mode, the timer counter stops counting and remains at that particular count value until STOP mode is exited by an interrupt. If STOP mode is exited by power-on or external reset, the counter is forced to $FFFC but if it is exited by external interrupt ($\overline{IRQ}$) then the counter resumes from its stopped value.

Another feature of the programmable timer is that if at least one valid input capture edge occurs at one of the TCAP pins while in STOP mode, the corresponding input capture detect circuitry is armed. This action does not wake the MCU or set any timer flags, but when the MCU does wake-up there will be an active input capture flag (and data) from that first valid edge which occurred during STOP mode.

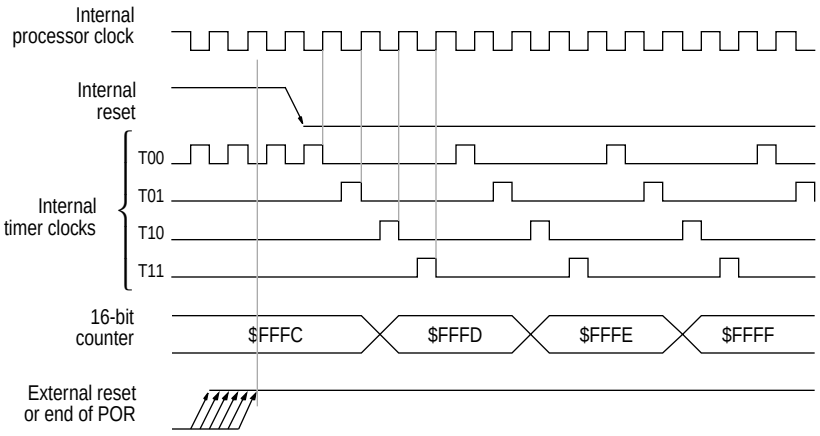
If STOP mode is exited by an external reset then no such input capture flag or data action takes place even if there was a valid input capture edge (at one of the TCAP pins) during STOP mode.

5.7 Timer during WAIT mode

The timer system is not affected by WAIT mode and continues normal operation. Any valid timer interrupt will wake-up the system.

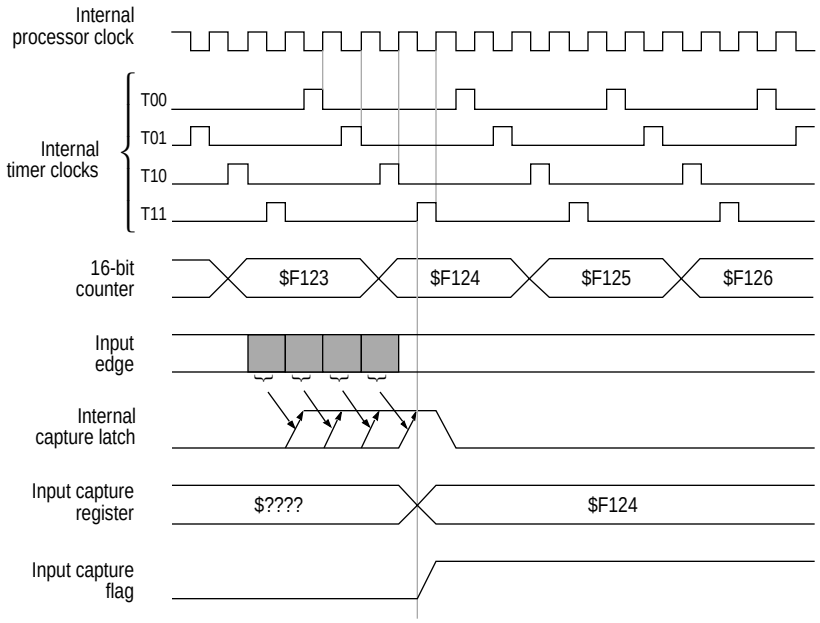
5.8 Timer state diagrams

The relationships between the internal clock signals, the counter contents and the status of the flag bits are shown in the following figures. It should be noted that the signals labelled ‘internal’ (processor clock, timer clocks and reset) are not available to the user.



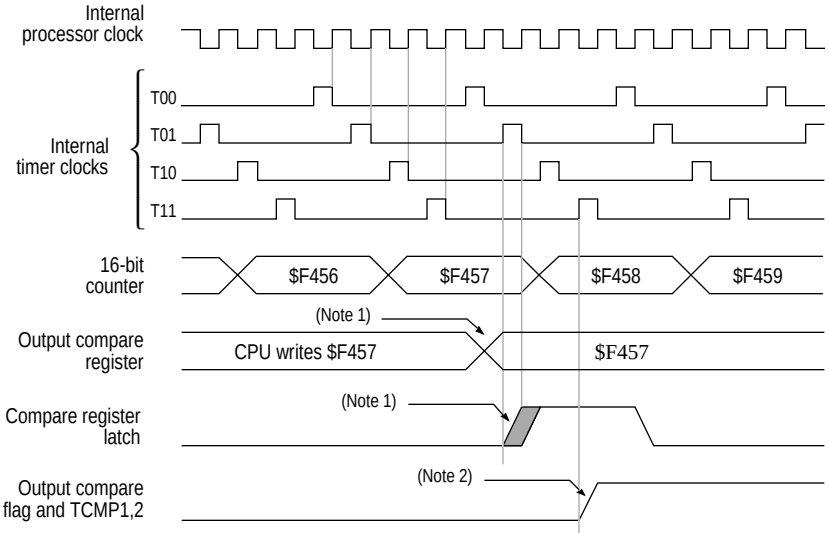
Note: The counter and timer control registers are the only ones affected by power-on or external reset.

Figure 5-2 Timer state timing diagram for reset



Note: If the input edge occurs in the shaded area from one timer state T10 to the next timer state T10, then the input capture flag will be set during the next T11 state.

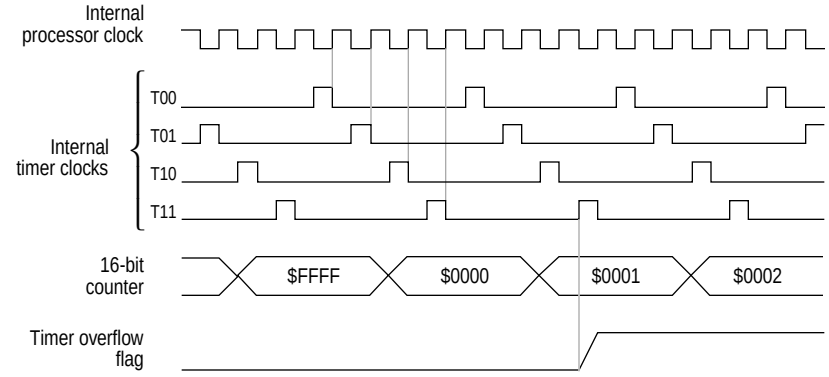
Figure 5-3 Timer state timing diagram for input capture



Note: 1 The CPU write to the compare registers may take place at any time, but a compare only occurs at timer state T01. Thus a four cycle difference may exist between the write to the compare register and the actual compare.

2 The output compare flag is set at the timer state T11 that follows the comparison match ($F457 in this example).

Figure 5-4 Timer state timing diagram for output compare



Note: The timer overflow flag is set at timer state T11 (transition of counter from $FFFF to $0000). It is cleared by a read of the timer status register during the internal processor clock high time, followed by a read of the counter low register.

Figure 5-5 Timer state timing diagram for timer overflow

6
SERIAL COMMUNICATIONS INTERFACE

A full-duplex asynchronous serial communications interface (SCI) is provided with a standard non-return-to-zero (NRZ) format and a variety of baud rates. The SCI transmitter and receiver are functionally independent and have their own baud rate generator; however they share a common baud rate prescaler and data format.

The serial data format is standard mark/space (NRZ) and provides one start bit, eight or nine data bits, and one stop bit.

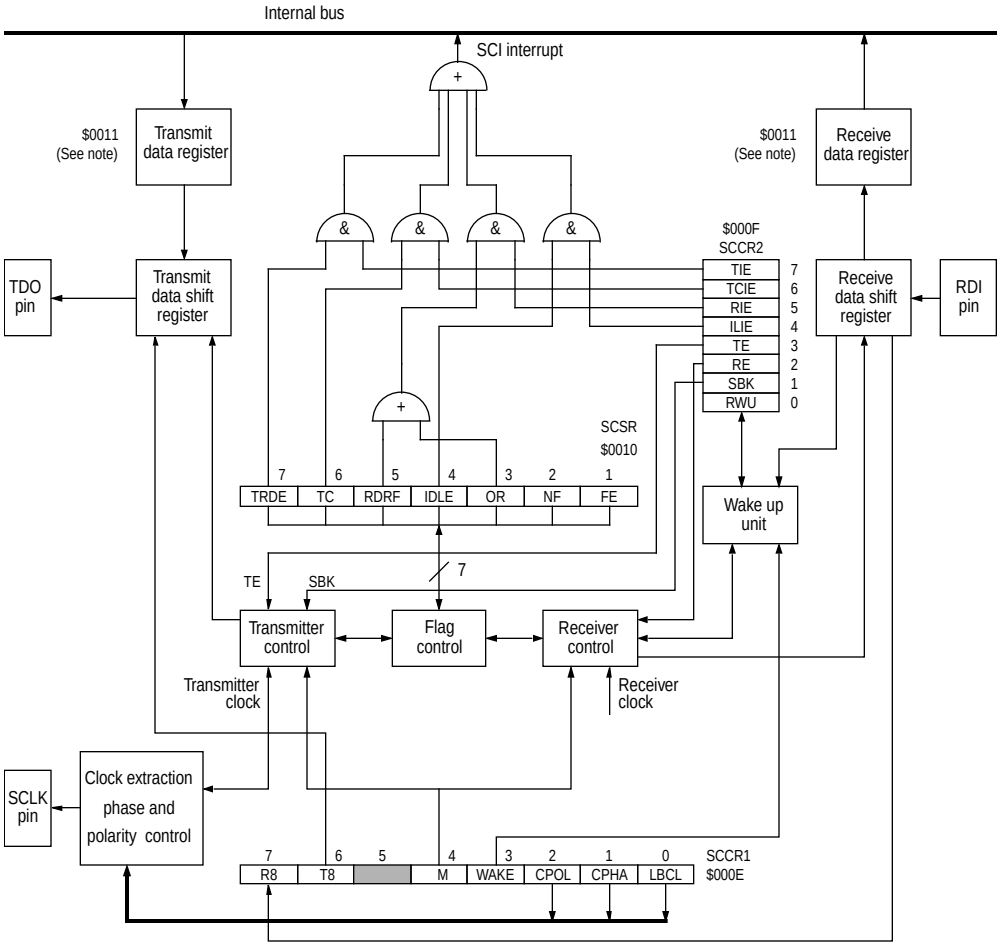
The SCLK pin is the output of the transmitter clock. It outputs the transmitter data clock for synchronous transmission (no clocks on start bit and stop bit, and a software option to send clock on last data bit). This allows control of peripherals containing shift registers (e.g. LCD drivers). Phase and polarity of these clocks are software programmable.

Any SCI bidirectional communication requires a two-wire system: receive data in (RDI) and transmit data out (TDO).

‘Baud’ and ‘bit rate’ are used synonymously in the following description.

6.1 SCI two-wire system features

- Standard NRZ (mark/space) format
- Advanced error detection method with noise detection for noise duration of up to 1/16th bit time
- Full-duplex operation (simultaneous transmit and receive)
- 32 software selectable baud rates
- Different baud rates for transmit and receive; for each transmit baud rate, 8 possible receive baud rates
- Software selectable word length (eight or nine bits)
- Separate transmitter and receiver enable bits
- Capable of being interrupt driven
- Transmitter clocks available without altering the regular transmitter or receiver functions
- Four separate enable bits for interrupt control



Note: The serial communications data register (SCI SCDR) is controlled by the internal R/$\overline{W}$ signal. It is the transmit data register when written to and the receive data register when read.

Figure 6-1 Serial communications interface block diagram

6.2 SCI receiver features

- Receiver wake-up function (idle line or address bit)
- Idle line detection
- Framing error detection
- Noise detection
- Overrun detection
- Receiver data register full flag

6.3 SCI transmitter features

- Transmit data register empty flag
- Transmit complete flag
- Send break

6.4 Functional description

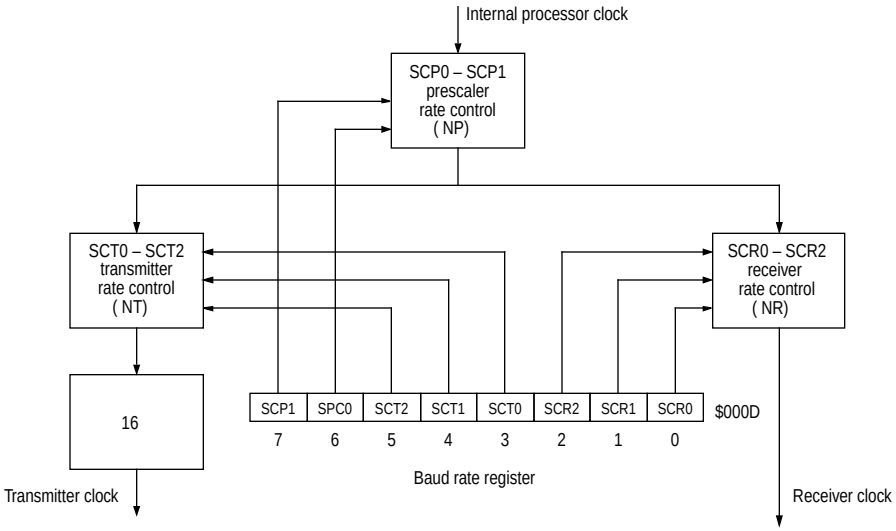
A block diagram of the SCI is shown in Figure 6-1. Option bits in serial control register1 (SCCR1) select the ‘wake-up’ method (WAKE bit) and data word length (M-bit) of the SCI. SCCR2 provides control bits that individually enable the transmitter and receiver, enable system interrupts and provide the wake-up enable bit (RWU) and the send break code bit (SBK). Control bits in the baud rate register (BAUD) allow the user to select one of 32 different baud rates for the transmitter and receiver (see Section 6.11.5).

Data transmission is initiated by writing to the serial communications data register (SCDR). Provided the transmitter is enabled, data stored in the SCDR is transferred to the transmit data shift register. This transfer of data sets the transmit data register empty flag (TDRE) in the SCI status register (SCSR) and generates an interrupt (if transmitter interrupts are enabled). The transfer of data to the transmit data shift register is synchronized with the bit rate clock (see Figure 6-2). All data is transmitted least significant bit first. Upon completion of data transmission, the transmission complete flag (TC) in the SCSR is set (provided no pending data, preamble or break is to be sent) and an interrupt is generated (if the transmit complete interrupt is enabled). If the transmitter is disabled, and the data, preamble or break (in the transmit data shift register) has been sent, the TC bit will also be set. This will also generate an interrupt if the transmission complete interrupt enable bit (TCIE) is set. If the transmitter is disabled during a transmission, the character being transmitted will be completed before the transmitter gives up control of the TDO pin.

When SCDR is read, it contains the last data byte received, provided that the receiver is enabled. The receive data register full flag bit (RDRF) in the SCSR is set to indicate that a data byte has been transferred from the input serial shift register to the SCDR; this will cause an interrupt if the receiver interrupt is enabled. The data transfer from the input serial shift register to the SCDR is synchronized by the receiver bit rate clock. The OR (overrun), NF (noise), or FE (framing) error flags in the SCSR may be set if data reception errors occurred.

An idle line interrupt is generated if the idle line interrupt is enabled and the IDLE bit (which detects idle line transmission) in SCSR is set. This allows a receiver that is not in the wake-up mode to detect the end of a message or the preamble of a new message, or to resynchronize with the transmitter. A valid character must be received before the idle line condition or the IDLE bit will not be set and idle line interrupt will not be generated.

The SCP0 and SCP1 bits function as a prescaler for SCR0–SCR2 to generate the receiver baud rate and for SCT0–SCT2 to generate the transmitter baud rate. Together, these eight bits provide multiple transmitter/receiver rate combinations for a given crystal frequency (see Figure 6-2). This register should only be written to while both the transmitter and receiver are disabled (TE=0, RE=0).



Note: There is a fixed rate divide-by-16 before the transmitter to compensate for the inherent divide-by-16 of the receiver (sampling). This means that by loading the same value for both the transmitter and receiver baud rate selector, the same baud rates can be obtained.

Figure 6-2 SCI rate generator division

6.5 Data format

Receive data or transmit data is the serial data that is transferred to the internal data bus from the receive data input pin (RDI) or from the internal bus to the transmit data output pin (TDO). The non-return-to-zero (NRZ) data format shown in Figure 6-3 is used and must meet the following criteria:

- The idle line is brought to a logic one state prior to transmission/reception of a character.
- A start bit (logic zero) is used to indicate the start of a frame.
- The data is transmitted and received least significant bit first.
- A stop bit (logic one) is used to indicate the end of a frame. A frame consists of a start bit, a character of eight or nine data bits, and a stop bit.
- A break is defined as the transmission or reception of a low (logic zero) for at least one complete frame time (10 zeros for 8-bit format, 11 zeros for 9-bit).

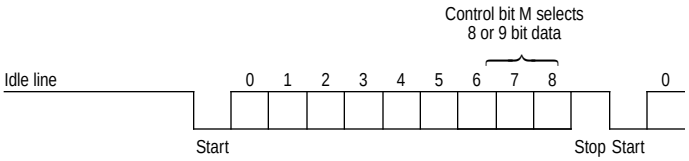


Figure 6-3 Data format

6.6 Receiver wake-up operation

The receiver logic hardware also supports a receiver wake-up function which is intended for systems having more than one receiver. With this function a transmitting device directs messages to an individual receiver or group of receivers by passing addressing information as the initial byte(s) of each message. The wake-up function allows receivers not addressed to remain in a dormant state for the remainder of the unwanted message. This eliminates any further software overhead to service the remaining characters of the unwanted message and thus improves system performance.

The receiver is placed in wake-up mode by setting the receiver wake-up bit (RWU) in the SCCR2 register. While RWU is set, all of the receiver related status flags (RDRF, IDLE, OR, NF, and FE) are inhibited (cannot become set). Note that the idle line detect function is inhibited while the RWU bit is set. Although RWU may be cleared by a software write to SCCR2, it would be unusual to do so. Normally RWU is set by software and is cleared automatically in hardware by one of the two methods described below.

6.6.1 Idle line wake-up

In idle line wake-up mode, a dormant receiver wakes up as soon as the RDI line becomes idle. Idle is defined as a continuous logic high level on the RDI line for ten (or eleven) full bit times. Systems using this type of wake-up must provide at least one character time of idle between messages to wake up sleeping receivers, but must not allow any idle time between characters within a message.

6.6.2 Address mark wake-up

In address mark wake-up, the most significant bit (MSB) in a character is used to indicate whether it is an address (1) or data (0) character. Sleeping receivers will wake up whenever an address character is received. Systems using this method for wake-up would set the MSB of the first character of each message and leave it clear for all other characters in the message. Idle periods may be present within messages and no idle time is required between messages for this wake-up method.

6.7 Receive data in (RDI)

Receive data is the serial data that is applied through the input line and the SCI to the internal bus. The receiver circuitry clocks the input at a rate equal to 16 times the baud rate. This time is referred to as the RT rate in Figure 6-4 and as the receiver clock in Figure 6-2.

The receiver clock generator is controlled by the baud rate register, as shown in Figure 6-1 and Figure 6-2; however, the SCI is synchronized by the start bit, independent of the transmitter.

Once a valid start bit is detected, the start bit, each data bit and the stop bit are sampled three times at RT intervals 8 RT, 9 RT and 10 RT (1 RT is the position where the bit is expected to start), as shown in Figure 6-5. The value of the bit is determined by voting logic which takes the value of the majority of the samples. A noise flag is set when all three samples on a valid start bit or data bit or the stop bit do not agree.

6.8 Start bit detection

When the input (idle) line is detected low, it is tested for three more sample times (referred to as the start edge verification samples in Figure 6-4). If at least two of these three verification samples detect a logic zero, a valid start bit has been detected, otherwise the line is assumed to be idle. A noise flag is set if one of the three verification samples detect a logic one, thus a valid start bit could be assumed with a set noise flag present.

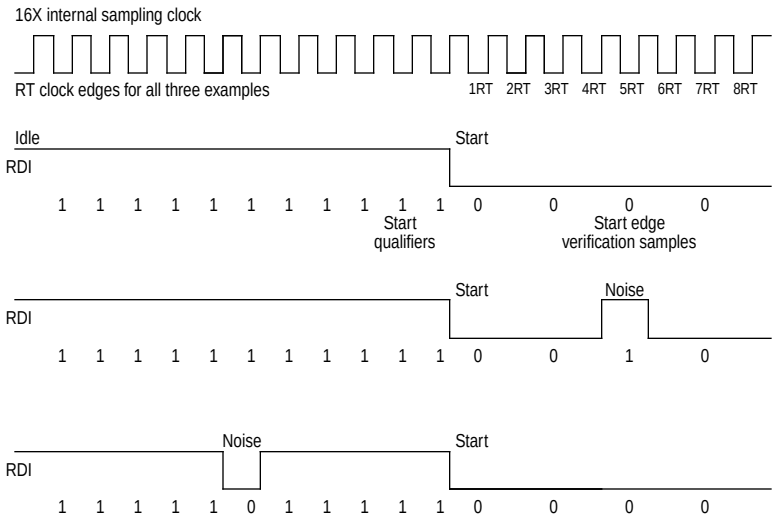


Figure 6-4 SCI examples of start bit sampling technique

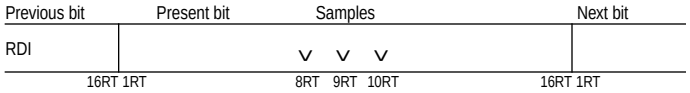
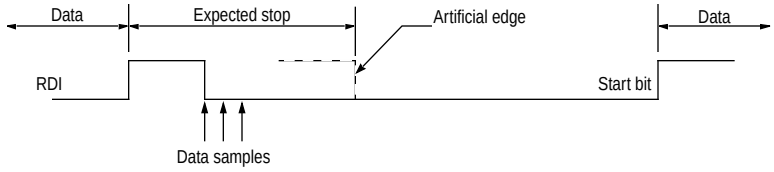


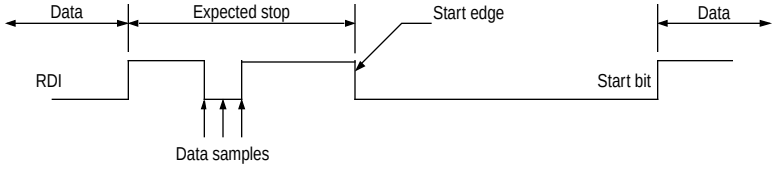
Figure 6-5 SCI sampling technique used on all bits

If there has been a framing error without detection of a break (10 zeros for 8 bit format or 11 zeros for 9 bit format), the circuit continues to operate as if there actually was a stop bit, and the start edge will be placed artificially. The last bit received in the data shift register is inverted to a logic one, and the three logic one start qualifiers (shown in Figure 6-4) are forced into the sample shift register during the interval when detection of a start bit is anticipated (see Figure 6-6); therefore, the start bit will be accepted no sooner than it is anticipated.

If the receiver detects that a break (RDRF = 1, FE = 1, receiver data register = $0000) produced the framing error, the start bit will not be artificially induced and the receiver must actually detect a logic one before the start bit can be recognised (see Figure 6-7).



a) Case 1: receive line low during artificial edge



b) Case 2: receive line high during expected start edge

Figure 6-6 Artificial start following a framing error

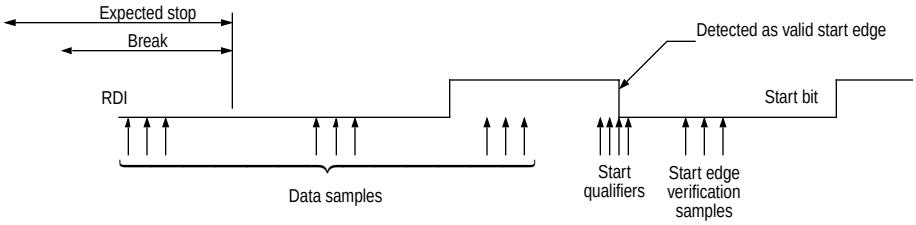


Figure 6-7 SCI start bit following a break

6.9 Transmit data out (TDO)

Transmit data is the serial data from the internal data bus that is applied through the SCI to the output line. Data format is as discussed in Section 6.5 and shown in Figure 6-3. The transmitter generates a bit time by using a derivative of the RT clock, thus producing a transmission rate equal to 1/16th that of the receiver sample clock (assuming the same baud rate is selected for both the receiver and transmitter).

6.10 SCI synchronous transmission

The SCI transmitter allows the user to control a one way synchronous serial transmission. The SCLK pin is the clock output of the SCI transmitter. No clocks are sent to that pin during start bit and stop bit. Depending on the state of the LBCL bit (bit 0 of SCCR1), clocks will or will not be activated during the last valid data bit (address mark). The CPOL bit (bit 2 of SCCR1) allows the user to select the clock polarity, and the CPHA bit (bit 1 of SCCR1) allows the user to select the phase of the external clock (see Figure 6-8, Figure 6-9 and Figure 6-10).

During idle, preamble and send break, the external SCLK clock is not activated.

These options allow the user to serially control peripherals which consist of shift registers, without losing any functions of the SCI transmitter which can still talk to other SCI receivers. These options do not affect the SCI receiver which is independent of the transmitter.

The SCLK pin works in conjunction with the TDO pin. When the SCI transmitter is disabled (TE = 0), the SCLK and TDO pins go to the high impedance state.

Note: The LBCL, CPOL and CPHA bits have to be selected before enabling the transmitter to ensure that the clocks function correctly. These bits should not be changed while the transmitter is enabled.

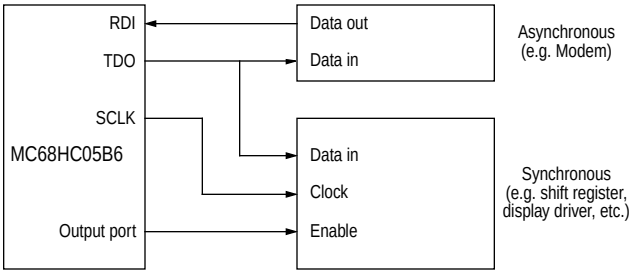


Figure 6-8 SCI example of synchronous and asynchronous transmission

6.11 SCI registers

The SCI system is configured and controlled by five registers: SCDR, SCCR1, SCCR2, SCSR, and BAUD.

6.11.1 Serial communications data register (SCDR)

	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
SCI data (SCDR)	$0011									0000 0000

The SCDR is controlled by the internal R/$\overline{W}$ signal and performs two functions in the SCI. It acts as the receive data register (RDR) when it is read and as the transmit data register (TDR) when it is written. Figure 6-1 shows this register as two separate registers, RDR and TDR. The RDR provides the interface from the receive shift register to the internal data bus and the TDR provides the parallel interface from the internal data bus to the transmit shift register.

The receive data register is a read-only register containing the last byte of data received from the shift register for the internal data bus. The RDR full bit (RDRF) in the serial communications status register is set to indicate that a byte has been transferred from the input serial shift register to the SCDR. The transfer is synchronized with the receiver bit rate clock (from the receiver control) as shown in Figure 6-1. All data is received with the least significant bit first.

The transmit data register (TDR) is a write-only register containing the next byte of data to be applied to the transmit shift register from the internal data bus. As long as the transmitter is enabled, data stored in the SCDR is transferred to the transmit shift register (after the current byte in the shift register has been transmitted).

The transfer is synchronized with the transmitter bit rate clock (from the transmitter control) as shown in Figure 6-1. All data is received with the least significant bit first.

6.11.2 Serial communications control register 1 (SCCR1)

	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
SCI control 1 (SCCR1)	$000E	R8	T8		M	WAKE	CPOL	CPHA	LBCL	Undefined

The SCI control register 1 (SCCR1) contains control bits related to the nine data bit character format, the receiver wake-up feature and the options to output the transmitter clocks for synchronous transmissions.

R8 — Receive data bit 8

This read-only bit is the ninth serial data bit received when the SCI system is configured for nine data bit operation (M = 1). The most significant bit (bit 8) of the received character is transferred into this bit at the same time as the remaining eight bits (bits 0–7) are transferred from the serial receive shifter to the SCI receive data register.

T8 — Transmit data bit 8

This read/write bit is the ninth data bit to be transmitted when the SCI system is configured for nine data bit operation (M = 1). When the eight low order bits (bits 0–7) of a transmit character are transferred from the SCI data register to the serial transmit shift register, this bit (bit 8) is transferred to the ninth bit position of the shifter.

M — Mode (select character format)

The read/write M-bit controls the character length for both the transmitter and receiver at the same time. The 9th data bit is most commonly used as an extra stop bit or in conjunction with the ‘address mark’ wake-up method. It can also be used as a parity bit (see Table 6-1).

1 (set) – Start bit, 8 data bits, 1 stop bit.

0 (clear) – Start bit, 9 data bits, 1 stop bit.

Table 6-1 Method of receiver wake-up

WAKE	M	Method of receiver wake-up
0	x	Detection of an idle line allows the next data type received to cause the receive data register to fill and produce an RDRF flag.
1	0	Detection of a received one in the eighth data bit allows an RDRF flag and associated error flags.
1	1	Detection of a received one in the ninth data bit allows an RDRF flag and associated error flags.

x = Don’t care

WAKE — Wake-up mode select

This bit allows the user to select the method for receiver wake-up. The WAKE bit can be read or written to any time. See Table 6-1.

1 (set) – Wake-up on address mark.

0 (clear) – Wake-up on idle line.

CPOL – Clock polarity

This bit allows the user to select the polarity of the clocks to be sent to the SCLK pin. It works in conjunction with the CPHA bit to produce the desired clock-data relation (see Figure 6-9 and Figure 6-10).

1 (set) – Steady high value at SCLK pin outside transmission window.

0 (clear) – Steady low value at SCLK pin outside transmission window.

This bit should not be manipulated while the transmitter is enabled.

CPHA – Clock phase

This bit allows the user to select the phase of the clocks to be sent to the SCLK pin. This bit works in conjunction with the CPOL bit to produce the desired clock-data relation (see Figure 6-9 and Figure 6-10).

1 (set) – SCLK clock line activated at beginning of data bit.

0 (clear) – SCLK clock line activated in middle of data bit.

This bit should not be manipulated while the transmitter is enabled.

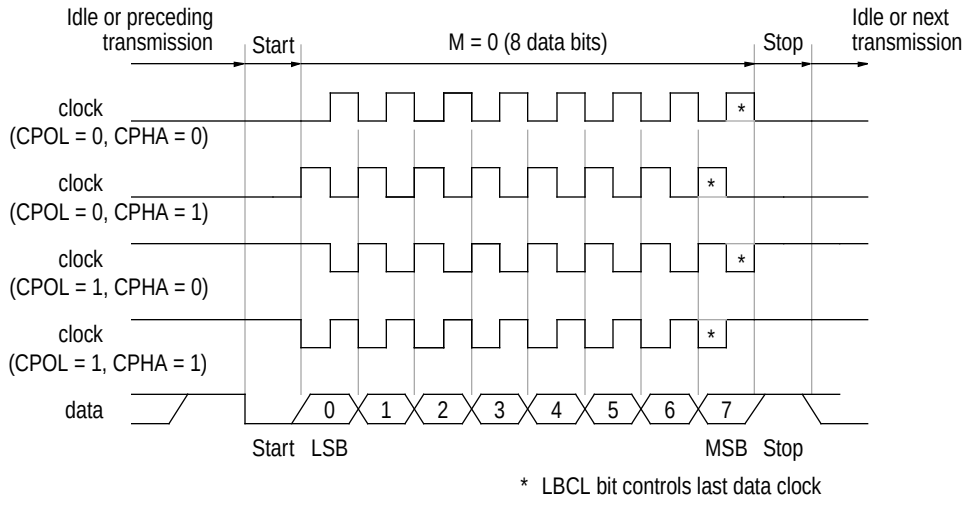


Figure 6-9 SCI data clock timing diagram (M=0)

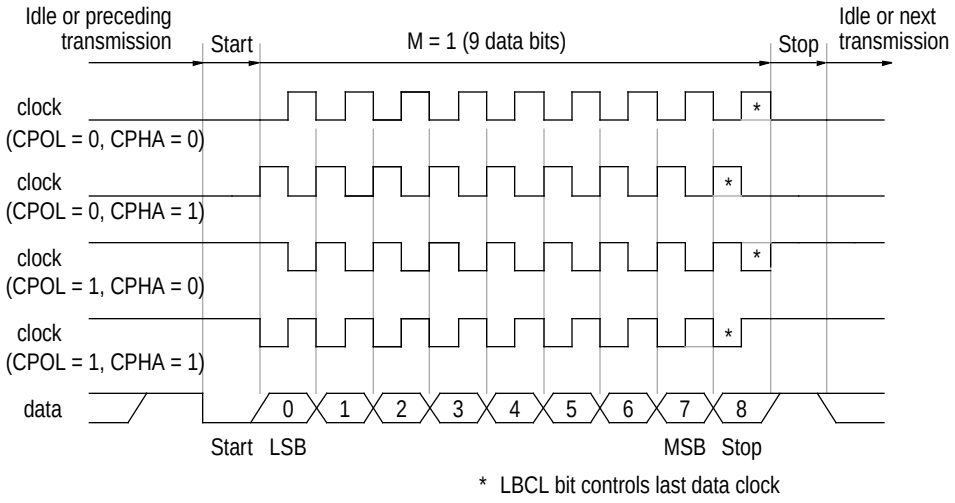


Figure 6-10 SCI data clock timing diagram (M=1)

LBCL – Last bit clock

This bit allows the user to select whether the clock associated with the last data bit transmitted (MSB) has to be output to the SCLK pin. The clock of the last data bit is output to the SCLK pin if the LBCL bit is a logic one, and is not output if it is a logic zero.

The last bit is the 8th or 9th data bit transmitted depending on the 8 or 9 bit format selected by M-bit (seeTable 6-2).

This bit should not be manipulated while the transmitter is enabled.

Table 6-2 SCI clock on SCLK pin

Data format	M-bit	LBCL bit	Number of clocks on SCLK pin
8 bit	0	0	7
8 bit	0	1	8
9 bit	1	0	8
9 bit	1	1	9

6.11.3 Serial communications control register 2 (SCCR2)

The SCI control register 2 (SCCR2) provides the control bits that enable/disable individual SCI functions.

	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
SCI control (SCCR2)	$000F	TIE	TCIE	RIE	ILIE	TE	RE	RWU	SBK	0000 0000

TIE — Transmit interrupt enable

1 (set) – TDRE interrupts enabled.

0 (clear) – TDRE interrupts disabled.

TCIE — Transmit complete interrupt enable

1 (set) – TC interrupts enabled.

0 (clear) – TC interrupts disabled.

RIE — Receiver interrupt enable

1 (set) – RDRF and OR interrupts enabled.

0 (clear) – RDRF and OR interrupts disabled.

ILIE — Idle line interrupt enable

1 (set) – IDLE interrupts enabled.

0 (clear) – IDLE interrupts disabled.

TE — Transmitter enable

When the transmit enable bit is set, the transmit shift register output is applied to the TDO line and the corresponding clocks are applied to the SCLK pin. Depending on the state of control bit M (SCCR1), a preamble of 10 (M = 0) or 11 (M = 1) consecutive ones is transmitted when software sets the TE bit from a cleared state.

If a transmission is in progress and a zero is written to TE, the transmitter will wait until after the present byte has been transmitted before placing the TDO and the SCLK pin in the idle, high impedance state.

If the TE bit has been written to a zero and then set to a one before the current byte is transmitted, the transmitter will wait for that byte to be transmitted and will then initiate transmission of a new preamble. After this latest transmission, and provided the TDRE bit is set (no new data to transmit), the line remains idle (driven high while TE = 1); otherwise, normal transmission occurs. This function allows the user to neatly terminate a transmission sequence.

After loading the last byte in the serial communications data register and receiving the TDRE flag, the user should clear TE. Transmission of the last byte will then be completed and the line will go idle.

1 (set) – Transmitter enabled.

0 (clear) – Transmitter disabled.

RE — Receiver enable

1 (set) – Receiver enabled.

0 (clear) – Receiver disabled.

When RE is clear (receiver disabled) all the status bits associated with the receiver (RDRF, IDLE, OR, NF and FE) are inhibited.

RWU — Receiver wake-up

When the receiver wake-up bit is set by the user software, it puts the receiver to sleep and enables the wake-up function. The type of wake-up mode for the receiver is determined by the WAKE bit discussed above (in the SCCR1). When the RWU bit is set, no status flags will be set. Flags which were set previously will not be cleared when RWU is set.

If the WAKE bit is cleared, RWU is cleared by the SCI logic after receiving 10 (M = 0) or 11 (M =1) consecutive ones. Under these conditions, RWU cannot be set if the line is idle. If the WAKE bit is set, RWU is cleared after receiving an address bit. The RDRF flag will then be set and the address byte stored in the receiver data register.

SBK — Send break

If the send break bit is toggled set and cleared, the transmitter sends 10 (M = 0) or 11 (M = 1) zeros and then reverts to idle sending data. If SBK remains set, the transmitter will continually send whole blocks of zeros (sets of 10 or 11) until cleared. At the completion of the break code, the transmitter sends at least one high bit to guarantee recognition of a valid start bit.

6.11.4 Serial communications status register (SCSR)

	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
SCI status (SCSR)	$0010	TDRE	TC	RDRF	IDLE	OR	NF	FE		1100 000u

The serial communications status register (SCSR) provides inputs to the interrupt logic circuits for generation of the SCI system interrupt. In addition, a noise flag bit and a framing error bit are also contained in the SCSR.

TDRE — Transmit data register empty flag

This bit is set when the contents of the transmit data register are transferred to the serial shift register. New data will not be transmitted unless the SCSR register is read before writing to the transmit data register to clear the TDRE flag.

If the TDRE bit is clear, this indicates that the transfer has not yet occurred and a write to the serial communications data register will overwrite the previous value. The TDRE bit is cleared by accessing the serial communications status register (with TDRE set) followed by writing to the serial communications data register.

TC — Transmit complete flag

This bit is set to indicate that the SCI transmitter has no meaningful information to transmit (no data in shifter, no preamble, no break). When TC is set the serial line will go idle (continuous MARK). The TC bit is cleared by accessing the serial communications data register (with TC set) followed by writing to the serial communications data register. It does not inhibit the transmitter function in any way.

RDRF — Receive data register full flag

This bit is set when the contents of the receiver serial shift register are transferred to the receiver data register.

If multiple errors are detected in any one received word, the NF and RDRF bits will be affected as appropriate during the same clock cycle. The RDRF bit is cleared when the serial communications status register is accessed (with RDRF set) followed by a read of the serial communications data register.

IDLE — Idle line detected flag

This bit is set when a receiver idle line is detected (the receipt of a minimum of ten/eleven consecutive “1”s). This bit will not be set by the idle line condition when the RWU bit is set. This allows a receiver that is not in the wake-up mode to detect the end of a message, detect the preamble of a new message or resynchronize with the transmitter. The IDLE bit is cleared by accessing the serial communications status register (with IDLE set) followed by a read of the serial communications data register. Once cleared, IDLE will not be set again until after RDRF has been set, (i.e. until after the line has been active and becomes idle again).

OR — Overrun error flag

This bit is set when a new byte is ready to be transferred from the receiver shift register to the receiver data register and the receive data register is already full (RDRF bit is set). Data transfer is inhibited until the RDRF bit is cleared. Data in the serial communications data register is valid in this case, but additional data received during an overrun condition (including the byte causing the overrun) will be lost.

The OR bit is cleared when the serial communications status register is accessed (with OR set) followed by a read of the serial communications data register.

NF — Noise error flag

This bit is set if there is noise on a ‘valid’ start bit, any of the data bits or on the stop bit. The NF bit is not set by noise on the idle line nor by invalid start bits. If there is noise, the NF bit is not set until the RDRF flag is set. Each data bit is sampled three times as described in Section 6.7.

The NF bit represents the status of the byte in the serial communications data register. For the byte being received (shifted in) there will be also a ‘working’ noise flag, the value of which will be transferred to the NF bit when the serial data is loaded into the serial communications data register. The NF bit does not generate an interrupt because the RDRF bit gets set with NF and can be used to generate the interrupt.

The NF bit is cleared when the serial communications status register is accessed (with NF set) followed by a read of the serial communications data register.

FE — Framing error flag

This bit is set when the word boundaries in the bit stream are not synchronized with the receiver bit counter (generated by the reception of a logic zero bit where a stop bit was expected). The FE bit reflects the status of the byte in the receive data register and the transfer from the receive shifter to the receive data register is inhibited by an overrun. The FE bit is set during the same cycle as the RDRF bit but does not get set in the case of an overrun (OR). The framing error flag inhibits further transfer of data into the receive data register until it is cleared.

The FE bit is cleared when the serial communications status register is accessed (with FE set) followed by a read of the serial communications data register.

6.11.5 Baud rate register (BAUD)

The baud rate register provides the means to select two different or equivalent baud rates for the transmitter and receiver.

	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
SCI baud rate (BAUD)	$000D	SCP1	SCP0	SCT2	SCT1	SCT0	SCR2	SCR1	SCR0	00uu uuuu

SCP1, SCP0 — Serial prescaler select bits

These read/write bits determine the prescale factor, NP, by which the internal processor clock is divided before it is applied to the transmitter and receiver rate control dividers, NT and NR. This common prescaled output is used as the input to a divider that is controlled by the SCR0–SCR2 bits for the SCI receiver, and by the SCT0–SCT2 bits for the transmitter.

Table 6-3 First prescaler stage

SCP1	SCP0	Prescaler division ratio (NP)
0	0	1
0	1	3
1	0	4
1	1	13

SCT2, SCT1,SCT0 — SCI rate select bits (transmitter)

These three read/write bits select the baud rates for the transmitter. The prescaler output is divided by the factors shown in Table 6-4.

Table 6-4 Second prescaler stage (transmitter)

SCT2	SCT1	SCT0	Transmitter division ratio (NT)
0	0	0	1
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	16
1	0	1	32
1	1	0	64
1	1	1	128

SCR2, SCR1, SCR0 — SCI rate select bits (receiver)

These three read/write bits select the baud rates for the receiver. The prescaler output described above is divided by the factors shown in Table 6-5.

Table 6-5 Second prescaler stage (receiver)

SCR2	SCR1	SCR0	Receiver division ratio (NR)
0	0	0	1
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	16
1	0	1	32
1	1	0	64
1	1	1	128

The following equations are used to calculate the receiver and transmitter baud rates:

$$\text{baudTx} = \frac{f_{osc}}{32 \bullet NP \bullet NT}$$

$$\text{baudRx} = \frac{f_{osc}}{32 \bullet NP \bullet NR}$$

where:

NP = prescaler divide ratio

NT = transmitter baud rate divide ratio

NR = receiver baud rate divide ratio

baudTx = transmitter baud rate

baudRx = receiver baud rate

f_{OSC} = oscillator frequency

6.12 Baud rate selection

The flexibility of the baud rate generator allows many different baud rates to be selected. A particular baud rate may be generated in several ways by manipulating the various prescaler and division ratio bits. Table 6-6 shows the baud rates that can be achieved, for five typical crystal frequencies. These are effectively the highest baud rates which can be achieved using a given crystal.

Table 6-6 SCI baud rate selection

							Crystal frequency – f_{osc} (MHz)				
SCP1	**SCP0**	**SCT/R2**	**SCT/R1**	**SCT/R0**	**NP**	**NT/NR**	**4.194304**	**4.00**	**2.4576**	**2.00**	**1.8432**
0	0	0	0	0	1	1	131072	125000	76800	62500	57600
0	0	0	0	1	1	2	65536	62500	38400	31250	28800
0	0	0	1	0	1	4	32768	31250	19200	15625	14400
0	0	0	1	1	1	8	16384	15625	9600	7813	7200
0	0	1	0	0	1	16	8192	7813	4800	3906	3600
0	0	1	0	1	1	32	4096	3906	2400	1953	1800
0	0	1	1	0	1	64	2048	1953	1200	977	900
0	0	1	1	1	1	128	1024	977	600	488	450
0	1	0	0	0	3	1	43691	41667	25600	20833	19200
0	1	0	0	1	3	2	21845	20833	12800	10417	9600
0	1	0	1	0	3	4	10923	10417	6400	5208	4800
0	1	0	1	1	3	8	5461	5208	3200	2604	2400
0	1	1	0	0	3	16	2731	2604	1600	1302	1200
0	1	1	0	1	3	32	1365	1302	800	651	600
0	1	1	1	0	3	64	683	651	400	326	300
0	1	1	1	1	3	128	341	326	200	163	150
1	0	0	0	0	4	1	32768	31250	19200	15625	14400
1	0	0	0	1	4	2	16384	15625	9600	7813	7200
1	0	0	1	0	4	4	8192	7813	4800	3906	3600
1	0	0	1	1	4	8	4096	3906	2400	1953	1800
1	0	1	0	0	4	16	2048	1953	1200	977	900
1	0	1	0	1	4	32	1024	977	600	488	450
1	0	1	1	0	4	64	512	488	300	244	225
1	0	1	1	1	4	128	256	244	150	122	113
1	1	0	0	0	13	1	10082	9615	5908	4808	4431
1	1	0	0	1	13	2	5041	4808	2954	2404	2215
1	1	0	1	0	13	4	2521	2404	1477	1202	1108
1	1	0	1	1	13	8	1260	1202	738	601	554
1	1	1	0	0	13	16	630	601	369	300	277
1	1	1	0	1	13	32	315	300	185	150	138
1	1	1	1	0	13	64	158	150	92	75	69
1	1	1	1	1	13	128	79	75	46	38	35

Note: The examples shown above do not apply when the part is operating in slow mode (see Section 2.4.3).

6.13 SCI during STOP mode

When the MCU enters STOP mode, the baud rate generator driving the receiver and transmitter is shut down. This stops all SCI activity. Both the receiver and the transmitter are unable to operate.

If the STOP instruction is executed during a transmitter transfer, that transfer is halted. When STOP mode is exited as a result of an external interrupt, that particular transmission resumes.

If the receiver is receiving data when the STOP instruction is executed, received data sampling is stopped (baud generator stops) and the rest of the data is lost.

Warning: For the above reasons, all SCI transactions should be in the idle state when the STOP instruction is executed.

6.14 SCI during WAIT mode

The SCI system is not affected by WAIT mode and continues normal operation. Any valid SCI interrupt will wake-up the system. If required, the SCI system can be disabled prior to entering WAIT mode by writing a zero to the transmitter and receiver enable bits in the serial communication control register 2 at $000F. This action will result in a reduction of power consumption during WAIT mode.

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7
PULSE LENGTH D/A CONVERTERS

The pulse length D/A converter (PLM) system works in conjunction with the timer to execute two 8-bit D/A conversions, with a choice of two repetition rates. (See Figure 7-1.)

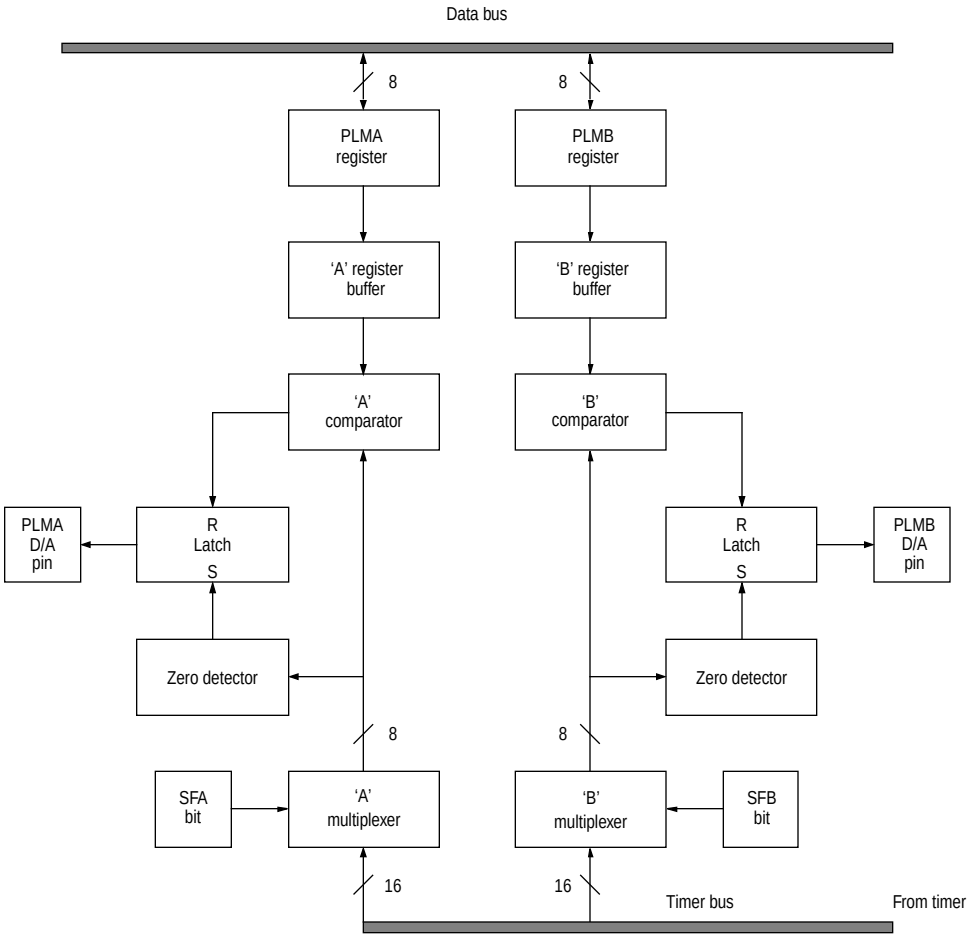


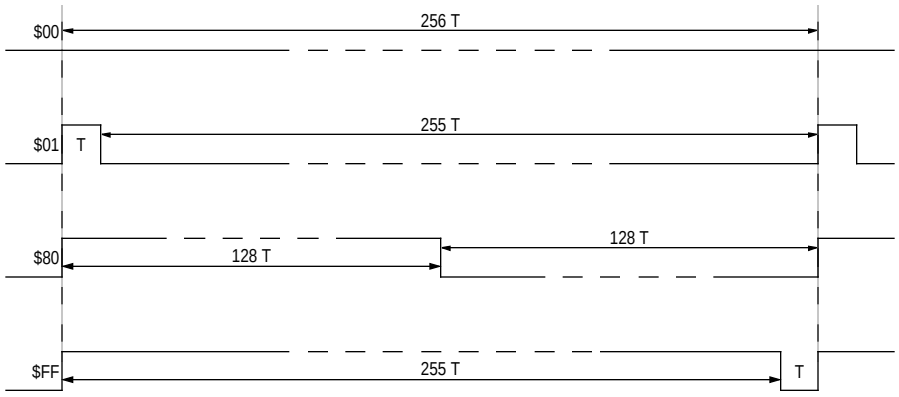
Figure 7-1 PLM system block diagram

The D/A converter has two data registers associated with it, PLMA and PLMB.

	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
Pulse length modulation A (PLMA)	$000A									0000 0000
Pulse length modulation B (PLMB)	$000B									0000 0000

This is a dual 8-bit resolution D/A converter associated with two output pins (PLMA and PLMB). The outputs are pulse length modulated signals whose duty cycle ratio may be modified. These signals can be used directly as PLMs, or the filtered average may be used as general purpose analog outputs.

The longest repetition period is 4096 times the programmable timer clock period (CPU clock multiplied by four), and the shortest repetition period is 256 times the programmable timer clock period (the repetition rate frequencies for a 4 MHz crystal are 122 Hz and 1953 Hz respectively). Registers PLMA ($0A) and PLMB ($0B) are associated with the pulse length values of the two counters. A value of $00 loaded into these registers results in a continuously low output on the corresponding D/A output pin. A value of $80 results in a 50% duty cycle output, and so on, to the maximum value $FF corresponding to an output which is at ‘1’ for 255/256 of the cycle. When the MCU makes a write to register PLMA or PLMB the new value will only be picked up by the D/A converters at the end of a complete cycle of conversion. This results in a monotonic change of the DC component at the output without overshoots or vicious starts (a vicious start is an output which gives totally erroneous PLM during the period immediately following an update of the PLM D/A registers). This feature is achieved by double buffering of the PLM D/A registers. Examples of PWM output waveforms are shown in Figure 7-2.



T = 4 CPU clocks in fast mode and 64 CPU clocks in slow mode

Figure 7-2 PLM output waveform examples

Note: Since the PLM system uses the timer counter, PLM results will be affected while resetting the timer counter. Both D/A registers are reset to $00 during power-on or external reset. WAIT mode does not affect the output waveform of the D/A converters.

7.1 Miscellaneous register

	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
Miscellaneous	$000C	POR	INTP	INTN	INTE	SFA	SFB	SM	WDOG	?001 000?

SFA — Slow or fast mode selection for PLMA

This bit allows the user to select the slow or fast mode of the PLMA pulse length modulation output.

1 (set) – Slow mode PLMA (4096 x timer clock period).

0 (clear) – Fast mode PLMA (256 x timer clock period).

SFB — Slow or fast mode selection for PLMB

This bit allows the user to select the slow or fast mode of the PLMB pulse length modulation output.

1 (set) – Slow mode PLMB (4096 x timer clock period).

0 (clear) – Fast mode PLMB (256 x timer clock period).

The highest speed of the PLM system corresponds to the frequency of the TOF bit being set, multiplied by 256. The lowest speed of the PLM system corresponds to the frequency of the TOF bit being set, multiplied by 16. Because the SFA bit and SFB bit are not double buffered, it is mandatory to set them to the desired values before writing to the PLM registers; not doing so could temporarily give incorrect values at the PLM outputs.

SM — Slow mode

1 (set) – The system runs at a bus speed 16 times lower than normal (f_{OSC}/32). SLOW mode affects all sections of the device, including SCI, A/D and timer.

0 (clear) – The system runs at normal bus speed (f_{OSC}/2).

The SM bit is cleared by external or power-on reset. The SM bit is automatically cleared when entering STOP mode.

Note: The bits that are shown shaded in the above representation are explained individually in the relevant sections of this manual. The complete register plus an explanation of each bit can be found in Section 3.8

7.2 PLM clock selection

The slow/fast mode of the PLM D/A converters is selected by bits 1, 2, and 3 of the miscellaneous register at address $000C (SFA bit for PLMA and SFB bit for PLMB). The slow/fast mode has no effect on the D/A converters' 8-bit resolution (see Figure 7-3).

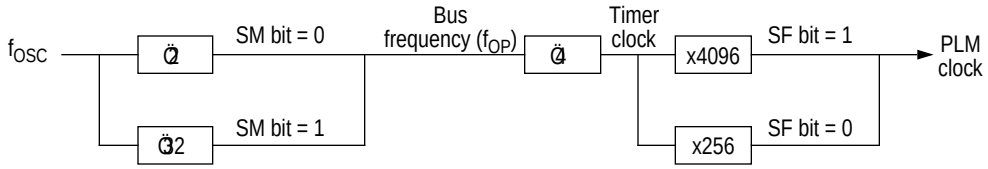


Figure 7-3 PLM clock selection

7.3 PLM during STOP mode

On entering STOP mode, the PLM outputs remain at their particular level. When STOP mode is exited by an interrupt, the PLM systems resume regular operation. If STOP mode is exited by power-on or external reset the registers values are forced to $00.

7.4 PLM during WAIT mode

The PLM system is not affected by WAIT mode and continues normal operation.

8
ANALOG TO DIGITAL CONVERTER

The analog to digital converter system consists of a single 8-bit successive approximation converter and a sixteen channel multiplexer. Eight of the channels are connected to the PD0/AN0 – PD7/AN7 pins of the MC68HC05B6 and the other eight channels are dedicated to internal reference points for test functions. The channel input pins do not have any internal output driver circuitry connected to them because such circuitry would load the analog input signals due to output buffer leakage current. There is one 8-bit result data register (address $08) and one 8-bit status/control register (address $09).

The A/D converter is ratiometric and two dedicated pins, VRH and VRL, are used to supply the reference voltage levels for all analog inputs. These pins are used in preference to the system power supply lines because any voltage drops in the bonding wires of the heavily loaded supply pins could degrade the accuracy of the A/D conversion. An input voltage equal to or greater than V_{RH} converts to $FF (full scale) with no overflow indication and an input voltage equal to V_{RL} converts to $00.

The A/D converter can operate from either the bus clock or an internal RC type oscillator. The internal RC type oscillator is activated by the ADRC bit in the A/D status/control register (ADSTAT) and can be used to give a sufficiently high clock rate to the A/D converter when the bus speed is too low to provide accurate results. When the A/D converter is not being used it can be disconnected, by clearing the ADON bit in the ADSTAT register, in order to save power (see Section 8.2.3).

For further information on A/D converter operation please refer to the M68HC11 Reference Manual — M68HC11RM/AD.

8.1 A/D converter operation

The A/D converter consists of an analog multiplexer, an 8-bit digital to analog converter capacitor array, a comparator and a successive approximation register (SAR) (see Figure 8-1).

There are eleven options that can be selected by the multiplexer; AN0–AN7, VRH, (VRH+VRL)/2 or VRL. Selection is done via the CHx bits in the ADSTAT register (see Section 8.2.3). AN0–AN7 are the only input points for A/D conversion operations; the others are reference points that can be used for test purposes.

The A/D reference input (AN0–AN7) is applied to a precision internal D/A converter. Control logic drives this D/A converter and the analog output is successively compared with the analog input sampled at the beginning of the conversion. The conversion is monotonic with no missing codes.

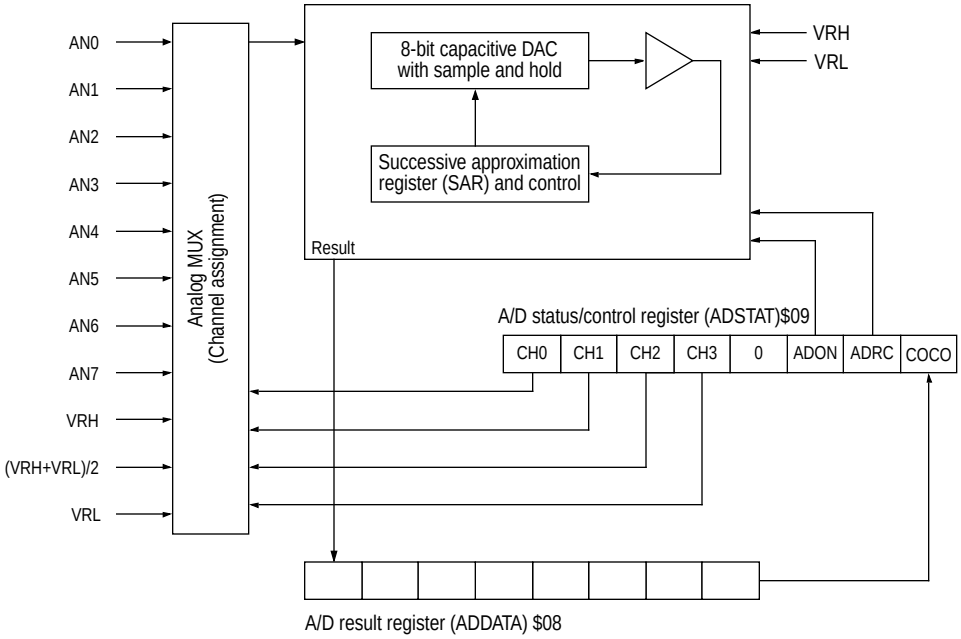


Figure 8-1 A/D converter block diagram

The result of each successive comparison is stored in the SAR and, when the conversion is complete, the contents of the SAR are transferred to the read-only result data register ($08), and the conversion complete flag, COCO, is set in the A/D status/control register ($09).

Warning: Any write to the A/D status/control register will abort the current conversion, reset the conversion complete flag and start a new conversion on the selected channel.

At power-on or external reset, both the ADRC and ADON bits are cleared; thus the A/D is disabled.

8.2 A/D registers

8.2.1 Port D data register (PORTD)

	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
Port D data (PORTD)	$0003	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0	Undefined

Port D is an input-only port which routes the eight analog inputs to the A/D converter. When the A/D converter is disabled, the pins are configured as standard input-only port pins, which can be read via the port D data register.

Note: When the A/D function is enabled, pins PD0–PD7 will act as analog inputs. Using a pin or pins as A/D inputs does not affect the ability to read port D as static inputs; however, reading port D during an A/D conversion sequence may inject noise on the analog inputs and result in reduced accuracy of the A/D result.
Performing a digital read of port D with levels other than V_{DD} or V_{SS} on the pins will result in greater power dissipation during the read cycle, and may give unpredictable results on the corresponding port D pins.

8.2.2 A/D result data register (ADDATA)

	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
A/D data (ADDATA)	$0008									0000 0000

ADDATA is a read-only register which is used to store the results of A/D conversions. Each result is loaded into the register from the SAR and the conversion complete flag, COCO, in the ADSTAT register is set.

8.2.3 A/D status/control register (ADSTAT)

	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
A/D status/control (ADSTAT)	$0009	COCO	ADRC	ADON	0	CH3	CH2	CH1	CH0	0000 0000

COCO — Conversion complete flag

1 (set) – COCO is set each time a conversion is complete, allowing the new result to be read from the A/D result data register ($08). The converter then starts a new conversion.

0 (clear) – COCO is cleared by reading the result data register or writing to the status/control register.

Reset clears the COCO flag.

ADRC — A/D RC oscillator control

The ADRC bit allows the user to control the A/D RC oscillator, which is used to provide a sufficiently high clock rate to the A/D to ensure accuracy when the chip is running at low speeds.

1 (set) – When the ADRC bit is set, the A/D RC oscillator is turned on and, if ADON is set, the A/D runs from the RC oscillator clock. See Table 8-1.

0 (clear) – When the ADRC bit is cleared, the A/D RC oscillator is turned-off and, if ADON is set, the A/D runs from the CPU clock.

When the A/D RC oscillator is turned on, it takes a time t_{ADRC} to stabilize (see Table 11-7 and Table 11-8). During this time A/D conversion results may be inaccurate.

Note: If the MCU bus clock falls below 1MHz, the A/D RC oscillator should be switched on.

Power-on or external reset clears the ADRC bit.

Table 8-1 A/D clock selection

ADRC	ADON	RC oscillator	A/D converter	Comments
0	0	OFF	OFF	A/D switched off.
0	1	OFF	ON	A/D using CPU clock.
1	0	ON	OFF	Allows the RC oscillator to stabilize.
1	1	ON	ON	A/D using RC oscillator clock.

ADON — A/D converter on

The ADON bit allows the user to enable/disable the A/D converter.

1 (set) – A/D converter is switched on.

0 (clear) – A/D converter is switched off.

When the A/D converter is switched on, it takes a time t_{ADON} for the current sources to stabilize (see Table 11-7 and Table 11-8). During this time A/D conversion results may be inaccurate.

Power-on or external reset will clear the ADON bit, thus disabling the A/D converter.

CH3–CH0 — A/D channels 3, 2, 1 and 0

The CH3–CH0 bits allow the user to determine which channel of the A/D converter multiplexer is selected. See Table 8-2 for channel selection.

Reset clears the CH0–CH3 bits.

Table 8-2 A/D channel assignment

CH3	CH2	CH1	CH0	Channel selected
0	0	0	0	AN0
0	0	0	1	AN1
0	0	1	0	AN2
0	0	1	1	AN3
0	1	0	0	AN4
0	1	0	1	AN5
0	1	1	0	AN6
0	1	1	1	AN7
1	0	0	0	VRH pin (high)
1	0	0	1	(VRH + VRL) / 2
1	0	1	0	VRL pin (low)
1	0	1	1	VRL pin (low)
1	1	0	0	VRL pin (low)
1	1	0	1	VRL pin (low)
1	1	1	0	VRL pin (low)
1	1	1	1	VRL pin (low)

8.3 A/D converter during STOP mode

When the MCU enters STOP mode with the A/D converter turned on, the A/D clocks are stopped and the A/D converter is disabled for the duration of STOP mode, including the 4064 cycles start-up time. If the A/D RC oscillator is in operation it will also be disabled.

8.4 A/D converter during WAIT mode

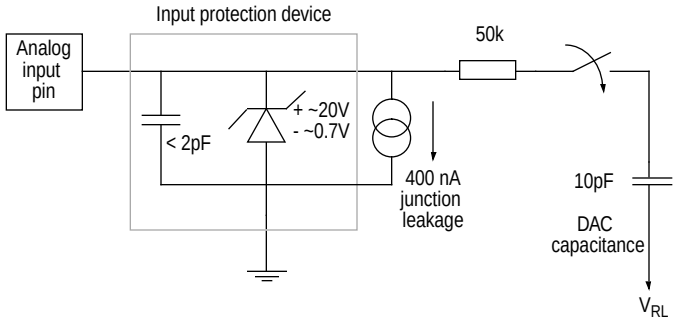
The A/D converter is not affected by WAIT mode and continues normal operation.

In order to reduce power consumption the A/D converter can be disconnected, under software control using the ADON bit and the ADRC bit in the A/D status/control register at $0009, before entering WAIT mode.

8.5 Port D analog input

The external analog voltage value to be processed by the A/D converter is sampled on an internal capacitor through a resistive path, provided by input-selection switches and a sampling aperture time switch, as shown in Figure 8-2. Sampling time is limited to 12 bus clock cycles. After sampling, the analog value is stored on the capacitor and held until the end of conversion. During this hold time, the analog input is disconnected from the internal A/D system and the external voltage source sees a high impedance input.

The equivalent analog input during sampling is an RC low-pass filter with a minimum resistance of 50 k and a capacitance of at least 10pF. It should be noted that these are typical values measured at room temperature.



Note: The analog switch is closed during the 12 cycle sample time only.

Figure 8-2 Electrical model of an A/D input pin

9
RESETS AND INTERRUPTS

9.1 Resets

The MC68HC05B6 can be reset in three ways: by the initial power-on reset function, by an active low input to the $\overline{\text{RESET}}$ pin or by a computer operating properly (COP) watchdog reset. Any of these resets will cause the program to go to its starting address, specified by the contents of memory locations $1FFE and $1FFF, and cause the interrupt mask bit in the condition code register to be set.

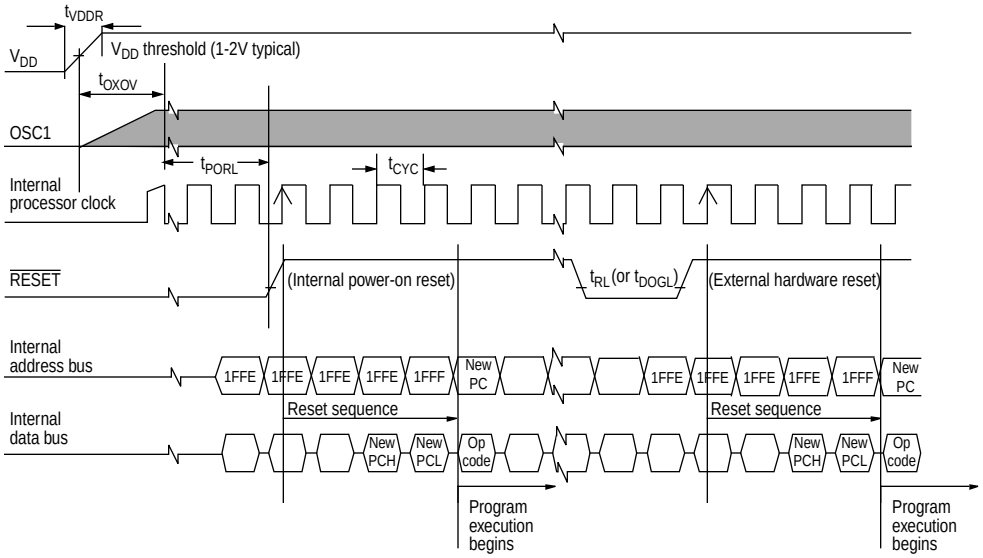


Figure 9-1 Reset timing diagram

9.1.1 Power-on reset

A power-on reset occurs when a positive transition is detected on VDD. The power-on reset function is strictly for power turn-on conditions and should not be used to detect drops in the power supply voltage. The power-on circuitry provides a stabilization delay (t_{PORL}) from when the oscillator becomes active. If the external $\overline{\text{RESET}}$ pin is low at the end of this delay then the processor remains in the reset state until $\overline{\text{RESET}}$ goes high. The user must ensure that the voltage on VDD has risen to a point where the MCU can operate properly by the time t_{PORL} has elapsed. If there is doubt, the external $\overline{\text{RESET}}$ pin should remain low until the voltage on VDD has reached the specified minimum operating voltage. This may be accomplished by connecting an external RC circuit to this pin to generate a power-on reset (POR). In this case, the time constant must be great enough to allow the oscillator circuit to stabilize.

During power-on reset, the $\overline{\text{RESET}}$ pin is driven low during a t_{PORL} delay start-up sequence. t_{PORL} is defined by a user specified mask option to be either 16 cycles or 4064 cycles (see Section 1.2).

A software distinction between a power-on reset and an external reset can be made using the POR bit in the miscellaneous register (see Section 9.1.2).

9.1.2 Miscellaneous register

	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
Miscellaneous	$000C	POR(1)	INTP	INTN	INTE	SFA	SFB	SM	WDOG(2)	?001 000?

(1) The POR bit is set each time there is a power-on reset.

(2) The state of the WDOG bit after reset is dependent on the mask option selected; 1=watchdog enabled, 0=watchdog disabled.

POR — Power-on reset bit

This bit is set each time the device is powered on. Therefore, the state of the POR bit allows the user to make a software distinction between a power-on and an external reset. This bit cannot be set by software and is cleared by writing it to zero.

1 (set) – A power-on reset has occurred.

0 (clear) – No power-on reset has occurred.

Note: The bits shown shaded in the above representation are explained individually in the relevant sections of this manual. The complete register plus an explanation of each bit can be found in Section 3.8.

9.1.3 $\overline{\text{RESET}}$ pin

When the oscillator is running in a stable condition, the MCU is reset when a logic zero is applied to the $\overline{\text{RESET}}$ input for a minimum period of 1.5 machine cycles (t_{CYC}). An internal Schmitt Trigger is used to improve noise immunity on this pin. When the $\overline{\text{RESET}}$ pin goes high, the MCU will resume operation on the following cycle. When a reset condition occurs internally, i.e. from POR or the COP watchdog, the $\overline{\text{RESET}}$ pin provides an active-low open drain output signal which may be used to reset external hardware. Current limitation to protect the pull-down device is provided in case an RC type external reset circuit is used.

9.1.4 Computer operating properly (COP) watchdog reset

The watchdog counter system consists of a divide-by-8 counter, preceded by a fixed divide-by-4 and a fixed divide-by-256 prescaler, plus control logic as shown in Figure 9-2. The divide-by-8 counter can be reset by software.

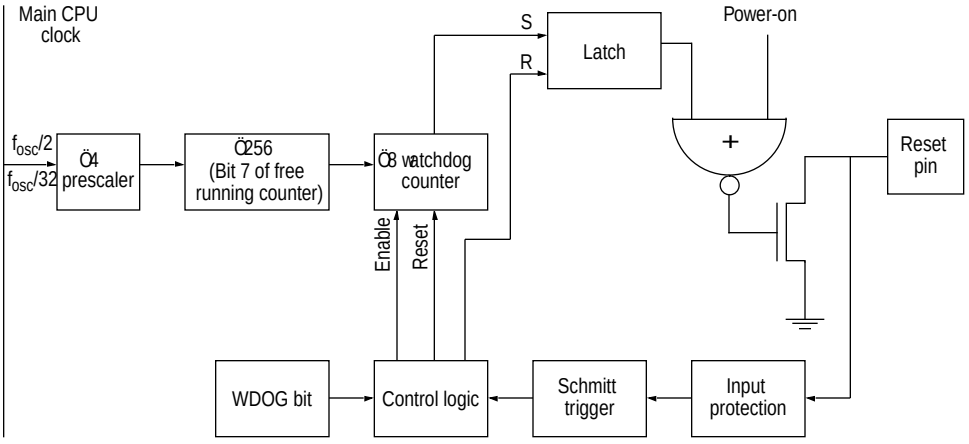


Figure 9-2 Watchdog system block diagram

Warning: The input to the watchdog system is derived from the carry output of bit 7 of the free running timer counter. Therefore, a reset of the timer may affect the period of the watchdog timeout.

The watchdog system can be automatically enabled, following power-on or external reset, via a mask option (see Section 1.2), or it can be enabled by software by writing a '1' to the WDOG bit in the miscellaneous register at $000C (see Section 9.1.2). Once enabled, the watchdog system

cannot be disabled by software (writing a ‘zero’ to the WDOG bit has no effect at any time). In addition, the WDOG bit acts as a reset mechanism for the watchdog counter. Writing a ‘1’ to this bit clears the counter to its initial value and prevents a watchdog timeout.

WDOG — Watchdog enable/disable

The WDOG bit can be used to enable the watchdog timer previously disabled by a mask option. Following a watchdog reset the state of the WDOG bit is as defined by the mask option specified.

1 (set) – Watchdog enabled and counter cleared.

0 (clear) – The watchdog cannot be disabled by software; writing a zero to this bit has no effect.

The divide-by-8 watchdog counter will generate a main reset of the chip when it reaches its final state; seven clocks are necessary to bring the watchdog counter from its clear state to its final state. This reset appears after time t_{DOG} since the last clear or since the enable of the watchdog counter system. The watchdog counter, therefore, has to be cleared periodically, by software, with a period less than t_{DOG}.

The reset generated by the watchdog system is apparent at the $\overline{\text{RESET}}$ pin (see Figure 9-2). The $\overline{\text{RESET}}$ pin level is re-entered in the control logic, and when it has been maintained at level ‘zero’ for a minimum of t_{DOGL}, the $\overline{\text{RESET}}$ pin is released.

9.1.4.1 COP watchdog during STOP mode

The STOP instruction is inhibited when the watchdog system is enabled. If a STOP instruction is executed while the watchdog system is enabled, then a watchdog reset will occur as if there were a watchdog timeout. In the case of a watchdog reset due to a STOP instruction, the oscillator will not be affected, thus there will be no t_{PORL} cycles start-up delay. On start-up, the watchdog will be configured according to the user specified mask option.

9.1.4.2 COP watchdog during WAIT mode

The state of the watchdog during WAIT mode is selected via a mask option (see Section 1.2) to be one of the options below:

Watchdog enabled — the watchdog counter will continue to operate during WAIT mode and a reset will occur after time t_{DOG}.

Watchdog disabled — on entering WAIT mode, the watchdog counter system is reset and disabled. On exiting WAIT mode the counter resumes normal operation.

9.1.5 Functions affected by reset

When processing stops within the MCU for any reason, i.e. power-on reset, external reset or the execution of a STOP or WAIT instruction, various internal functions of the MCU are affected. Table 9-1 shows the resulting action of any type of system reset, but not necessarily in the order in which they occur.

Table 9-1 Effect of $\overline{\text{RESET}}$, POR, STOP and WAIT

Function/effect	$\overline{\text{RESET}}$	POR	WAIT	STOP
Timer prescaler set to zero	x	x	–	–
Timer counter set to $FFFC	x	x	–	–
All timer enable bits cleared (disable)	x	x	–	–
Data direction registers cleared (inputs)	x	x	–	–
Stack pointer set to $00FF	x	x	–	–
Force internal address bus to restart	x	x	–	–
Vector $1FFE, $1FFF	x	x	–	–
Interrupt mask bit (I-bit CCR) set to 1	x	x	–	–
Interrupt mask bit (I-bit CCR) cleared	–	–	x	x
Set interrupt enable bit (INTE)	x	x	–	–
Set POR bit in miscellaneous register	–	x	–	–
Reset STOP latch	x	x	–	–
Reset $\overline{\text{IRQ}}$ latch	x	x	–	–
Reset WAIT latch	x	x	–	–
SCI disabled	x	x	–	–
SCI status bits cleared (except TDRE and TC)	x	x	–	–
SCI interrupt enable bits cleared	x	x	–	–
SCI status bits TDRE and TC set	x	x	–	–
Oscillator disabled for 4064 cycles	–	x	–	x
Timer clock cleared	–	x	–	x
SCI clock cleared	–	x	–	x
A/D disabled	x	x	–	x
SM bit in the miscellaneous register cleared	x	x	–	x
Watchdog counter reset	x	x	x	x
WDOG bit in the miscellaneous register reset	x	x	–	x
EEPROM control bits (see Section 3.5.1)	x	x	–	x

x = Described action takes place

– = Described action does not take place

9.2 Interrupts

The MCU can be interrupted by four different sources: three maskable hardware interrupts and one non maskable software interrupt:

- External signal on the $\overline{\text{IRQ}}$ pin
- Serial communications interface (SCI)
- Programmable timer
- Software interrupt instruction (SWI)

Interrupts cause the processor to save the register contents on the stack and to set the interrupt mask (I-bit) to prevent additional interrupts. The RTI instruction (ReTurn from Interrupt) causes the register contents to be recovered from the stack and normal processing to resume. While executing the RTI instruction, the value of the I-bit is replaced by the corresponding I-bit stored on the stack.

Unlike reset, hardware interrupts do not cause the current instruction execution to be halted, but are considered pending until the current instruction is complete. The current instruction is the one already fetched and being operated on. When the current instruction is complete, the processor checks all pending hardware interrupts. If interrupts are not masked (I-bit clear) and the corresponding interrupt enable bit is set, the processor proceeds with interrupt processing; otherwise, the next instruction is fetched and executed.

Note: Power-on and external reset clear all interrupt enable bits, but set the INTE bit in the miscellaneous register, thus preventing interrupts during the reset sequence.

9.2.1 Interrupt priorities

Each potential interrupt source is assigned a priority level, which means that if more than one interrupt is pending at the same time, the processor will service the one with the highest priority first. For example, if both an external interrupt and a timer interrupt are pending after an instruction execution, the external interrupt is serviced first.

Table 9-2 shows the relative priority of all the possible interrupt sources. Figure 9-3 shows the interrupt processing flow.

9.2.2 Nonmaskable software interrupt (SWI)

The software interrupt (SWI) is an executable instruction and a nonmaskable interrupt: it is executed regardless of the state of the I-bit in the CCR. If the I-bit is zero (interrupts enabled), SWI is executed after interrupts that were pending when the SWI was fetched, but before interrupts

Table 9-2 Interrupt priorities

Source	Register	Flags	Vector address	Priority
Reset	—	—	$1FFE, $1FFF	highest
Software interrupt (SWI)	—	—	$1FFC, $1FFD	
External interrupt ($\overline{IRQ}$)	—	—	$1FFA, $1FFB	
Timer input captures	TSR	ICF1, ICF2	$1FF8, $1FF9	
Timer output compares	TSR	OCF1, OCF2	$1FF6, $1FF7	
Timer overflow	TSR	TOF	$1FF4, $1FF5	
Serial communications interface (SCI)	SCSR	TDRE, TC, OR, RDRF, IDLE	$1FF2, $1FF3	lowest

generated after the SWI was fetched. The SWI interrupt service routine address is specified by the contents of memory locations $1FFC and $1FFD.

9.2.3 Maskable hardware interrupts

If the interrupt mask bit in the CCR is set, all maskable interrupts (internal and external) are masked. Clearing the I-bit allows interrupt processing to occur.

Note: The internal interrupt latch is cleared in the first part of the interrupt service routine; therefore, one external interrupt pulse could be latched and serviced as soon as the I-bit is cleared.

9

9.2.3.1 External interrupt ($\overline{IRQ}$)

If the interrupt mask in the condition code register has been cleared and the interrupt enable bit (INTE) is set and the signal on the external interrupt pin ($\overline{IRQ}$) satisfies the condition selected by the option control bits (INTP and INTN), then the external interrupt is recognized. INTE, INTP and INTN are all bits contained in the miscellaneous register at $000C. When the interrupt is recognized, the current state of the CPU is pushed onto the stack and the I-bit is set. This masks further interrupts until the present one is serviced. The external interrupt service routine address is specified by the content of memory locations $1FFA and $1FFB.

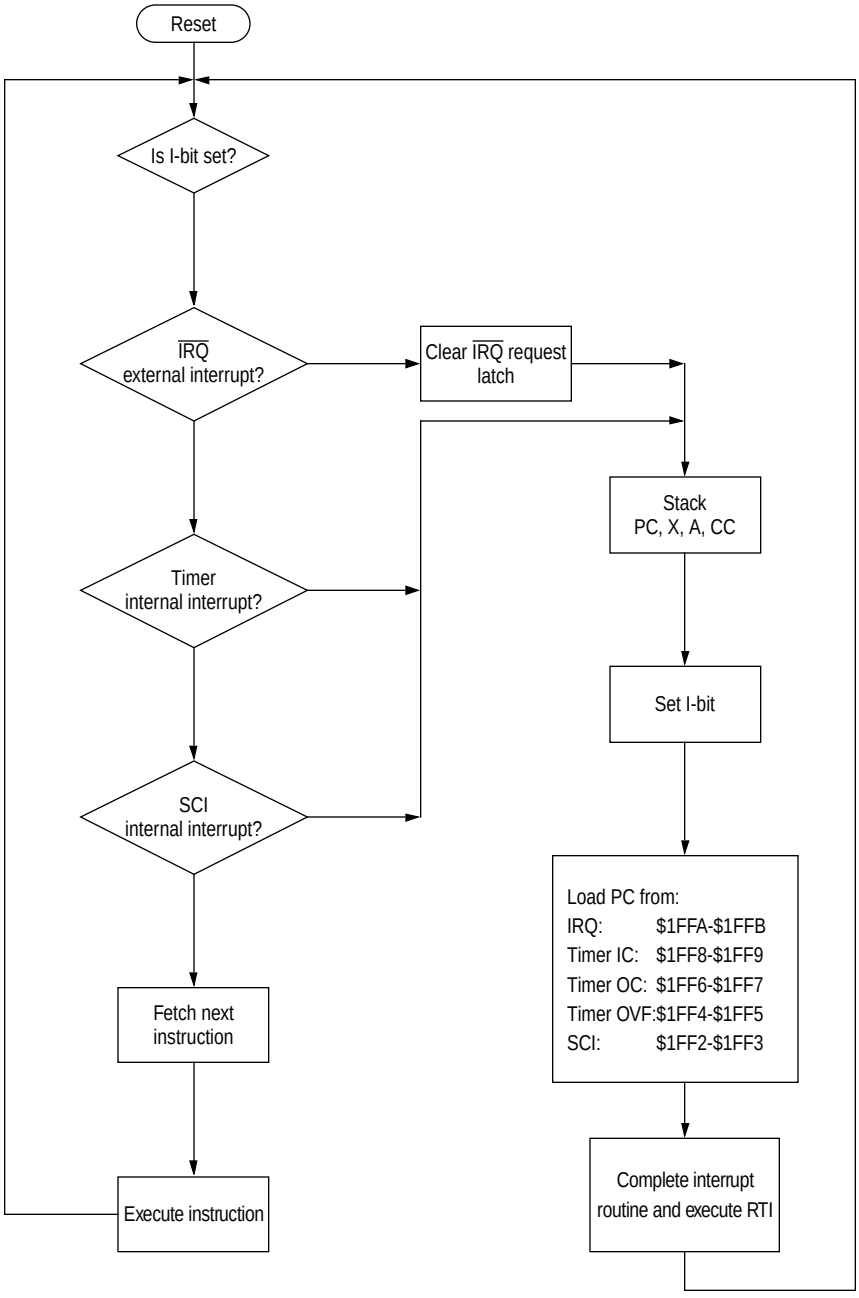


Figure 9-3 Interrupt flow chart

9.2.3.2 Miscellaneous register

	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
Miscellaneous	$000C	POR	INTP	INTN	INTE	SFA	SFB	SM	WDOG	?001 000?

Note: The bits shown shaded in the above representation are explained individually in the relevant sections of this manual. The complete register plus an explanation of each bit can be found in Section 3.8.

INTP, INTN — External interrupt sensitivity options

These two bits allow the user to select which edge the $\overline{IRQ}$ pin is sensitive to as shown in Table 9-3. Both bits can be written to only while the I-bit is set, and are cleared by power-on or external reset. Therefore the device is initialised with negative edge and low level sensitivity.

Table 9-3 $\overline{IRQ}$ sensitivity

INTP	INTN	$\overline{IRQ}$ sensitivity
0	0	Negative edge and low level sensitive
0	1	Negative edge only
1	0	Positive edge only
1	1	Positive and negative edge sensitive

INTE — External interrupt enable

1 (set) – External interrupt function ($\overline{IRQ}$) enabled.

0 (clear) – External interrupt function ($\overline{IRQ}$) disabled.

The INTE bit can be written to only while the I-bit is set, and is set by power-on or external reset, thus enabling the external interrupt function.

Table 9-3 describes the various triggering options available for the $\overline{IRQ}$ pin, however it is important to re-emphasize here that in order to avoid any conflict and spurious interrupt, it is only possible to change the external interrupt options while the I-bit is set. Any attempt to change the external interrupt option while the I-bit is clear will be unsuccessful. If an external interrupt is pending, it will automatically be cleared when selecting a different interrupt option.

Note: If the external interrupt function is disabled by the INTE bit and an external interrupt is sensed by the edge detector circuitry, then the interrupt request is latched and the interrupt stays pending until the INTE bit is set. The internal latch of the external interrupt is cleared in the first part of the service routine (except for the low level

interrupt which is not latched); therefore, only one external interrupt pulse can be latched during t_{ILIL} and serviced as soon as the I-bit is cleared.

9.2.3.3 Timer interrupts

There are five different timer interrupt flags (ICF1, ICF2, OCF1, OCF2 and TOF) that will cause a timer interrupt whenever they are set and enabled. These five interrupt flags are found in the five most significant bits of the timer status register (TSR) at location $0013. ICF1 and ICF2 will vector to the service routine defined by $1FF8-$1FF9, OCF1 and OCF2 will vector to the service routine defined by $1FF6–$1FF7 and TOF will vector to the service routine defined by $1FF4–$1FF5 as shown in Figure 5-1.

There are three corresponding enable bits; ICIE for ICF1 and ICF2, OCIE for OCF1 and OCF2, and TOIE for TOF. These enable bits are located in the timer control register (TCR) at address $0012. See Section 5.2.1 and Section 5.2.2 for further information.

9.2.3.4 Serial communications interface (SCI) interrupts

There are five different interrupt flags (TDRE, TC, OR, RDRF and IDLE) that cause SCI interrupts whenever they are set and enabled. These five interrupt flags are found in the five most significant bits of the SCI status register (SCSR) at location $0010.

There are four corresponding enable bits: TIE for TDRE, TCIE for TC, RIE for OR and RDRF, and ILIE for IDLE. These enable bits are located in the serial communications control register 2 (SCCR2) at address $000F. See Section 6.11.3 and Section 6.11.4.

The SCI interrupt causes the program counter to vector to the address pointed to by memory locations $1FF2 and $1FF3 which contain the starting address of the interrupt service routine. Software in the SCI interrupt service routine must determine the priority and cause of the interrupt by examining the interrupt flags and the status bits located in the serial communications status register SCSR (address $0010).

The general sequence for clearing an interrupt is a software sequence of accessing the serial communications status register while the flag is set followed by a read or write of an associated register. Refer to Section 6 for a description of the SCI system and its interrupts.

9.2.4 Hardware controlled interrupt sequence

The following three functions: reset, STOP and WAIT, are not in the strictest sense interrupts. However, they are acted upon in a similar manner. Flowcharts for STOP and WAIT are shown in Figure 2-4.

RESET: A reset condition causes the program to vector to its starting address, which is contained in memory locations $1FFE (MSB) and $1FFF (LSB). The I-bit in the condition code register is also set, to disable interrupts.

STOP: The STOP instruction causes the oscillator to be turned off and the processor to 'sleep' until an external interrupt ($\overline{IRQ}$) or occurs or the device is reset.

WAIT: The WAIT instruction causes all processor clocks to stop, but leaves the timer clocks running. This 'rest' state of the processor can be cleared by reset, an external interrupt ($\overline{IRQ}$), a timer interrupt or an SCI interrupt. There are no special WAIT vectors for these individual interrupts.

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10
CPU CORE AND INSTRUCTION SET

This section provides a description of the CPU core registers, the instruction set and the addressing modes of the MC68HC05B6.

10.1 Registers

The MCU contains five registers, as shown in the programming model of Figure 10-1. The interrupt stacking order is shown in Figure 10-2.

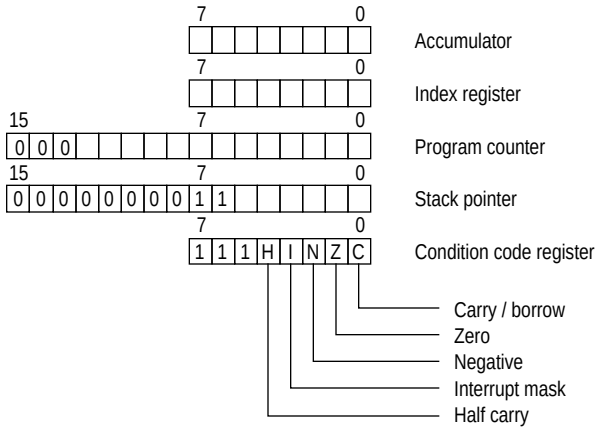

Figure 10-1 Programming model

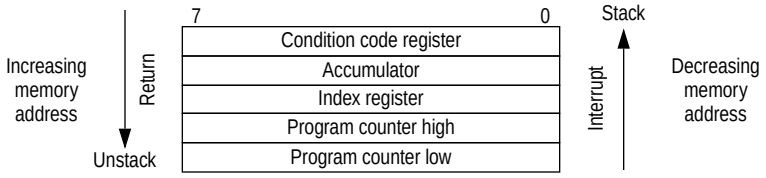

Figure 10-2 Stacking order

10.1.1 Accumulator (A)

The accumulator is a general purpose 8-bit register used to hold operands and results of arithmetic calculations or data manipulations.

10.1.2 Index register (X)

The index register is an 8-bit register, which can contain the indexed addressing value used to create an effective address. The index register may also be used as a temporary storage area.

10.1.3 Program counter (PC)

The program counter is a 16-bit register, which contains the address of the next byte to be fetched. Although the M68HC05 CPU core can address 64 kbytes of memory, the actual address range of the MC68HC05B6 is limited to 8 kbytes. The three most significant bits of the Program Counter are therefore not used and are permanently set to zero.

10.1.4 Stack pointer (SP)

The stack pointer is a 16-bit register, which contains the address of the next free location on the stack. During an MCU reset or the reset stack pointer (RSP) instruction, the stack pointer is set to location $00FF. The stack pointer is then decremented as data is pushed onto the stack and incremented as data is pulled from the stack.

When accessing memory, the ten most significant bits are permanently set to 0000000011. These ten bits are appended to the six least significant register bits to produce an address within the range of $00C0 to $00FF. Subroutines and interrupts may use up to 64 (decimal) locations. If 64 locations are exceeded, the stack pointer wraps around and overwrites the previously stored information. A subroutine call occupies two locations on the stack; an interrupt uses five locations.

10.1.5 Condition code register (CCR)

The CCR is a 5-bit register in which four bits are used to indicate the results of the instruction just executed, and the fifth bit indicates whether interrupts are masked. These bits can be individually tested by a program, and specific actions can be taken as a result of their state. Each bit is explained in the following paragraphs.

Half carry (H)

This bit is set during ADD and ADC operations to indicate that a carry occurred between bits 3 and 4.

Interrupt (I)

When this bit is set all maskable interrupts are masked. If an interrupt occurs while this bit is set, the interrupt is latched and remains pending until the interrupt bit is cleared.

Negative (N)

When set, this bit indicates that the result of the last arithmetic, logical, or data manipulation was negative.

Zero (Z)

When set, this bit indicates that the result of the last arithmetic, logical, or data manipulation was zero.

Carry/borrow (C)

When set, this bit indicates that a carry or borrow out of the arithmetic logical unit (ALU) occurred during the last arithmetic operation. This bit is also affected during bit test and branch instructions and during shifts and rotates.

10.2 Instruction set

The MCU has a set of 62 basic instructions. They can be grouped into five different types as follows:

- Register/memory
- Read/modify/write
- Branch
- Bit manipulation
- Control

The following paragraphs briefly explain each type. All the instructions within a given type are presented in individual tables.

This MCU uses all the instructions available in the M146805 CMOS family plus one more: the unsigned multiply (MUL) instruction. This instruction allows unsigned multiplication of the contents of the accumulator (A) and the index register (X). The high-order product is then stored in the index register and the low-order product is stored in the accumulator. A detailed definition of the MUL instruction is shown in Table 10-1.

10.2.1 Register/memory Instructions

Most of these instructions use two operands. The first operand is either the accumulator or the index register. The second operand is obtained from memory using one of the addressing modes. The jump unconditional (JMP) and jump to subroutine (JSR) instructions have no register operand. Refer to Table 10-2 for a complete list of register/memory instructions.

10.2.2 Branch instructions

These instructions cause the program to branch if a particular condition is met; otherwise, no operation is performed. Branch instructions are two-byte instructions. Refer to Table 10-3.

10.2.3 Bit manipulation instructions

The MCU can set or clear any writable bit that resides in the first 256 bytes of the memory space (page 0). All port data and data direction registers, timer and serial interface registers, control/status registers and a portion of the on-chip RAM reside in page 0. An additional feature allows the software to test and branch on the state of any bit within these locations. The bit set, bit clear, bit test and branch functions are all implemented with single instructions. For the test and branch instructions, the value of the bit tested is also placed in the carry bit of the condition code register. Refer to Table 10-4.

10.2.4 Read/modify/write instructions

These instructions read a memory location or a register, modify or test its contents, and write the modified value back to memory or to the register. The test for negative or zero (TST) instruction is an exception to this sequence of reading, modifying and writing, since it does not modify the value. Refer to Table 10-5 for a complete list of read/modify/write instructions.

10.2.5 Control instructions

These instructions are register reference instructions and are used to control processor operation during program execution. Refer to Table 10-6 for a complete list of control instructions.

10.2.6 Tables

Tables for all the instruction types listed above follow. In addition there is a complete alphabetical listing of all the instructions (see Table 10-7 and Table 10-8), and an opcode map for the instruction set of the M68HC05 MCU family (see Table 10-9).

Table 10-1 MUL instruction

Operation	**X:A ← X*A**			
Description	Multiplies the eight bits in the index register by the eight bits in the accumulator and places the 16-bit result in the concatenated accumulator and index register.			
Condition codes	H : Cleared I : Not affected N : Not affected Z : Not affected C : Cleared			
Source	MUL			
Form	Addressing mode	Cycles	Bytes	Opcode
	Inherent	11	1	$42

Table 10-2 Register/memory instructions

		Addressing modes																	
		Immediate			**Direct**			**Extended**			**Indexed (no offset)**			**Indexed (8-bit offset)**			**Indexed (16-bit offset)**		
Function	**Mnemonic**	**Opcode**	**# Bytes**	**# Cycles**	**Opcode**	**# Bytes**	**# Cycles**	**Opcode**	**# Bytes**	**# Cycles**	**Opcode**	**# Bytes**	**# Cycles**	**Opcode**	**# Bytes**	**# Cycles**	**Opcode**	**# Bytes**	**# Cycles**
Load A from memory	LDA	A6	2	2	B6	2	3	C6	3	4	F6	1	3	E6	2	4	D6	3	5
Load X from memory	LDX	AE	2	2	BE	2	3	CE	3	4	FE	1	3	EE	2	4	DE	3	5
Store A in memory	STA				B7	2	4	C7	3	5	F7	1	4	E7	2	5	D7	3	6
Store X in memory	STX				BF	2	4	CF	3	5	FF	1	4	EF	2	5	DF	3	6
Add memory to A	ADD	AB	2	2	BB	2	3	CB	3	4	FB	1	3	EB	2	4	DB	3	5
Add memory and carry to A	ADC	A9	2	2	B9	2	3	C9	3	4	F9	1	3	E9	2	4	D9	3	5
Subtract memory	SUB	A0	2	2	B0	2	3	C0	3	4	F0	1	3	E0	2	4	D0	3	5
Subtract memory from A with borrow	SBC	A2	2	2	B2	2	3	C2	3	4	F2	1	3	E2	2	4	D2	3	5
AND memory with A	AND	A4	2	2	B4	2	3	C4	3	4	F4	1	3	E4	2	4	D4	3	5
OR memory with A	ORA	AA	2	2	BA	2	3	CA	3	4	FA	1	3	EA	2	4	DA	3	5
Exclusive OR memory with A	EOR	A8	2	2	B8	2	3	C8	3	4	F8	1	3	E8	2	4	D8	3	5
Arithmetic compare A with memory	CMP	A1	2	2	B1	2	3	C1	3	4	F1	1	3	E1	2	4	D1	3	5
Arithmetic compare X with memory	CPX	A3	2	2	B3	2	3	C3	3	4	F3	1	3	E3	2	4	D3	3	5
Bit test memory with A (logical compare)	BIT	A5	2	2	B5	2	3	C5	3	4	F5	1	3	E5	2	4	D5	3	5
Jump unconditional	JMP				BC	2	2	CC	3	3	FC	1	2	EC	2	3	DC	3	4
Jump to subroutine	JSR				BD	2	5	CD	3	6	FD	1	5	ED	2	6	DD	3	7

Table 10-3 Branch instructions

		Relative addressing mode		
Function	**Mnemonic**	**Opcode**	**# Bytes**	**# Cycles**
Branch always	BRA	20	2	3
Branch never	BRN	21	2	3
Branch if higher	BHI	22	2	3
Branch if lower or same	BLS	23	2	3
Branch if carry clear	BCC	24	2	3
(Branch if higher or same)	(BHS)	24	2	3
Branch if carry set	BCS	25	2	3
(Branch if lower)	(BLO)	25	2	3
Branch if not equal	BNE	26	2	3
Branch if equal	BEQ	27	2	3
Branch if half carry clear	BHCC	28	2	3
Branch if half carry set	BHCS	29	2	3
Branch if plus	BPL	2A	2	3
Branch if minus	BMI	2B	2	3
Branch if interrupt mask bit is clear	BMC	2C	2	3
Branch if interrupt mask bit is set	BMS	2D	2	3
Branch if interrupt line is low	BIL	2E	2	3
Branch if interrupt line is high	BIH	2F	2	3
Branch to subroutine	BSR	AD	2	6

Table 10-4 Bit manipulation instructions

		Addressing Modes					
		Bit set/clear			Bit test and branch		
Function	**Mnemonic**	**Opcode**	**# Bytes**	**# Cycles**	**Opcode**	**# Bytes**	**# Cycles**
Branch if bit n is set	BRSET n (n=0–7)				2•n	3	5
Branch if bit n is clear	BRCLR n (n=0–7)				01+2•n	3	5
Set bit n	BSET n (n=0–7)	10+2•n	2	5			
Clear bit n	BCLR n (n=0–7)	11+2•n	2	5			

Table 10-5 Read/modify/write instructions

		Addressing modes														
		Inherent (A)			Inherent (X)			Direct			Indexed (no offset)			Indexed (8-bit offset)		
Function	Mnemonic	Opcode	# Bytes	# Cycles	Opcode	# Bytes	# Cycles	Opcode	# Bytes	# Cycles	Opcode	# Bytes	# Cycles	Opcode	# Bytes	# Cycles
Increment	INC	4C	1	3	5C	1	3	3C	2	5	7C	1	5	6C	2	6
Decrement	DEC	4A	1	3	5A	1	3	3A	2	5	7A	1	5	6A	2	6
Clear	CLR	4F	1	3	5F	1	3	3F	2	5	7F	1	5	6F	2	6
Complement	COM	43	1	3	53	1	3	33	2	5	73	1	5	63	2	6
Negate (two's complement)	NEG	40	1	3	50	1	3	30	2	5	70	1	5	60	2	6
Rotate left through carry	ROL	49	1	3	59	1	3	39	2	5	79	1	5	69	2	6
Rotate right through carry	ROR	46	1	3	56	1	3	36	2	5	76	1	5	66	2	6
Logical shift left	LSL	48	1	3	58	1	3	38	2	5	78	1	5	68	2	6
Logical shift right	LSR	44	1	3	54	1	3	34	2	5	74	1	5	64	2	6
Arithmetic shift right	ASR	47	1	3	57	1	3	37	2	5	77	1	5	67	2	6
Test for negative or zero	TST	4D	1	3	5D	1	3	3D	2	4	7D	1	4	6D	2	5
Multiply	MUL	42	1	11												

Table 10-6 Control instructions

		Inherent addressing mode		
Function	Mnemonic	Opcode	# Bytes	# Cycles
Transfer A to X	TAX	97	1	2
Transfer X to A	TXA	9F	1	2
Set carry bit	SEC	99	1	2
Clear carry bit	CLC	98	1	2
Set interrupt mask bit	SEI	9B	1	2
Clear interrupt mask bit	CLI	9A	1	2
Software interrupt	SWI	83	1	10
Return from subroutine	RTS	81	1	6
Return from interrupt	RTI	80	1	9
Reset stack pointer	RSP	9C	1	2
No-operation	NOP	9D	1	2
Stop	STOP	8E	1	2
Wait	WAIT	8F	1	2

Table 10-7 Instruction set (1 of 2)

Mnemonic	Addressing modes										Condition codes				
	INH	IMM	DIR	EXT	REL	IX	IX1	IX2	BSC	BTB	H	I	N	Z	C
ADC												•			
ADD												•			
AND											•	•			•
ASL											•	•			
ASR											•	•			
BCC											•	•	•	•	•
BCLR											•	•	•	•	•
BCS											•	•	•	•	•
BEQ											•	•	•	•	•
BHCC											•	•	•	•	•
BHCS											•	•	•	•	•
BHI											•	•	•	•	•
BHS											•	•	•	•	•
BIH											•	•	•	•	•
BIL											•	•	•	•	•
BIT											•	•			•
BLO											•	•	•	•	•
BLS											•	•	•	•	•
BMC											•	•	•	•	•
BMI											•	•	•	•	•
BMS											•	•	•	•	•
BNE											•	•	•	•	•
BPL											•	•	•	•	•
BRA											•	•	•	•	•
BRN											•	•	•	•	•
BRCLR											•	•	•	•	
BRSET											•	•	•	•	
BSET											•	•	•	•	•
BSR											•	•	•	•	•
CLC											•	•	•	•	0
CLI											•	0	•	•	•
CLR											•	•	0	1	•
CMP											•	•			

Address mode abbreviations

BSC	Bit set/clear	IMM	Immediate
BTB	Bit test & branch	IX	Indexed (no offset)
DIR	Direct	IX1	Indexed, 1 byte offset
EXT	Extended	IX2	Indexed, 2 byte offset
INH	Inherent	REL	Relative

Not implemented

Condition code symbols

H	Half carry (from bit 3)	↕	Tested and set if true, cleared otherwise
I	Interrupt mask	•	Not affected
N	Negate (sign bit)	?	Load CCR from stack
Z	Zero	0	Cleared
C	Carry/borrow	1	Set

Table 10-8 Instruction set (2 of 2)

Mnemonic	Addressing modes										Condition codes				
	INH	IMM	DIR	EXT	REL	IX	IX1	IX2	BSC	BTB	H	I	N	Z	C
COM											•	•			1
CPX											•	•			
DEC											•	•			•
EOR											•	•			•
INC											•	•			•
JMP											•	•	•	•	•
JSR											•	•	•	•	•
LDA											•	•			•
LDX											•	•			•
LSL											•	•			
LSR											•	•	0		
MUL											0	•	•	•	0
NEG											•	•			
NOP											•	•	•	•	•
ORA											•	•			•
ROL											•	•			
ROR											•	•			
RSP											•	•	•	•	•
RTI											?	?	?	?	?
RTS											•	•	•	•	•
SBC											•	•			
SEC											•	•	•	•	1
SEI											•	1	•	•	•
STA											•	•			•
STOP											•	0	•	•	•
STX											•	•			•
SUB											•	•			
SWI											•	1	•	•	•
TAX											•	•	•	•	•
TST											•	•			•
TXA											•	•	•	•	•
WAIT											•	0	•	•	•

Address mode abbreviations

BSC	Bit set/clear	IMM	Immediate
BTB	Bit test & branch	IX	Indexed (no offset)
DIR	Direct	IX1	Indexed, 1 byte offset
EXT	Extended	IX2	Indexed, 2 byte offset
INH	Inherent	REL	Relative

Not implemented

Condition code symbols

H	Half carry (from bit 3)		Tested and set if true, cleared otherwise
I	Interrupt mask	•	Not affected
N	Negate (sign bit)	?	Load CCR from stack
Z	Zero	0	Cleared
C	Carry/borrow	1	Set

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Table 10-9 M68HC05 opcode map

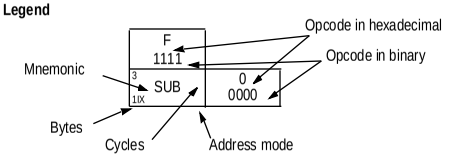
	Bit manipulation		Branch	Read/modify/write					Control		Register/memory						
	BTB	BSC	REL	DIR	INH	INH	IX1	IX	INH	INH	IMM	DIR	EXT	IX2	IX1	IX	
High / Low	0 0000	1 0001	2 0010	3 0011	4 0100	5 0101	6 0110	7 0111	8 1000	9 1001	A 1010	B 1011	C 1100	D 1101	E 1110	F 1111	High / Low
0 0000	5 BRSET0 3BTB	5 BSET0 2BSC	3 BRA 2REL	5 NEG 2DIR	3 NEGA 1INH	3 NEGX 1INH	6 NEG 2IX1	5 NEG 1IX	9 RTI 1INH		2 SUB 2IMM	3 SUB 2DIR	4 SUB 3EXT	5 SUB 3IX2	4 SUB 2IX1	3 SUB 1IX	0 0000
1 0001	5 BRCLR0 3BTB	5 BCLR0 2BSC	3 BRN 2REL						6 RTS 1INH		2 CMP 2IMM	3 CMP 2DIR	4 CMP 3EXT	5 CMP 3IX2	4 CMP 2IX1	3 CMP 1IX	1 0001
2 0010	5 BRSET1 3BTB	5 BSET1 2BSC	3 BHI 2REL		11 MUL 1INH						2 SBC 2IMM	3 SBC 2DIR	4 SBC 3EXT	5 SBC 3IX2	4 SBC 2IX1	3 SBC 1IX	2 0010
3 0011	5 BRCLR1 3BTB	5 BCLR1 2BSC	3 BLS 2REL	5 COM 2DIR	3 COMA 1INH	3 COMX 1INH	6 COM 2IX1	5 COM 1IX	10 SWI 1INH		2 CPX 2IMM	3 CPX 2DIR	4 CPX 3EXT	5 CPX 3IX2	4 CPX 2IX1	3 CPX 1IX	3 0011
4 0100	5 BRSET2 3BTB	5 BSET2 2BSC	3 BCC 2REL	5 LSR 2DIR	3 LSRA 1INH	3 LSRX 1INH	6 LSR 2IX1	5 LSR 1IX			2 AND 2IMM	3 AND 2DIR	4 AND 3EXT	5 AND 3IX2	4 AND 2IX1	3 AND 1IX	4 0100
5 0101	5 BRCLR2 3BTB	5 BCLR2 2BSC	3 BCS 2REL								2 BIT 2IMM	3 BIT 2DIR	4 BIT 3EXT	5 BIT 3IX2	4 BIT 2IX1	3 BIT 1IX	5 0101
6 0110	5 BRSET3 3BTB	5 BSET3 2BSC	3 BNE 2REL	5 ROR 2DIR	3 RORA 1INH	3 RORX 1INH	6 ROR 2IX1	5 ROR 1IX			2 LDA 2IMM	3 LDA 2DIR	4 LDA 3EXT	5 LDA 3IX2	4 LDA 2IX1	3 LDA 1IX	6 0110
7 0111	5 BRCLR3 3BTB	5 BCLR3 2BSC	3 BEQ 2REL	5 ASR 2DIR	3 ASRA 1INH	3 ASRX 1INH	6 ASR 2IX1	5 ASR 1IX		2 TAX 1INH		4 STA 2DIR	5 STA 3EXT	6 STA 3IX2	5 STA 2IX1	4 STA 1IX	7 0111
8 1000	5 BRSET4 3BTB	5 BSET4 2BSC	3 BHCC 2REL	5 LSL 2DIR	3 LSLA 1INH	3 LSLX 1INH	6 LSL 2IX1	5 LSL 1IX		2 CLC 1INH	2 EOR 2IMM	3 EOR 2DIR	4 EOR 3EXT	5 EOR 3IX2	4 EOR 2IX1	3 EOR 1IX	8 1000
9 1001	5 BRCLR4 3BTB	5 BCLR4 2BSC	3 BHCS 2REL	5 ROL 2DIR	3 ROLA 1INH	3 ROLX 1INH	6 ROL 2IX1	5 ROL 1IX		2 SEC 1INH	2 ADC 2IMM	3 ADC 2DIR	4 ADC 3EXT	5 ADC 3IX2	4 ADC 2IX1	3 ADC 1IX	9 1001
A 1010	5 BRSET5 3BTB	5 BSET5 2BSC	3 BPL 2REL	5 DEC 2DIR	3 DECA 1INH	3 DECX 1INH	6 DEC 2IX1	5 DEC 1IX		2 CLI 1INH	2 ORA 2IMM	3 ORA 2DIR	4 ORA 3EXT	5 ORA 3IX2	4 ORA 2IX1	3 ORA 1IX	A 1010
B 1011	5 BRCLR5 3BTB	5 BCLR5 2BSC	3 BMI 2REL							2 SEI 1INH	2 ADD 2IMM	3 ADD 2DIR	4 ADD 3EXT	5 ADD 3IX2	4 ADD 2IX1	3 ADD 1IX	B 1011
C 1100	5 BRSET6 3BTB	5 BSET6 2BSC	3 BMC 2REL	5 INC 2DIR	3 INCA 1INH	3 INCX 1INH	6 INC 2IX1	5 INC 1IX		2 RSP 1INH		2 JMP 2DIR	3 JMP 3EXT	4 JMP 3IX2	3 JMP 2IX1	2 JMP 1IX	C 1100
D 1101	5 BRCLR6 3BTB	5 BCLR6 2BSC	3 BMS 2REL	4 TST 2DIR	3 TSTA 1INH	3 TSTX 1INH	5 TST 2IX1	4 TST 1IX		2 NOP 1INH	6 BSR 2REL	5 JSR 2DIR	6 JSR 3EXT	7 JSR 3IX2	6 JSR 2IX1	5 JSR 1IX	D 1101
E 1110	5 BRSET7 3BTB	5 BSET7 2BSC	3 BIL 2REL						2 STOP 1INH		2 LDX 2IMM	3 LDX 2DIR	4 LDX 3EXT	5 LDX 3IX2	4 LDX 2IX1	3 LDX 1IX	E 1110
F 1111	5 BRCLR7 3BTB	5 BCLR7 2BSC	3 BIH 2REL	5 CLR 2DIR	3 CLRA 1INH	3 CLRX 1INH	6 CLR 2IX1	5 CLR 1IX	2 WAIT 1INH	2 TXA 1INH		4 STX 2DIR	5 STX 3EXT	6 STX 3IX2	5 STX 2IX1	4 STX 1IX	F 1111

Abbreviations for address modes and registers

BSC	Bit set/clear	IX	Indexed (no offset)
BTB	Bit test and branch	IX1	Indexed, 1 byte (8-bit) offset
DIR	Direct	IX2	Indexed, 2 byte (16-bit) offset
EXT	Extended	REL	Relative
INH	Inherent	A	Accumulator
IMM	Immediate	X	Index register

Not implemented

Legend



10.3 Addressing modes

Ten different addressing modes provide programmers with the flexibility to optimize their code for all situations. The various indexed addressing modes make it possible to locate data tables, code conversion tables and scaling tables anywhere in the memory space. Short indexed accesses are single byte instructions; the longest instructions (three bytes) enable access to tables throughout memory. Short absolute (direct) and long absolute (extended) addressing are also included. One or two byte direct addressing instructions access all data bytes in most applications. Extended addressing permits jump instructions to reach all memory locations.

The term ‘effective address’ (EA) is used in describing the various addressing modes. The effective address is defined as the address from which the argument for an instruction is fetched or stored. The ten addressing modes of the processor are described below. Parentheses are used to indicate ‘contents of’ the location or register referred to. For example, (PC) indicates the contents of the location pointed to by the PC (program counter). An arrow indicates ‘is replaced by’ and a colon indicates concatenation of two bytes. For additional details and graphical illustrations, refer to the ***M6805 HMOS/M146805 CMOS Family Microcomputer/ Microprocessor User's Manual*** or to the ***M68HC05 Applications Guide***.

10.3.1 Inherent

In the inherent addressing mode, all the information necessary to execute the instruction is contained in the opcode. Operations specifying only the index register or accumulator, as well as the control instruction, with no other arguments are included in this mode. These instructions are one byte long.

10.3.2 Immediate

In the immediate addressing mode, the operand is contained in the byte immediately following the opcode. The immediate addressing mode is used to access constants that do not change during program execution (e.g. a constant used to initialize a loop counter).

$$EA = PC+1;\ PC \leftarrow PC+2$$

10.3.3 Direct

In the direct addressing mode, the effective address of the argument is contained in a single byte following the opcode byte. Direct addressing allows the user to directly address the lowest 256 bytes in memory with a single two-byte instruction.

$$EA = (PC+1);\ PC \leftarrow PC+2$$
$$\text{Address bus high} \leftarrow 0;\ \text{Address bus low} \leftarrow (PC+1)$$

10.3.4 Extended

In the extended addressing mode, the effective address of the argument is contained in the two bytes following the opcode byte. Instructions with extended addressing mode are capable of referencing arguments anywhere in memory with a single three-byte instruction. When using the Motorola assembler, the user need not specify whether an instruction uses direct or extended addressing. The assembler automatically selects the short form of the instruction.

EA = (PC+1):(PC+2); PC ← PC+3
Address bus high ← (PC+1); Address bus low ← (PC+2)

10.3.5 Indexed, no offset

In the indexed, no offset addressing mode, the effective address of the argument is contained in the 8-bit index register. This addressing mode can access the first 256 memory locations. These instructions are only one byte long. This mode is often used to move a pointer through a table or to hold the address of a frequently referenced RAM or I/O location.

EA = X; PC ← PC+1
Address bus high ← 0; Address bus low ← X

10.3.6 Indexed, 8-bit offset

In the indexed, 8-bit offset addressing mode, the effective address is the sum of the contents of the unsigned 8-bit index register and the unsigned byte following the opcode. Therefore the operand can be located anywhere within the lowest 511 memory locations. This addressing mode is useful for selecting the mth element in an n element table.

EA = X+(PC+1); PC ← PC+2
Address bus high ← K; Address bus low ← X+(PC+1)
where K = the carry from the addition of X and (PC+1)

10.3.7 Indexed, 16-bit offset

In the indexed, 16-bit offset addressing mode, the effective address is the sum of the contents of the unsigned 8-bit index register and the two unsigned bytes following the opcode. This address mode can be used in a manner similar to indexed, 8-bit offset except that this three-byte instruction allows tables to be anywhere in memory. As with direct and extended addressing, the Motorola assembler determines the shortest form of indexed addressing.

EA = X+[(PC+1):(PC+2)]; PC ← PC+3
Address bus high ← (PC+1)+K; Address bus low ← X+(PC+2)
where K = the carry from the addition of X and (PC+2)

10.3.8 Relative

The relative addressing mode is only used in branch instructions. In relative addressing, the contents of the 8-bit signed byte (the offset) following the opcode are added to the PC if, and only if, the branch conditions are true. Otherwise, control proceeds to the next instruction. The span of relative addressing is from –126 to +129 from the opcode address. The programmer need not calculate the offset when using the Motorola assembler, since it calculates the proper offset and checks to see that it is within the span of the branch.

EA = PC+2+(PC+1); PC ← EA if branch taken;
otherwise EA = PC ← PC+2

10.3.9 Bit set/clear

In the bit set/clear addressing mode, the bit to be set or cleared is part of the opcode. The byte following the opcode specifies the address of the byte in which the specified bit is to be set or cleared. Any read/write bit in the first 256 locations of memory, including I/O, can be selectively set or cleared with a single two-byte instruction.

EA = (PC+1); PC ← PC+2
Address bus high ← 0; Address bus low ← (PC+1)

10.3.10 Bit test and branch

The bit test and branch addressing mode is a combination of direct addressing and relative addressing. The bit to be tested and its condition (set or clear) is included in the opcode. The address of the byte to be tested is in the single byte immediately following the opcode byte (EA1). The signed relative 8-bit offset in the third byte (EA2) is added to the PC if the specified bit is set or cleared in the specified memory location. This single three-byte instruction allows the program to branch based on the condition of any readable bit in the first 256 locations of memory. The span of branch is from –125 to +130 from the opcode address. The state of the tested bit is also transferred to the carry bit of the condition code register.

EA1 = (PC+1); PC ← PC+2
Address bus high ← 0; Address bus low ← (PC+1)
EA2 = PC+3+(PC+2); PC ← EA2 if branch taken;
otherwise PC ← PC+3

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11
ELECTRICAL SPECIFICATIONS

This section contains the electrical specifications and associated timing information for the MC68HC05B6.

11.1 Maximum ratings

Table 11-1 Maximum ratings

Rating	Symbol	Value	Unit
Supply voltage(1)	V_{DD}	– 0.5 to +7.0	V
Input voltage	V_{IN}	V_{SS} – 0.5 to V_{DD} + 0.5	V
Input voltage – Self-check mode ($\overline{IRQ}$ pin only)	V_{IN}	V_{SS} – 0.5 to 2V_{DD} + 0.5	V
Operating temperature range – Standard (MC68HC05B6) – Extended (MC68HC05B6C) – Automotive (MC68HC05B6M)	T_A	T_L to T_H 0 to +70 –40 to +85 –40 to +125	C
Storage temperature range	T_{STG}	– 65 to +150	C
Current drain per pin (excluding VDD and VSS)(2) – Source – Sink	 I_D I_S	 25 45	 mA mA

(1) All voltages are with respect to V_{SS}.

(2) Maximum current drain per pin is for one pin at a time, limited by an external resistor.

Note: This device contains circuitry designed to protect against damage due to high electrostatic voltages or electric fields. However, it is recommended that normal precautions be taken to avoid the application of any voltages higher than those given in the maximum ratings table to this high impedance circuit. For maximum reliability all unused inputs should be tied to either V_{SS} or V_{DD}.

11.2 Thermal characteristics and power considerations

Table 11-2 Package thermal characteristics

Characteristics	Symbol	Value	Unit
Thermal resistance			
– 64-pin quad flat package	θ_{JA}	50	C/W
– Plastic 56 pin shrink DIL package	θ_{JA}	50	C/W
– Plastic 52 pin PLCC package	θ_{JA}	50	C/W

The average chip junction temperature, T_J, in degrees Celsius can be obtained from the following equation:

$$T_J = T_A + (P_D \bullet \theta_{JA}) \quad [1]$$

where:

T_A = Ambient temperature (C)

θ_{JA} = Package thermal resistance, junction-to-ambient (C/W)

$P_D = P_{INT} + P_{I/O}$ (W)

P_{INT} = Internal chip power = $I_{DD} \bullet V_{DD}$ (W)

$P_{I/O}$ = Power dissipation on input and output pins (user determined)

An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = \frac{K}{T_J + 273} \quad [2]$$

Solving equations [1] and [2] for K gives:

$$K = P_D \bullet (T_A + 273) + \theta_{JA} \bullet P_D^2 \quad [3]$$

where K is a constant for a particular part. K can be determined by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained for any value of T_A by solving the above equations. The package thermal characteristics are shown in Table 11-2.

Voltage	Pins	R1	R2	C
4.5V	PA0–7, PB0–7, PC0–7	3.26k	2.38k	50pF
3.0V	PA0–7, PB0–7, PC0–7	10.91k	6.32k	50pF

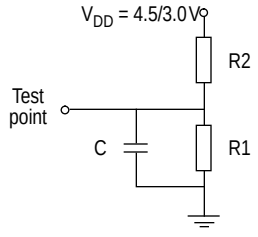

Figure 11-1 Equivalent test load

11.3 DC electrical characteristics

Table 11-3 DC electrical characteristics for 5V operation

(V_{DD} = 5 Vdc ± 10%, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H)

Characteristic[1]	Symbol	Min	Typ[2]	Max	Unit
Output voltage I_{LOAD} = – 10 µA I_{LOAD} = +10 µA	 V_{OH} V_{OL}	 V_{DD} – 0.1 —	 — —	 — 0.1	V
Output high voltage (I_{LOAD} = 0.8 mA) PA0–7, PB0–7, PC0–7, TCMP1, TCMP2 Output high voltage (I_{LOAD} = 1.6 mA) TDO, SCLK, PLMA, PLMB	 V_{OH} V_{OH}	 V_{DD} – 0.8 V_{DD} – 0.8	 V_{DD} – 0.4 V_{DD} – 0.4	 — —	V
Output low voltage (I_{LOAD} = 1.6 mA) PA0–7, PB0–7, PC0–7, TCMP1, TCMP2, TDO, SCLK, PLMA, PLMB Output low voltage (I_{LOAD} = 1.6 mA) $\overline{RESET}$	 V_{OL} V_{OL}	 — 	 0.1 0.4	 0.4 1	V
Input high voltage PA0–7, PB0–7, PC0–7, PD0–7, OSC1, $\overline{IRQ}$, $\overline{RESET}$, TCAP1, TCAP2, RDI	V_{IH}	0.7V_{DD}	—	V_{DD}	V
Input low voltage PA0–7, PB0–7, PC0–7, OSC1, $\overline{IRQ}$, $\overline{RESET}$, TCAP1, TCAP2, RDI	V_{IL}	V_{SS}	—	0.2V_{DD}	V
Supply current[3] RUN (SM = 0) (See Figure 11-2) RUN (SM = 1) (See Figure 11-3) WAIT (SM = 0) (See Figure 11-4) WAIT (SM = 1) (See Figure 11-5) STOP 0 to 70 (standard) – 40 to 85 (extended) – 40 to 105 (extended) – 40 to 125 (automotive)	 I_{DD}	 — — — — — — — —	 3.5 0.5 1 0.35 2 — — —	 6 1.5 2 1 10 20 60 60	 mA mA mA mA µA µA µA µA
High-Z leakage current PA0–7, PB0–7, PC0–7, TDO, $\overline{RESET}$, SCLK	I_{IL}	—	0.2	1	µA
Input current (0 to 70) $\overline{IRQ}$, OSC1, TCAP1, TCAP2, RDI, PD0/AN0-PD7/AN7 (channel not selected)	I_{IN}	—	0.2 0.2	1 1	µA
Input current (– 40 to 125) $\overline{IRQ}$, OSC1, TCAP1, TCAP2, RDI,	I_{IN}	—	—	5	µA
Capacitance Ports (as input or output), $\overline{RESET}$, TDO, SCLK $\overline{IRQ}$, TCAP1, TCAP2, OSC1, RDI PD0/AN0–PD7/AN7 (A/D off) PD0/AN0–PD7/AN7 (A/D on)	 C_{OUT} C_{IN} C_{IN} C_{IN}	 — — — —	 — — 12 22	 12 8 TBD TBD	 pF pF pF pF

(1) All I_{DD} measurements taken with suitable decoupling capacitors across the power supply to suppress the transient switching currents inherent in CMOS designs (see Section 2).

(2) Typical values are at mid point of voltage range and at 25 C only

(3) RUN and WAIT I_{DD}: measured using an external square-wave clock source (f_{OSC} = 4.2MHz); all inputs 0.2 V from rail; no DC loads; maximum load on outputs 50pF (20pF on OSC2).
STOP /WAIT I_{DD}: all ports configured as inputs; V_{IL} = 0.2 V and $V_{IH} = V_{DD}$ – 0.2 V: STOP I_{DD} measured with OSC1 = V_{DD}.
WAIT I_{DD} is affected linearly by the OSC2 capacitance.

11.3.1 I_{DD} trends for 5V operation

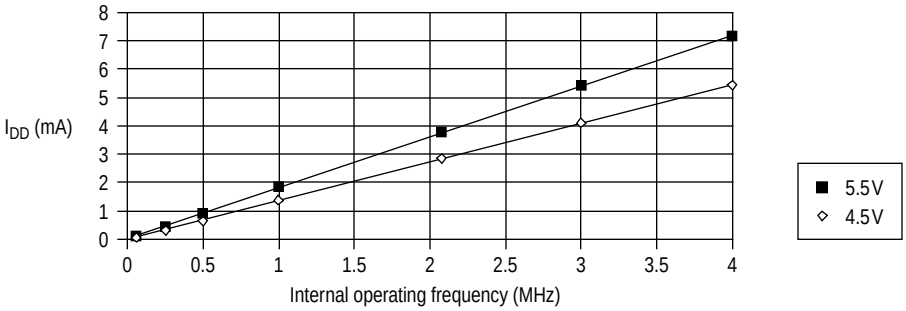

Figure 11-2 Run I_{DD} vs internal operating frequency (4.5V, 5.5V)

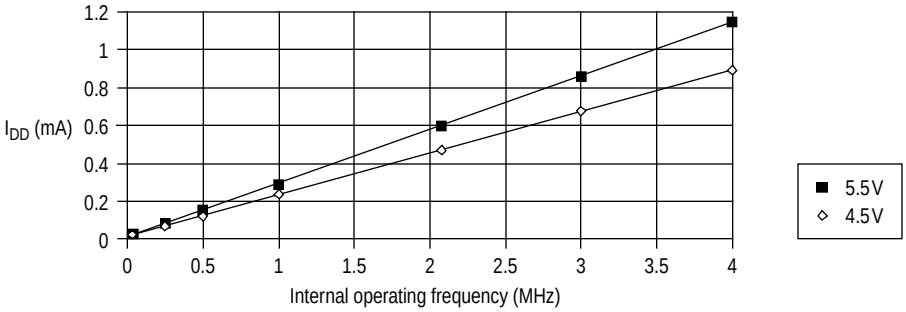

Figure 11-3 Run I_{DD} (SM = 1) vs internal operating frequency (4.5V, 5.5V)

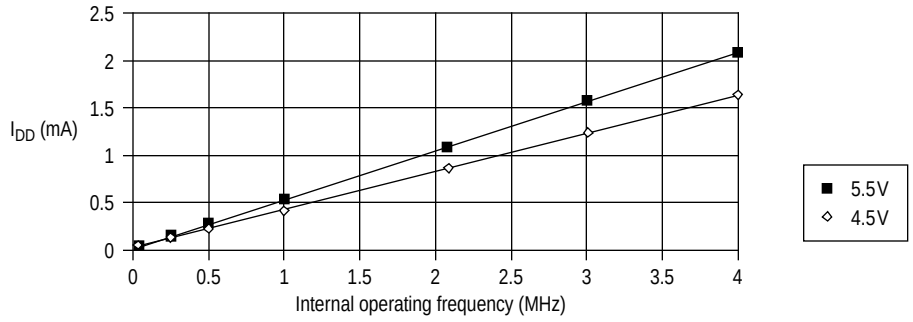

Figure 11-4 Wait I_{DD} vs internal operating frequency (4.5V, 5.5V)

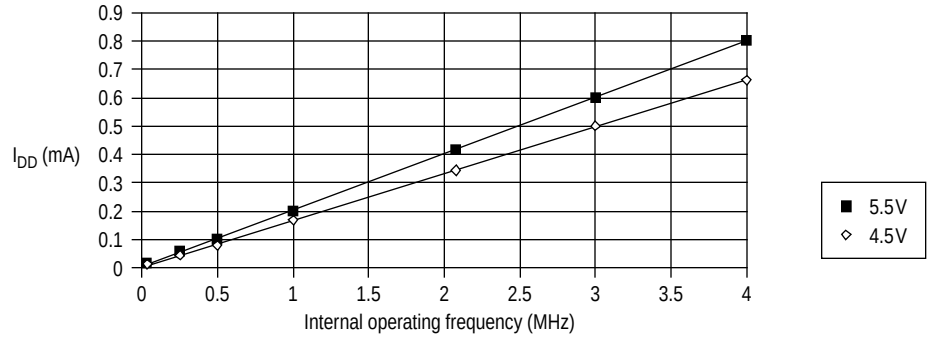

Figure 11-5 Wait I_{DD} (SM = 1) vs internal operating frequency (4.5V, 5.5V)

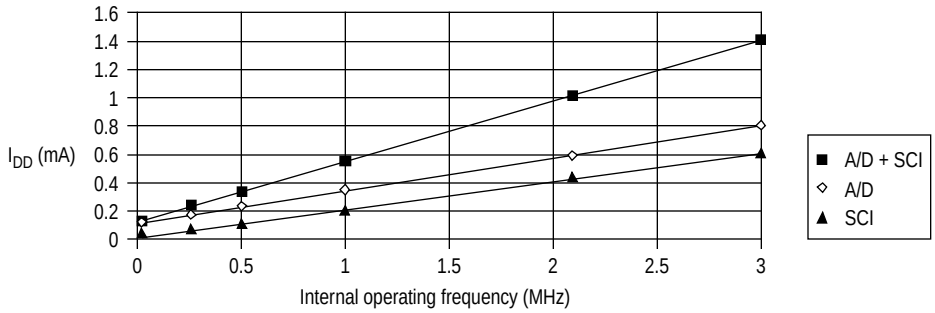

Figure 11-6 Increase in I_{DD} vs frequency for A/D, SCI systems active, VDD = 5.5V

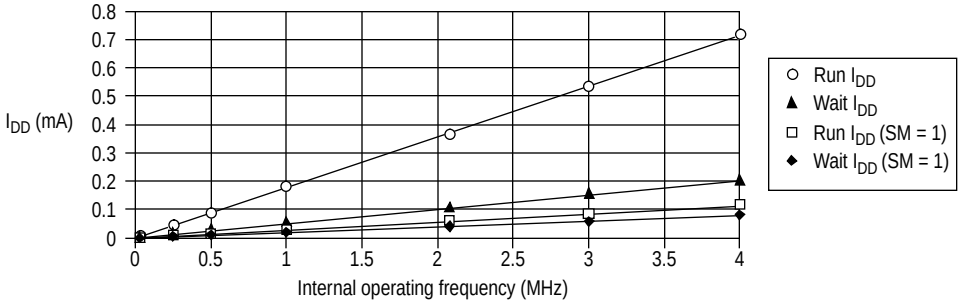

Figure 11-7 I_{DD} vs mode vs internal operating frequency, V_{DD} = 5.5V

Table 11-4 DC electrical characteristics for 3.3V operation

(V_{DD} = 3.3Vdc ± 10%, V_{SS} = 0Vdc, $T_A = T_L$ to T_H)

Characteristic[1]	Symbol	Min	Typ[2]	Max	Unit
Output voltage I_{LOAD} = – 10 µA I_{LOAD} = +10 µA	 V_{OH} V_{OL}	 V_{DD} – 0.1 —	 — —	 — 0.1	V
Output high voltage (I_{LOAD} = 0.2mA) PA0–7, PB0–7, PC0–7, TCMP1, TCMP2 Output high voltage (I_{LOAD} = 0.4mA) TDO, SCLK, PLMA, PLMB	 V_{OH} V_{OH}	 V_{DD} – 0.3 V_{DD} – 0.3	 V_{DD} – 0.1 V_{DD} – 0.1	 — —	V
Output low voltage (I_{LOAD} = 0.4mA) PA0–7, PB0–7, PC0–7, TCMP1, TCMP2, TDO, SCLK, PLMA, PLMB Output low voltage (I_{LOAD} = 0.4mA) $\overline{RESET}$	V_{OL} V_{OL}	—	0.1 0.2	0.3 0.6	V
Input high voltage PA0–7, PB0–7, PC0–7, PD0–7, OSC1, $\overline{IRQ}$, $\overline{RESET}$, TCAP1, TCAP2, RDI	V_{IH}	0.7V_{DD}	—	V_{DD}	V
Input low voltage PA0–7, PB0–7, PC0–7, OSC1, $\overline{IRQ}$, $\overline{RESET}$, TCAP1, TCAP2, RDI	V_{IL}	V_{SS}	—	0.2V_{DD}	V
Supply current[3] RUN (SM = 0) (See Figure 11-2) RUN (SM = 1) (See Figure 11-3) WAIT (SM = 0) (See Figure 11-4) WAIT (SM = 1) (See Figure 11-5) STOP 0 to 70 (standard) – 40 to 85 (extended) – 40 to 105 (extended) – 40 to 125 (automotive)	 I_{DD}	 — — — — — — — —	 1.2 0.2 0.4 0.15 1 — — —	 3 1 1.5 0.5 10 10 40 40	 mA mA mA mA µA µA µA µA
High-Z leakage current PA0–7, PB0–7, PC0–7, TDO, $\overline{RESET}$, SCLK	I_{IL}	—	0.2	1	µA
Input current (0 to 70) $\overline{IRQ}$, OSC1, TCAP1, TCAP2, RDI, PD0/AN0-PD7/AN7 (channel not selected)	I_{IN}	—	0.2 0.2	1 1	µA
Input current (– 40 to 125) $\overline{IRQ}$, OSC1, TCAP1, TCAP2, RDI,	I_{IN}	—	—	5	µA
Capacitance Ports (as input or output), $\overline{RESET}$, TDO, SCLK $\overline{IRQ}$, TCAP1, TCAP2, OSC1, RDI PD0/AN0–PD7/AN7 (A/D off) PD0/AN0–PD7/AN7 (A/D on)	 C_{OUT} C_{IN} C_{IN} C_{IN}	 — — — —	 — — 12 22	 12 8 TBD TBD	 pF pF pF pF

(1) All I_{DD} measurements taken with suitable decoupling capacitors across the power supply to suppress the transient switching currents inherent in CMOS designs (see Section 2).

(2) Typical values are at mid point of voltage range and at 25 C only

(3) RUN and WAIT I_{DD}: measured using an external square-wave clock source (f_{OSC} = 2.1MHz); all inputs 0.2 V from rail; no DC loads; maximum load on outputs 50pF (20pF on OSC2).
STOP /WAIT I_{DD}: all ports configured as inputs; V_{IL} = 0.2 V and $V_{IH} = V_{DD}$ – 0.2 V: STOP I_{DD} measured with OSC1 = V_{DD}.
WAIT I_{DD} is affected linearly by the OSC2 capacitance.

11.3.2 I_{DD} trends for 3.3V operation

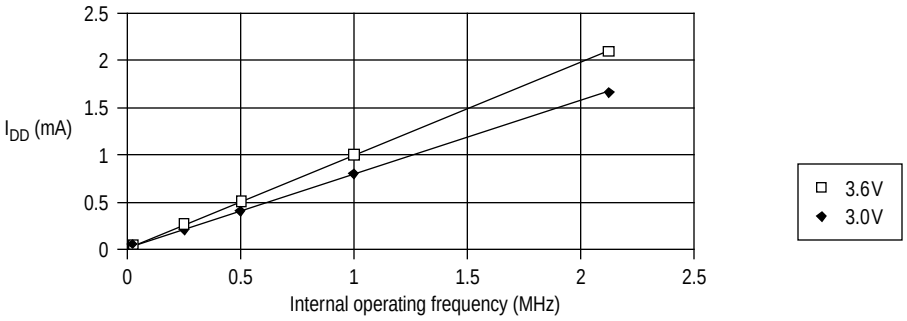

Figure 11-8 Run I_{DD} vs internal operating frequency (3 V, 3.6 V)

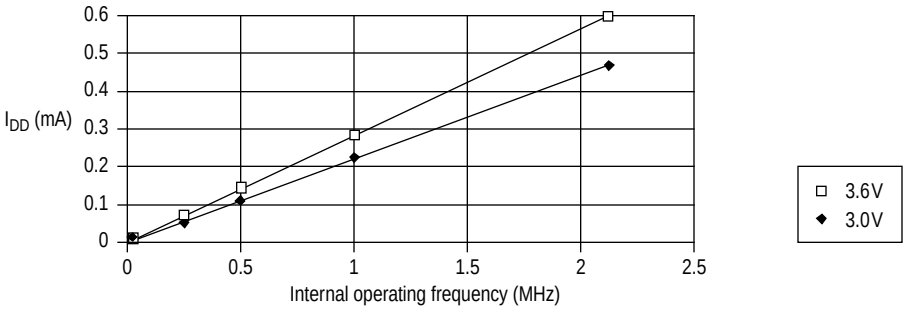

Figure 11-9 Run I_{DD} (SM = 1) vs internal operating frequency (3V,3.6V)

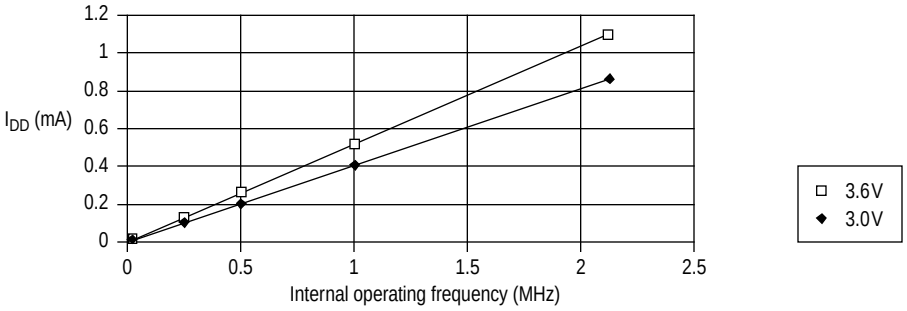

Figure 11-10 Wait I_{DD} vs internal operating frequency (3V, 3.6V)

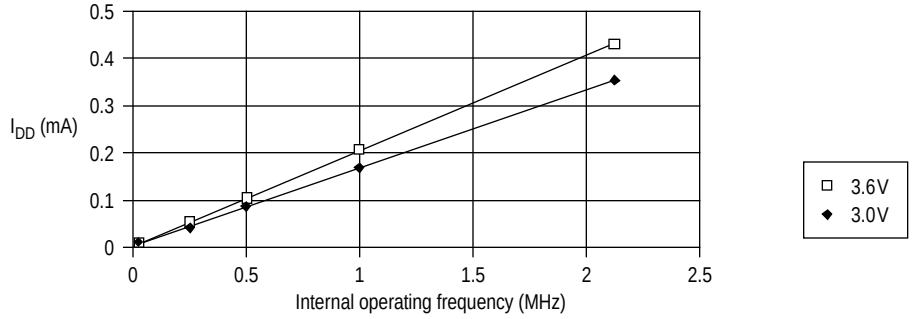

Figure 11-11 Wait I_{DD} (SM = 1) vs internal operating frequency (3V, 3.6V)

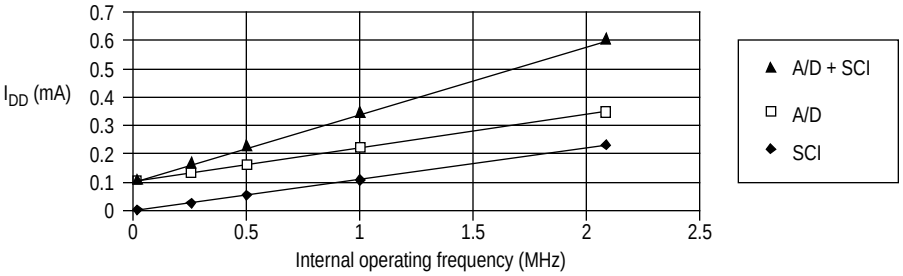

Figure 11-12 Increase in I_{DD} vs frequency for A/D, SCI systems active, V_{DD} = 3.6V

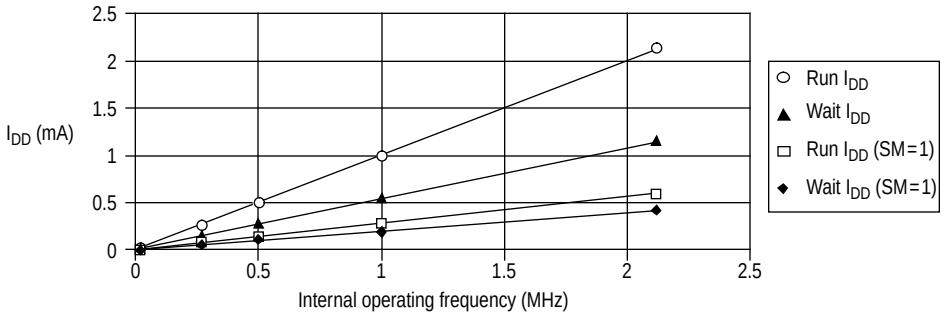

Figure 11-13 I_{DD} vs mode vs internal operating frequency, V_{DD} = 3.6V

11.4 A/D converter characteristics

Table 11-5 A/D characteristics for 5V operation

(V_{DD} = 5.0 Vdc 10%, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H)

Characteristic	Parameter	Min	Max	Unit
Resolution	Number of bits resolved by the A/D	8	—	Bit
Non-linearity	Max deviation from the best straight line through the A/D transfer characteristics ($V_{RH} = V_{DD}$ and V_{RL} = 0V)	—	0.5	LSB
Quantization error	Uncertainty due to converter resolution	—	0.5	LSB
Absolute accuracy	Difference between the actual input voltage and the full-scale equivalent of the binary code output code for all errors	—	1	LSB
Conversion range	Analog input voltage range	V_{RL}	V_{RH}	V
V_{RH}	Maximum analog reference voltage	V_{RL}	V_{DD} + 0.1	V
V_{RL}	Minimum analog reference voltage	V_{SS} – 0.1	V_{RH}	V
V_R(1)	Minimum difference between V_{RH} and V_{RL}	3	—	V
Conversion time	Total time to perform a single analog to digital conversion a. External clock (OSC1, OSC2) b. Internal RC oscillator	 — —	 32 32	 t_{CYC} µs
Monotonicity	Conversion result never decreases with an increase in input voltage and has no missing codes	GUARANTEED		
Zero input reading	Conversion result when $V_{IN} = V_{RL}$	00	—	Hex
Full scale reading	Conversion result when $V_{IN} = V_{RH}$	—	FF	Hex
Sample acquisition time	Analog input acquisition sampling a. External clock (OSC1, OSC2) b. Internal RC oscillator(2)	 — —	 12 12	 t_{CYC} s
Sample/hold capacitance	Input capacitance on PD0/AN0–PD7/AN7	—	12	pF
Input leakage(3)	Input leakage on A/D pins PD0/AN0–PD7/AN7, VRL, VRH	—	1	µA

(1) Performance verified down to 2.5V VR, but accuracy is tested and guaranteed at VR = 5V 10%.

(2) Source impedances greater than 10k will adversely affect internal charging time during input sampling.

(3) The external system error caused by input leakage current is approximately equal to the product of R source and input current. Input current to A/D channel will be dependent on external source impedance (see Figure 8-2).

Table 11-6 A/D characteristics for 3.3V operation

(V_{DD} = 3.3 Vdc ± 10%, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H)

Characteristic	Parameter	Min	Max	Unit
Resolution	Number of bits resolved by the A/D	8	—	Bit
Non-linearity	Max deviation from the best straight line through the A/D transfer characteristics ($V_{RH} = V_{DD}$ and V_{RL} = 0V)	—	1	LSB
Quantization error	Uncertainty due to converter resolution	—	1	LSB
Absolute accuracy	Difference between the actual input voltage and the full-scale equivalent of the binary code output code for all errors	—	2	LSB
Conversion range	Analog input voltage range	V_{RL}	V_{RH}	V
V_{RH}	Maximum analog reference voltage	V_{RL}	V_{DD} + 0.1	V
V_{RL}	Minimum analog reference voltage	V_{SS} – 0.1	V_{RH}	V
V_R	Minimum difference between V_{RH} and V_{RL}	3	—	V
Conversion time	Total time to perform a single analog to digital conversion Internal RC oscillator	—	32	µs
Monotonicity	Conversion result never decreases with an increase in input voltage and has no missing codes	GUARANTEED		
Zero input reading	Conversion result when $V_{IN} = V_{RL}$	00	—	Hex
Full scale reading	Conversion result when $V_{IN} = V_{RH}$	—	FF	Hex
Sample acquisition time	Analog input acquisition sampling Internal RC oscillator(1)	—	12	s
Sample/hold capacitance	Input capacitance on PD0/AN0–PD7/AN7	—	12	pF
Input leakage(2)	Input leakage on A/D pins PD0/AN0–PD7/AN7, VRL, VRH	—	1	µA

(1) Source impedances greater than 10k will adversely affect internal charging time during input sampling.

(2) The external system error caused by input leakage current is approximately equal to the product of R source and input current. Input current to A/D channel will be dependent on external source impedance (see Figure 8-2).

11.5 Control timing

Table 11-7 Control timing for 5V operation

(V_{DD} = 5.0 Vdc ± 10%, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H)

Characteristic	Symbol	Min	Max	Unit
Frequency of operation				
Crystal option	f_{OSC}	—	4.2	MHz
External clock option	f_{OSC}	dc	4.2	MHz
Internal operating frequency (f_{OSC}/2)				
Crystal	f_{OP}	dc	2.1	MHz
External clock	f_{OP}	dc	2.1	MHz
Cycle time (see Figure 9-1)	t_{CYC}	480	—	ns
Crystal oscillator start-up time (see Figure 9-1)	t_{OXOV}	—	100	ms
Stop recovery start-up time (crystal oscillator)	t_{ILCH}		100	ms
RC oscillator stabilization time	t_{ADRC}		100	ms
A/D converter stabilization time	t_{ADON}		500	µs
External RESET input pulse width	t_{RL}	1.5	—	t_{CYC}
Power-on RESET output pulse width				
4064 cycle	t_{PORL}	4064	—	t_{CYC}
16 cycle	t_{PORL}	16	—	t_{CYC}
Watchdog RESET output pulse width	t_{DOGL}	1.5	—	t_{CYC}
Watchdog time-out	t_{DOG}	6144	7168	t_{CYC}
EEPROM byte erase time				
0 to 70 (standard)	t_{ERA}	10	—	ms
– 40 to 85 (extended)	t_{ERA}	10	—	ms
– 40 to 125 (automotive)	t_{ERA}	10	—	ms
EEPROM byte program time(1)				
0 to 70 (standard)	t_{PROG}	10	—	ms
– 40 to 85 (extended)	t_{PROG}	10	—	ms
– 40 to 125 (automotive)	t_{PROG}	20	—	ms
Timer (see Figure 11-14)				
Resolution(2)	t_{RESL}	4	—	t_{CYC}
Input capture pulse width	t_{TH}, t_{TL}	125	—	ns
Input capture pulse period	t_{TLTL}	—(3)	—	t_{CYC}
Interrupt pulse width (edge-triggered)	t_{ILIH}	125	—	ns
Interrupt pulse period	t_{ILIL}	—(4)	—	t_{CYC}
OSC1 pulse width	t_{OH}, t_{OL}	90	—	ns

(1) For bus frequencies less than 2 MHz, the internal RC oscillator should be used when programming the EEPROM.

(2) Since a 2-bit prescaler in the timer must count four external cycles (t_{cyc}), this is the limiting factor in determining the timer resolution.

(3) The minimum period t_{TLTL} should not be less than the number of cycle times it takes to execute the capture interrupt service routine plus 24 t_{cyc}.

(4) The minimum period t_{ILIL} should not be less than the number of cycle times it takes to execute the interrupt service routine plus 21 t_{cyc}.

Table 11-8 Control timing for 3.3V operation

(V_{DD} = 3.3Vdc 10%, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H)

Characteristic	Symbol	Min	Max	Unit
Frequency of operation				
Crystal option	f_{OSC}	—	2.0	MHz
External clock option	f_{OSC}	dc	2.0	MHz
Internal operating frequency (f_{OSC}/2)				
Crystal	f_{OP}	—	1.0	MHz
External clock	f_{OP}	dc	1.0	MHz
Cycle time (see Figure 9-1)	t_{CYC}	1000	—	ns
Crystal oscillator start-up time (see Figure 9-1)	t_{OXOV}	—	100	ms
Stop recovery start-up time (crystal oscillator)	t_{ILCH}		100	ms
RC oscillator stabilization time	t_{ADRC}		100	ms
A/D converter stabilization time	t_{ADON}		500	µs
External $\overline{\text{RESET}}$ input pulse width	t_{RL}	1.5	—	t_{CYC}
Power-on $\overline{\text{RESET}}$ output pulse width				
4064 cycle	t_{PORL}	4064	—	t_{CYC}
16 cycle	t_{PORL}	16	—	t_{CYC}
Watchdog $\overline{\text{RESET}}$ output pulse width	t_{DOGL}	1.5	—	t_{CYC}
Watchdog time-out	t_{DOG}	6144	7168	t_{CYC}
EEPROM byte erase time				
0 to 70 (standard)	t_{ERA}	30	—	ms
– 40 to 85 (extended)	t_{ERA}	30	—	ms
– 40 to 125 (automotive)	t_{ERA}	30	—	ms
EEPROM byte program time(1)				
0 to 70 (standard)	t_{PROG}	30	—	ms
– 40 to 85 (extended)	t_{PROG}	30	—	ms
– 40 to 125 (automotive)	t_{PROG}	30	—	ms
Timer (see Figure 11-14)				
Resolution(2)	t_{RESL}	4	—	t_{CYC}
Input capture pulse width	t_{TH}, t_{TL}	250	—	ns
Input capture pulse period	t_{TLTL}	—(3)	—	t_{CYC}
Interrupt pulse width (edge-triggered)	t_{ILIH}	250	—	ns
Interrupt pulse period	t_{ILIL}	—(4)	—	t_{CYC}
OSC1 pulse width	t_{OH}, t_{OL}	200	—	ns

(1) For bus frequencies less than 2 MHz, the internal RC oscillator should be used when programming the EEPROM.

(2) Since a 2-bit prescaler in the timer must count four external cycles (t_{cyc}), this is the limiting factor in determining the timer resolution.

(3) The minimum period t_{TLTL} should not be less than the number of cycle times it takes to execute the capture interrupt service routine plus 24 t_{cyc}.

(4) The minimum period t_{ILIL} should not be less than the number of cycle times it takes to execute the interrupt service routine plus 21 t_{cyc}.

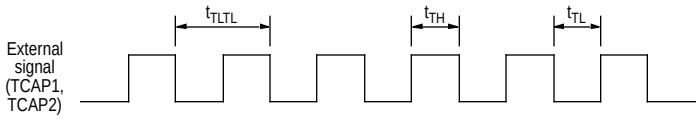

Figure 11-14 Timer relationship

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12
MECHANICAL DATA

12.1 MC68HC05B6 pin configurations

12.1.1 52-pin plastic leaded chip carrier (PLCC)

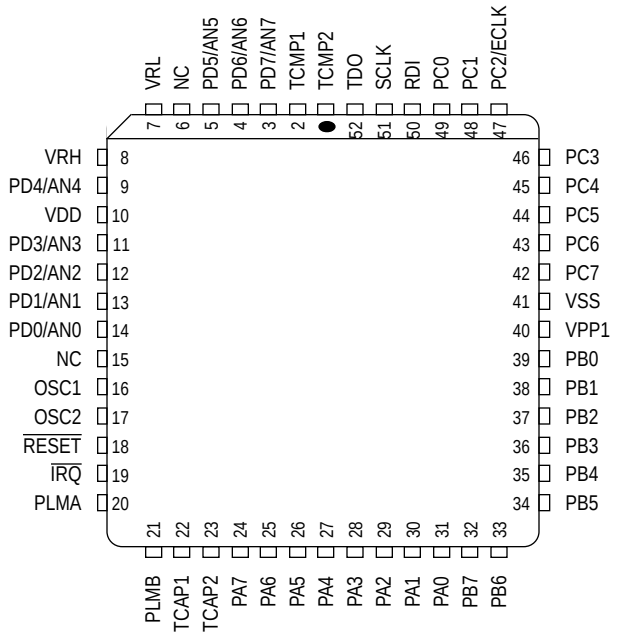
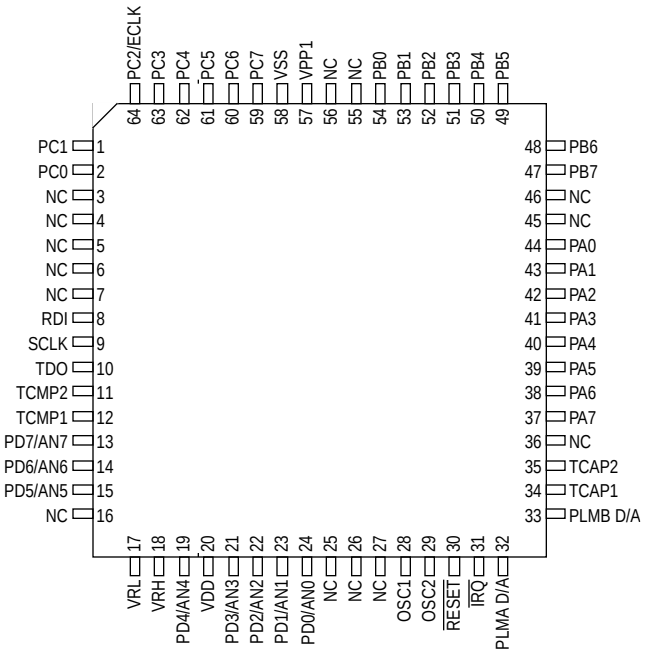


Figure 12-1 52-pin PLCC pinout

12.1.2 64-pin quad flat pack (QFP)



Device	Pin 27	Pin 57
MC68HC05B4	NC	NC
MC68HC05B6 MC68HC05B8 MC68HC05B16 MC68HC05B32	NC	VPP1
MC68HC705B5	Not available in this package	
MC68HC705B16	VPP6	VPP1
MC68HC705B32	VPP6	VPP1

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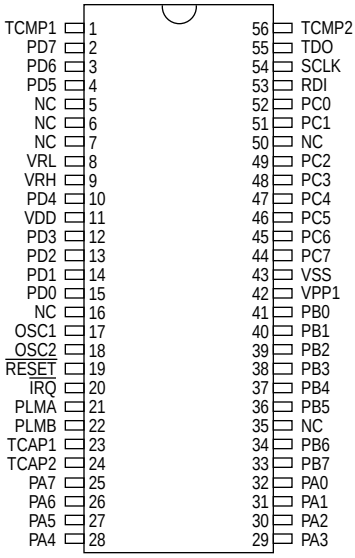
Figure 12-2 64-pin QFP pinout

12.1.3 56-pin shrink dual in line package (SDIP)

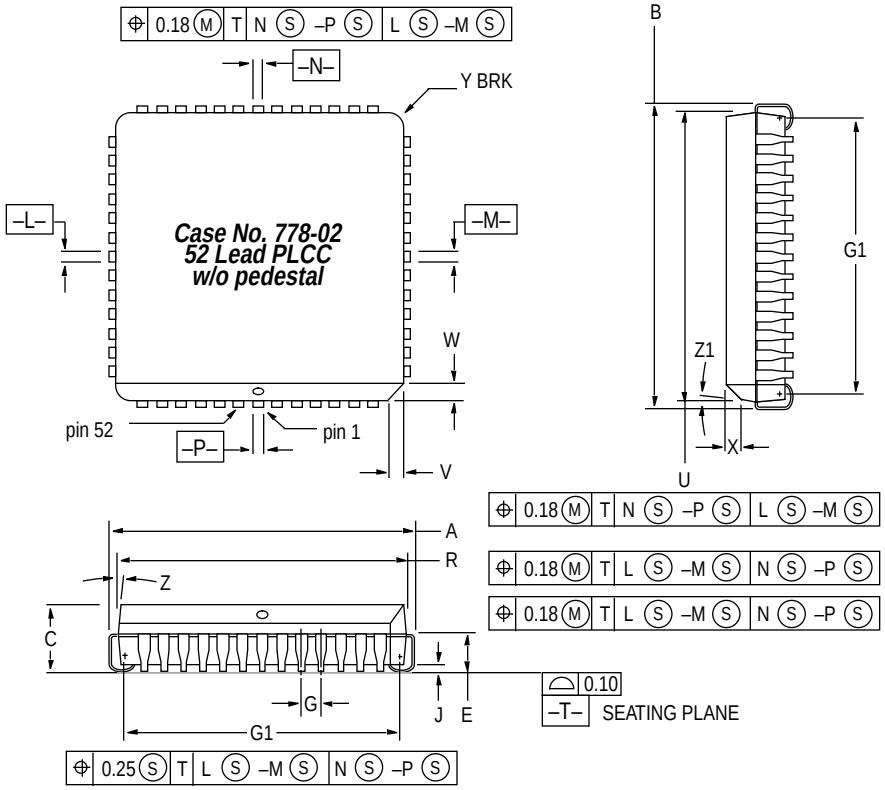


Device	Pin 16	Pin 42
MC68HC05B4	NC	NC
MC68HC05B6	NC	VPP1
MC68HC05B8	NC	VPP1
MC68HC05B16	NC	VPP1
MC68HC05B32	NC	VPP1
MC68HC705B5	VPP	NC
MC68HC705B32	VPP6	VPP1

Figure 12-3 56-pin SDIP pinout

12.2 MC68HC05B6 mechanical dimensions

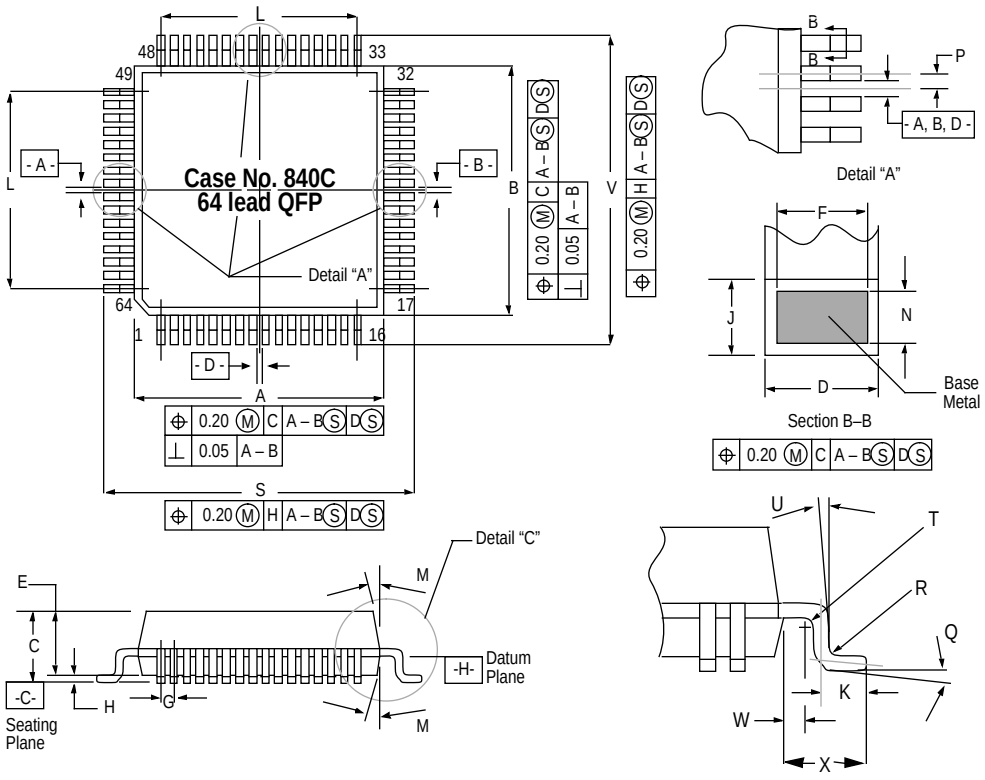
12.2.1 52-pin plastic leaded chip carrier (PLCC)



Dim.	Min.	Max.	Notes	Dim.	Min.	Max.
A	19.94	20.19		U	19.05	19.20
B	19.94	20.19		V	1.07	1.21
C	4.20	4.57	1. Datums –L–, –M–, –N– and –P– are determined where top of lead shoulder exits plastic body at mould parting line.	W	1.07	1.21
E	2.29	2.79	2. Dimension G1, true position to be measured at datum –T– (seating plane).	X	1.07	1.42
F	0.33	0.48		Y	—	0.50
G	1.27 BSC		3. Dimensions R and U do not include mould protrusion. Allowable mould protrusion is 0.25mm per side.	Z	2	10
H	0.66	0.81	4. Dimensions and tolerancing per ANSI Y 14.5M, 1982.	G1	18.04	18.54
J	0.51	—	5. All dimensions in mm.	K1	1.02	—
K	0.64	—		Z1	2	10
R	19.05	19.20				

Figure 12-4 52-pin PLCC mechanical dimensions

12.2.2 64-pin quad flat pack (QFP)



Dim.	Min.	Max.
A	13.90	14.10
B	13.90	14.10
C	2.067	2.457
D	0.30	0.45
E	2.00	2.40
F	0.30	—
G	0.80 BSC	
H	0.067	0.250
J	0.130	0.230
K	0.50	0.66
L	12.00 REF	

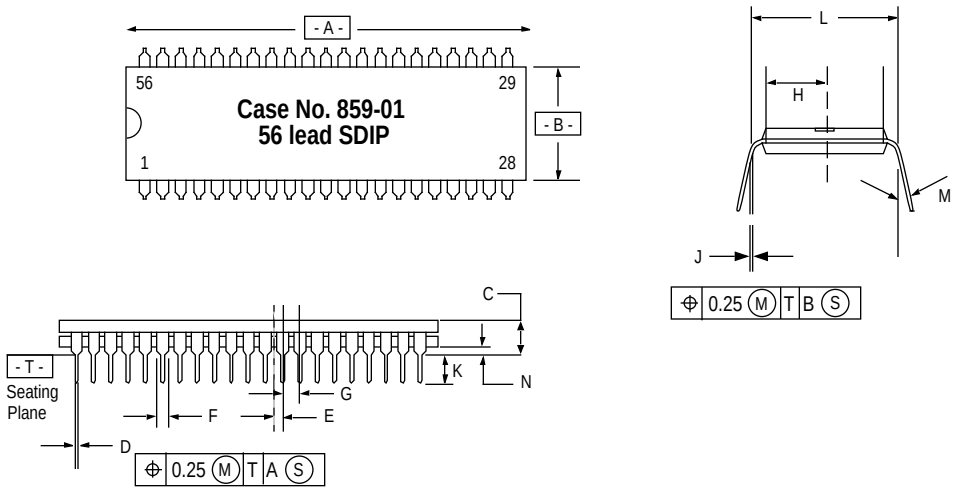
Notes

1. Datum Plane –H– is located at bottom of lead and is coincident with the lead where the lead exits the plastic body at the bottom of the parting line.
2. Datums A–B and –D to be determined at Datum Plane –H–.
3. Dimensions S and V to be determined at seating plane –C–.
4. Dimensions A and B do not include mould protrusion. Allowable mould protrusion is 0.25mm per side. Dimensions A and B do include mould mismatch and are determined at Datum Plane –H–.
5. Dimension D does not include dambar protrusion. Allowable dambar protrusion shall be 0.08 total in excess of the D dimension at maximum material condition. Dambar cannot be located on the lower radius or the foot.
6. Dimensions and tolerancing per ANSI Y 14.5M, 1982.
7. All dimensions in mm.

Dim.	Min.	Max.
M	5	10
N	0.130	0.170
P	0.40 BSC	
Q	2	8
R	0.13	0.30
S	16.20	16.60
T	0.20 REF	
U	9	15
V	16.20	16.60
W	0.042 NOM	
X	1.10	1.30

Figure 12-5 64-pin QFP mechanical dimensions

12.2.3 56-pin shrink dual in line package (SDIP)



Dim.	Min.	Max.	Notes	Dim.	Min.	Max.
A	51.69	52.45		H	7.62 BSC	
B	13.72	14.22	1. **Due to space limitations, this case shall be represented by a general case outline, rather than one showing all the leads.**	J	0.20	0.38
C	3.94	5.08	2. Dimensions and tolerancing per ANSI Y 14.5 1982.	K	2.92	3.43
D	0.36	0.56	3. All dimensions in mm.	L	15.24 BSC	
E	0.89 BSC		4. Dimension L to centre of lead when formed parallel.	M	0	15
F	0.81	1.17	5. Dimensions A and B do not include mould flash. Allowable mould flash is 0.25 mm.	N	0.51	1.02
G	1.778 BSC					

Figure 12-6 56-pin SDIP mechanical dimensions

13
ORDERING INFORMATION

This section describes the information needed to order the MC68HC05B6 and other family members.

To initiate a ROM pattern for the MCU, it is necessary to contact your local field service office, local sales person or Motorola representative. Please note that you will need to supply details such as: mask option selections; temperature range; oscillator frequency; package type; electrical test requirements; and device marking details so that an order can be processed, and a customer specific part number allocated. Refer to Table 13-1 for appropriate part numbers. The part number consists of the device title plus the appropriate suffix. For example, the MC68HC05B6 in 52-pin PLCC package at –40 to +85˚C would be ordered as: MC68HC05B6CFN.

Table 13-1 MC order numbers

Device Title	Package Type	Suffix 0 to 70 C	Suffix -40 to +85 C	Suffix -40 to +105 C	Suffix -40 to +125 C
MC68HC05B6	52-pin PLCC	FN	CFN	N/A	MFN
	64-pin QFP	FU	CFU	N/A	MFU
	56-pin SDIP	B	CB	N/A	MB
MC68HC05B4	52-pin PLCC	FN	CFN	N/A	MFN
	56-pin SDIP	B	CB	N/A	MB
MC68HC05B8	52-pin PLCC	FN	CFN	N/A	MFN
	64-pin QFP	FU	CFU	N/A	MFU
	56-pin SDIP	B	CB	N/A	MB
MC68HC05B16	52-pin PLCC	FN	CFN	VFN	N/A
	64-pin QFP	FU	CFU	VFU	N/A
	56-pin SDIP	B	CB	VB	N/A
MC68HC05B32	52-pin PLCC	FN	N/A	VFN	N/A
	64-pin QFP	FU	N/A	VFU	N/A
	56-pin SDIP	B	N/A	VB	N/A
MC68HC705B5	52-pin PLCC	FN	CFN	VFN	MFN
	56-pin SDIP	B	CB	VB	MB
MC68HC705B16	52-pin PLCC	FN	CFN	VFN	N/A
	64-pin QFP	FU	CFU	VFU	N/A
MC68HC705B32	52-pin PLCC	FN	N/A	VFN	N/A
	64-pin QFP	FU	N/A	VFU	N/A
	56-pin SDIP	B	N/A	VB	N/A

13.1 EPROMS

For the MC68HC05B6, an 8 kbyte EPROM programmed with the customer's software (positive logic for address and data) should be submitted for pattern generation. All unused bytes should be programmed to $00. The size of EPROM which should be used for all other family members is listed in Table 13-2.

The EPROM should be clearly labelled, placed in a conductive IC carrier and securely packed.

Table 13-2 EPROMs for pattern generation

Device	Size of EPROM
MC68HC05B4	8 kbyte
MC68HC05B8	8 kbyte
MC68HC05B16	16 kbyte
MC68HC05B32	32 kbyte

13.2 Verification media

All original pattern media (EPROMs) are filed for contractual purposes and are not returned. A computer listing of the ROM code will be generated and returned with a listing verification form. The listing should be thoroughly checked and the verification form completed, signed and returned to Motorola. The signed verification form constitutes the contractual agreement for creation of the custom mask. If desired, Motorola will program blank EPROMs (supplied by the customer) from the data file used to create the custom mask, to aid in the verification process.

13.3 ROM verification units (RVU)

Ten MCUs containing the customer's ROM pattern will be provided for program verification. These units will have been made using the custom mask but are for ROM verification only. For expediency, they are usually unmarked and are tested only at room temperature (25 C) and at 5 Volts. These RVUs are included in the mask charge and are not production parts. They are neither backed nor guaranteed by Motorola Quality Assurance.

A
MC68HC05B4

The MC68HC05B4 is a device similar to the MC68HC05B6, but without EEPROM and having a reduced ROM size of 4 kbytes. The entire MC68HC05B6 data sheet applies to the MC68HC05B4, with the exceptions outlined in this appendix.

Features

- 4158 bytes User ROM (including 14 bytes User vectors)
- No EEPROM

Section 3.5, ‘EEPROM’, therefore, does not apply to the MC68HC05B4, and the register at address $07 only allows the user to select whether or not the ECLK should appear at PC2, using bit 3 of $07. All other bits of this register read as ‘0’.

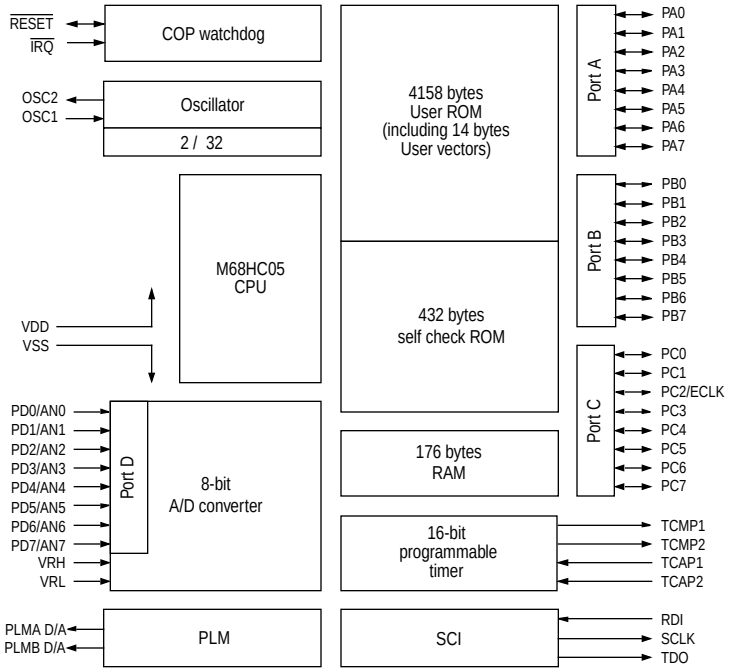


Figure A-1 MC68HC05B4 block diagram

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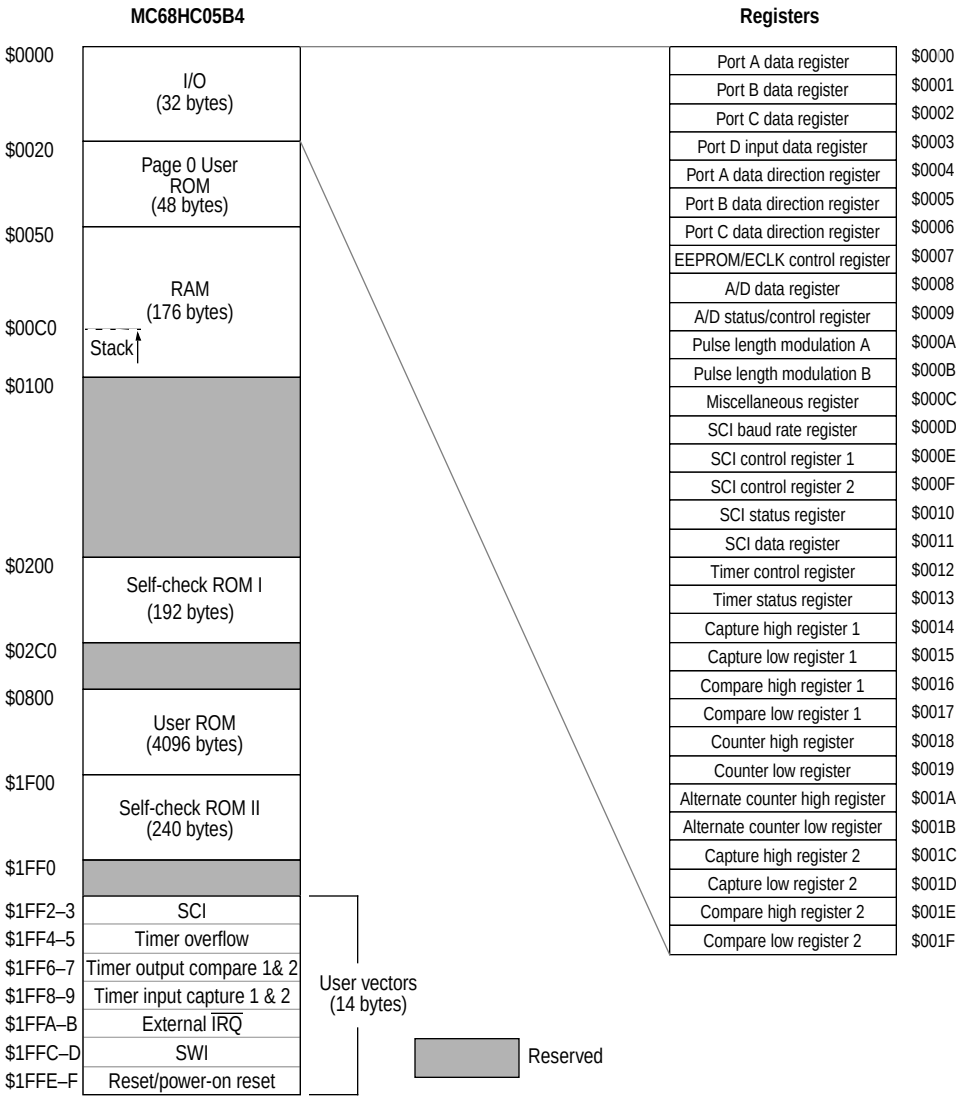

Figure A-2 Memory map of the MC68HC05B4

Table A-1 Register outline

Register name	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
Port A data (PORTA)	$0000									Undefined
Port B data (PORTB)	$0001									Undefined
Port C data (PORTC)	$0002						PC2/ ECLK			Undefined
Port D data (PORTD)	$0003	PD7/ AN7	PD6/ AN6	PD5/ AN5	PD4/ AN4	PD3/ AN3	PD2/ AN2	PD1/ AN1	PD0/ AN0	Undefined
Port A data direction (DDRA)	$0004									0000 0000
Port B data direction (DDRB)	$0005									0000 0000
Port C data direction (DDRC)	$0006									0000 0000
ECLK control	$0007	0	0	0	0	ECLK	0	0	0	0000 0000
A/D data (ADDATA)	$0008									0000 0000
A/D status/control (ADSTAT)	$0009	COCO	ADRC	ADON	0	CH3	CH2	CH1	CH0	0000 0000
Pulse length modulation A (PLMA)	$000A									0000 0000
Pulse length modulation B (PLMB)	$000B									0000 0000
Miscellaneous	$000C	POR(1)	INTP	INTN	INTE	SFA	SFB	SM	WDOG (2)	?001 000?
SCI baud rate (BAUD)	$000D	SPC1	SPC0	SCT1	SCT0	SCT0	SCR2	SCR1	SCR0	00uu uuuu
SCI control 1 (SCCR1)	$000E	R8	T8		M	WAKE	CPOL	CPHA	LBCL	uuuu uuuu
SCI control 2 (SCCR2)	$000F	TIE	TCIE	RIE	ILIE	TE	RE	RWU	SBK	0000 0000
SCI status (SCSR)	$0010	TDRE	TC	RDRF	IDLE	OR	NF	FE		1100 000u
SCI data (SCDR)	$0011									0000 0000
Timer control (TCR)	$0012	ICIE	OCIE	TOIE	FOLV2	FOLV1	OLV2	IEDG1	OLVL1	0000 00u0
Timer status (TSR)	$0013	ICF1	OCF1	TOF	ICF2	OCF2				uuuu uuuu
Input capture high 1	$0014									Undefined
Input capture low 1	$0015									Undefined
Output compare high 1	$0016									Undefined
Output compare low 1	$0017									Undefined
Timer counter high	$0018									1111 1111
Timer counter low	$0019									1111 1100
Alternate counter high	$001A									1111 1111
Alternate counter low	$001B									1111 1100
Input capture high 2	$001C									Undefined
Input capture low 2	$001D									Undefined
Output compare high 2	$001E									Undefined
Output compare low 2	$001F									Undefined

(1) This bit is set each time there is a power-on reset.

(2) The state of the WDOG bit after reset is dependent upon the mask option selected; 1=watchdog enabled, 0=watchdog disabled.

B
MC68HC05B8

The MC68HC05B8 is a device similar to the MC68HC05B6, but with an increased ROM size of 7.25 kbytes. The entire MC68HC05B6 data sheet applies to the MC68HC05B8, with the exceptions outlined in this appendix.

Features

- 7230 bytes User ROM (including 14 bytes User vectors)

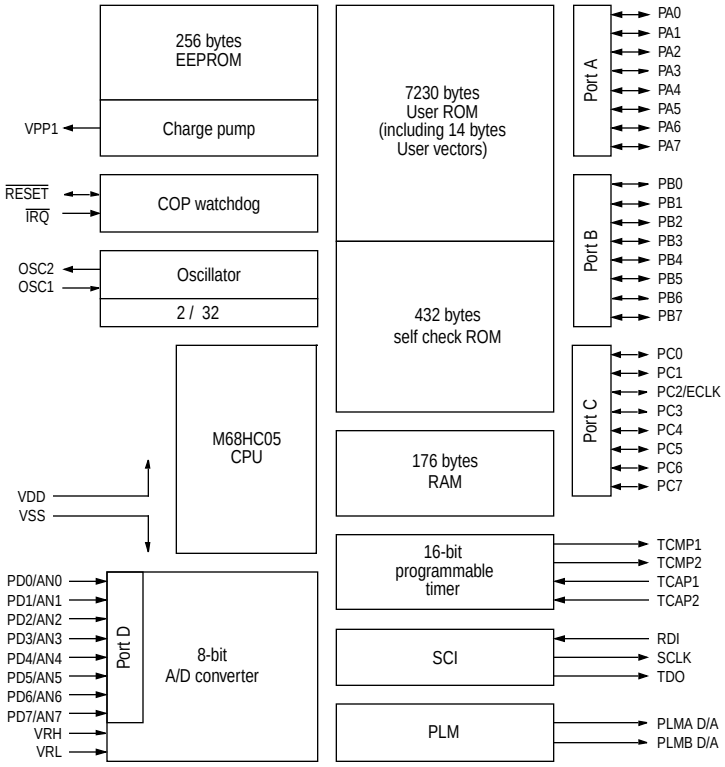

Figure B-1 MC68HC05B8 block diagram

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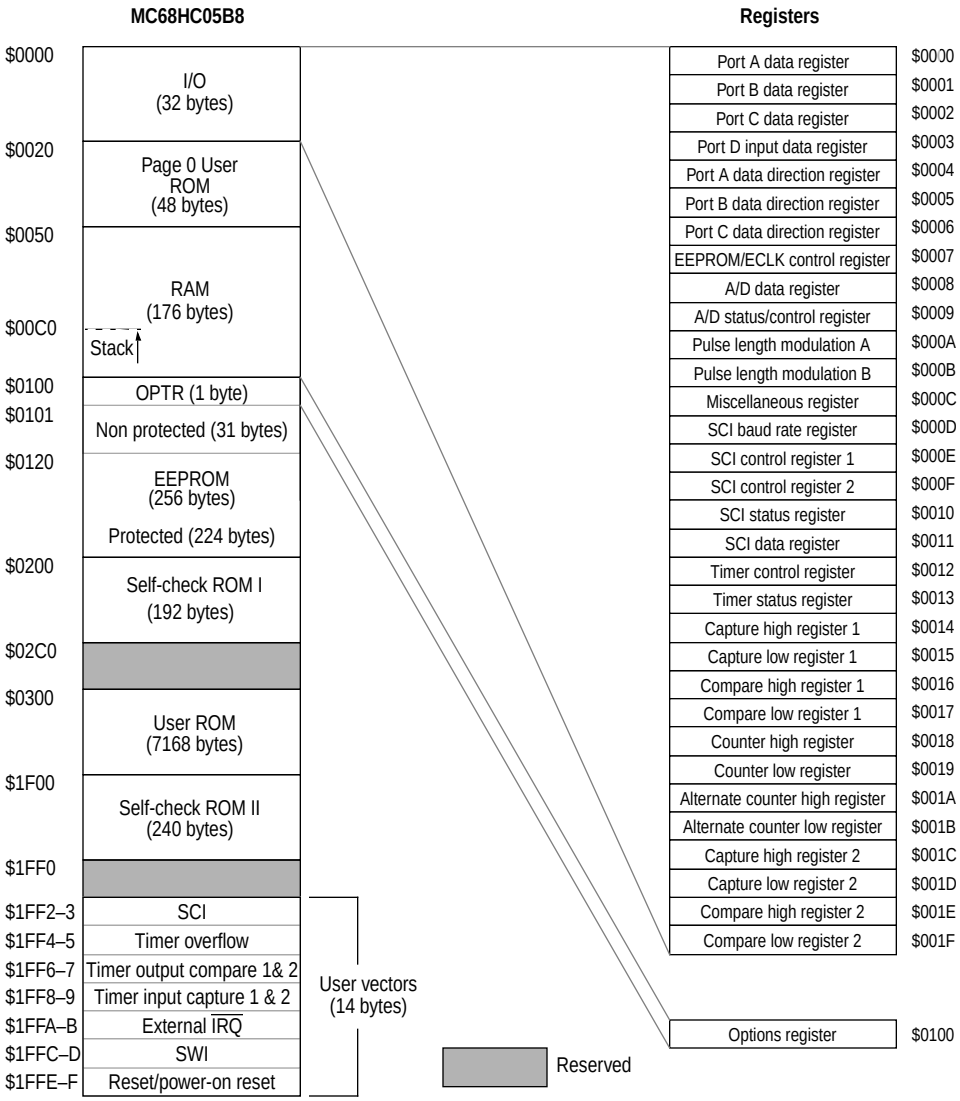


Figure B-2 Memory map of the MC68HC05B8

Table B-1 Register outline

Register name	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
Port A data (PORTA)	$0000									Undefined
Port B data (PORTB)	$0001									Undefined
Port C data (PORTC)	$0002						PC2/ ECLK			Undefined
Port D data (PORTD)	$0003	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0	Undefined
Port A data direction (DDRA)	$0004									0000 0000
Port B data direction (DDRB)	$0005									0000 0000
Port C data direction (DDRC)	$0006									0000 0000
EEPROM/ECLK control	$0007	0	0	0	0	ECLK	E1ERA	E1LAT	E1PGM	0000 0000
A/D data (ADDATA)	$0008									0000 0000
A/D status/control (ADSTAT)	$0009	COCO	ADRC	ADON	0	CH3	CH2	CH1	CH0	0000 0000
Pulse length modulation A (PLMA)	$000A									0000 0000
Pulse length modulation B (PLMB)	$000B									0000 0000
Miscellaneous	$000C	POR(1)	INTP	INTN	INTE	SFA	SFB	SM	WDOG(2)	?001 000?
SCI baud rate (BAUD)	$000D	SPC1	SPC0	SCT1	SCT0	SCT0	SCR2	SCR1	SCR0	00uu uuuu
SCI control 1 (SCCR1)	$000E	R8	T8		M	WAKE	CPOL	CPHA	LBCL	Undefined
SCI control 2 (SCCR2)	$000F	TIE	TCIE	RIE	ILIE	TE	RE	RWU	SBK	0000 0000
SCI status (SCSR)	$0010	TDRE	TC	RDRF	IDLE	OR	NF	FE		1100 000u
SCI data (SCDR)	$0011									0000 0000
Timer control (TCR)	$0012	ICIE	OCIE	TOIE	FOLV2	FOLV1	OLV2	IEDG1	OLVL1	0000 00u0
Timer status (TSR)	$0013	ICF1	OCF1	TOF	ICF2	OCF2				Undefined
Input capture high 1	$0014									Undefined
Input capture low 1	$0015									Undefined
Output compare high 1	$0016									Undefined
Output compare low 1	$0017									Undefined
Timer counter high	$0018									1111 1111
Timer counter low	$0019									1111 1100
Alternate counter high	$001A									1111 1111
Alternate counter low	$001B									1111 1100
Input capture high 2	$001C									Undefined
Input capture low 2	$001D									Undefined
Output compare high 2	$001E									Undefined
Output compare low 2	$001F									Undefined
Options (OPTR)(3)	$0100							EE1P	SEC	Not affected

(1) This bit is set each time there is a power-on reset.

(2) The state of the WDOG bit after reset is dependent upon the mask option selected; 1=watchdog enabled, 0=watchdog disabled.

(3) This register is implemented in EEPROM; therefore reset has no effect on the individual bits.

C
MC68HC705B5

The MC68HC705B5 is a device similar to the MC68HC05B6, but with the 6 kbytes ROM and 256 bytes EEPROM replaced by a single EPROM array. In addition, the self-check routines available on the MC68HC05B6 are replaced by bootstrap firmware. The MC68HC705B5 is intended to operate as a one time programmable (OTP) version of the MC68HC05B6 or the MC68HC05B4, meaning that the application program can never be erased once it has been loaded into the EPROM. The entire MC68HC05B6 data sheet applies to the MC68HC705B5, with the exceptions outlined in this appendix.

Features

- 6206 bytes EPROM (including 14 bytes User vectors)
- No EEPROM
- Bootstrap firmware
- Simultaneous programming of up to 4 bytes
- Data protection for program code
- Optional pull-down resistors on port B and port C
- Additional temperature range available; -40 to +105 C
- MC68HC05B6 mask options are programmable using control bits held in the options register

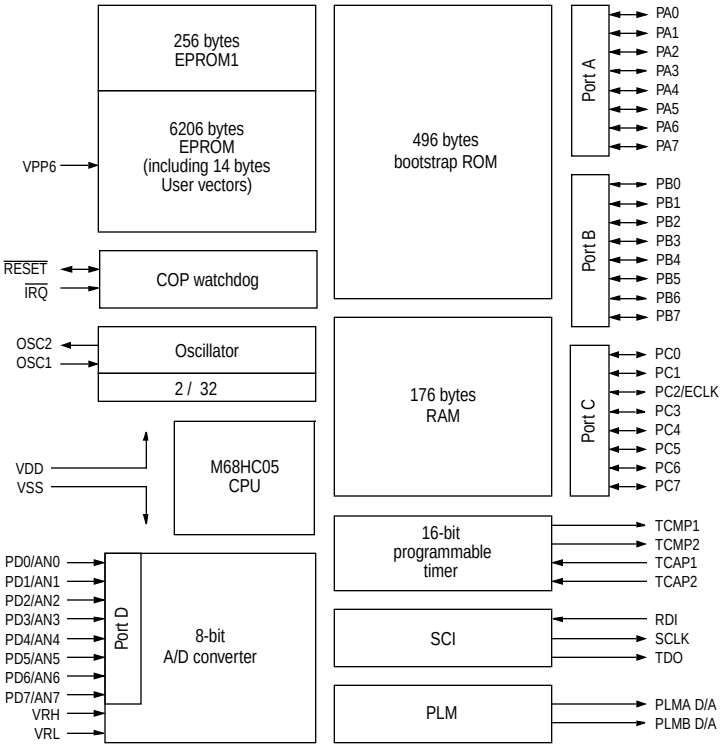


Figure C-1 MC68HC705B5 block diagram

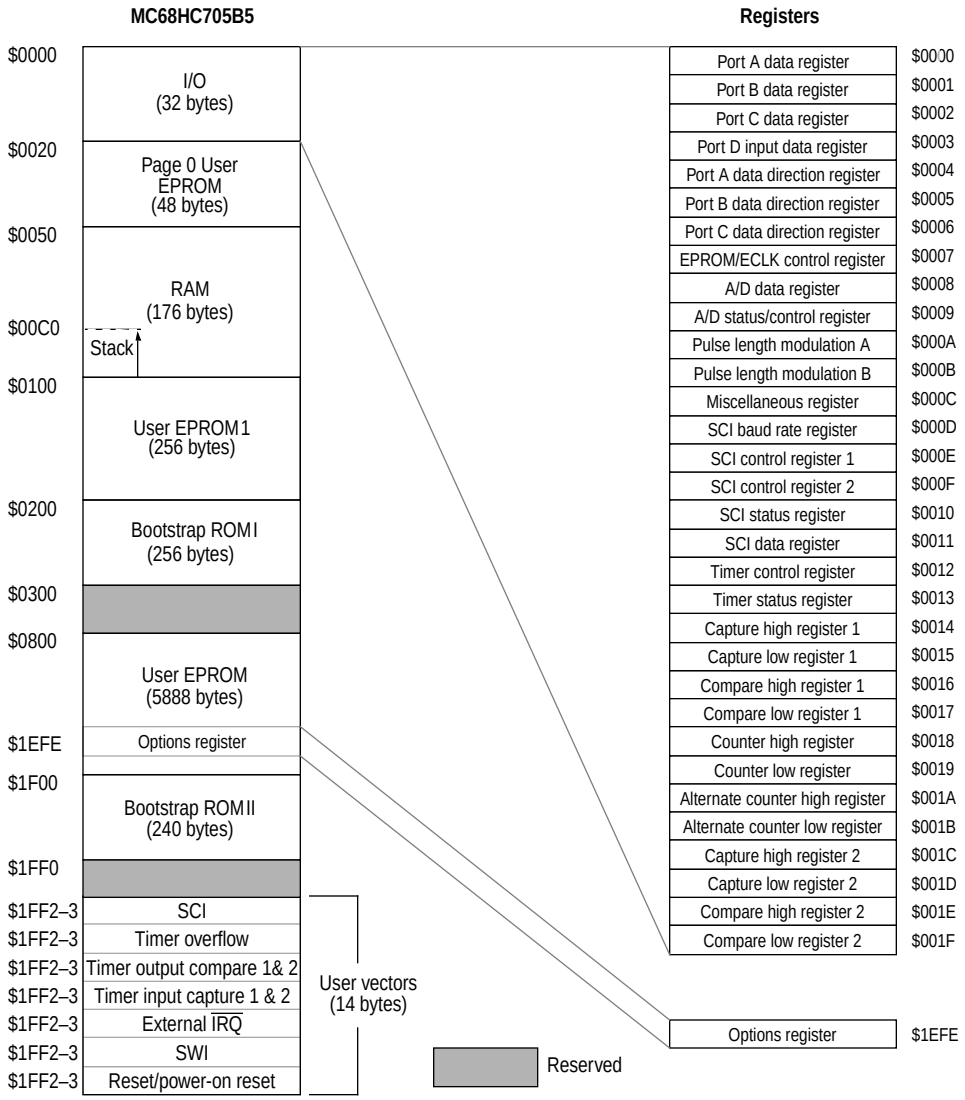


Figure C-2 Memory map of the MC68HC705B5

Table C-1 Register outline

Register name	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
Port A data (PORTA)	$0000									Undefined
Port B data (PORTB)	$0001									Undefined
Port C data (PORTC)	$0002						PC2/ ECLK			Undefined
Port D data (PORTD)	$0003	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0	Undefined
Port A data direction (DDRA)	$0004									0000 0000
Port B data direction (DDRB)	$0005									0000 0000
Port C data direction (DDRC)	$0006									0000 0000
EPROM/ECLK control	$0007		EPPT(1)	ELAT	EPGM	ECLK				u?00 0uuu
A/D data (ADDATA)	$0008									0000 0000
A/D status/control (ADSTAT)	$0009	COCO	ADRC	ADON	0	CH3	CH2	CH1	CH0	0000 0000
Pulse length modulation A (PLMA)	$000A									0000 0000
Pulse length modulation B (PLMB)	$000B									0000 0000
Miscellaneous	$000C	POR(2)	INTP	INTN	INTE	SFA	SFB	SM	WDOG(3)	?001 000?
SCI baud rate (BAUD)	$000D	SPC1	SPC0	SCT1	SCT0	SCT0	SCR2	SCR1	SCR0	00uu uuuu
SCI control 1 (SCCR1)	$000E	R8	T8		M	WAKE	CPOL	CPHA	LBCL	uuuu
SCI control 2 (SCCR2)	$000F	TIE	TCIE	RIE	ILIE	TE	RE	RWU	SBK	0000 0000
SCI status (SCSR)	$0010	TDRE	TC	RDRF	IDLE	OR	NF	FE		1100 000u
SCI data (SCDR)	$0011									0000 0000
Timer control (TCR)	$0012	ICIE	OCIE	TOIE	FOLV2	FOLV1	OLV2	IEDG1	OLVL1	0000 00u0
Timer status (TSR)	$0013	ICF1	OCF1	TOF	ICF2	OCF2				uuuu
Input capture high 1	$0014									Undefined
Input capture low 1	$0015									Undefined
Output compare high 1	$0016									Undefined
Output compare low 1	$0017									Undefined
Timer counter high	$0018									1111 1111
Timer counter low	$0019									1111 1100
Alternate counter high	$001A									1111 1111
Alternate counter low	$001B									1111 1100
Input capture high 2	$001C									Undefined
Input capture low 2	$001D									Undefined
Output compare high 2	$001E									Undefined
Output compare low 2	$001F									Undefined
Options (OPTR)(4)	$1EFE		EPP	0	RTIM	RWAT	WWAT	PBPD	PCPD	Not affected

(1) This bit reflects the state of the EPP bit in the options register ($1EFE) at reset.

(2) This bit is set each time the device is powered-on.

(3) The state of the WDOG bit after reset depends on the mask option selected; ‘1’ = watchdog enabled and ‘0’ = watchdog disabled.

(4) Because this register is implemented in EPROM, reset has no effect on the state of the individual bits.

C.1 EPROM

The MC68HC705B5 has a total of 6206 bytes of EPROM, 256 bytes being reserved for the EPROM1 array (see Figure C-2). The EPP bit (EPROM protect) is not operative on the EPROM1 array, making it possible to program it after the main EPROM has been programmed and protected. The reset and interrupt vectors are located at $1FF2-$1FFF and the EPROM control register described in Section C.2.1 is located at address $0007.

The EPROM array is supplied by the VPP6 pin in both read and programming modes. Typically the user's software will be loaded in a programming board where VPP6 is controlled by one of the bootstrap loader routines (bootloader mode). It will then be placed in an application where no programming occurs (user mode). In this case the VPP6 pin should be hardwired to V_{DD}.

An erased EPROM byte reads as $00.

Warning: A minimum V_{DD} voltage must be applied to the VPP6 pin at all times, including power-on, as a lower voltage could damage the device.

C.1.1 EPROM programming operation

The User program can be used to program some EPROM locations, provided the proper procedure is followed. In particular, the programming sequence must be running in RAM, as the EPROM will not be available for code execution while the ELAT bit is set. The VPP6 switching must occur externally, after the EPGM bit is set, for example, under the control of a signal generated on a pin by the programming routine.

Note: When the part becomes a PROM, only the cumulative programming of bits to logic 1 is possible if multiple programming is made on the same byte.

To allow simultaneous programming of up to 4 bytes, they must be in the same group of addresses which share the same most significant address bits; only the two LSBs can change.

C.2 EPROM registers

C.2.1 EPROM control register

	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
EPROM/ECLK control	$0007		EPPT(1)	ELAT	EPGM	ECLK				u?00 0uuu

(1) This bit is a copy of the EPP bit in the options register at $1EFE and therefore its state on reset will be the same as that for the EPP bit.

Bit 7 — Factory use only

This bit is strictly for factory use only and will always read zero.

EPPT — EPROM protect test bit

This bit is a copy of the EPROM protect bit (EPP) located in the option register. When ELAT is set, the EPPT bit can be tested by the software to check if the EPROM array is protected or not, since the EPROM content is not available when ELAT is set.

POR or external reset modifies this bit to reflect the state of the EPP bit in the options register.

ELAT — EPROM programming latch enable bit

1 (set) – When set, this bit allows latching of the address and up to 4 data bytes for further programming, provided EPGM is zero.

0 (clear) – When cleared, program and interrupt routines can be executed and data can be read in the EPROM or firmware ROM.

STOP, power-on and external reset clear this bit.

EPGM — EPROM programming bit

This bit is the EPROM program enable bit. It can be set to ‘1’ to enable programming only after ELAT is set and at least one byte is written to the EPROM. It is not possible to clear EPGM by software, but clearing ELAT will always clear EPGM.

ECLK — External clock option bit

See Section 4.3.

C.3 Options register (OPTR)

	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
Options (OPTR)(1)	$1EFE		EPP	0	RTIM	RWAT	WWAT	PBPD	PCPD	Not affected

(1) This register is implemented in EPROM, therefore reset has no effect on the state of the individual bits.

Note: This register can only be written to while the device is in bootloader mode.

Bit 7 — Factory use only

Warning: This bit is strictly for factory use only and will always read zero to avoid accidental damage to the device. Any attempt to write to this bit could result in physical damage.

EPP — EPROM protect

This bit protects the contents of the main EPROM against accidental modification; it has no effect on reading or executing code in the EPROM.

1 (set) – EPROM contents are protected.

0 (clear) – EPROM contents are not protected.

RTIM — Reset time

This bit can modify t_{PORL}, i.e. the time that the $\overline{\text{RESET}}$ pin is kept low following a power-on reset. This feature is handled in the ROM part via a mask option.

1 (set) – t_{PORL} = 16 cycles.

0 (clear) – t_{PORL} = 4064 cycles.

RWAT — Watchdog after reset

This bit can modify the status of the watchdog counter after reset.

1 (set) – The watchdog will be active immediately following power-om or external reset (except in bootstrap mode).

0 (clear) – The watchdog system will be disabled after power-on or external reset.

WWAT — Watchdog during WAIT mode

This bit can modify the status of the watchdog counter during WAIT mode.

1 (set) – The watchdog will be active during WAIT mode.

0 (clear) – The watchdog system will be disabled during WAIT mode.

PBPD – Port B pull-down resistors

1 (set) – Pull-down resistors are connected to all 8 pins of port B; the pull-down, R_{PD}, is active only while the pin is an input.

0 (clear) – No pull-down resistors are connected.

PCPD — Port C pull-down resistors

1 (set) – Pull-down resistors are connected to all 8 pins of port C; the pull-down, R_{PD}, is active only while the pin is an input.

0 (clear) – No pull-down resistors are connected.

The combination of bit 0 and bit 1 allows the option of pull-down resistors on 0, 8 or 16 inputs. This feature is not available on the MC68HC05B6.

C.4 Bootstrap mode

The 432 bytes of self-check firmware on the MC68HC05B6 are replaced with 496 bytes of bootstrap firmware. The bootstrap firmware located from $0200 to $02FF and $1F00 to $1FEF can be used to program the EPROM, to check if the EPROM is erased and to load and execute data in RAM.

When the MC68HC705B5 is placed in the bootstrap mode, the bootstrap reset vector is fetched and the bootstrap firmware starts to execute. Table C-2 shows the conditions required to enter each level of bootstrap mode on the rising edge of $\overline{\text{RESET}}$. The hold time on the $\overline{\text{IRQ}}$ and TCAP1 pins after the external $\overline{\text{RESET}}$ pin is brought high is two clock cycles.

Table C-2 Mode of operation selection

$\overline{\text{IRQ}}$ pin	TCAP1 pin	PD2	PD3	PD4	Mode
V_{SS} to V_{DD}	V_{SS} to V_{DD}	x	x	x	Single chip
+ 9 Volts	V_{DD}	0	1	0	Erased EPROM verification
+ 9 Volts	V_{DD}	x	0	0	EPROM parallel bootstrap load
+ 9 Volts	V_{DD}	x	1	1	EPROM (RAM) serial bootstrap load and execute
+ 9 Volts	V_{DD}	x	0	1	RAM parallel bootstrap load and execute

x = Don't care

The bootstrap program first copies part of itself into RAM, as the program cannot be executed in ROM during verification/programming of the EPROM. It then sets the TCMP1 output to a logic high level.

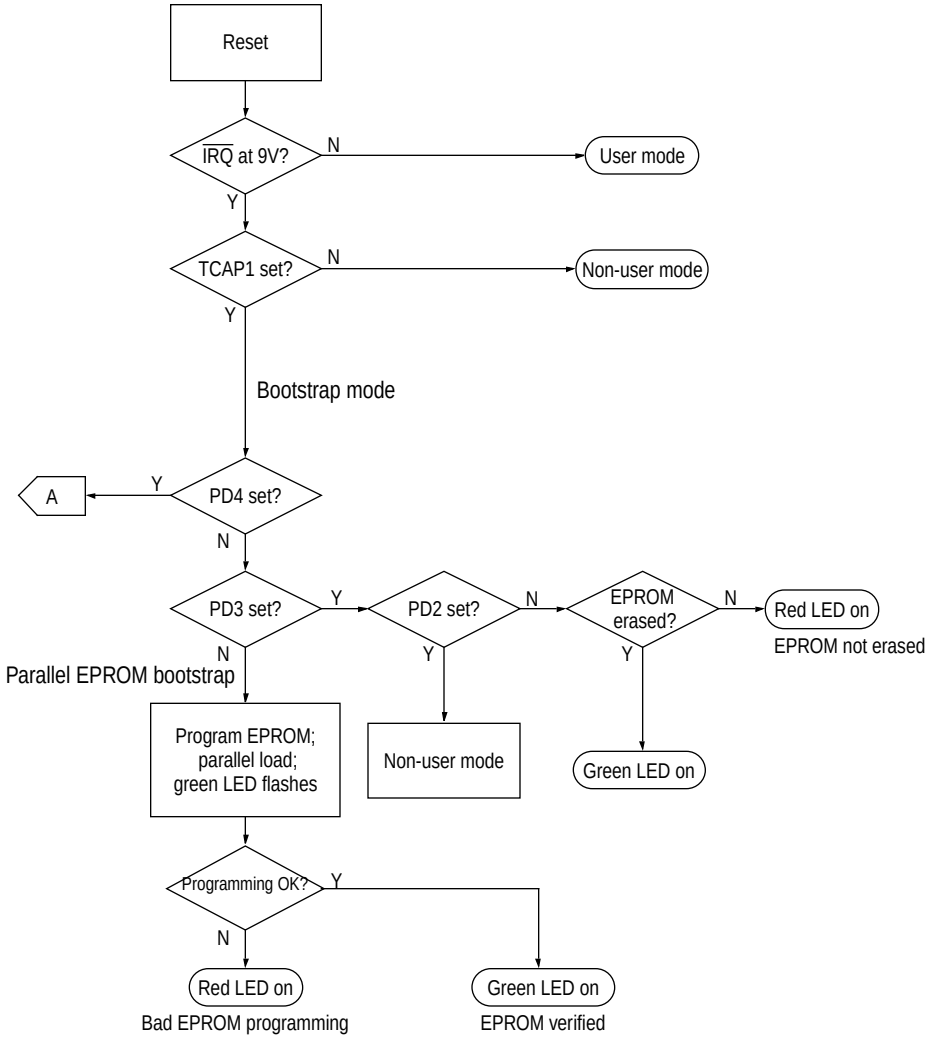


Figure C-3 Modes of operation flow chart (1 of 2)

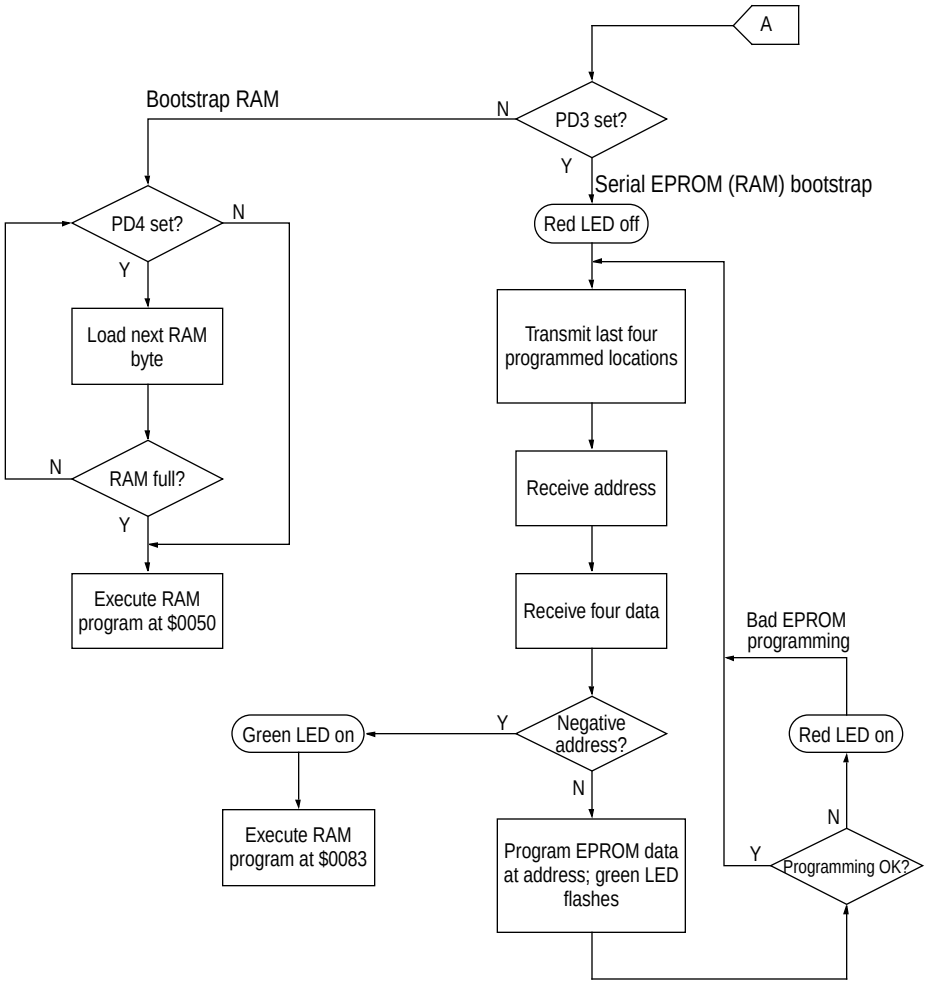


Figure C-4 Modes of operation flow chart (2 of 2)

C.4.1 Erased EPROM verification

The flowchart in Figure C-3 and Figure C-4 shows that the on-chip bootstrap routines can be used to check if the EPROM is erased (all $00s). If a non $00 byte is detected, the red LED stays on and the routine will stay in a loop. Only when the whole EPROM content is verified as erased will the green LED be turned on.

C.4.2 EPROM parallel bootstrap load

When this mode is selected, the EPROM is loaded in increasing address order with non EPROM segments being skipped by the loader. Simultaneous programming is performed by reading four bytes of data before actual programming is performed, thus dividing the loading time of the internal EPROM by four.

When PD2=0, the programming time is set to 5 milliseconds and the program/verify routine takes approximately 15 seconds.

Parallel data is entered through Port A, while the 13-bit address is output on port B and PC0 to PC4. If the data comes from an external EPROM, the handshake can be disabled by connecting together PC5 and PC6. If the data is supplied via a parallel interface, handshaking will be provided by PC5 and PC6 according to the timing diagram of Figure C-5.

During programming, the green LED flashes at about 3 Hz.

Upon completion of the programming operation, the EPROM content is checked against the external data source. If programming is verified the green LED stays on, while an error causes the red LED to be turned on. Figure C-6 shows a circuit that can be used to program the EPROM (or to load and execute data in the RAM).

Note: The entire EPROM can be loaded from the external source; if it is desired to leave a segment undisturbed, the data for this segment should be all zeros.

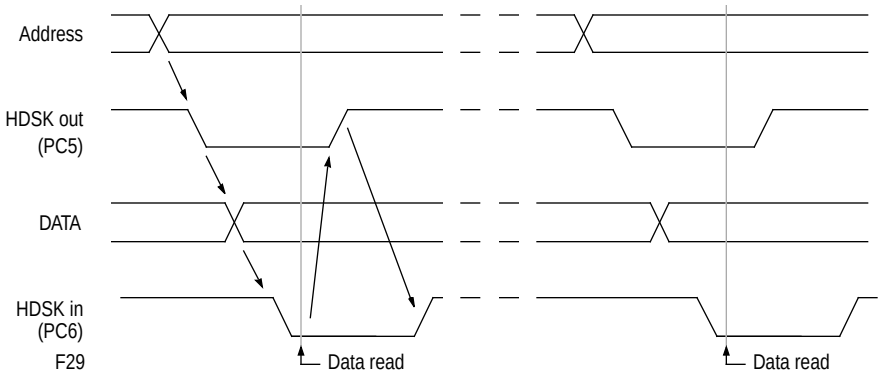


Figure C-5 Timing diagram with handshake

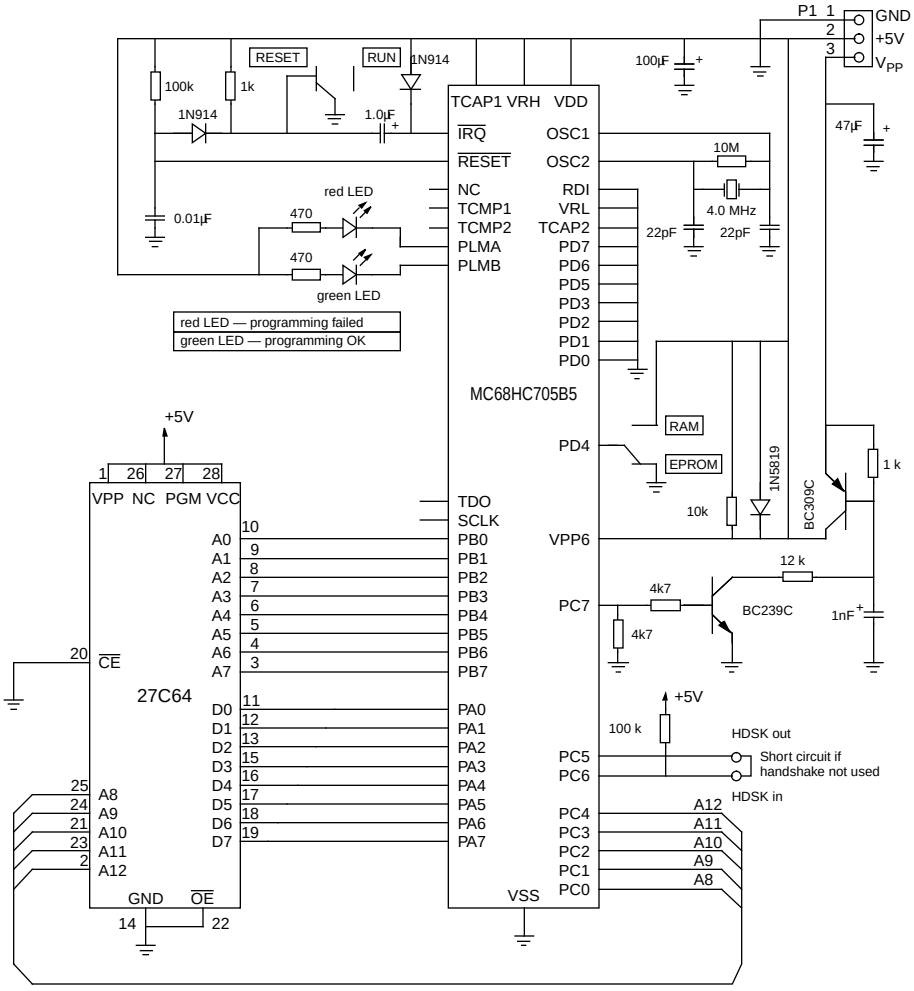


Figure C-6 EPROM(RAM) parallel bootstrap schematic diagram

C.4.3 EPROM (RAM) serial bootstrap load and execute

The serial routine communicates through the SCI with an external host, typically a PC, by means of an RS232 link at 9600 baud, 8-bit, no parity and full duplex.

Data format is not ASCII, but 8-bit binary, so a complementary program must be run by the host to supply the required format. Such a program is available for the IBM PC from Motorola.

The EPROM bootstrap routines are used to customise the OTP EPROM. To increase the speed of programming, four bytes are programmed in parallel while the data is simultaneously transmitted and received in full duplex. This implies that while 4 bytes are being programmed, the next 4 bytes are received and the preceding 4 bytes are echoed. The format accepted by the serial loader is as follows:

[address n high] [address n low] [data(n)] [data (n+1)] [data (n+2)] [data (n+3)]

Address n must have the two LSBs at zero so that n, n+1, n+2 and n+3 have identical MSBs. These blocks of four bytes do not need to be contiguous, as a new address is transmitted for each new group.

The protocol is as follows:

1. The MC68HC705B5 sends the last two bytes programmed to the host as a prompt; this allows verification by the host of proper programming.
2. In response to the first byte prompt, the host sends the first address byte.
3. After receiving the first address byte, the MC68HC705B5 sends the next byte programmed.
4. The exchange of data continues until the MC68HC705B5 has sent the four data bytes and the host has sent the 2 address data bytes and 4 data bytes.
5. If the data is non zero, it is programmed at the address provided, while the next address and bytes are received and the previous data is echoed.
6. Loop to 1.

After reset, the MC68HC705B5 serial bootstrap routine will first echo two blocks of four bytes at $0000, as no data is programmed yet.

If the data sent in is $00, no programming in the EPROM takes place, and the contents of the accessed location are returned as a prompt. The entire EPROM memory can be read in this fashion (serial dump). The red LED will be on if the data read from the EPROM is not $00.

Serial RAM loading and execute can be accomplished in this mode. A RAM byte will be written if the address sent by the host in the serial protocol points to the RAM.

In the RAM bootloader mode, all interrupt vectors are mapped to pseudo-vectors in RAM (see Table C-3). This allows programmers to use their own service-routine addresses. Each pseudo-vector is allowed three bytes of space rather than the two bytes for normal vectors, because an explicit jump (JMP) opcode is needed to cause the desired jump to the user's service-routine address.

Table C-3 Bootstrap vector targets in RAM

Vector targets in RAM	
SCI interrupt	$00E4
Timer overflow	$00E7
Timer output compare	$00EA
Timer input capture	$00ED
$\overline{IRQ}$	$00F0
SWI	$00F3

A 10-byte stack is also reserved at the top of the RAM allowing, for example, one interrupt and two sub-routine levels.

Program execution is triggered by sending a negative (bit 7 set) high address; execution starts at address XADR ($0083).

The RAM addresses between $0050 and $0082 are used by the loader and are therefore not available to the user during serial loading/executing.

Refer to Figure C-7 shows a suitable circuit. Figure C-9 shows address and data bus timing.

C.4.4 RAM parallel bootstrap load and execute

The RAM bootstrap program will start loading the RAM with external data (e.g. from a 2564 or 2764 EPROM). Before loading a new byte, the state of the PD4/AN4 pin is checked; if this pin goes to level ‘0’, or if the RAM is full, then control is given to the loaded program at address $0050.

If the data is supplied by a parallel interface, handshaking will be provided by PC5 and PC6 according to Figure C-10. If the data comes from an external EPROM, the handshake can be disabled by connecting together PC5 and PC6.

Figure C-8 shows a circuit that can be used to load the RAM with short test programs. Up to 8 programs can be loaded in turn from the EPROM. Selection is accomplished by means of the switches connected to the EPROM higher address lines (A8 through A10). If the user program sets PC0 to level ‘1’, the external EPROM will be disabled, rendering both port A outputs and port B inputs available.

The EPROM parallel bootstrap loader circuit (Figure C-6) can also be used, provided VPP is tied to V_{DD}. The high order address lines will be at zero. The LEDs will stay off.

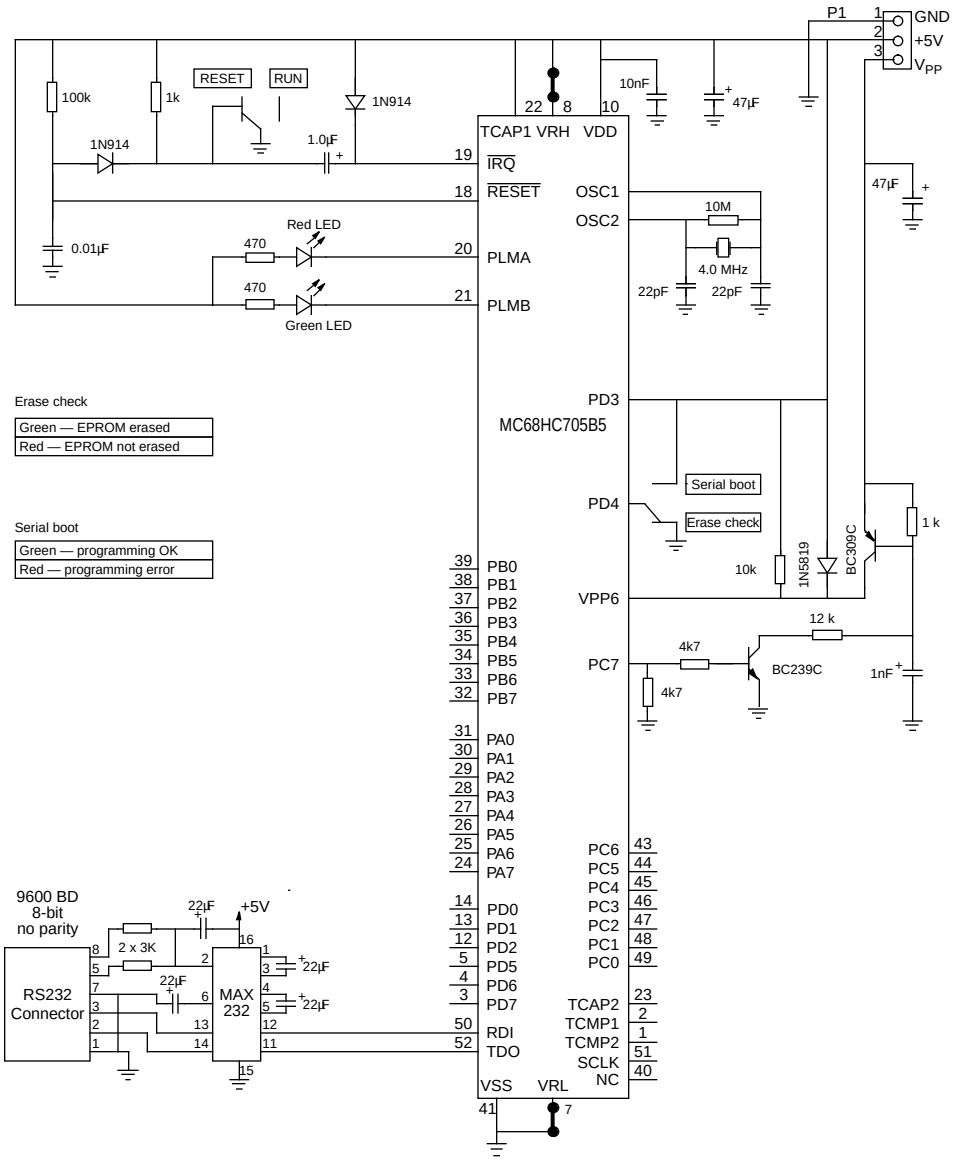


Figure C-7 EPROM (RAM) serial bootstrap schematic diagram

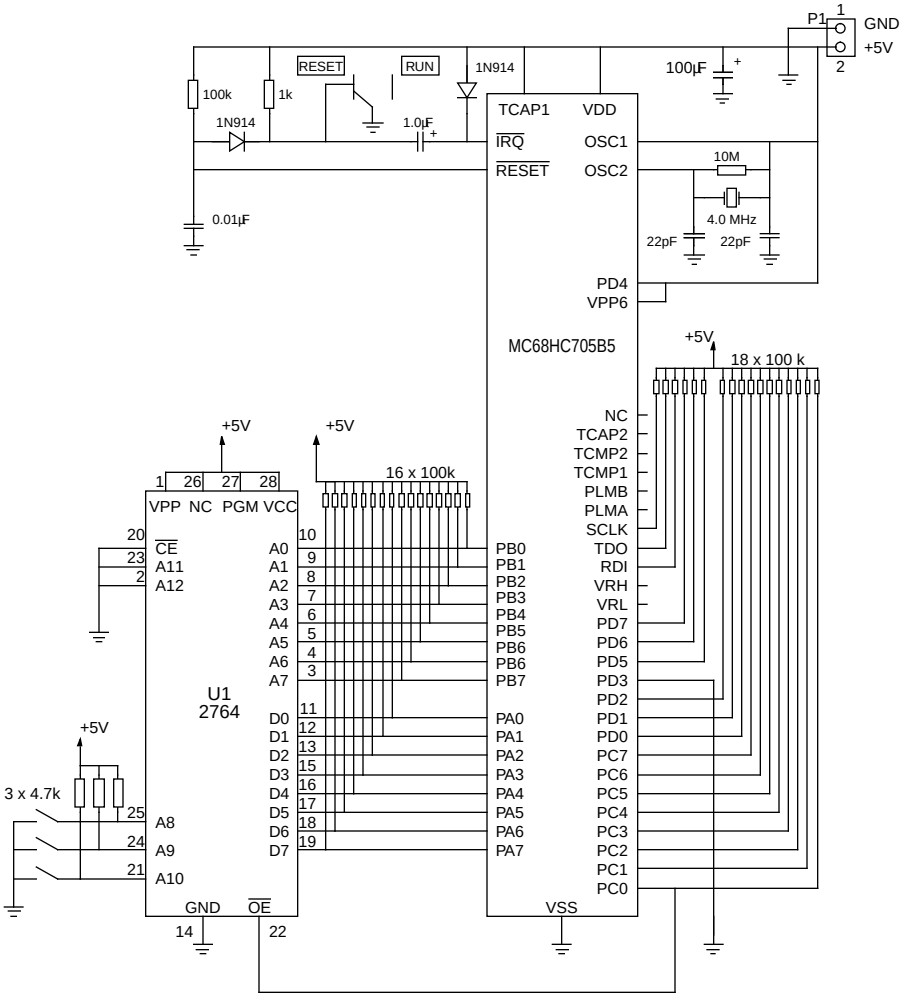
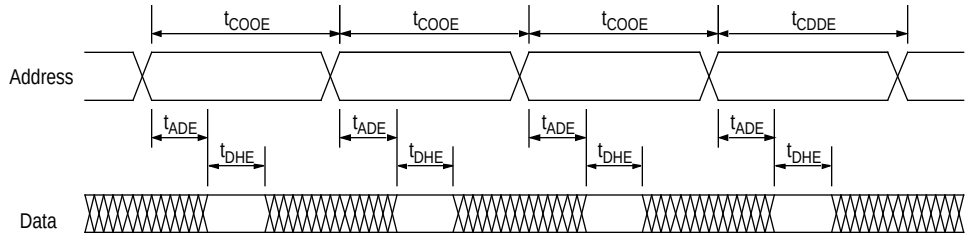


Figure C-8 RAM parallel bootstrap schematic diagram

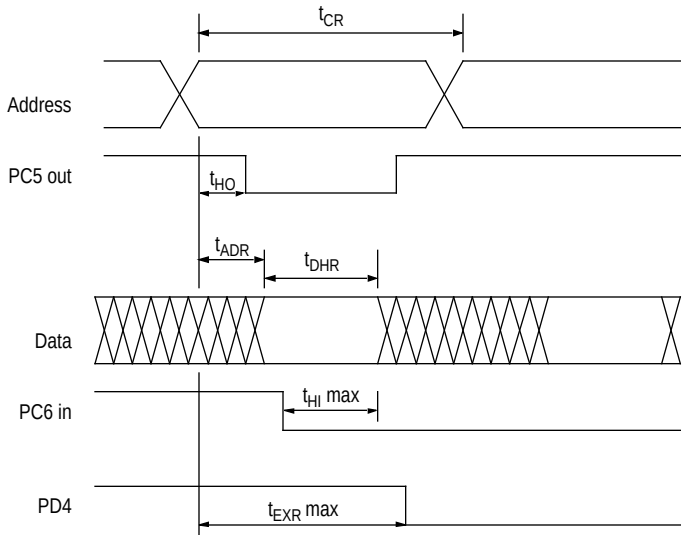
C.4.5 Bootstrap loader timing diagrams



t_{ADE} max (address to data delay)	5 machine cycles
t_{DHA} min (data hold time)	14 machine cycles
t_{COOE} (load cycle time)	117 machine cycles < t_{COOE} < 150 machine cycles
t_{CDDE} (programming cycle time)	t_{COOE} + t_{PROG} (5 ms nominal)

1 machine cycle = $1/(2f_0(Xtal))$

Figure C-9 EPROM parallel bootstrap loader timing diagram



t_{ADR} max (address to data delay; PC6=PC5)	16 machine cycles
t_{DHR} min (data hold time)	4 machine cycles
t_{CR} (load cycle time; PC6=PC5)	49 machine cycles
t_{HO} (PC5 handshake out delay)	5 machine cycles
t_{HI} max (PC6 handshake in, data hold time)	10 machine cycles
t_{EXR} max (max delay for transition to be recognised during this cycle; PC6=PC5	30 machine cycles

1 machine cycle = $1/(2f_0(Xtal))$

Figure C-10 RAM parallel loader timing diagram

C.5 DC electrical characteristics

Note: The complete table of DC electrical characteristics can be found in Section 11.3. The values contained in the following table should be used in conjunction with those quoted in that section.

Table C-4 Additional DC electrical characteristics for MC68HC705B5

(V_{DD} = 5 Vdc 10%, V_{SS} = 0 Vdc, T_A = 25 C)

Characteristic	Symbol	Min	Typ	Max	Unit
Input current Port B and port C pull-down (V_{IN}=V_{IH})	I_{RPD}		80		µA
EPROM absolute maximum voltage	V_{PP6} max	V_{DD}	—	18	V
EPROM programming voltage	V_{PP6}	15.0	15.5	16	V
EPROM programming current	I_{PP6}	—	—	18	mA
EPROM read voltage	V_{PP6R}	V_{DD}	V_{DD}	V_{DD}	V

C.6 Control timing

Note: The complete table of control timing can be found in Section 11.5. The values contained in the following table should be used in conjunction with those quoted in that section.

Table C-5 Additional control timing for MC68HC705B5

(V_{DD} = 5 Vdc 10%, V_{SS} = 0 Vdc, T_A = 25 C)

Characteristic	Symbol	Min	Typ	Max	Unit
EPROM programming time	t_{PROG}	5	—	20	ms

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D
MC68HC05B16

The MC68HC05B16 is a device similar to the MC68HC05B6, but with increased RAM, ROM and self-check ROM sizes. The entire MC68HC05B6 data sheet, including the electrical characteristics, applies to the MC68HC05B16, with the exceptions outlined in this appendix.

Features

- 15 kbytes User ROM
- 352 bytes of RAM
- 496 bytes self-check ROM
- 52-pin PLCC, 56-pin SDIP and 64-pin QFP packages

D.1 Self-check routines

The self-check routines for the MC68HC05B16 are identical to those of the MC68HC05B6 with the following exception.

The count byte on the MC68HC05B16 can be any value up to 256 ($00). The first 176 bytes are loaded into RAM I and the remainder is loaded into RAM II starting at $0250.

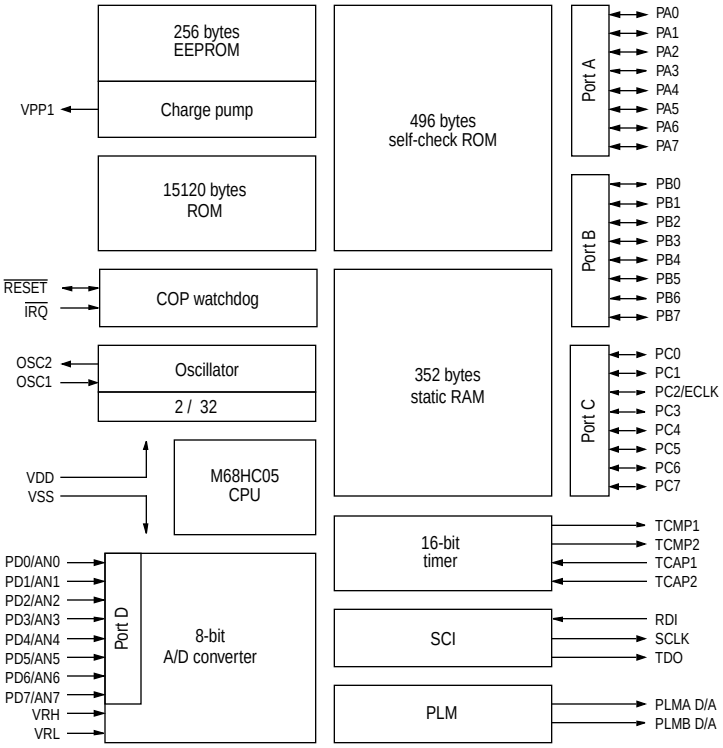

Figure D-1 MC68HC05B16 block diagram

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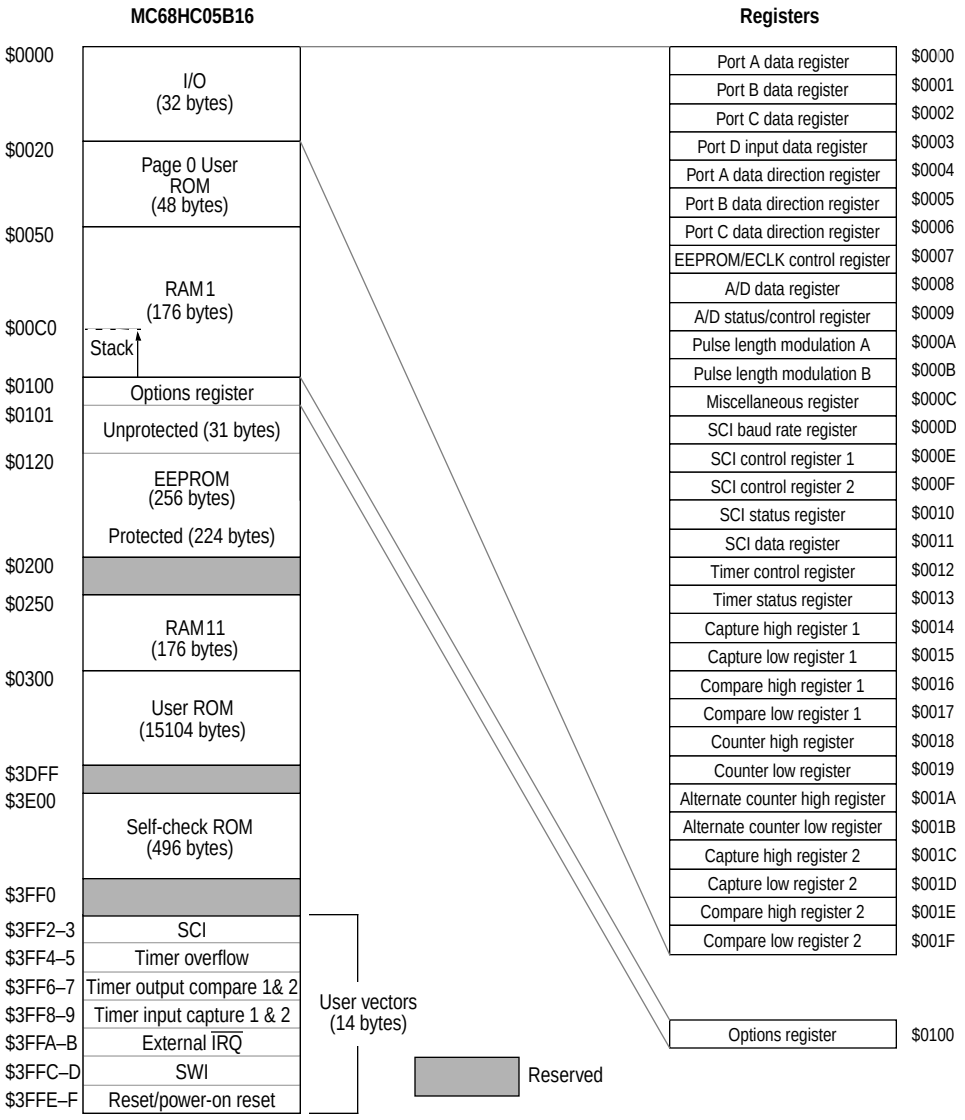

Figure D-2 Memory map of the MC68HC05B16

Table D-1 Register outline

Register name	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
Port A data (PORTA)	$0000									Undefined
Port B data (PORTB)	$0001									Undefined
Port C data (PORTC)	$0002						PC2/ ECLK			Undefined
Port D data (PORTD)	$0003	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0	Undefined
Port A data direction (DDRA)	$0004									0000 0000
Port B data direction (DDRB)	$0005									0000 0000
Port C data direction (DDRC)	$0006									0000 0000
EEPROM/ECLK control	$0007	0	0	0	0	ECLK	E1ERA	E1LAT	E1PGM	0000 0000
A/D data (ADDATA)	$0008									0000 0000
A/D status/control (ADSTAT)	$0009	COCO	ADRC	ADON	0	CH3	CH2	CH1	CH0	0000 0000
Pulse length modulation A (PLMA)	$000A									0000 0000
Pulse length modulation B (PLMB)	$000B									0000 0000
Miscellaneous	$000C	POR(1)	INTP	INTN	INTE	SFA	SFB	SM	WDOG(2)	?001 000?
SCI baud rate (BAUD)	$000D	SPC1	SPC0	SCT1	SCT0	SCT0	SCR2	SCR1	SCR0	00uu uuuu
SCI control 1 (SCCR1)	$000E	R8	T8		M	WAKE	CPOL	CPHA	LBCL	Undefined
SCI control 2 (SCCR2)	$000F	TIE	TCIE	RIE	ILIE	TE	RE	RWU	SBK	0000 0000
SCI status (SCSR)	$0010	TDRE	TC	RDRF	IDLE	OR	NF	FE		1100 000u
SCI data (SCDR)	$0011									0000 0000
Timer control (TCR)	$0012	ICIE	OCIE	TOIE	FOLV2	FOLV1	OLV2	IEDG1	OLVL1	0000 00u0
Timer status (TSR)	$0013	ICF1	OCF1	TOF	ICF2	OCF2				Undefined
Input capture high 1	$0014									Undefined
Input capture low 1	$0015									Undefined
Output compare high 1	$0016									Undefined
Output compare low 1	$0017									Undefined
Timer counter high	$0018									1111 1111
Timer counter low	$0019									1111 1100
Alternate counter high	$001A									1111 1111
Alternate counter low	$001B									1111 1100
Input capture high 2	$001C									Undefined
Input capture low 2	$001D									Undefined
Output compare high 2	$001E									Undefined
Output compare low 2	$001F									Undefined
Options (OPTR)(3)	$0100							EE1P	SEC	Not affected

(1) This bit is set each time there is a power-on reset.

(2) The state of the WDOG bit after reset is dependent upon the mask option selected; 1=watchdog enabled, 0=watchdog disabled.

(3) This register is implemented in EEPROM; therefore reset has no effect on the individual bits.

E
MC68HC705B16

To ensure correct operation of the MC68HC705B16 after power-on, the device must be reset a second time after power-on. This can be done in software using the MC68HC705B16 watchdog.

The following software sub-routine should be used:

```
RESET2    BSET    0, $0C    Start watchdog
          STOP              STOP causes immediate watchdog
                            system reset
```

The interrupt vector at $3FF0 and $3FF1 must be initialised with the RESET2 address value.

The MC68HC705B16 is a device similar to the MC68HC05B6, but with increased RAM and 15 kbytes of EPROM instead of 6 kbytes of ROM. In addition, the self-check routines available in the MC68HC05B6 are replaced by bootstrap firmware. The MC68HC705B16 is an OTPROM (one-time programmable ROM) version of the MC68HC05B16, meaning that once the application program has been loaded in the EPROM it can never be erased. The entire MC68HC05B6 data sheet applies to the MC68HC705B16, with the exceptions outlined in this appendix.

Features

- 15 kbytes EPROM
- 352 bytes of RAM
- 576 bytes bootstrap ROM
- Simultaneous programming of up to 8 bytes of EPROM
- Optional pull-down resistors available on all port B and port C pins
- 52-pin PLCC and 64-pin QFP packages

Note: The electrical characteristics of the MC68HC05B6 as provided in Section 11 do not apply to the MC68HC705B16. Data specific to the MC68HC705B16 can be found in this appendix.

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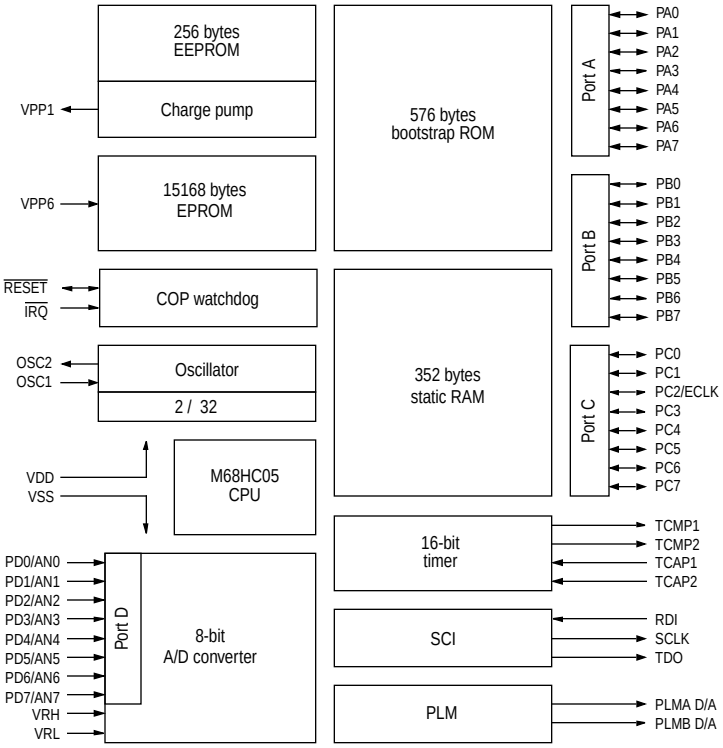


Figure E-1 MC68HC705B16 block diagram

14

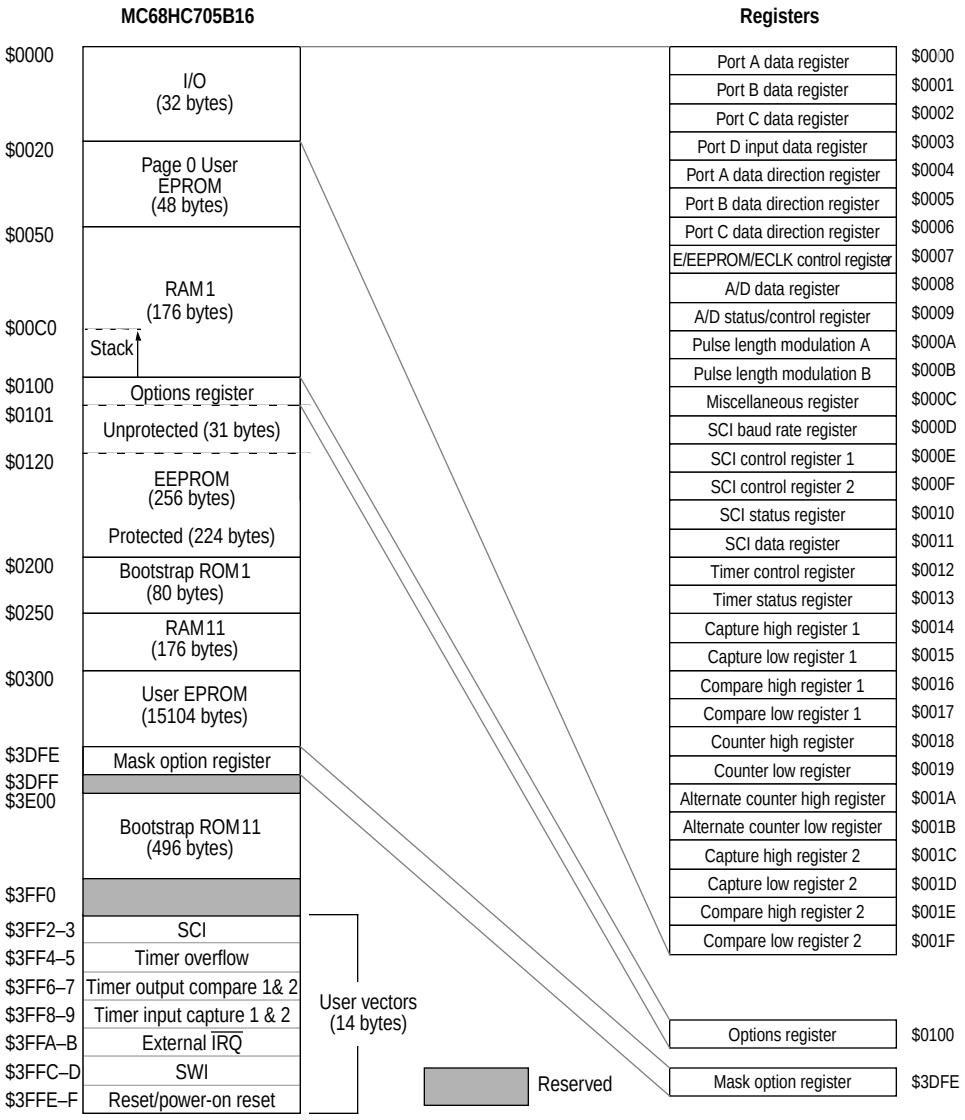


Figure E-2 Memory map of the MC68HC705B16

Table E-1 Register outline

Register name	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
Port A data (PORTA)	$0000									Undefined
Port B data (PORTB)	$0001									Undefined
Port C data (PORTC)	$0002						PC2/ ECLK			Undefined
Port D data (PORTD)	$0003	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0	Undefined
Port A data direction (DDRA)	$0004									0000 0000
Port B data direction (DDRB)	$0005									0000 0000
Port C data direction (DDRC)	$0006									0000 0000
EPROM/EEPROM/ECLK control	$0007			E6LAT	E6PGM	ECLK	E1ERA	E1LAT	E1PGM	0000 0000
A/D data (ADDATA)	$0008									0000 0000
A/D status/control (ADSTAT)	$0009	COCO	ADRC	ADON	0	CH3	CH2	CH1	CH0	0000 0000
Pulse length modulation A (PLMA)	$000A									0000 0000
Pulse length modulation B (PLMB)	$000B									0000 0000
Miscellaneous	$000C	POR(1)	INTP	INTN	INTE	SFA	SFB	SM	WDOG(2)	?001 000?
SCI baud rate (BAUD)	$000D	SPC1	SPC0	SCT1	SCT0	SCT0	SCR2	SCR1	SCR0	00uu uuuu
SCI control 1 (SCCR1)	$000E	R8	T8		M	WAKE	CPOL	CPHA	LBCL	Undefined
SCI control 2 (SCCR2)	$000F	TIE	TCIE	RIE	ILIE	TE	RE	RWU	SBK	0000 0000
SCI status (SCSR)	$0010	TDRE	TC	RDRF	IDLE	OR	NF	FE		1100 000u
SCI data (SCDR)	$0011									0000 0000
Timer control (TCR)	$0012	ICIE	OCIE	TOIE	FOLV2	FOLV1	OLV2	IEDG1	OLVL1	0000 00u0
Timer status (TSR)	$0013	ICF1	OCF1	TOF	ICF2	OCF2				Undefined
Input capture high 1	$0014									Undefined
Input capture low 1	$0015									Undefined
Output compare high 1	$0016									Undefined
Output compare low 1	$0017									Undefined
Timer counter high	$0018									1111 1111
Timer counter low	$0019									1111 1100
Alternate counter high	$001A									1111 1111
Alternate counter low	$001B									1111 1100
Input capture high 2	$001C									Undefined
Input capture low 2	$001D									Undefined
Output compare high 2	$001E									Undefined
Output compare low 2	$001F									Undefined
Options (OPTR)(3)	$0100							EE1P	SEC	Not affected
Mask option register (MOR)(4)	$3DFE				RTIM	RWAT	WWAT	PBPD	PCPD	Not affected

(1) This bit is set each time there is a power-on reset.

(2) The state of the WDOG bit after reset is dependent upon the mask option selected; 1=watchdog enabled, 0=watchdog disabled.

(3) This register is implemented in EEPROM; therefore reset has no effect on the individual bits.

(4) This register is implemented in EPROM; therefore reset has no effect on the individual bits.

E.1 EPROM

The MC68HC705B16 memory map is given in Figure E-2. The device has a total of 15168 bytes of EPROM (including 14 bytes for User vectors) and 256 bytes of EEPROM.

The EPROM array is supplied by the VPP6 pin in both read and program modes. Typically the user's software would be loaded into a programming board where V_{PP6} is controlled by one of the bootstrap loader routines. It would then be placed in an application where no programming occurs. In this case the VPP6 pin should be hardwired to V_{DD}.

Warning: A minimum V_{DD} voltage must be applied to the VPP6 pin at all times, including power-on. Failure to do so could result in permanent damage to the device.

E.1.1 EPROM read operation

The execution of a program in the EPROM address range or a load from the EPROM are both read operations. The E6LAT bit in the EPROM/EEPROM control register should be cleared to '0' which automatically resets the E6PGM bit. In this way the EPROM is read like a normal ROM. Reading the EPROM with the E6LAT bit set will give data that does not correspond to the actual memory content. As interrupt vectors are in EPROM, they will not be loaded when E6LAT is set. Similarly, the bootstrap ROM routines cannot be executed when E6LAT is set. In read mode, the VPP6 pin must be at the V_{DD} level. When entering the STOP mode, the EPROM is automatically set to the read mode.

Note: An erased byte reads as $00.

E.1.2 EPROM program operation

Typically the EPROM will be programmed by the bootstrap routines resident in the on-chip ROM. However, the user program can be used to program some EPROM locations if the proper procedure is followed. In particular, the programming sequence must be running in RAM, as the EPROM will not be available for code execution while the E6LAT bit is set. The V_{PP6} switching must occur externally after the E6PGM bit is set, for example under control of a signal generated on a pin by the programming routine.

Note: When the part becomes a PROM, only the cumulative programming of bits to logic '1' is possible if multiple programming is made on the same byte.

To allow simultaneous programming of up to eight bytes, these bytes must be in the same group of addresses which share the same most significant address bits; only the three least significant bits can change.

E.1.3 EPROM/EEPROM/ECLK control register

	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
EPROM/EEPROM/ECLK control	$0007			E6LAT	E6PGM	ECLK	E1ERA	E1LAT	E1PGM	0000 0000

E6LAT — EPROM programming latch enable bit

1 (set) – Address and up to eight data bytes can be latched into the EPROM for further programming providing the E6PGM bit is cleared.

0 (clear) – Data can be read from the EPROM or firmware ROM; the E6PGM bit is reset to zero when E6LAT is ‘0’.

STOP, power-on and external reset clear the E6LAT bit.

Note: After the t_{ERA1} erase time or t_{PROG1} programming time, the E6LAT bit has to be reset to zero in order to clear the E6PGM bit.

E6PGM — EPROM program enable bit

This bit is the EPROM program enable bit. It can be set to ‘1’ to enable programming only after E6LAT is set and at least one byte is written to the EPROM. It is not possible to clear this bit using software but clearing E6LAT will always clear E6PGM.

Table E-2 EPROM control bits description

E6LAT	E6PGM	Description
0	0	Read/execute in EPROM
1	0	Ready to write address/data to EPROM
1	1	programming in progress

Note: The E6PGM bit can never be set while the E6LAT bit is at zero.

ECLK

See Section 4.3.

E1ERA — EEPROM erase/programming bit

Providing the E1LAT and E1PGM bits are at logic one, this bit indicates whether the access to the EEPROM is for erasing or programming purposes.

1 (set) – An erase operation will take place.

0 (clear) – A programming operation will take place.

Once the program/erase EEPROM address has been selected, E1ERA cannot be changed.

E1LAT — EEPROM programming latch enable bit

1 (set) – Address and data can be latched into the EEPROM for further program or erase operations, providing the E1PGM bit is cleared.

0 (clear) – Data can be read from the EEPROM. The E1ERA bit and the E1PGM bit are reset to zero when E1LAT is '0'.

STOP, power-on and external reset clear the E1LAT bit.

Note: After the t_{ERA1} erase time or t_{PROG1} programming time, the E1LAT bit has to be reset to zero in order to clear the E1ERA bit and the E1PGM bit.

E1PGM — EEPROM charge pump enable/disable

1 (set) – Internal charge pump generator switched on.

0 (clear) – Internal charge pump generator switched off.

When the charge pump generator is on, the resulting high voltage is applied to the EEPROM array. This bit cannot be set before the data is selected, and once this bit has been set it can only be cleared by clearing the E1LAT bit.

A summary of the effects of setting/clearing bits 0, 1 and 2 of the control register are given in Table E-3.

Table E-3 EEPROM control bits description

E1ERA	E1LAT	E1PGM	Description
0	0	0	Read condition
0	1	0	Ready to load address/data for program/erase
0	1	1	Byte programming in progress
1	1	0	Ready for byte erase (load address)
1	1	1	Byte erase in progress

Note: The E1PGM and E1ERA bits are cleared when the E1LAT bit is at zero.

E.1.4 Mask option register

	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
Mask option register (MOR)(1)	$3DFE				RTIM	RWAT	WWAT	PBPD	PCPD	Not affected

(1) This register is implemented in EPROM; therefore reset has no effect on the individual bits.

RTIM — Reset time

This bit can modify the time t_{PORL}, where the $\overline{\text{RESET}}$ pin is kept low after a power-on reset.

1 (set) – t_{PORL} = 16 cycles.

0 (clear) – t_{PORL} = 4064 cycles.

RWAT — Watchdog after reset

This bit can modify the status of the watchdog counter after reset. Usually, the watchdog system is disabled after power-on or external reset but when this bit is set, it will be active immediately after the following resets (except in bootstrap mode).

WWAT — Watchdog during WAIT mode

This bit can modify the status of the watchdog counter in WAIT mode. Normally, the watchdog system is disabled in WAIT mode but when this bit is set, the watchdog will be active in WAIT mode.

PBPD — Port B pull-down

This bit, when programmed, connects a resistive pull-down on each pin of port B. This pull-down, R_{PD}, is active on a given pin only while it is an input.

PCPD — Port C pull-down

This bit, when programmed, connects a resistive pull-down on each pin of port C. This pull-down, R_{PD}, is active on a given pin only while it is an input.

E.1.5 EEPROM options register (OPTR)

	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
Options (OPTR)(1)	$0100							EE1P	SEC	Not affected

(1) This register is implemented in EEPROM; therefore reset has no effect on the individual bits.

EE1P – EEPROM protect bit

In order to achieve a higher degree of protection, the EEPROM is effectively split into two parts, both working from the VPP1 charge pump. Part 1 of the EEPROM array (32 bytes from $0100 to $011F) cannot be protected; part 2 (224 bytes from $0120 to $01FF) is protected by the EE1P bit in the options register.

1 (set) – Part 2 of the EEPROM array is not protected; all 256 bytes of EEPROM can be accessed for any read, erase or programming operations.

0 (clear) – Part 2 of the EEPROM array is protected; any attempt to erase or program a location will be unsuccessful.

When this bit is set to 1 (erased), the protection will remain until the next power-on or external reset. EE1P can only be written to ‘0’ when the E1LAT bit in the EEPROM control register is set.

Note: The EEPROM1 protect function is disabled while in bootstrap mode.

SEC — Secure bit

This bit allows the EPROM and EEPROM1 to be secured from external access. When this bit is in the erased state (set), the EPROM and EEPROM1 content is not secured and the device may be used in non user mode. When the SEC bit is programmed to ‘zero’, the EPROM and EEPROM1 content is secured by prohibiting entry to the non user mode. To deactivate the secure bit, the EPROM has to be erased by exposure to a high density ultraviolet light, and the device has to be entered into the EPROM erase verification mode with PD1 set. When the SEC bit is changed, its new value will have no effect until the next power-on or external reset.

1 (set) – EEPROM/EPROM not protected.

0 (clear) – EEPROM/EPROM protected.

E.2 Bootstrap mode

The 432 bytes of self-check firmware on the MC68HC05B6 are replaced by 576 bytes of bootstrap firmware. A detailed description of the modes of operation within bootstrap mode is given below.

The bootstrap program in mask ROM address locations $0200 to $024F and $3E00 to $3FEF can be used to program the EPROM and the EEPROM, to check if the EPROM is erased or to load and execute data in RAM.

After reset, while going to the bootstrap mode, the vector located at address $3FEE and $3FEF (RESET) is fetched to start execution of the bootstrap program. To place the part in bootstrap mode, the $\overline{IRQ}$ pin should be at + 9V with the TCAP1 pin 'high' during transition of the $\overline{RESET}$ pin from low to high. The hold time on the $\overline{IRQ}$ and TCAP1 pins is two clock cycles after the external $\overline{RESET}$ pin is brought high.

When the MC68HC705B16 is placed in the bootstrap mode, the bootstrap reset vector is fetched and the bootstrap firmware starts to execute. Table E-4 shows the conditions required to enter each level of bootstrap mode on the rising edge of $\overline{RESET}$.

Table E-4 Mode of operation selection

$\overline{IRQ}$ pin	TCAP1 pin	PD1	PD2	PD3	PD4	Mode
V_{SS} to V_{DD}	V_{SS} to V_{DD}	x	x	x	x	Single chip
+ 9 Volts	V_{DD}	0	0	x	0	Erased EPROM verification (EEV)
+ 9 Volts	V_{DD}	1	0	0	0	Erased EPROM verification; erase EEPROM; EPROM/EEPROM parallel program/verify
+ 9 Volts	V_{DD}	1	0	1	0	Erased EPROM verification; erase EEPROM; EPROM/EEPROM/ RAM serial bootstrap load and execute
+ 9 Volts	V_{DD}	x	x	0	1	RAM parallel bootstrap load and execute (if SEC bit = 1)
+ 9 Volts	V_{DD}	x	x	1	1	Serial EPROM/EEPROM/RAM bootloader (if SEC = 1)

x = Don't care

The bootstrap program first copies part of itself in RAM (except 'RAM parallel load'), as the program cannot be executed in ROM during verification/programming of the EPROM. It then sets the TCMP1 output to a logic high level.

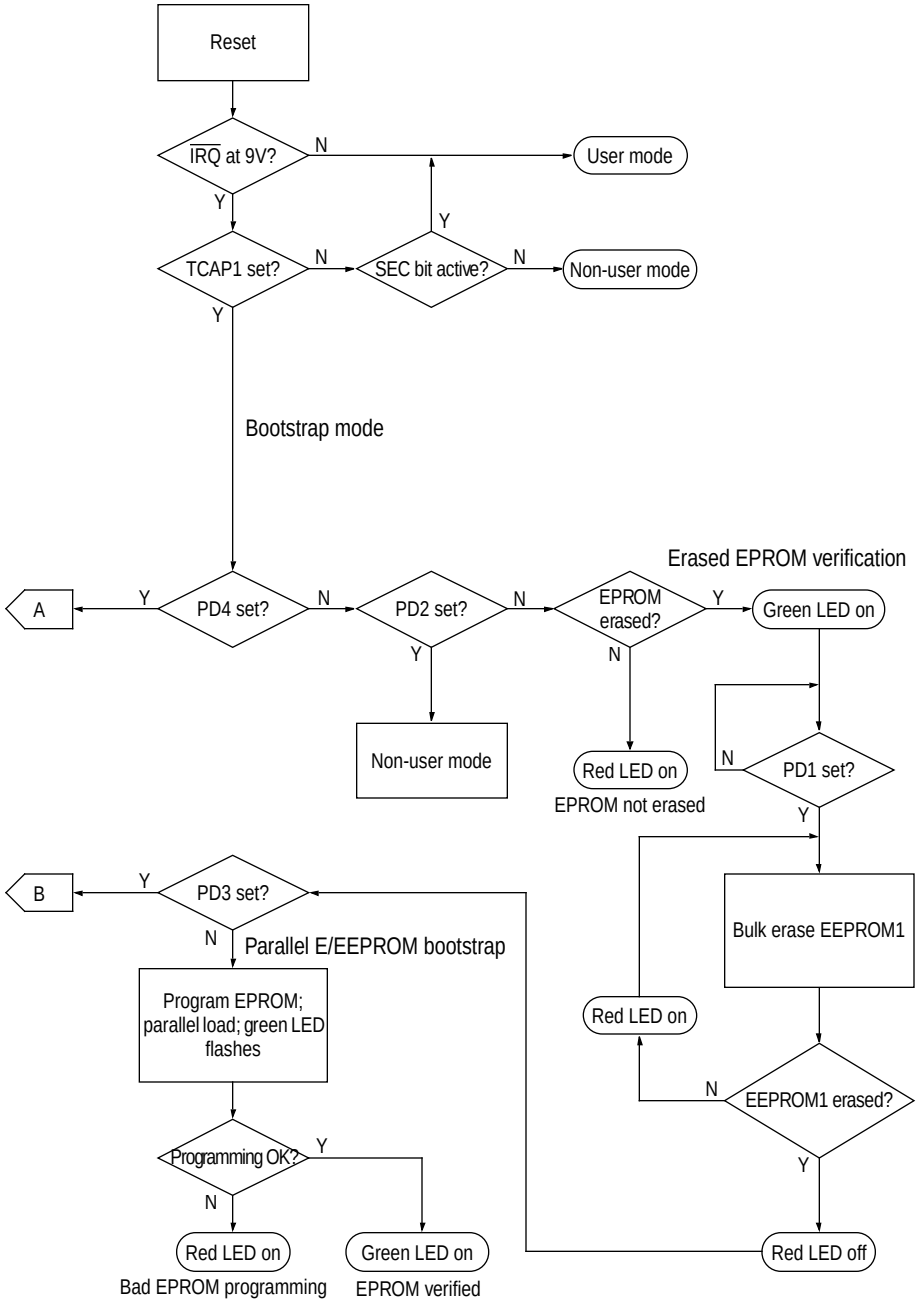


Figure E-3 Modes of operation flow chart (1 of 2)

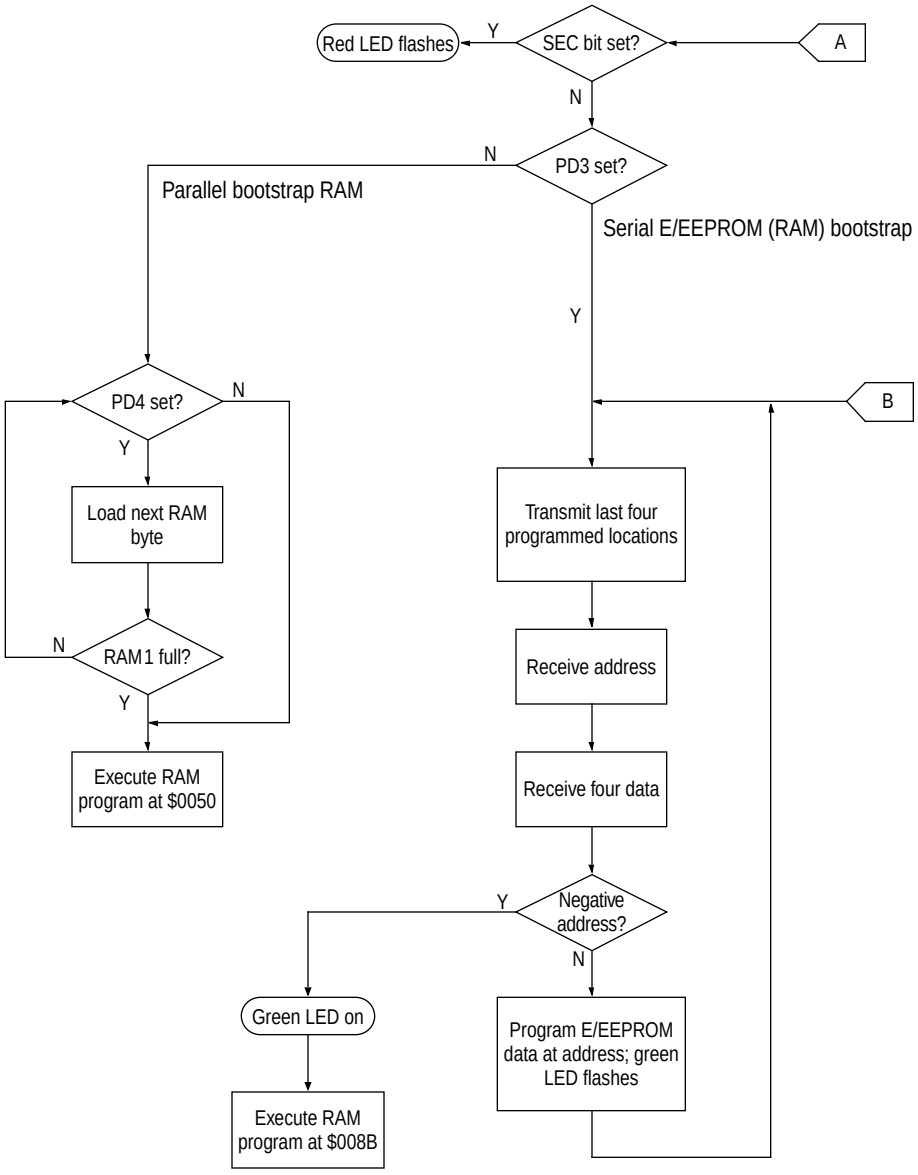


Figure E-4 Modes of operation flow chart (2 of 2)

E.2.1 Erased EPROM verification

If a non $00 byte is detected, the red LED is turned on and the routine stops (see Figure E-3 and Figure E-4). Only when the entire EPROM content is verified as erased does the green LED switch on. PD1 is then checked. If PD1=0, the bootstrap program stops here and no programming occurs until such time as a high level is sensed on PD1. If PD1=1, the bootstrap program proceeds to erase the EEPROM1 for a nominal 100 ms (4.0 MHz crystal). It is then checked for complete erasure; if a non $FF byte is detected, the red LED is turned on, and erase is performed a second time, and so on until total erasure is verified. At this point, both EPROM and EEPROM1 are completely erased and the security bit is cleared. The programming operation can then be performed. A schematic diagram of the circuit required for erased EPROM verification is shown in Figure E-7.

E.2.2 EPROM/EEPROM parallel bootstrap

Before the parallel bootstrap routines begin, the erased EPROM verification program is executed as described in Section E.2.1. When PD2=0, the programming time is set to 5 milliseconds with the bootstrap program and verify for the EPROM taking approximately 15 seconds. The EPROM is loaded in increasing address order with non EPROM segments being skipped by the loader. Simultaneous programming is performed by reading eight bytes of data before actual programming is performed, thus the loading time of the internal EPROM is divided by eight.

Parallel data is entered through Port A, while the 14-bit address is output on port B, PC0 to PC4 and TCMP2. If the data comes from an external EPROM, the handshake can be disabled by connecting together PC5 and PC6. If the data is supplied by a parallel interface, handshaking will be provided by PC5 and PC6 according to the timing diagram of Figure E-5 (see also Figure E-6).

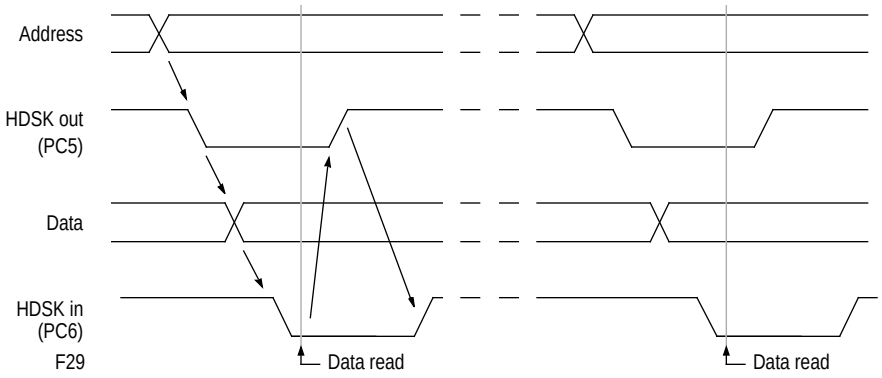
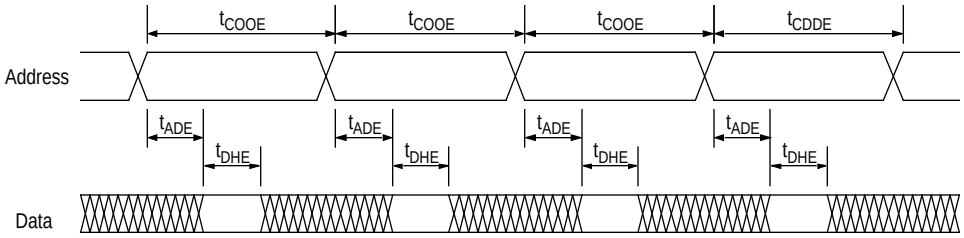


Figure E-5 Timing diagram with handshake

During programming, the green LED will flash at about 3 Hz.

Upon completion of the programming operation, the contents of the EPROM and EEPROM1 are checked against the external data source. If programming is verified the green LED stays on, while an error will cause the red LED to be turned on. Figure E-7 is a schematic diagram of a circuit that can be used to program the EPROM or to load and execute data in the RAM.

Note: The entire EPROM and EEPROM1 can be loaded from the external source; if it is desired to leave a segment undisturbed, the data for this segment should be all zeros for EPROM data and all $FFs for EEPROM1 data.



t_{ADE} max (address to data delay)	5 machine cycles
t_{DHA} min (data hold time)	14 machine cycles
t_{COOE} (load cycle time)	117 machine cycles < t_{COOE} < 150 machine cycles
t_{CDDE} (programming cycle time)	t_{COOE} + t_{PROG} (5ms nominal for EPROM; 10ms for EEPROM1))

1 machine cycle = $1/(2f_0(Xtal))$

Figure E-6 Parallel EPROM loader timing diagram

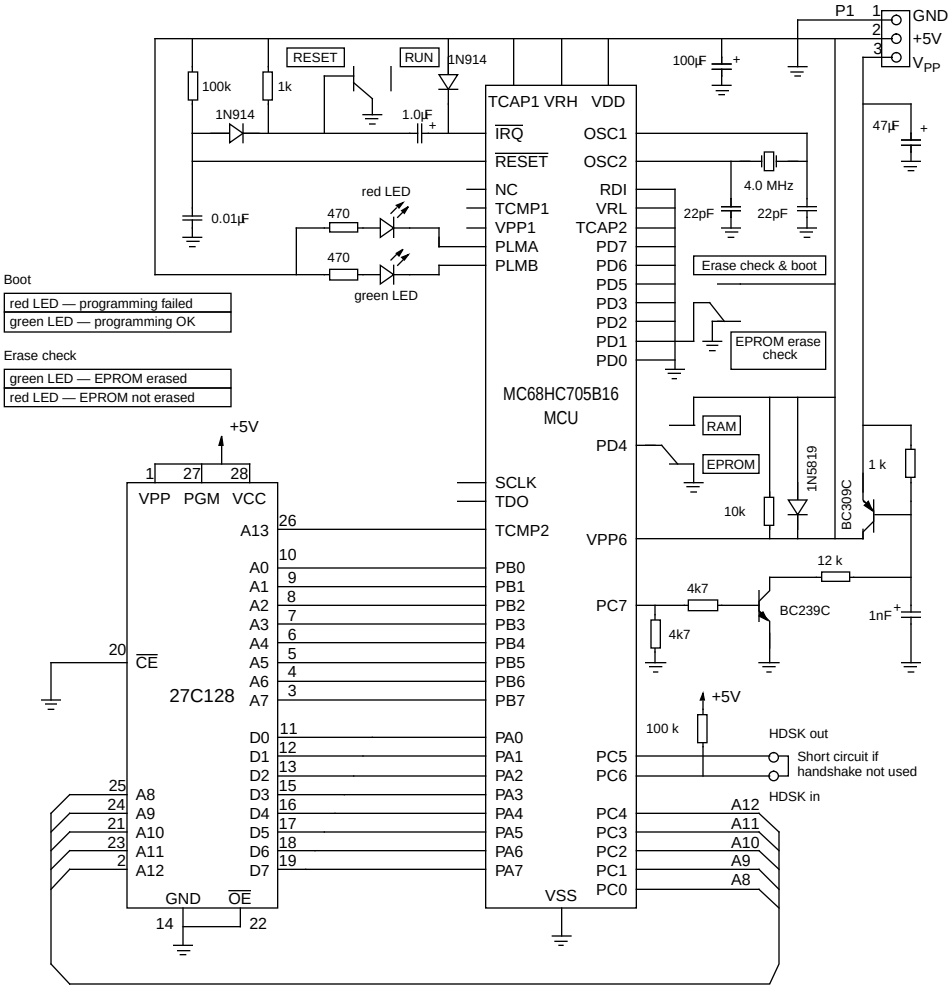


Figure E-7 EPROM Parallel bootstrap schematic diagram

E.2.3 EEPROM/EPROM/RAM serial bootstrap

For erased EPROM verification, PD4 must be at ‘0’. In this case, erased EPROM verification executes as described in Section E.2.1 before control is given to the serial routine.

If PD4 is at ‘1’, the program initially checks the state of the security bit. If the security bit is active (‘0’), the program will not enter serial bootstrap and the red LED will flash. Otherwise the serial bootstrap program will be executed according to Figure E-3 and Figure E-4.

The serial routine communicates through the SCI with an external host, typically a PC, by means of an RS232 link at 9600 baud, 8-bit, no parity and full duplex. Refer to Figure E-8 for a schematic diagram of a suitable circuit.

Note: Data format is not ASCII, but 8-bit binary, so a complementary program must be run by the host to supply the required format. Such a program is available for the IBM PC from Motorola.

The EPROM bootstrap routines are used to customise the OTP EPROM. To increase the speed of programming the 15 kbytes, four bytes are programmed while the data is simultaneously transmitted back and forward in full duplex. This implies that while 4 bytes are being programmed the next 4 bytes are received and the preceding 4 bytes are echoed. The format accepted by the serial loader is as follows:

1 EPROM locations

[address n high] [address n low] [data(n)] [data (n+1)] [data (n+2)] [data (n+3)]

Address n must have the two least significant bits at zero so that n, n+1, n+2 and n+3 have identical most significant bits. These blocks of four bytes do not need to be contiguous, as a new address is transmitted for each new group.

2 EEPROM1 locations

[address n high] [address n low] [data(n)] [dummy data 1] [dummy data 2] [dummy data 3]

The same four byte protocol of data exchange is used, but only the first data value is programmed at address n. The three following dummy data values must be sent to be in agreement with the protocol, but are not significant.

The protocol is as follows:

1 The MC68HC705B16 sends the last two bytes programmed to the host as a prompt; this also allows the host to verify that programming has been carried out correctly.

2 In response to the first byte prompt, the host sends the first address byte.

3 After receiving the first address byte, the MC68HC705B16 sends the next byte programmed.

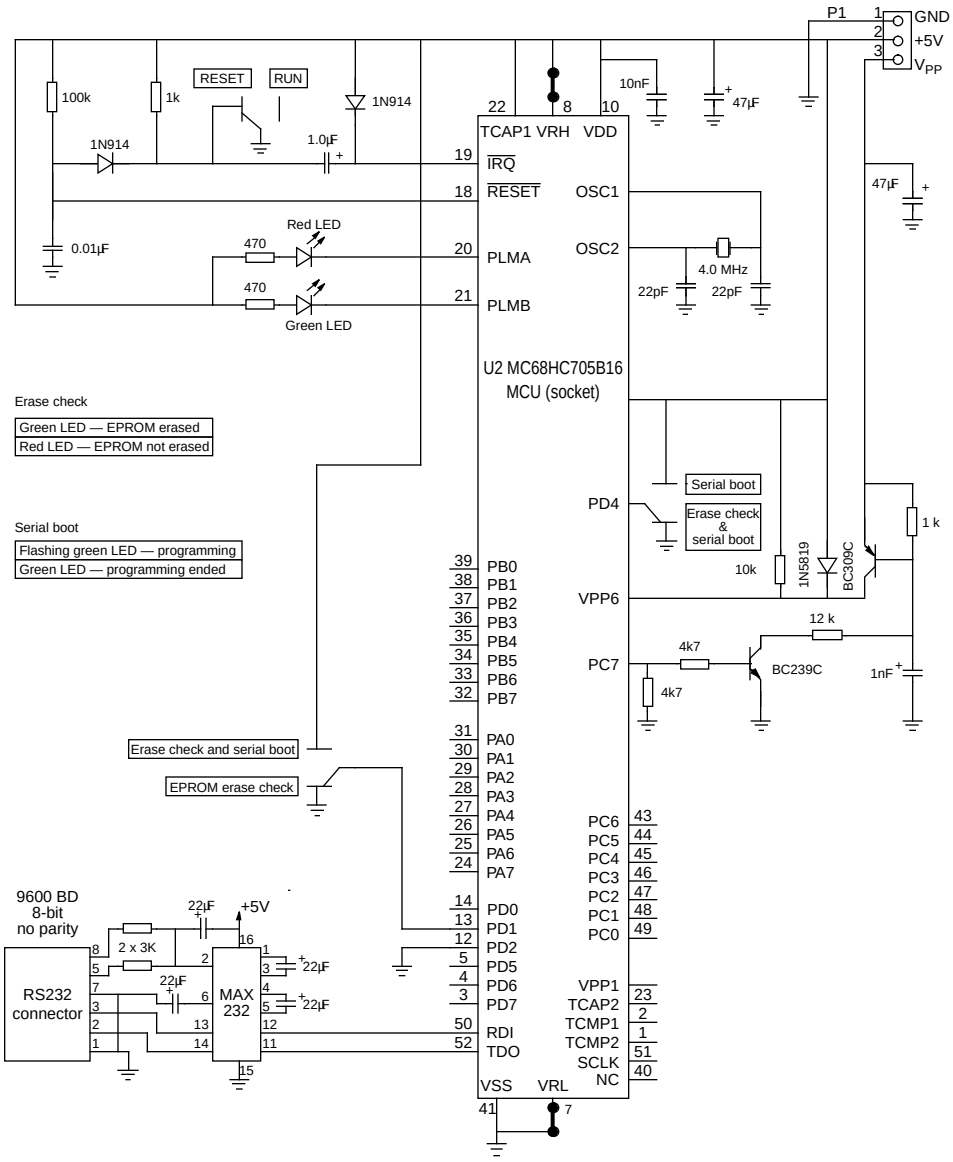


Figure E-8 RAM/EPROM/EEPROM serial bootstrap schematic diagram

4 The exchange of data continues until the MC68HC705B16 has sent the four data bytes and the host has sent the 2 address data bytes and 4 data bytes.

5 If the data is different from $00 for EPROM or $FF for EEPROM, it is programmed at the address provided, while the next address and bytes are received and the previous data is echoed.

6 Loop to 1.

After reset, the MC68HC705B16 serial bootstrap routine will first echo two blocks of four bytes at $00, as no data is programmed yet.

If the data received is $00 for EPROM locations or $FF for EEPROM locations, no programming in the EPROM and EEPROM1 takes place, and the contents of the accessed location are returned as a prompt. The entire EPROM/EEPROM memory can be read in this fashion (serial dump).

Warning: When using this function with a programmed device, the device must be placed into RAM/EPROM/EEPROM serial bootstrap mode without EPROM erase check (PD4 = 1).

Serial RAM loading and execute can be accomplished in this mode. A RAM byte will be written if the address sent by the host in the serial protocol points to the RAM.

RAM bytes $008B–$00E3 and $0250–$02ED are available for user test programs. A 10-byte stack resides at the top of RAM1, allowing, for example, one interrupt and two sub-routine levels. The RAM addresses between $0050 and $008A are used by the loader and are therefore not available to the user during serial loading/executing.

If the SEC bit is at ‘1’, program execution is triggered by sending a negative (bit 7 set) high address; execution starts at address XADR ($008B).

In the RAM bootloader mode, all interrupt vectors are mapped to pseudo-vectors in RAM (see Table E-5). This allows programmers to use their own service-routine addresses. Each pseudo-vector is allowed three bytes of space rather than the two bytes for normal vectors, because an explicit jump (JMP) opcode is needed to cause the desired jump to the user’s service routine address.

Table E-5 Bootstrap vector targets in RAM

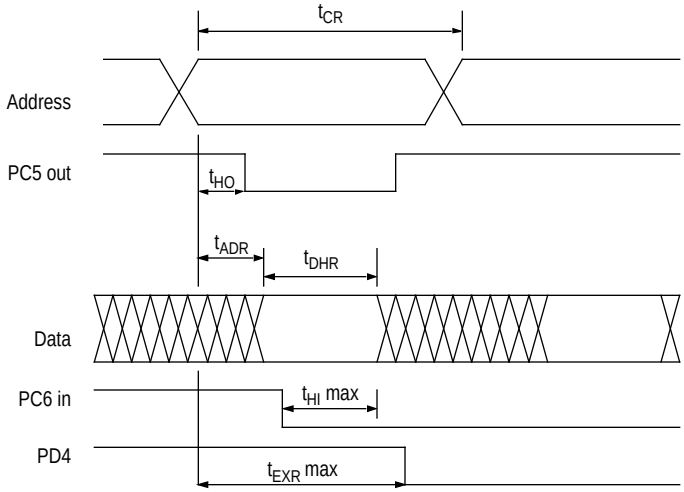
Vector targets in RAM	
SCI interrupt	$02EE
Timer overflow	$02F1
Timer output compare	$02F4
Timer input capture	$02F7
$\overline{\text{IRQ}}$	$02FA
SWI	$02FD

E.2.4 RAM parallel bootstrap

The program first checks the state of the security bit. If the SEC bit is active, i.e. ‘0’, the program will not enter the RAM bootstrap mode and the red LED will flash. Otherwise the RAM bootstrap program will start loading the RAM with external data (e.g. from a 2564 or 2764 EPROM). Before loading a new byte the state of the PD4/AN4 pin is checked. If this pin goes to level ‘0’, or if the RAM is full, then control is given to the loaded program at address $0050. See Figure E-3 and Figure E-4.

If the data is supplied by a parallel interface, handshaking will be provided by PC5 and PC6 according to Figure E-9. If the data comes from an external EPROM, the handshake can be disabled by connecting together PC5 and PC6.

Figure E-10 provides a schematic diagram of a circuit that can be used to load the RAM with short test programs. Up to 8 programs can be loaded in turn from the EPROM. Selection is accomplished by means of the switches connected to the EPROM higher address lines (A8 through A10). If the user program sets PC0 to level ‘1’, this will disable the external EPROM, thus rendering both port A output and port B input available. The EPROM parallel bootstrap loader schematic can also be used (Figure E-7), provided VPP is at V_{DD} level. The high order address lines will be at zero. The LEDs will stay off.



t_{ADR} max (address to data delay; PC6=PC5)	16 machine cycles
t_{DHR} min (data hold time)	4 machine cycles
t_{CR} (load cycle time; PC6=PC5)	49 machine cycles
t_{HO} (PC5 handshake out delay)	5 machine cycles
t_{HI} max (PC6 handshake in, data hold time)	10 machine cycles
t_{EXR} max (max delay for transition to be recognised during this cycle; PC6=PC5	30 machine cycles

1 machine cycle = $1/(2f_0(Xtal))$

Figure E-9 Parallel RAM loader timing diagram

E.2.4.1 Jump to start of RAM ($0050)

PD4 must be high during the first 49 program cycles and pulled low before the 68th cycle for immediate jump execution at address $0050.

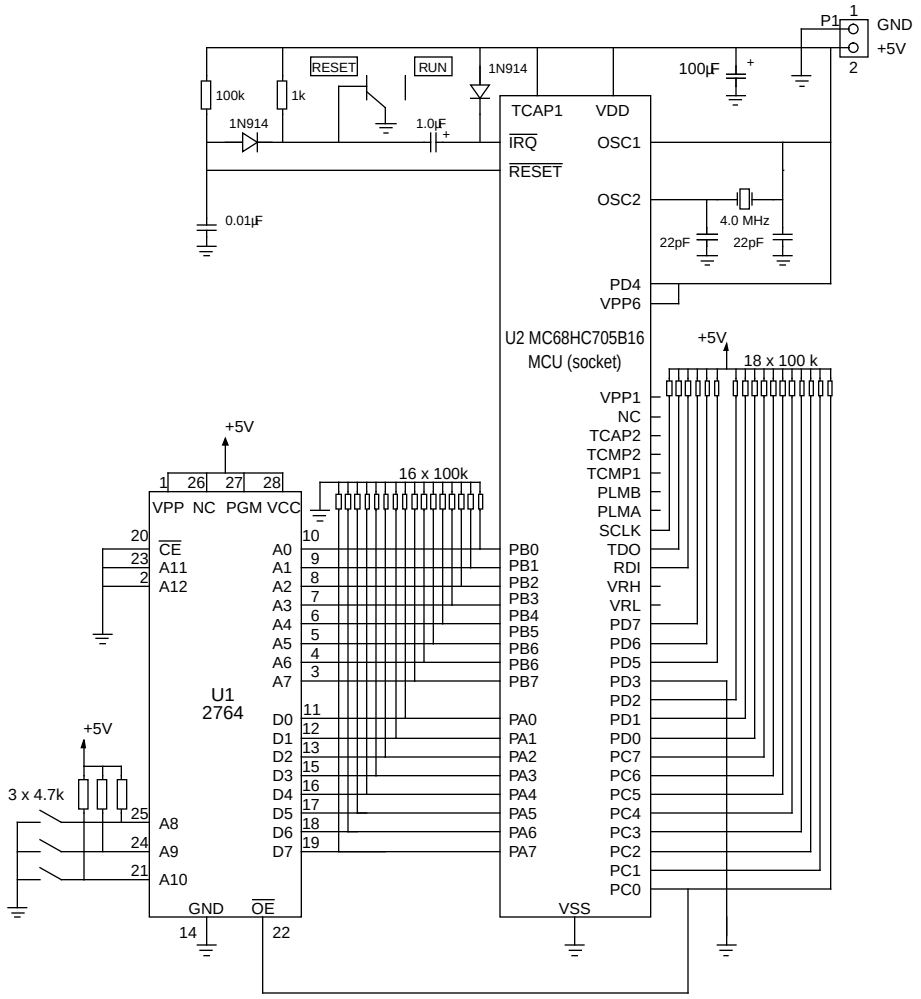


Figure E-10 RAM parallel bootstrap schematic diagram

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Note:

E.2.5 Maximum ratings

Table E-6 Maximum ratings

Rating	Symbol	Value	Unit
Supply voltage(1)	V_{DD}	– 0.5 to +7.0	V
Input voltage	V_{IN}	V_{SS} – 0.5 to V_{DD} + 0.5	V
Input voltage – Self-check mode ($\overline{IRQ}$ pin only)	V_{IN}	V_{SS} – 0.5 to $2V_{DD}$ + 0.5	V
Operating temperature range – Standard (MC68HC705B16) – Extended (MC68HC705B16C) – Industrial (MC68HC705B16V) – Automotive (MC68HC705B16M)	T_A	T_L to T_H 0 to +70 –40 to +85 –40 to +105 –40 to +125	C
Storage temperature range	T_{STG}	– 65 to +150	C
Current drain per pin (excluding VDD and VSS)(2) – Source – Sink	 I_D I_S	 25 45	 mA mA

(1) All voltages are with respect to V_{SS}.

(2) Maximum current drain per pin is for one pin at a time, limited by an external resistor.

Note: This device contains circuitry designed to protect against damage due to high electrostatic voltages or electric fields. However, it is recommended that normal precautions be taken to avoid the application of any voltages higher than those given in the maximum ratings table to this high impedance circuit. For maximum reliability all unused inputs should be tied to either V_{SS} or V_{DD}.

E.2.6 Thermal characteristics and power considerations

Table E-7 Package thermal characteristics

Characteristics	Symbol	Value	Unit
Thermal resistance			
– 64-pin quad flat package	θ_{JA}	50	C/W
– Plastic 56 pin shrink DIL package	Not available for this device		
– Plastic 52 pin PLCC package	θ_{JA}	50	C/W

The average chip junction temperature, T_J, in degrees Celsius can be obtained from the following equation:

$$T_J = T_A + (P_D \bullet \theta_{JA}) \quad [1]$$

where:

T_A = Ambient temperature (C)

θ_{JA} = Package thermal resistance, junction-to-ambient (C/W)

$P_D = P_{INT} + P_{I/O}$ (W)

P_{INT} = Internal chip power = $I_{DD} \bullet V_{DD}$ (W)

$P_{I/O}$ = Power dissipation on input and output pins (user determined)

An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = \frac{K}{T_J + 273} \quad [2]$$

Solving equations [1] and [2] for K gives:

$$K = P_D \bullet (T_A + 273) + \theta_{JA} \bullet P_D^2 \quad [3]$$

where K is a constant for a particular part. K can be determined by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained for any value of T_A by solving the above equations. The package thermal characteristics are shown in Table E-7.

Voltage	Pins	R1	R2	C
4.5V	PA0–7, PB0–7, PC0–7	3.26k	2.38k	50pF
3.0V	PA0–7, PB0–7, PC0–7	10.91k	6.32k	50pF

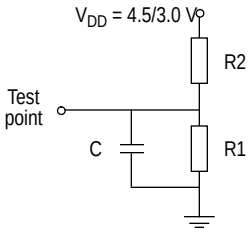

Figure E-11 Equivalent test load

E.2.7 DC electrical characteristics

Table E-8 DC electrical characteristics for 5V operation

(V_{DD} = 5 Vdc 10%, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H)

Characteristic[1]	Symbol	Min	Typ[2]	Max	Unit
Output voltage I_{LOAD} = – 10 µA I_{LOAD} = +10 µA	 V_{OH} V_{OL}	 V_{DD} – 0.1 —	 — —	 — 0.1	V
Output high voltage (I_{LOAD} = 0.8mA) PA0–7, PB0–7, PC0–7, TCMP1, TCMP2 Output high voltage (I_{LOAD} = 1.6mA) TDO, SCLK, PLMA, PLMB	 V_{OH} V_{OH}	 V_{DD} – 0.8 V_{DD} – 0.8	 V_{DD} – 0.4 V_{DD} – 0.4	 — —	V
Output low voltage (I_{LOAD} = 1.6mA) PA0–7, PB0–7, PC0–7, TCMP1, TCMP2, TDO, SCLK, PLMA, PLMB Output low voltage (I_{LOAD} = 1.6mA) $\overline{RESET}$	 V_{OL} V_{OL}	 — 	 0.1 0.4	 0.4 1	V
Input high voltage PA0–7, PB0–7, PC0–7, PD0–7, OSC1, $\overline{IRQ}$, $\overline{RESET}$, TCAP1, TCAP2, RDI	V_{IH}	$0.7V_{DD}$	—	V_{DD}	V
Input low voltage PA0–7, PB0–7, PC0–7, PD0–7, OSC1, $\overline{IRQ}$, $\overline{RESET}$, TCAP1, TCAP2, RDI	V_{IL}	V_{SS}	—	$0.2V_{DD}$	V
Supply current[3] RUN (SM = 0) (See Figure 11-2) RUN (SM = 1) (See Figure 11-3) WAIT (SM = 0) (See Figure 11-4) WAIT (SM = 1) (See Figure 11-5) STOP 0 to 70 (standard) – 40 to 85 (extended) – 40 to 105 (industrial) – 40 to 125 (automotive)	 I_{DD} I_{DD} I_{DD} I_{DD} I_{DD} I_{DD} I_{DD} I_{DD}	 — — — — — — — —	 5.0 1.0 1.5 0.9 2 — — —	 6 1.5 2 1 10 20 60 60	 mA mA mA mA µA µA µA µA
EPROM Absolute maximum voltage Programming voltage Programming current Read voltage	 V_{PP6} max V_{PP6} I_{PP6} V_{PP6R}	 V_{DD} 15 — V_{DD}	 — 15.5 50 V_{DD}	 18 16 64 V_{DD} 10%	 V V mA V
High-Z leakage current PA0–7, PB0–7, PC0–7, TDO, $\overline{RESET}$, SCLK	I_{IL}	—	0.2	1	µA
Input current Port B and port C pull-down ($V_{IN}=V_{IH}$)	I_{RPD}		80		µA
Input current (0 to 70) $\overline{IRQ}$, OSC1, TCAP1, TCAP2, RDI, PD0/AN0-PD7/AN7 (channel not selected)	I_{IN}	—	0.2	1	µA
Input current (– 40 to 125) $\overline{IRQ}$, OSC1, TCAP1, TCAP2, RDI, PD0/AN0-PD7/AN7 (channel not selected)	I_{IN}	—	—	5	µA
Capacitance Ports (as input or output), $\overline{RESET}$, TDO, SCLK $\overline{IRQ}$, TCAP1, TCAP2, OSC1, RDI PD0/AN0–PD7/AN7 (A/D off) PD0/AN0–PD7/AN7 (A/D on)	 C_{OUT} C_{IN} C_{IN} C_{IN}	 — — — —	 — — 12 22	 12 8 — —	 pF pF pF pF

(1) All I_{DD} measurements taken with suitable decoupling capacitors across the power supply to suppress the transient switching currents inherent in CMOS designs (see Section 2).

(2) Typical values are at mid point of voltage range and at 25 C only

(3) RUN and WAIT I_{DD}: measured using an external square-wave clock source (f_{OSC} = 4.2MHz); all inputs 0.2 V from rail; no DC loads; maximum load on outputs 50pF (20pF on OSC2).
STOP /WAIT I_{DD}: all ports configured as inputs; V_{IL} = 0.2 V and $V_{IH} = V_{DD} – 0.2$ V: STOP I_{DD} measured with OSC1 = V_{DD}.
WAIT I_{DD} is affected linearly by the OSC2 capacitance.

Table E-9 DC electrical characteristics for 3.3V operation

(V_{DD} = 3.3Vdc ± 10%, V_{SS} = 0Vdc, $T_A = T_L$ to T_H)

Characteristic[1]	Symbol	Min	Typ[2]	Max	Unit
Output voltage					
I_{LOAD} = – 10 µA	V_{OH}	V_{DD} – 0.1	—	—	V
I_{LOAD} = +10 µA	V_{OL}	—	—	0.1	
Output high voltage (I_{LOAD} = 0.8mA)					
PA0–7, PB0–7, PC0–7, TCMP1, TCMP2	V_{OH}	V_{DD} – 0.3	V_{DD} – 0.1	—	V
Output high voltage (I_{LOAD} = 1.6mA)					
TDO, SCLK, PLMA, PLMB	V_{OH}	V_{DD} – 0.3	V_{DD} – 0.1	—	
Output low voltage (I_{LOAD} = 1.6mA)					
PA0–7, PB0–7, PC0–7, TCMP1, TCMP2, TDO, SCLK, PLMA, PLMB	V_{OL}	—	0.1	0.4	V
Output low voltage (I_{LOAD} = 1.6mA)					
$\overline{RESET}$	V_{OL}		0.2	0.6	
Input high voltage					
PA0–7, PB0–7, PC0–7, PD0–7, OSC1, $\overline{IRQ}$, $\overline{RESET}$, TCAP1, TCAP2, RDI	V_{IH}	0.7V_{DD}	—	V_{DD}	V
Input low voltage					
PA0–7, PB0–7, PC0–7, OSC1, $\overline{IRQ}$, $\overline{RESET}$, TCAP1, TCAP2, RDI	V_{IL}	V_{SS}	—	0.2V_{DD}	V
Supply current[3]					
RUN (SM = 0) (See Figure 11-2)	I_{DD}	—	2.0	3	mA
RUN (SM = 1) (See Figure 11-3)	I_{DD}	—	0.8	1	mA
WAIT (SM = 0) (See Figure 11-4)	I_{DD}	—	1.0	1.5	mA
WAIT (SM = 1) (See Figure 11-5)	I_{DD}	—	0.4	0.5	mA
STOP					
0 to 70 (standard)	I_{DD}	—	1	10	µA
– 40 to 85 (extended)	I_{DD}	—	—	10	µA
– 40 to 105 (industrial)	I_{DD}	—	—	40	µA
– 40 to 125 (automotive)	I_{DD}	—	—	40	µA
High-Z leakage current					
PA0–7, PB0–7, PC0–7, TDO, $\overline{RESET}$, SCLK	I_{IL}	—	0.2	1	µA
Input current					µA
Port B and port C pull-down (V_{IN}=V_{IH})	I_{RPD}		80		
Input current (0 to 70)					
$\overline{IRQ}$, OSC1, TCAP1, TCAP2, RDI, PD0/AN0-PD7/AN7 (channel not selected)	I_{IN}	—	0.2	1	µA
Input current (– 40 to 125)					
$\overline{IRQ}$, OSC1, TCAP1, TCAP2, RDI, PD0/AN0-PD7/AN7 (channel not selected)	I_{IN}	—	—	5	µA
Capacitance					
Ports (as input or output), $\overline{RESET}$, TDO, SCLK	C_{OUT}	—	—	12	pF
$\overline{IRQ}$, TCAP1, TCAP2, OSC1, RDI	C_{IN}	—	—	8	pF
PD0/AN0–PD7/AN7 (A/D off)	C_{IN}	—	12	—	pF
PD0/AN0–PD7/AN7 (A/D on)	C_{IN}	—	22	—	pF

(1) All I_{DD} measurements taken with suitable decoupling capacitors across the power supply to suppress the transient switching currents inherent in CMOS designs (see Section 2).

(2) Typical values are at mid point of voltage range and at 25 C only

(3) RUN and WAIT I_{DD}: measured using an external square-wave clock source (f_{OSC} = 2.0MHz); all inputs 0.2 V from rail; no DC loads; maximum load on outputs 50pF (20pF on OSC2).
STOP /WAIT I_{DD}: all ports configured as inputs; V_{IL} = 0.2 V and V_{IH} = V_{DD} – 0.2 V: STOP I_{DD} measured with OSC1 = V_{DD}.
WAIT I_{DD} is affected linearly by the OSC2 capacitance.

E.2.8 A/D converter characteristics

Table E-10 A/D characteristics for 5V operation

(V_{DD} = 5.0 Vdc 10%, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H)

Characteristic	Parameter	Min	Max	Unit
Resolution	Number of bits resolved by the A/D	8	—	Bit
Non-linearity	Max deviation from the best straight line through the A/D transfer characteristics ($V_{RH} = V_{DD}$ and V_{RL} = 0V)	—	0.5	LSB
Quantization error	Uncertainty due to converter resolution	—	0.5	LSB
Absolute accuracy	Difference between the actual input voltage and the full-scale equivalent of the binary code output code for all errors	—	1	LSB
Conversion range	Analog input voltage range	V_{RL}	V_{RH}	V
V_{RH}	Maximum analog reference voltage	V_{RL}	V_{DD} + 0.1	V
V_{RL}	Minimum analog reference voltage	V_{SS} – 0.1	V_{RH}	V
V_R(1)	Minimum difference between V_{RH} and V_{RL}	3	—	V
Conversion time	Total time to perform a single analog to digital conversion a. External clock (OSC1, OSC2) b. Internal RC oscillator	 — —	 32 32	 t_{CYC} µs
Monotonicity	Conversion result never decreases with an increase in input voltage and has no missing codes	GUARANTEED		
Zero input reading	Conversion result when $V_{IN} = V_{RL}$	00	—	Hex
Full scale reading	Conversion result when $V_{IN} = V_{RH}$	—	FF	Hex
Sample acquisition time	Analog input acquisition sampling a. External clock (OSC1, OSC2) b. Internal RC oscillator(2)	 — —	 12 12	 t_{CYC} s
Sample/hold capacitance	Input capacitance on PD0/AN0–PD7/AN7	—	12	pF
Input leakage(3)	Input leakage on A/D pins PD0/AN0–PD7/AN7, VRL, VRH	—	1	µA

(1) Performance verified down to 2.5V VR, but accuracy is tested and guaranteed at VR = 5V 10%.

(2) Source impedances greater than 10k will adversely affect internal charging time during input sampling.

(3) The external system error caused by input leakage current is approximately equal to the product of R source and input current. Input current to A/D channel will be dependent on external source impedance (see Figure 8-2).

E.3 Control timing

Table E-11 A/D characteristics for 3.3V operation

(V_{DD} = 3.3 Vdc 10%, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H)

Characteristic	Parameter	Min	Max	Unit
Resolution	Number of bits resolved by the A/D	8	—	Bit
Non-linearity	Max deviation from the best straight line through the A/D transfer characteristics ($V_{RH} = V_{DD}$ and V_{RL} = 0V)	—	1	LSB
Quantization error	Uncertainty due to converter resolution	—	1	LSB
Absolute accuracy	Difference between the actual input voltage and the full-scale equivalent of the binary code output code for all errors	—	2	LSB
Conversion range	Analog input voltage range	V_{RL}	V_{RH}	V
V_{RH}	Maximum analog reference voltage	V_{RL}	V_{DD} + 0.1	V
V_{RL}	Minimum analog reference voltage	V_{SS} – 0.1	V_{RH}	V
V_R	Minimum difference between V_{RH} and V_{RL}	3	—	V
Conversion time	Total time to perform a single analog to digital conversion Internal RC oscillator	—	32	µs
Monotonicity	Conversion result never decreases with an increase in input voltage and has no missing codes	GUARANTEED		
Zero input reading	Conversion result when $V_{IN} = V_{RL}$	00	—	Hex
Full scale reading	Conversion result when $V_{IN} = V_{RH}$	—	FF	Hex
Sample acquisition time	Analog input acquisition sampling Internal RC oscillator(1)	—	12	s
Sample/hold capacitance	Input capacitance on PD0/AN0–PD7/AN7	—	12	pF
Input leakage(2)	Input leakage on A/D pins PD0/AN0–PD7/AN7, VRL, VRH	—	1	µA

(1) Source impedances greater than 10k will adversely affect internal charging time during input sampling.

(2) The external system error caused by input leakage current is approximately equal to the product of R source and input current. Input current to A/D channel will be dependent on external source impedance (see Figure 8-2).

Table E-12 Control timing for 5V operation

(V_{DD} = 5.0 Vdc ± 10%, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H)

Characteristic	Symbol	Min	Max	Unit
Frequency of operation				
Crystal option	f_{OSC}	—	4.2	MHz
External clock option	f_{OSC}	dc	4.2	MHz
Internal operating frequency (f_{OSC}/2)				
Crystal	f_{OP}	dc	2.1	MHz
External clock	f_{OP}	dc	2.1	MHz
Cycle time (see Figure 9-1)	t_{CYC}	480	—	ns
Crystal oscillator start-up time (see Figure 9-1)	t_{OXOV}	—	100	ms
Stop recovery start-up time (crystal oscillator)	t_{ILCH}		100	ms
RC oscillator stabilization time	t_{ADRC}		100	ms
A/D converter stabilization time	t_{ADON}		500	µs
External RESET input pulse width	t_{RL}	1.5	—	t_{CYC}
Power-on RESET output pulse width				
4064 cycle	t_{PORL}	4064	—	t_{CYC}
16 cycle	t_{PORL}	16	—	t_{CYC}
Watchdog RESET output pulse width	t_{DOGL}	1.5	—	t_{CYC}
Watchdog time-out	t_{DOG}	6144	7168	t_{CYC}
EPROM programming time	t_{PROG}	5	20	ms
EEPROM byte erase time				
0 to 70 (standard)	t_{ERA}	10	—	ms
– 40 to 85 (extended)	t_{ERA}	10	—	ms
– 40 to 105 (industrial)	t_{ERA}	10	—	ms
– 40 to 125 (automotive)	t_{ERA}	10	—	ms
EEPROM byte program time(1)				
0 to 70 (standard)	t_{PROG}	10	—	ms
– 40 to 85 (extended)	t_{PROG}	10	—	ms
– 40 to 105 (industrial)	t_{PROG}	15	—	ms
– 40 to 125 (automotive)	t_{PROG}	20	—	ms
Timer (see Figure E-12)				
Resolution(2)	t_{RESL}	4	—	t_{CYC}
Input capture pulse width	t_{TH}, t_{TL}	125	—	ns
Input capture pulse period	t_{TLTL}	—(3)	—	t_{CYC}
Interrupt pulse width (edge-triggered)	t_{ILIH}	125	—	ns
Interrupt pulse period	t_{ILIL}	—(4)	—	t_{CYC}
OSC1 pulse width	t_{OH}, t_{OL}	90	—	ns

(1) For bus frequencies less than 2 MHz, the internal RC oscillator should be used when programming the EEPROM.

(2) Since a 2-bit prescaler in the timer must count four external cycles (t_{cyc}), this is the limiting factor in determining the timer resolution.

(3) The minimum period t_{TLTL} should not be less than the number of cycle times it takes to execute the capture interrupt service routine plus 24 t_{cyc}.

(4) The minimum period t_{ILIL} should not be less than the number of cycle times it takes to execute the interrupt service routine plus 21 t_{cyc}.

Table E-13 Control timing for 3.3V operation

(V_{DD} = 3.3Vdc 10%, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H)

Characteristic	Symbol	Min	Max	Unit
Frequency of operation				
Crystal option	f_{OSC}	—	2.0	MHz
External clock option	f_{OSC}	dc	2.0	MHz
Internal operating frequency (f_{OSC}/2)				
Crystal	f_{OP}	—	1.0	MHz
External clock	f_{OP}	dc	1.0	MHz
Cycle time (see Figure 9-1)	t_{CYC}	1000	—	ns
Crystal oscillator start-up time (see Figure 9-1)	t_{OXOV}	—	100	ms
Stop recovery start-up time (crystal oscillator)	t_{ILCH}		100	ms
RC oscillator stabilization time	t_{ADRC}		100	ms
A/D converter stabilization time	t_{ADON}		500	µs
External $\overline{\text{RESET}}$ input pulse width	t_{RL}	1.5	—	t_{CYC}
Power-on $\overline{\text{RESET}}$ output pulse width				
4064 cycle	t_{PORL}	4064	—	t_{CYC}
16 cycle	t_{PORL}	16	—	t_{CYC}
Watchdog $\overline{\text{RESET}}$ output pulse width	t_{DOGL}	1.5	—	t_{CYC}
Watchdog time-out	t_{DOG}	6144	7168	t_{CYC}
EPROM programming time	t_{PROG}	5	20	ms
EEPROM byte erase time				
0 to 70 (standard)	t_{ERA}	30	—	ms
– 40 to 85 (extended)	t_{ERA}	30	—	ms
– 40 to 105 (industrial)	t_{ERA}	30	—	ms
– 40 to 125 (automotive)	t_{ERA}	30	—	ms
EEPROM byte program time(1)				
0 to 70 (standard)	t_{PROG}	30	—	ms
– 40 to 85 (extended)	t_{PROG}	30	—	ms
– 40 to 85 (industrial)	t_{PROG}	30	—	ms
– 40 to 125 (automotive)	t_{PROG}	30	—	ms
Timer (see Figure E-12)				
Resolution(2)	t_{RESL}	4	—	t_{CYC}
Input capture pulse width	t_{TH}, t_{TL}	250	—	ns
Input capture pulse period	t_{TLTL}	—(3)	—	t_{CYC}
Interrupt pulse width (edge-triggered)	t_{ILIH}	250	—	ns
Interrupt pulse period	t_{ILIL}	—(4)	—	t_{CYC}
OSC1 pulse width	t_{OH}, t_{OL}	200	—	ns

(1) For bus frequencies less than 2 MHz, the internal RC oscillator should be used when programming the EEPROM.

(2) Since a 2-bit prescaler in the timer must count four external cycles (t_{cyc}), this is the limiting factor in determining the timer resolution.

(3) The minimum period t_{TLTL} should not be less than the number of cycle times it takes to execute the capture interrupt service routine plus 24 t_{cyc}.

(4) The minimum period t_{ILIL} should not be less than the number of cycle times it takes to execute the interrupt service routine plus 21 t_{cyc}.

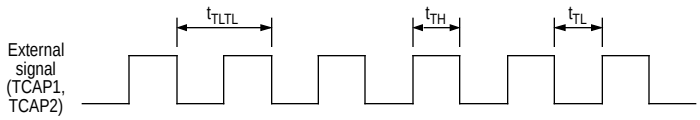

Figure E-12 Timer relationship

F
MC68HC05B32

The MC68HC05B32 is a device similar to the MC68HC05B6, but with increased RAM and ROM sizes. The entire MC68HC05B6 data sheet applies to the MC68HC05B32, with the exceptions outlined in this appendix.

Features

- 31248 bytes User ROM
- No page zero ROM
- 528 bytes of RAM
- 638 bytes of self-check ROM
- 52-pin PLCC, 56-pin SDIP and 64-pin QFP packages

Note: Preliminary electrical specifications for the MC68HC05B32 should be taken as being identical to those for the MC68HC705B32. When silicon is fully available, the part will be re-characterised and new data made available.

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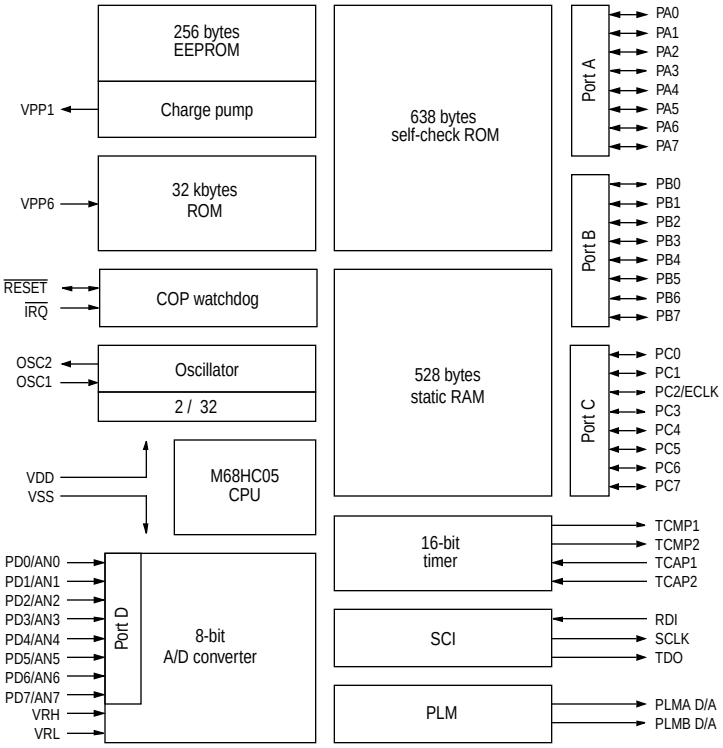

Figure F-1 MC68HC05B32 block diagram

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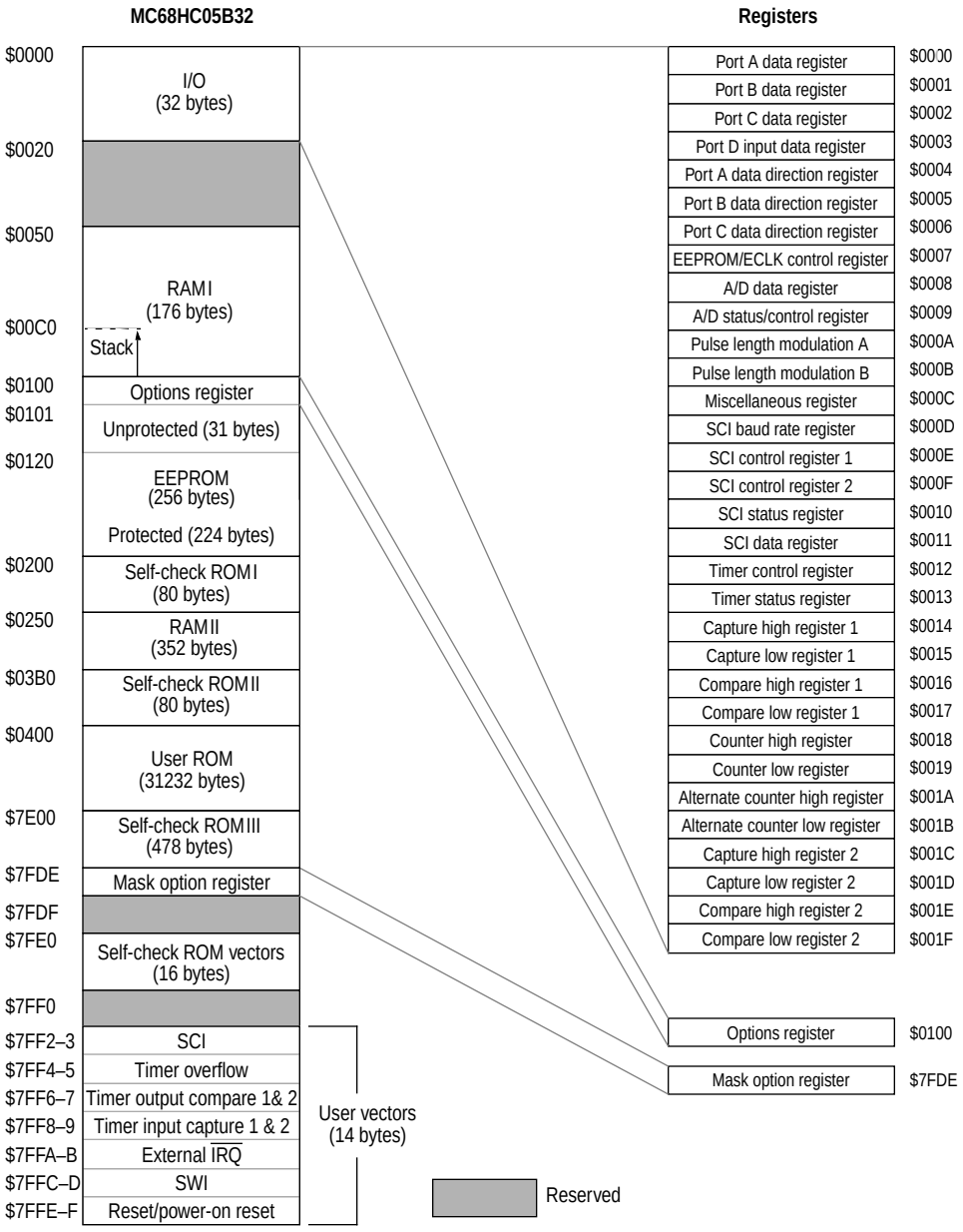

Figure F-2 Memory map of the MC68HC05B32

Table F-1 Register outline

Register name	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
Port A data (PORTA)	$0000									Undefined
Port B data (PORTB)	$0001									Undefined
Port C data (PORTC)	$0002						PC2/ ECLK			Undefined
Port D data (PORTD)	$0003	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0	Undefined
Port A data direction (DDRA)	$0004									0000 0000
Port B data direction (DDRB)	$0005									0000 0000
Port C data direction (DDRC)	$0006									0000 0000
EEPROM/ECLK control	$0007	0	0	0	0	ECLK	E1ERA	E1LAT	E1PGM	0000 0000
A/D data (ADDATA)	$0008									0000 0000
A/D status/control (ADSTAT)	$0009	COCO	ADRC	ADON	0	CH3	CH2	CH1	CH0	0000 0000
Pulse length modulation A (PLMA)	$000A									0000 0000
Pulse length modulation B (PLMB)	$000B									0000 0000
Miscellaneous	$000C	POR(1)	INTP	INTN	INTE	SFA	SFB	SM	WDOG(2)	?001 000?
SCI baud rate (BAUD)	$000D	SPC1	SPC0	SCT1	SCT0	SCT0	SCR2	SCR1	SCR0	00uu uuuu
SCI control 1 (SCCR1)	$000E	R8	T8		M	WAKE	CPOL	CPHA	LBCL	Undefined
SCI control 2 (SCCR2)	$000F	TIE	TCIE	RIE	ILIE	TE	RE	RWU	SBK	0000 0000
SCI status (SCSR)	$0010	TDRE	TC	RDRF	IDLE	OR	NF	FE		1100 000u
SCI data (SCDR)	$0011									0000 0000
Timer control (TCR)	$0012	ICIE	OCIE	TOIE	FOLV2	FOLV1	OLV2	IEDG1	OLVL1	0000 00u0
Timer status (TSR)	$0013	ICF1	OCF1	TOF	ICF2	OCF2				Undefined
Input capture high 1	$0014									Undefined
Input capture low 1	$0015									Undefined
Output compare high 1	$0016									Undefined
Output compare low 1	$0017									Undefined
Timer counter high	$0018									1111 1111
Timer counter low	$0019									1111 1100
Alternate counter high	$001A									1111 1111
Alternate counter low	$001B									1111 1100
Input capture high 2	$001C									Undefined
Input capture low 2	$001D									Undefined
Output compare high 2	$001E									Undefined
Output compare low 2	$001F									Undefined
Options (OPTR)(3)	$0100							EE1P	SEC	Not affected
Mask option register (MOR)(4)	$7FDE				RTIM	RWAT	WWAT	PBPD	PCPD	Not affected

(1) This bit is set each time there is a power-on reset.

(2) The state of the WDOG bit after reset is dependent upon the mask option selected; 1 = watchdog enabled, 0 = watchdog disabled.

(3) This register is implemented in EEPROM; therefore reset has no effect on the individual bits.

(4) This register is implemented in ROM; therefore reset has no effect on the individual bits.

G
MC68HC705B32

The MC68HC705B32 is an EPROM version of the MC68HC05B32, with the ROM replaced by a similar amount of EPROM and with a bootstrap mode instead of a self-check mode. The entire MC68HC05B6 data sheet applies to the MC68HC705B32, with the exceptions outlined in this appendix.

Features

- 31248 bytes user EPROM
- No page zero EPROM at $20–$4F
- 528 bytes of RAM
- 638 bytes bootstrap ROM instead of 432 bytes of self-check ROM
- Simultaneous programming of up to 16 bytes of EPROM
- 52-pin PLCC, 56-pin SDIP and 64-pin QFP packages

Note: The electrical characteristics from the MC68HC05B6 data sheet should not be used for the MC68HC705B32. Data specific to this device can be found in Section G.2.6 and Section G.2.8.

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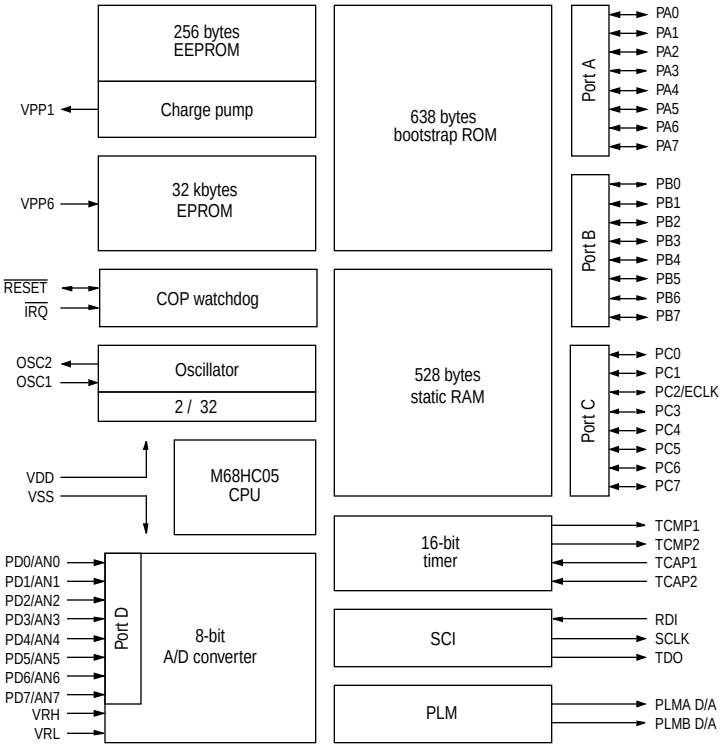

Figure G-1 MC68HC705B32 block diagram

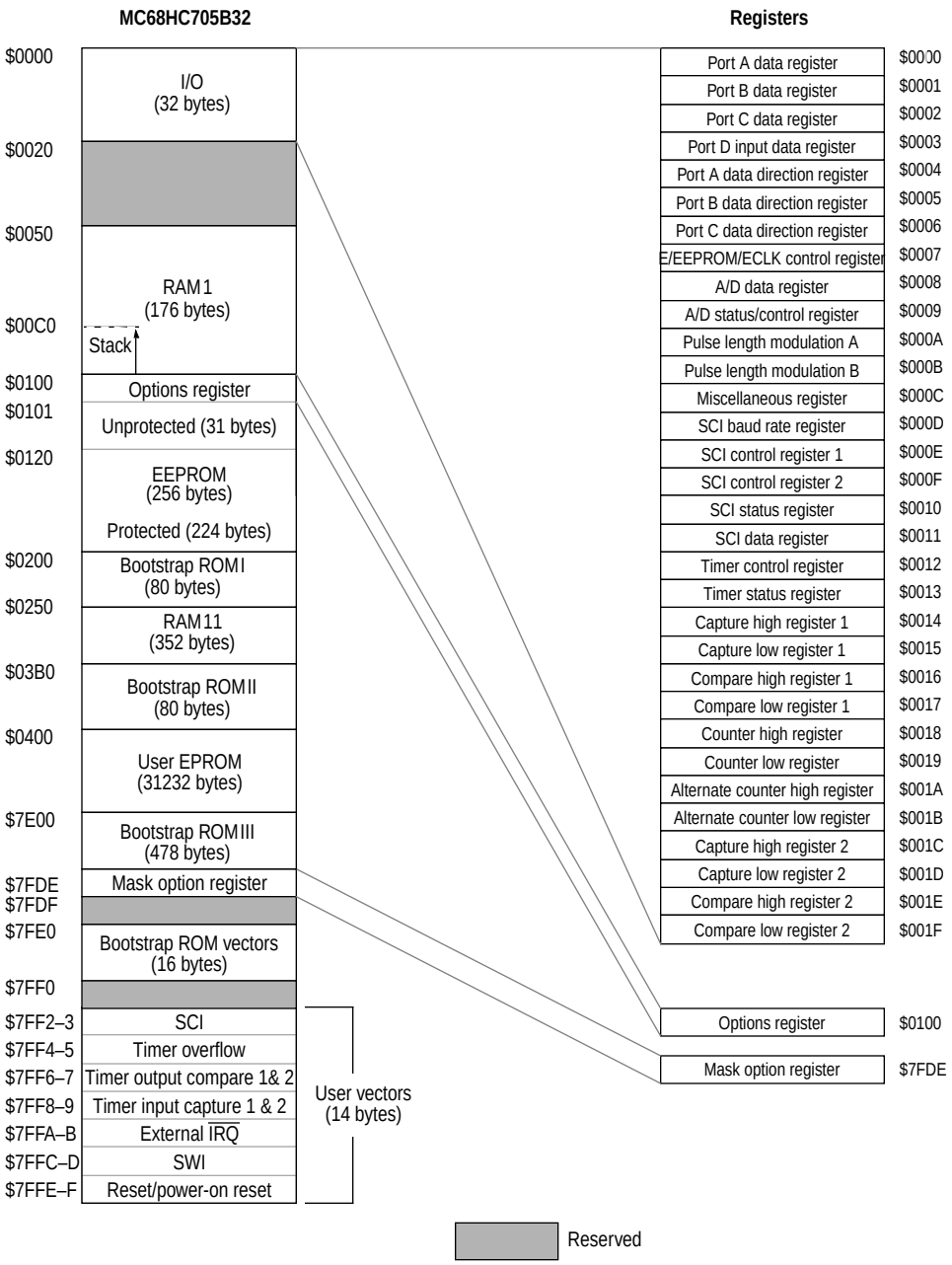

Figure G-2 Memory map of the MC68HC705B32

Table G-1 Register outline

Register name	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
Port A data (PORTA)	$0000									Undefined
Port B data (PORTB)	$0001									Undefined
Port C data (PORTC)	$0002						PC2/ ECLK			Undefined
Port D data (PORTD)	$0003	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0	Undefined
Port A data direction (DDRA)	$0004									0000 0000
Port B data direction (DDRB)	$0005									0000 0000
Port C data direction (DDRC)	$0006									0000 0000
EPROM/EEPROM/ECLK control	$0007		0	E6LAT	E6PGM	ECLK	E1ERA	E1LAT	E1PGM	u000 0000
A/D data (ADDATA)	$0008									0000 0000
A/D status/control (ADSTAT)	$0009	COCO	ADRC	ADON	0	CH3	CH2	CH1	CH0	0000 0000
Pulse length modulation A (PLMA)	$000A									0000 0000
Pulse length modulation B (PLMB)	$000B									0000 0000
Miscellaneous	$000C	POR(1)	INTP	INTN	INTE	SFA	SFB	SM	WDOG(2)	?001 000?
SCI baud rate (BAUD)	$000D	SPC1	SPC0	SCT1	SCT0	SCT0	SCR2	SCR1	SCR0	00uu uuuu
SCI control 1 (SCCR1)	$000E	R8	T8		M	WAKE	CPOL	CPHA	LBCL	Undefined
SCI control 2 (SCCR2)	$000F	TIE	TCIE	RIE	ILIE	TE	RE	RWU	SBK	0000 0000
SCI status (SCSR)	$0010	TDRE	TC	RDRF	IDLE	OR	NF	FE		1100 000u
SCI data (SCDR)	$0011									0000 0000
Timer control (TCR)	$0012	ICIE	OCIE	TOIE	FOLV2	FOLV1	OLV2	IEDG1	OLVL1	0000 00u0
Timer status (TSR)	$0013	ICF1	OCF1	TOF	ICF2	OCF2				Undefined
Input capture high 1	$0014									Undefined
Input capture low 1	$0015									Undefined
Output compare high 1	$0016									Undefined
Output compare low 1	$0017									Undefined
Timer counter high	$0018									1111 1111
Timer counter low	$0019									1111 1100
Alternate counter high	$001A									1111 1111
Alternate counter low	$001B									1111 1100
Input capture high 2	$001C									Undefined
Input capture low 2	$001D									Undefined
Output compare high 2	$001E									Undefined
Output compare low 2	$001F									Undefined
Options (OPTR)(3)	$0100							EE1P	SEC	Not affected
Mask option register (MOR)(4)	$7FDE				RTIM	RWAT	WWAT	PBPD	PCPD	Not affected

(1) This bit is set each time there is a power-on reset.

(2) The state of the WDOG bit after reset is dependent upon the mask option selected; 1=watchdog enabled, 0=watchdog disabled.

(3) This register is implemented in EEPROM; therefore reset has no effect on the individual bits.

(4) This register is implemented in EPROM; therefore reset has no effect on the individual bits.

G.1 EPROM

Figure G-2 shows the MC68HC705B32 memory map. The device has a total of 31232 bytes of EPROM (including 14 bytes for User vectors) and 256 bytes of EEPROM.

The EPROM array is supplied by the VPP6 pin in both read and program modes. Typically the user's software will be loaded into a programming board where V_{PP6} is controlled by one of the bootstrap loader routines. It will then be placed in an application where no programming occurs. In this case the VPP6 pin should be hardwired to V_{DD}.

Warning: A minimum V_{DD} voltage must be applied to the VPP6 pin at all times, including power-on. Failure to do so could result in permanent damage to the device.

G.1.1 EPROM read operation

The execution of a program in the EPROM address range or a load from the EPROM are both read operations. The E6LAT bit in the EPROM/EEPROM control register should be cleared to '0' which automatically resets the E6PGM bit. In this way the EPROM is read like a normal ROM. Reading the EPROM with the E6LAT bit set will give data that does not correspond to the actual memory content. As interrupt vectors are in EPROM, they will not be loaded when E6LAT is set. Similarly, the bootstrap ROM routines cannot be executed when E6LAT is set. In read mode, the VPP6 pin must be at the V_{DD} level. When entering the STOP mode, the EPROM is automatically set to the read mode.

Note: An erased byte reads as $00.

G.1.2 EPROM program operation

Typically, the EPROM will be programmed by the bootstrap routines resident in the on-chip ROM. However, the user program can be used to program some EPROM locations if the proper procedure is followed. In particular, the programming sequence must be running in RAM, as the EPROM will not be available for code execution while the E6LAT bit is set. The V_{PP6} switching must occur externally after EPGM is set, for example under control of a signal generated on a pin by the programming routine.

Note: When the part becomes a PROM, only the cumulative programming of bits to logic '1' is possible if multiple programming is made on the same byte.

To allow simultaneous programming of up to sixteen bytes, these bytes must be in the same group of addresses which share the same most significant address bits; only the four LSBs can change.

G.1.3 EPROM/EEPROM control register

	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
EPROM/EEPROM/ECLK control	$0007		0	E6LAT	E6PGM	ECLK	E1ERA	E1LAT	E1PGM	u000 0000

E6LAT — EPROM programming latch enable bit

1 (set) – Address and up to sixteen data bytes can be latched into the EPROM for further programming providing the E6PGM bit is cleared.

0 (clear) – Data can be read from the EPROM or firmware ROM; the E6PGM bit is reset to zero when E6LAT is ‘0’.

STOP, power-on and external reset clear the E6LAT bit.

Note: After the t_{ERA1} erase time or t_{PROG1} programming time, the E6LAT bit has to be reset to zero in order to clear the E6PGM bit.

E6PGM — EPROM program enable bit

This bit is the EPROM program enable bit. It can be set to ‘1’ to enable programming only after E6LAT is set and at least one byte is written to the EPROM. It is not possible to clear this bit using software but clearing E6LAT will always clear E6PGM.

Table G-2 EPROM control bits description

E6LAT	E6PGM	Description
0	0	Read/execute in EPROM
1	0	Ready to write address/data to EPROM
1	1	programming in progress

Note: All combinations are not shown in the above table, since the E6PGM bit is cleared when the E6LAT bit is at zero, and will result in a read condition.

ECLK

See Section 4.3.

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E1ERA — EEPROM erase/programming bit

Providing the E1LAT and E1PGM bits are at logic one, this bit indicates whether the access to the EEPROM is for erasing or programming purposes.

1 (set) – An erase operation will take place.

0 (clear) – A programming operation will take place.

Once the program/erase EEPROM address has been selected, E1ERA cannot be changed.

E1LAT — EEPROM programming latch enable bit

1 (set) – Address and data can be latched into the EEPROM for further program or erase operations, providing the E1PGM bit is cleared.

0 (clear) – Data can be read from the EEPROM. The E1ERA bit and the E1PGM bit are reset to zero when E1LAT is '0'.

STOP, power-on and external reset clear the E1LAT bit.

Note: After the t_{ERA1} erase time or t_{PROG1} programming time, the E1LAT bit has to be reset to zero in order to clear the E1ERA bit and the E1PGM bit.

E1PGM — EEPROM charge pump enable/disable

1 (set) – Internal charge pump generator switched on.

0 (clear) – Internal charge pump generator switched off.

When the charge pump generator is on, the resulting high voltage is applied to the EEPROM array. This bit cannot be set before the data is selected, and once this bit has been set it can only be cleared by clearing the E1LAT bit.

A summary of the effects of setting/clearing bits 0, 1 and 2 of the control register are given in Table G-3.

Table G-3 EEPROM control bits description

E1ERA	E1LAT	E1PGM	Description
0	0	0	Read condition
0	1	0	Ready to load address/data for program/erase
0	1	1	Byte programming in progress
1	1	0	Ready for byte erase (load address)
1	1	1	Byte erase in progress

Note: The E1PGM and E1ERA bits are cleared when the E1LAT bit is at zero.

G.1.4 Mask option register

	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
Mask option register (MOR)(1)	$7FDE				RTIM	RWAT	WWAT	PBPD	PCPD	Not affected

(1) Because this register is implemented in EPROM, reset has no effect on the individual bits.

RTIM

This bit can modify the time t_{PORL}, where the $\overline{\text{RESET}}$ pin is kept low after a power-on reset.

1 (set) – t_{PORL} = 16 cycles.

0 (clear) – t_{PORL} = 4064 cycles.

RWAT

This bit can modify the status of the watchdog counter after reset. Usually, the watchdog system is disabled after power-on or external reset but when this bit is set, it will be active immediately after the following resets (except in bootstrap mode).

WWAT

This bit can modify the status of the watchdog counter in WAIT mode. Normally, the watchdog system is disabled in WAIT mode but when this bit is set, the watchdog will be active in WAIT mode.

PBPD

This bit, when programmed, connects a resistive pull-down on all 8 pins of port B. This pull-down, R_{PD}, is active on a given pin only while it is an input.

PCPD

This bit, when programmed, connects a resistive pull-down on all 8 pins of port C. This pull-down, R_{PD}, is active on a given pin only while it is an input.

G.1.5 Options register (OPTR)

	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
Options (OPTR)(1)	$0100							EE1P	SEC	Not affected

(1) Because this register is implemented in EEPROM, reset has no effect on the individual bits.

EE1P – EEPROM protect bit

In order to achieve a higher degree of protection, the EEPROM is effectively split into two parts, both working from the VPP1 charge pump. Part 1 of the EEPROM array (32 bytes from $0100 to $011F) cannot be protected; part 2 (224 bytes from $0120 to $01FF) is protected by the EE1P bit of the options register.

1 (set) – Part 2 of the EEPROM array is not protected; all 256 bytes of EEPROM can be accessed for any read, erase or programming operations.

0 (clear) – Part 2 of the EEPROM array is protected; any attempt to erase or program a location will be unsuccessful.

When this bit is set to 1 (erased), the protection will remain until the next power-on or external reset. EE1P can only be written to ‘0’ when the E1LAT bit in the EEPROM control register is set.

Note: The EEPROM1 protect function is disabled while in bootstrap mode.

SEC — Secure bit

This bit allows the EPROM and EEPROM1 to be secured from external access. When this bit is in the erased state (set), the EPROM and EEPROM1 content is not secured and the device may be used in non user mode. When the SEC bit is programmed to ‘zero’, the EPROM and EEPROM1 content is secured by prohibiting entry to the non user mode. To deactivate the secure bit, the EPROM has to be erased by exposure to a high density ultraviolet light, and the device has to be entered into the EPROM erase verification mode with PD1 set. When the SEC bit is changed, its new value will have no effect until the next power-on or external reset.

1 (set) – EEPROM/EPROM not protected.

0 (clear) – EEPROM/EPROM protected.

G.2 Bootstrap mode

The 432 bytes of self-check firmware on the MC68HC05B6 are replaced by 654 bytes of bootstrap firmware. A detailed description of the modes of operation within bootstrap mode is given below.

The bootstrap program in mask ROM address locations $0200 to $024F, $03B0 to $3FFF, $7E00 to $7FDD and $7FE0 to $7FEF can be used to program the EPROM and the EEPROM, to check if the EPROM is erased or to load and execute data in RAM.

After reset, while going to the bootstrap mode, the vector located at address $7FEE and $7FEF ($\overline{\text{RESET}}$) is fetched to start execution of the bootstrap program. To place the part in bootstrap mode, the $\overline{\text{IRQ}}$ pin should be at $2xV_{DD}$ with the TCAP1 pin 'high' during transition of the $\overline{\text{RESET}}$ pin from low to high. The hold time on the $\overline{\text{IRQ}}$ and TCAP1 pins is two clock cycles after the external $\overline{\text{RESET}}$ pin is brought high.

When the MC68HC705B32 is placed in the bootstrap mode, the bootstrap reset vector will be fetched and the bootstrap firmware will start to execute. Table G-4 shows the conditions required to enter each level of bootstrap mode on the rising edge of $\overline{\text{RESET}}$.

Table G-4 Mode of operation selection

$\overline{\text{IRQ}}$ pin	TCAP1 pin	PD1	PD2	PD3	PD4	Mode
V_{SS} to V_{DD}	V_{SS} to V_{DD}	x	x	x	x	Single chip
+ 9 Volts	V_{DD}	0	0	0	x	Erased EPROM verification
+ 9 Volts	V_{DD}	1	0	0	0	Erased EPROM verification; erase EEPROM; EPROM/EEPROM parallel program/verify
+ 9 Volts	V_{DD}	0	1	0	0	Erased EPROM verification; no EEPROM erase if SEC is zero (parallel mode)
+ 9 Volts	V_{DD}	1	1	0	0	Erased EPROM verification; erase EEPROM; EPROM parallel program/verify (no E^2)
+ 9 Volts	V_{DD}	x	1	1	0	Jump to start of RAM ($0051); SEC bit = 0
+ 9 Volts	V_{DD}	0	1	0	1	EPROM and EEPROM verification; SEC bit = 0 (parallel mode)
+ 9 Volts	V_{DD}	x	x	1	1	Serial RAM load/execute – similar to MC68HC05B6 but can fill RAM I, II and III

x = Don't care

The bootstrap program will first copy part of itself in RAM (except 'RAM parallel load'), as the program cannot be executed in ROM during verification/programming of the EPROM. It will then set the TCMP1 output to a logic high level, unlike the MC68HC05B6 which keeps TCMP1 low. This can be used to distinguish between the two circuits and, in particular, for selection of the VPP level and current capability.

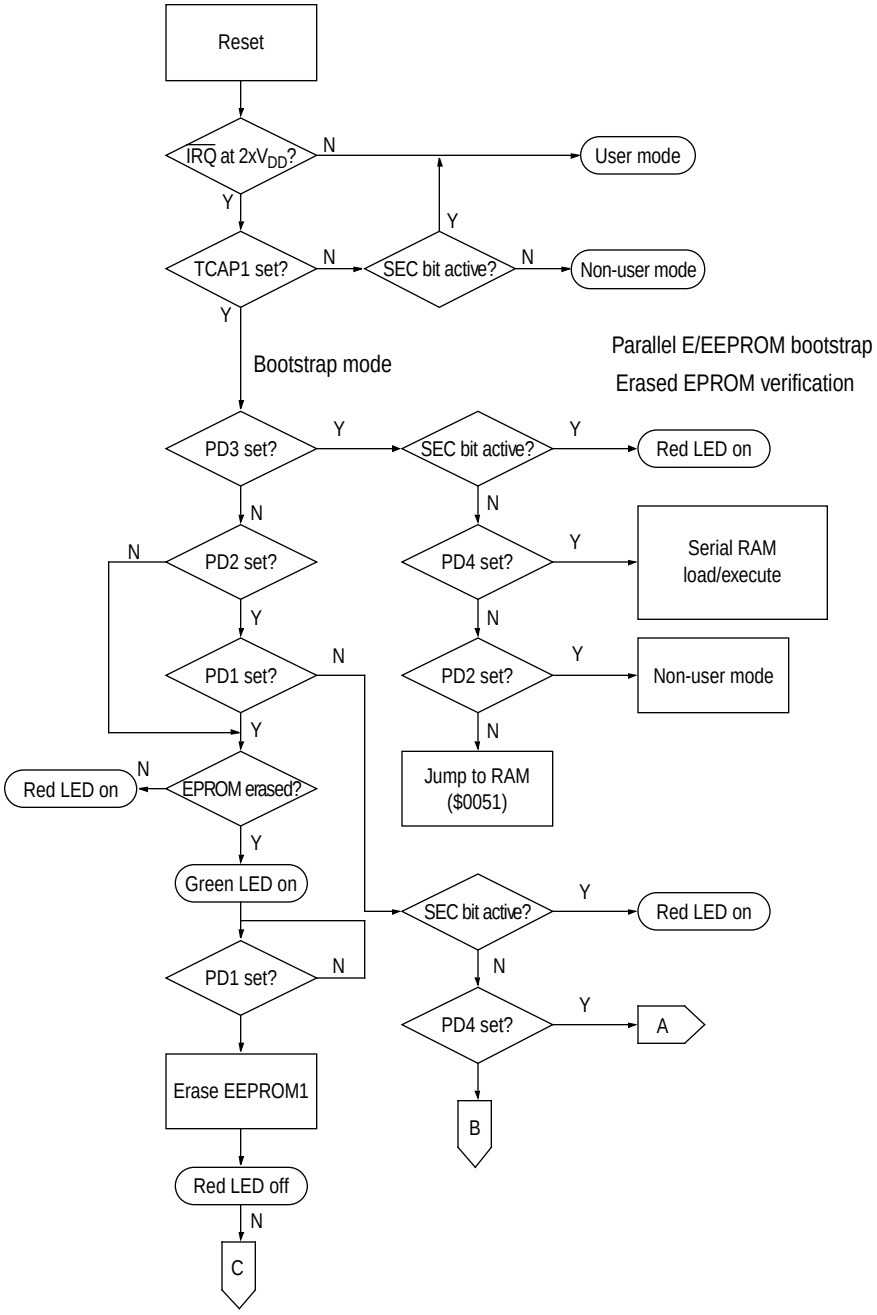


Figure G-3 Modes of operation flow chart (1 of 2)

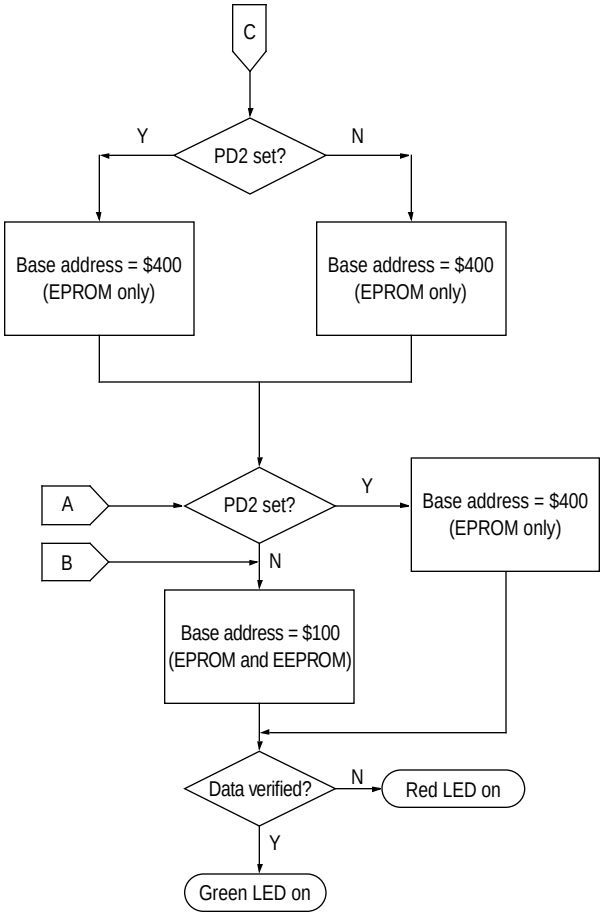


Figure G-4 Modes of operation flow chart (2 of 2)

G.2.1 Erased EPROM verification

If a non $00 byte is detected, the red LED will be turned on and the routine will stop (see Figure G-3 and Figure G-4). Only when the whole EPROM content is verified as erased will the green LED be turned on. PD1 is then checked. If PD1=0, the bootstrap program stops here and no programming occurs until such time as a high level is sensed on PD1. If PD1 = 1, the bootstrap program proceeds to erase the EEPROM1 for a nominal 2.5 seconds (4.0 MHz crystal). It is then checked for complete erasure; if any EEPROM byte is not erased, the program will stop before erasing the SEC byte. When both EPROM and EEPROM1 are completely erased and the security bit is cleared the programming operation can be performed. A schematic diagram of the circuit required for erased EPROM verification is shown in Figure G-7.

G.2.2 EPROM/EEPROM parallel bootstrap

Within this mode there are various subsections which can be utilised by correctly configuring the port pins shown in Table G-4.

The erased EPROM verification program will be executed first as described in Section G.2.1. When PD2=0, the programming time is set to 5 milliseconds with the bootstrap program and verify for the EPROM taking approximately 15 seconds. The EPROM will be loaded in increasing address order with non EPROM segments being skipped by the loader. Simultaneous programming is performed by reading sixteen bytes of data before actual programming is performed, thus dividing the loading time of the internal EPROM by 16. If any block of 16 EPROM bytes or 1 EEPROM byte of data is in the erased state, no programming takes place, thus speeding up the execution time.

Parallel data is entered through Port A, while the 15-bit address is output on port B, PC0 to PC4 and TCMP1 and TCMP2. If the data comes from an external EPROM, the handshake can be disabled by connecting together PC5 and PC6. If the data is supplied by a parallel interface, handshake will be provided by PC5 and PC6 according to the timing diagram of Figure G-5 (see also Figure G-6).

During programming, the green LED will flash at about 3 Hz.

Upon completion of the programming operation, the EPROM and EEPROM1 content will be checked against the external data source. If programming is verified the green LED will stay on, while an error will cause the red LED to be turned on. Figure G-7 is a schematic diagram of a circuit which can be used to program the EPROM or to load and execute data in the RAM.

Note: The entire EPROM and EEPROM1 can be loaded from the external source; if it is desired to leave a segment undisturbed, the data for this segment should be all $00s for EPROM data and all $FFs for EEPROM1 data.

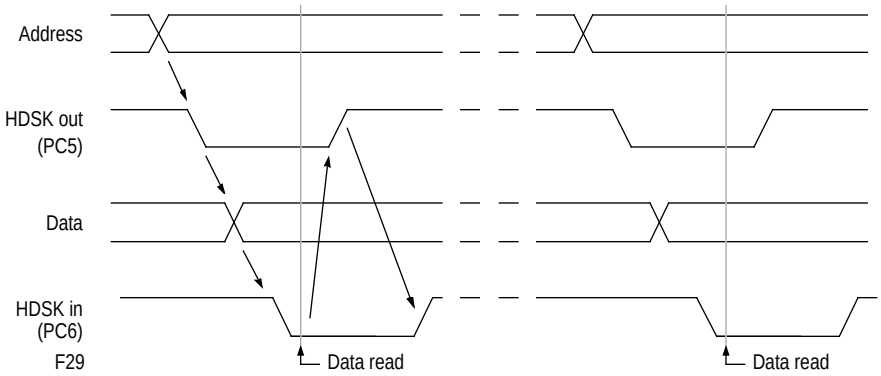
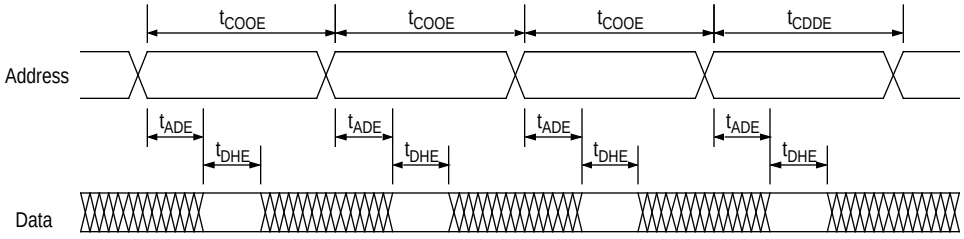


Figure G-5 Timing diagram with handshake



t_{ADE} max (address to data delay)	5 machine cycles
t_{DHA} min (data hold time)	14 machine cycles
t_{COOE} (load cycle time)	117 machine cycles < t_{COOE} < 150 machine cycles
t_{CDDE} (programming cycle time)	t_{COOE} + t_{PROG} (5 ms nominal for EPROM; 10ms for EEPROM1))

1 machine cycle = $1/(2f_0(Xtal))$

Figure G-6 Parallel EPROM loader timing diagram

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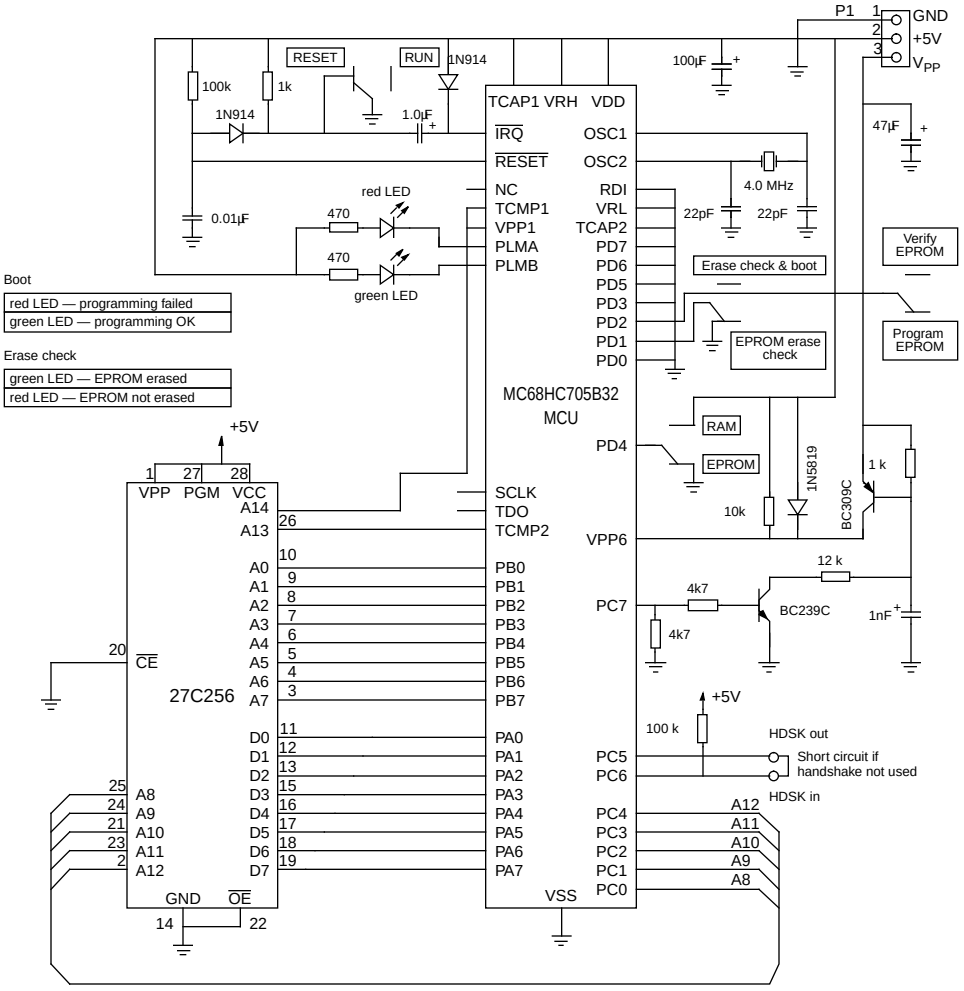


Figure G-7 EPROM parallel bootstrap schematic diagram

G.2.3 Serial RAM loader

This mode is similar to the RAM load/execute program for the MC68HC05B6 described in Section 2.2, with the additional features listed below. Table G-4 shows the entry conditions required for this mode.

If the first byte is less than $B0, the bootloader behaves exactly as the MC68HC05B6, i.e. count byte followed by data stored in $0050 to $00FF. If the count byte is larger than RAM I (176 bytes) then the code continues to fill RAM II then RAM III. In this case the count byte is ignored and the program execution begins at $0051 once the total RAM area is filled or if no data is received for 5 milliseconds.

The user must take care when using branches or jumps as his code will be relocated in RAM I, II and III. If the user intends to use the stack in his program, he should send NOP's to fill the desired stack area.

In the RAM bootloader mode, all interrupt vectors are mapped to pseudo-vectors in RAM (see Table G-5). This allows programmers to use their own service-routine addresses. Each pseudo-vector is allowed three bytes of space rather than the two bytes for normal vectors, because an explicit jump (JMP) opcode is needed to cause the desired jump to the users service-routine address.

Table G-5 Bootstrap vector targets in RAM

Vector targets in RAM	
SCI interrupt	$0063
Timer overflow	$0060
Timer output compare	$005D
Timer input capture	$005A
$\overline{\text{IRQ}}$	$0057
SWI	$0054

G.2.3.1 Jump to start of RAM ($0051)

The Jump to start of RAM program will be executed when bring the device out of reset with PD2 and PD3 at '1' and PD4 at '0'.

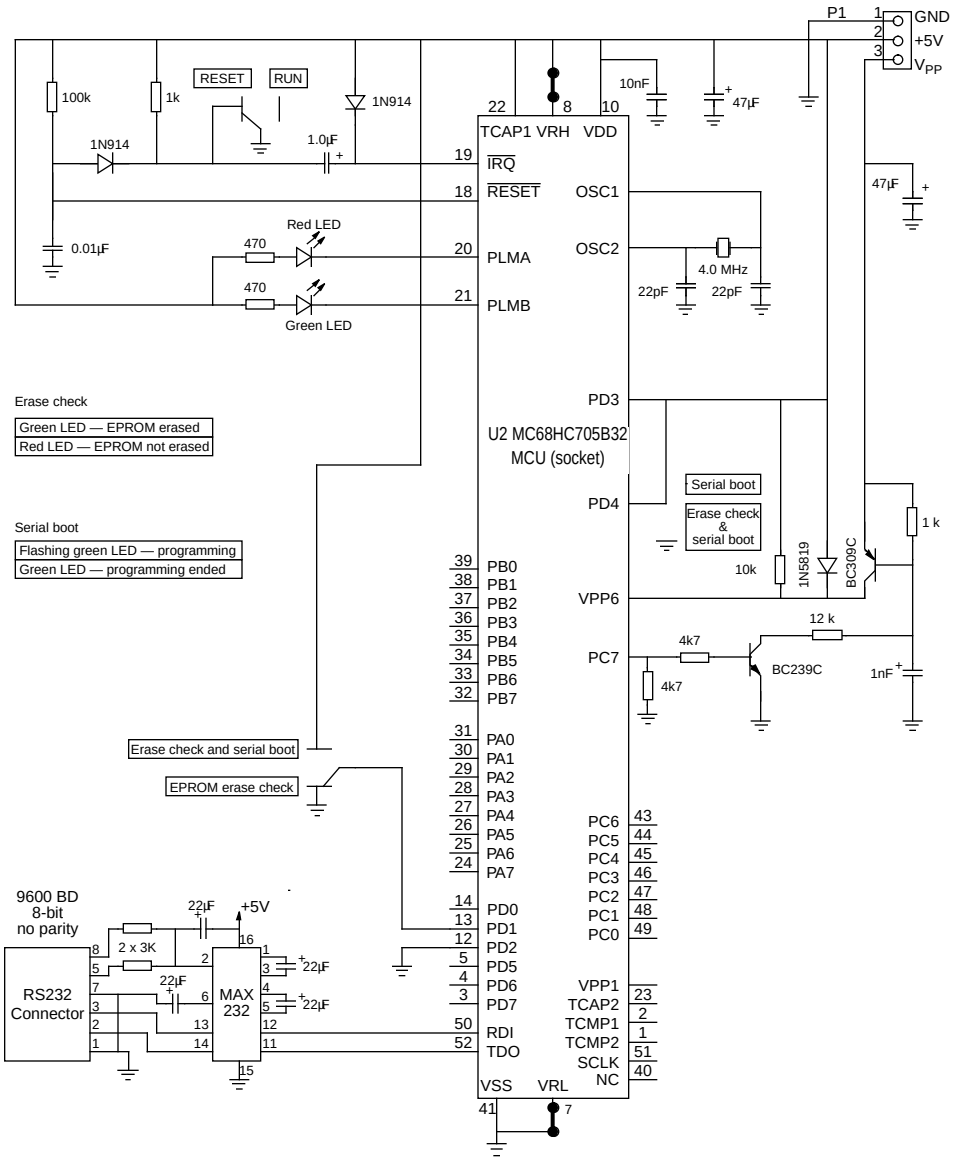
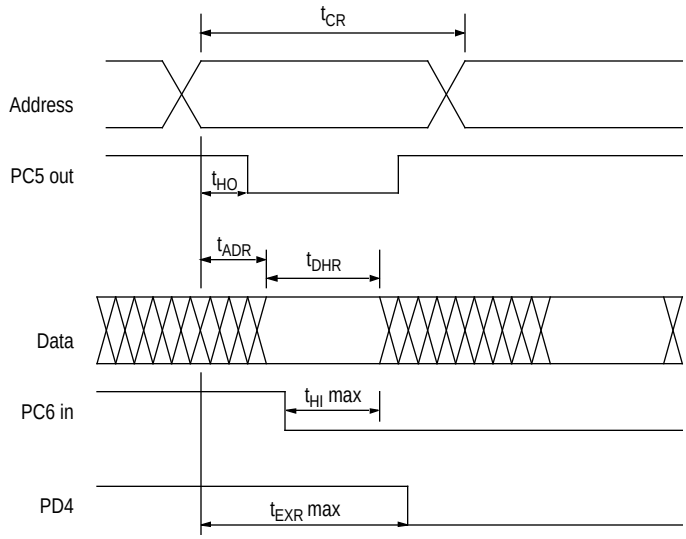


Figure G-8 RAM load and execute schematic diagram



t_{ADR} max (address to data delay; PC6=PC5)	16 machine cycles
t_{DHR} min (data hold time)	4 machine cycles
t_{CR} (load cycle time; PC6=PC5)	49 machine cycles
t_{HO} (PC5 handshake out delay)	5 machine cycles
t_{HI} max (PC6 handshake in, data hold time)	10 machine cycles
t_{EXR} max (max delay for transition to be recognised during this cycle; PC6=PC5	30 machine cycles

1 machine cycle = $1/(2f_0(Xtal))$

Figure G-9 Parallel RAM loader timing diagram

G.2.4 Maximum ratings

Table G-6 Maximum ratings

Rating	Symbol	Value	Unit
Supply voltage(1)	V_{DD}	– 0.5 to +7.0	V
Input voltage	V_{IN}	V_{SS} – 0.5 to V_{DD} + 0.5	V
Input voltage – Self-check mode ($\overline{IRQ}$ pin only)	V_{IN}	V_{SS} – 0.5 to 2V_{DD} + 0.5	V
Operating temperature range – Standard (MC68HC705B32) – Extended (MC68HC705B32C) – Industrial (MC68HC705B32V) – Automotive (MC68HC705B32M)	T_A	T_L to T_H 0 to +70 –40 to +85 –40 to +105 –40 to +125	C
Storage temperature range	T_{STG}	– 65 to +150	C
Current drain per pin (excluding VDD and VSS)(2) – Source – Sink	 I_D I_S	 25 45	 mA mA

(1) All voltages are with respect to V_{SS}.

(2) Maximum current drain per pin is for one pin at a time, limited by an external resistor.

Note: This device contains circuitry designed to protect against damage due to high electrostatic voltages or electric fields. However, it is recommended that normal precautions be taken to avoid the application of any voltages higher than those given in the maximum ratings table to this high impedance circuit. For maximum reliability all unused inputs should be tied to either V_{SS} or V_{DD}.

G.2.5 Thermal characteristics and power considerations

Table G-7 Package thermal characteristics

Characteristics	Symbol	Value	Unit
Thermal resistance			
– 64-pin quad flat package	θ_{JA}	50	C/W
– Plastic 56 pin shrink DIL package	θ_{JA}	50	C/W
– Plastic 52 pin PLCC package	θ_{JA}	50	C/W

The average chip junction temperature, T_J, in degrees Celsius can be obtained from the following equation:

$$T_J = T_A + (P_D \bullet \theta_{JA}) \quad [4]$$

where:

T_A = Ambient temperature (C)

θ_{JA} = Package thermal resistance, junction-to-ambient (C/W)

$P_D = P_{INT} + P_{I/O}$ (W)

P_{INT} = Internal chip power = $I_{DD} \bullet V_{DD}$ (W)

$P_{I/O}$ = Power dissipation on input and output pins (user determined)

An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = \frac{K}{T_J + 273} \quad [5]$$

Solving equations [1] and [2] for K gives:

$$K = P_D \bullet (T_A + 273) + \theta_{JA} \bullet P_D^2 \quad [6]$$

where K is a constant for a particular part. K can be determined by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained for any value of T_A by solving the above equations. The package thermal characteristics are shown in Table G-7.

Voltage	Pins	R1	R2	C
4.5V	PA0–7, PB0–7, PC0–7	3.26k	2.38k	50pF
3.0V	PA0–7, PB0–7, PC0–7	10.91k	6.32k	50pF

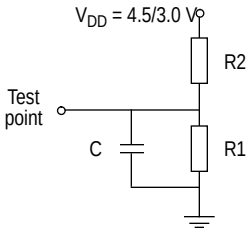


Figure G-10 Equivalent test load

G.2.6 DC electrical characteristics

Table G-8 DC electrical characteristics for 5V operation

(V_{DD} = 5 Vdc 10%, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H)

Characteristic[1]	Symbol	Min	Typ[2]	Max	Unit
Output voltage					
I_{LOAD} = – 10 µA	V_{OH}	V_{DD} – 0.1	—	—	V
I_{LOAD} = +10 µA	V_{OL}	—	—	0.1	
Output high voltage (I_{LOAD} = 0.8 mA)					
PA0–7, PB0–7, PC0–7, TCMP1, TCMP2	V_{OH}	V_{DD} – 0.8	V_{DD} – 0.4	—	V
Output high voltage (I_{LOAD} = 1.6 mA)					
TDO, SCLK, PLMA, PLMB	V_{OH}	V_{DD} – 0.8	V_{DD} – 0.4	—	
Output low voltage (I_{LOAD} = 1.6 mA)					
PA0–7, PB0–7, PC0–7, TCMP1, TCMP2, TDO, SCLK, PLMA, PLMB	V_{OL}	—	0.1	0.4	V
Output low voltage (I_{LOAD} = 1.6 mA)					
$\overline{RESET}$	V_{OL}		0.4	1	
Input high voltage					
PA0–7, PB0–7, PC0–7, PD0–7, OSC1, $\overline{IRQ}$, $\overline{RESET}$, TCAP1, TCAP2, RDI	V_{IH}	0.7V_{DD}	—	V_{DD}	V
Input low voltage					
PA0–7, PB0–7, PC0–7, OSC1, $\overline{IRQ}$, $\overline{RESET}$, TCAP1, TCAP2, RDI	V_{IL}	V_{SS}	—	0.2V_{DD}	V
Supply current[3]					
RUN (SM = 0) (See Figure 11-2)	I_{DD}	—	6	TBD	mA
RUN (SM = 1) (See Figure 11-3)	I_{DD}	—	1.5	TBD	mA
WAIT (SM = 0) (See Figure 11-4)	I_{DD}	—	2	TBD	mA
WAIT (SM = 1) (See Figure 11-5)	I_{DD}	—	1	TBD	mA
STOP					
0 to 70 (standard)	I_{DD}	—	10	TBD	µA
– 40 to 85 (extended)	I_{DD}	—	20	TBD	µA
– 40 to 105 (extended)	I_{DD}	—	60	TBD	µA
– 40 to 125 (automotive)	I_{DD}	—	60	TBD	µA
EPROM					
Absolute maximum voltage	V_{PP6} max	V_{DD}	—	18	V
Programming voltage	V_{PP6}	14.5	15.5	16	V
Programming current	I_{PP6}	—	50	64	mA
Read voltage	V_{PP6R}	V_{DD}	V_{DD}	V_{DD} 10%	V
High-Z leakage current					
PA0–7, PB0–7, PC0–7, TDO, $\overline{RESET}$, SCLK	I_{IL}	—	0.2	1	µA
Input current					
Port B and port C pull-down (V_{IN}=V_{IH})	I_{RPD}		80		µA
Input current (0 to 70)					
$\overline{IRQ}$, OSC1, TCAP1, TCAP2, RDI, PD0/AN0-PD7/AN7 (channel not selected)	I_{IN}	—	0.2	1	µA
Input current (– 40 to 125)					
$\overline{IRQ}$, OSC1, TCAP1, TCAP2, RDI, PD0/AN0-PD7/AN7 (channel not selected)	I_{IN}	—	—	5	µA

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Table G-8 DC electrical characteristics for 5V operation (Continued)

(V_{DD} = 5 Vdc 10%, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H)

Characteristic[1]	Symbol	Min	Typ[2]	Max	Unit
Capacitance					
Ports (as input or output), $\overline{\text{RESET}}$, TDO, SCLK	C_{OUT}	—	—	12	pF
$\overline{\text{IRQ}}$, TCAP1, TCAP2, OSC1, RDI	C_{OUT}	—	—	8	pF
PD0/AN0–PD7/AN7 (A/D off)	C_{IN}	—	12	—	pF
PD0/AN0–PD7/AN7 (A/D on)	C_{IN}	—	22	—	pF

(1) All I_{DD} measurements taken with suitable decoupling capacitors across the power supply to suppress the transient switching currents inherent in CMOS designs (see Section 2).

(2) Typical values are at mid point of voltage range and at 25 C only

(3) RUN and WAIT I_{DD}: measured using an external square-wave clock source (f_{OSC} = 4.2MHz); all inputs 0.2 V from rail; no DC loads; maximum load on outputs 50pF (20pF on OSC2).
STOP /WAIT I_{DD}: all ports configured as inputs; V_{IL} = 0.2 V and $V_{IH} = V_{DD} – 0.2$ V: STOP I_{DD} measured with OSC1 = V_{DD}.
WAIT I_{DD} is affected linearly by the OSC2 capacitance.

Table G-9 DC electrical characteristics for 3.3V operation

(V_{DD} = 3.3Vdc 10%, V_{SS} = 0Vdc, $T_A = T_L$ to T_H)

Characteristic[1]	Symbol	Min	Typ[2]	Max	Unit
Output voltage					
I_{LOAD} = – 10 µA	V_{OH}	V_{DD} – 0.1	—	—	V
I_{LOAD} = +10 µA	V_{OL}	—	—	0.1	
Output high voltage (I_{LOAD} = 0.8mA)					
PA0–7, PB0–7, PC0–7, TCMP1, TCMP2	V_{OH}	V_{DD} – 0.3	V_{DD} – 0.1	—	V
Output high voltage (I_{LOAD} = 1.6mA)					
TDO, SCLK, PLMA, PLMB	V_{OH}	V_{DD} – 0.3	V_{DD} – 0.1	—	
Output low voltage (I_{LOAD} = 1.6mA)					
PA0–7, PB0–7, PC0–7, TCMP1, TCMP2, TDO, SCLK, PLMA, PLMB	V_{OL}	—	0.1	0.4	V
Output low voltage (I_{LOAD} = 1.6mA)					
$\overline{RESET}$	V_{OL}		0.2	0.6	
Input high voltage					
PA0–7, PB0–7, PC0–7, PD0–7, OSC1, $\overline{IRQ}$, $\overline{RESET}$, TCAP1, TCAP2, RDI	V_{IH}	0.7V_{DD}	—	V_{DD}	V
Input low voltage					
PA0–7, PB0–7, PC0–7, OSC1, $\overline{IRQ}$, $\overline{RESET}$, TCAP1, TCAP2, RDI	V_{IL}	V_{SS}	—	0.2V_{DD}	V
Supply current[3]					
RUN (SM = 0) (See Figure 11-2)	I_{DD}	—	3	TBD	mA
RUN (SM = 1) (See Figure 11-3)	I_{DD}	—	1	TBD	mA
WAIT (SM = 0) (See Figure 11-4)	I_{DD}	—	1.5	TBD	mA
WAIT (SM = 1) (See Figure 11-5)	I_{DD}	—	0.5	TBD	mA
STOP					
0 to 70 (standard)	I_{DD}	—	10	TBD	µA
– 40 to 85 (extended)	I_{DD}	—	10	TBD	µA
– 40 to 105 (extended)	I_{DD}	—	40	TBD	µA
– 40 to 125 (automotive)	I_{DD}	—	40	TBD	µA
High-Z leakage current					
PA0–7, PB0–7, PC0–7, TDO, $\overline{RESET}$, SCLK	I_{IL}	—	0.2	1	µA
Input current (0 to 70)					
$\overline{IRQ}$, OSC1, TCAP1, TCAP2, RDI, PD0/AN0-PD7/AN7 (channel not selected)	I_{IN}	—	0.2	1	µA
Input current (– 40 to 125)					
$\overline{IRQ}$, OSC1, TCAP1, TCAP2, RDI, PD0/AN0-PD7/AN7 (channel not selected)	I_{IN}	—	—	5	µA
Capacitance					
Ports (as input or output), $\overline{RESET}$, TDO, SCLK	C_{OUT}	—	—	12	pF
$\overline{IRQ}$, TCAP1, TCAP2, OSC1, RDI	C_{OUT}	—	—	8	pF
PD0/AN0–PD7/AN7 (A/D off)	C_{IN}	—	12	—	pF
PD0/AN0–PD7/AN7 (A/D on)	C_{IN}	—	22	—	pF

(1) All I_{DD} measurements taken with suitable decoupling capacitors across the power supply to suppress the transient switching currents inherent in CMOS designs (see Section 2).

(2) Typical values are at mid point of voltage range and at 25 C only

(3) RUN and WAIT I_{DD}: measured using an external square-wave clock source (f_{OSC} = 2.1MHz); all inputs 0.2 V from rail; no DC loads; maximum load on outputs 50pF (20pF on OSC2).
STOP /WAIT I_{DD}: all ports configured as inputs; V_{IL} = 0.2 V and $V_{IH} = V_{DD}$ – 0.2 V: STOP I_{DD} measured with OSC1 = V_{DD}.
WAIT I_{DD} is affected linearly by the OSC2 capacitance.

G.2.7 A/D converter characteristics

Table G-10 A/D characteristics for 5V operation

(V_{DD} = 5.0 Vdc 10%, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H)

Characteristic	Parameter	Min	Max	Unit
Resolution	Number of bits resolved by the A/D	8	—	Bit
Non-linearity	Max deviation from the best straight line through the A/D transfer characteristics ($V_{RH} = V_{DD}$ and V_{RL} = 0V)	—	0.5	LSB
Quantization error	Uncertainty due to converter resolution	—	0.5	LSB
Absolute accuracy	Difference between the actual input voltage and the full-scale equivalent of the binary code output code for all errors	—	1	LSB
Conversion range	Analog input voltage range	V_{RL}	V_{RH}	V
V_{RH}	Maximum analog reference voltage	V_{RL}	V_{DD} + 0.1	V
V_{RL}	Minimum analog reference voltage	V_{SS} – 0.1	V_{RH}	V
V_R	Minimum difference between V_{RH} and V_{RL}	3	—	V
Conversion time	Total time to perform a single analog to digital conversion a. External clock (OSC1, OSC2) b. Internal RC oscillator	 — —	 32 32	 t_{CYC} µs
Monotonicity	Conversion result never decreases with an increase in input voltage and has no missing codes	GUARANTEED		
Zero input reading	Conversion result when $V_{IN} = V_{RL}$	00	—	Hex
Full scale reading	Conversion result when $V_{IN} = V_{RH}$	—	FF	Hex
Sample acquisition time	Analog input acquisition sampling a. External clock (OSC1, OSC2) b. Internal RC oscillator(1)	 — —	 12 12	 t_{CYC} s
Sample/hold capacitance	Input capacitance on PD0/AN0–PD7/AN7	—	12	pF
Input leakage(2)	Input leakage on A/D pins PD0/AN0–PD7/AN7, VRL, VRH	—	1	µA

(1) Source impedances greater than 10k will adversely affect internal charging time during input sampling.

(2) The external system error caused by input leakage current is approximately equal to the product of R source and input current. Input current to A/D channel will be dependent on external source impedance (see Figure 8-2).

G.2.8 Control timing

Table G-11 A/D characteristics for 3.3V operation

(V_{DD} = 3.3 Vdc 10%, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H)

Characteristic	Parameter	Min	Max	Unit
Resolution	Number of bits resolved by the A/D	8	—	Bit
Non-linearity	Max deviation from the best straight line through the A/D transfer characteristics ($V_{RH} = V_{DD}$ and V_{RL} = 0V)	—	1	LSB
Quantization error	Uncertainty due to converter resolution	—	1	LSB
Absolute accuracy	Difference between the actual input voltage and the full-scale equivalent of the binary code output code for all errors	—	2	LSB
Conversion range	Analog input voltage range	V_{RL}	V_{RH}	V
V_{RH}	Maximum analog reference voltage	V_{RL}	V_{DD} + 0.1	V
V_{RL}	Minimum analog reference voltage	V_{SS} – 0.1	V_{RH}	V
V_R	Minimum difference between V_{RH} and V_{RL}	3	—	V
Conversion time	Total time to perform a single analog to digital conversion Internal RC oscillator	—	32	µs
Monotonicity	Conversion result never decreases with an increase in input voltage and has no missing codes	GUARANTEED		
Zero input reading	Conversion result when $V_{IN} = V_{RL}$	00	—	Hex
Full scale reading	Conversion result when $V_{IN} = V_{RH}$	—	FF	Hex
Sample acquisition time	Analog input acquisition sampling Internal RC oscillator(1)	—	12	s
Sample/hold capacitance	Input capacitance on PD0/AN0–PD7/AN7	—	12	pF
Input leakage(2)	Input leakage on A/D pins PD0/AN0–PD7/AN7, VRL, VRH	—	1	µA

(1) Source impedances greater than 10k will adversely affect internal charging time during input sampling.

(2) The external system error caused by input leakage current is approximately equal to the product of R source and input current. Input current to A/D channel will be dependent on external source impedance (see Figure 8-2).

Table G-12 Control timing for 5V operation

(V_{DD} = 5.0 Vdc ± 10%, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H)

Characteristic	Symbol	Min	Max	Unit
Frequency of operation				
Crystal option	f_{OSC}	—	4.2	MHz
External clock option	f_{OSC}	dc	4.2	MHz
Internal operating frequency (f_{OSC}/2)				
Crystal	f_{OP}	—	2.1	MHz
External clock	f_{OP}	dc	2.1	MHz
Cycle time (see Figure 9-1)	t_{CYC}	480	—	ns
Crystal oscillator start-up time (see Figure 9-1)	t_{OXOV}	—	100	ms
Stop recovery start-up time (crystal oscillator)	t_{ILCH}		100	ms
External RESET input pulse width	t_{RL}	1.5	—	t_{CYC}
Power-on RESET output pulse width				
4064 cycle	t_{PORL}	4064	—	t_{CYC}
16 cycle	t_{PORL}	16	—	t_{CYC}
Watchdog RESET output pulse width	t_{DOGL}	1.5	—	t_{CYC}
Watchdog time-out	t_{DOG}	6144	7168	t_{CYC}
EPROM programming time	t_{PROG}	5	15	ms
EEPROM byte erase time				
0 to 70 (standard)	t_{ERA}	10	—	ms
– 40 to 85 (extended)	t_{ERA}	10	—	ms
– 40 to 105 (industrial)	t_{ERA}	10	—	ms
– 40 to 125 (automotive)	t_{ERA}	10	—	ms
EEPROM byte program time(1)				
0 to 70 (standard)	t_{PROG}	10	—	ms
– 40 to 85 (extended)	t_{PROG}	10	—	ms
– 40 to 105 (industrial)	t_{PROG}	15	—	ms
– 40 to 125 (automotive)	t_{PROG}	20	—	ms
Timer (see Figure G-11)				
Resolution(2)	t_{RESL}	4	—	t_{CYC}
Input capture pulse width	t_{TH}, t_{TL}	125	—	ns
Input capture pulse period	t_{TLTL}	—(3)	—	t_{CYC}
Interrupt pulse width (edge-triggered)	t_{ILIH}	125	—	ns
Interrupt pulse period	t_{ILIL}	—(4)	—	t_{CYC}
OSC1 pulse width	t_{OH}, t_{OL}	90	—	ns

(1) For bus frequencies less than 2 MHz, the internal RC oscillator should be used when programming the EEPROM.

(2) Since a 2-bit prescaler in the timer must count four external cycles (t_{cyc}), this is the limiting factor in determining the timer resolution.

(3) The minimum period t_{TLTL} should not be less than the number of cycle times it takes to execute the capture interrupt service routine plus 24 t_{cyc}.

(4) The minimum period t_{ILIL} should not be less than the number of cycle times it takes to execute the interrupt service routine plus 21 t_{cyc}.

Table G-13 Control timing for operation at 3.3V

(V_{DD} = 3.3Vdc 10%, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H)

Characteristic	Symbol	Min	Max	Unit
Frequency of operation				
Crystal option	f_{OSC}	—	2.0	MHz
External clock option	f_{OSC}	dc	2.0	MHz
Internal operating frequency (f_{OSC}/2)				
Crystal	f_{OP}	—	1.0	MHz
External clock	f_{OP}	dc	1.0	MHz
Cycle time (see Figure 9-1)	t_{CYC}	1000	—	ns
Crystal oscillator start-up time (see Figure 9-1)	t_{OXOV}	—	100	ms
Stop recovery start-up time (crystal oscillator)	t_{ILCH}		100	ms
External $\overline{\text{RESET}}$ input pulse width	t_{RL}	1.5	—	t_{CYC}
Power-on $\overline{\text{RESET}}$ output pulse width				
4064 cycle	t_{PORL}	4064	—	t_{CYC}
16 cycle	t_{PORL}	16	—	t_{CYC}
Watchdog $\overline{\text{RESET}}$ output pulse width	t_{DOGL}	1.5	—	t_{CYC}
Watchdog time-out	t_{DOG}	6144	7168	t_{CYC}
EEPROM byte erase time				
0 to 70 (standard)	t_{ERA}	30	—	ms
– 40 to 85 (extended)	t_{ERA}	30	—	ms
– 40 to 105 (industrial)	t_{ERA}	30	—	ms
– 40 to 125 (automotive)	t_{ERA}	30	—	ms
EEPROM byte program time(1)				
0 to 70 (standard)	t_{PROG}	30	—	ms
– 40 to 85 (extended)	t_{PROG}	30	—	ms
– 40 to 85 (industrial)	t_{PROG}	30	—	ms
– 40 to 125 (automotive)	t_{PROG}	30	—	ms
Timer (see Figure G-11)				
Resolution(2)	t_{RESL}	4	—	t_{CYC}
Input capture pulse width	t_{TH}, t_{TL}	250	—	ns
Input capture pulse period	t_{TLTL}	—(3)	—	t_{CYC}
Interrupt pulse width (edge-triggered)	t_{ILIH}	250	—	ns
Interrupt pulse period	t_{ILIL}	—(4)	—	t_{CYC}
OSC1 pulse width	t_{OH}, t_{OL}	100	—	ns

(1) For bus frequencies less than 2 MHz, the internal RC oscillator should be used when programming the EEPROM.

(2) Since a 2-bit prescaler in the timer must count four external cycles (t_{cyc}), this is the limiting factor in determining the timer resolution.

(3) The minimum period t_{TLTL} should not be less than the number of cycle times it takes to execute the capture interrupt service routine plus 24 t_{cyc}.

(4) The minimum period t_{ILIL} should not be less than the number of cycle times it takes to execute the interrupt service routine plus 21 t_{cyc}.

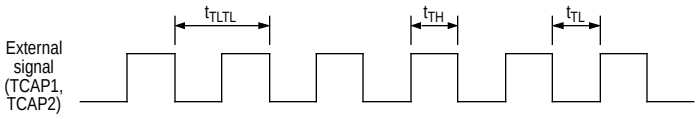

Figure G-11 Timer relationship

H
HIGH SPEED OPERATION

This section contains the electrical specifications and associated timing information for high speed versions of the MC68HC05B6 and MC68HC05B8 (f_{OSC} max = 8 MHz). The ordering information for these devices is contained in Table H-1.

Table H-1 Ordering information

Device title	Package	Suffix 0 to 70 C	Suffix -40 to +85 C
MC68HC05B6	52-pin PLCC	FN	CFN
	64-pin QFP	FU	CFU
	56-pin SDIP	B	CB
MC68HC05B8	52-pin PLCC	FN	CFN
	64-pin QFP	FU	CFU
	56-pin SDIP	B	CB

Note: The high speed version has the same device title as the standard version. High speed operation is selected via a check-box on the order form and will be confirmed on the listing verification form.

H.1 DC electrical characteristics

Table H-2 DC electrical characteristics for 5V operation

(V_{DD} = 5 Vdc 10%, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H)

Characteristic[1]	Symbol	Min	Typ[2]	Max	Unit
Output voltage					
I_{LOAD} = – 10 µA	V_{OH}	V_{DD} – 0.1	—	—	V
I_{LOAD} = +10 µA	V_{OL}	—	—	0.1	
Output high voltage (I_{LOAD} = 0.8 mA)					
PA0–7, PB0–7, PC0–7, TCMP1, TCMP2	V_{OH}	V_{DD} – 0.8	—	—	V
Output high voltage (I_{LOAD} = 1.6 mA)			—		
TDO, SCLK, PLMA, PLMB	V_{OH}	V_{DD} – 0.8	—	—	
Output low voltage (I_{LOAD} = 1.6 mA)					
PA0–7, PB0–7, PC0–7, TCMP1, TCMP2, TDO, SCLK, PLMA, PLMB	V_{OL}	—	—	0.4	V
Output low voltage (I_{LOAD} = 1.6 mA)		—	—		
$\overline{RESET}$	V_{OL}	—	—	1	
Input high voltage					
PA0–7, PB0–7, PC0–7, PD0–7, OSC1, $\overline{IRQ}$, $\overline{RESET}$, TCAP1, TCAP2, RDI	V_{IH}	0.7V_{DD}	—	V_{DD}	V
Input low voltage					
PA0–7, PB0–7, PC0–7, OSC1, $\overline{IRQ}$, $\overline{RESET}$, TCAP1, TCAP2, RDI	V_{IL}	V_{SS}	—	0.2V_{DD}	V
Supply current[3]					
RUN (SM = 0) (See Figure 11-2)		—	—	12	mA
RUN (SM = 1) (See Figure 11-3)		—	—	3	mA
WAIT (SM = 0) (See Figure 11-4)		—	—	4	mA
WAIT (SM = 1) (See Figure 11-5)	I_{DD}	—	—	2	mA
STOP					
0 to 70 (standard)		—	—	10	µA
– 40 to 85 (extended)		—	—	20	µA
High-Z leakage current					
PA0–7, PB0–7, PC0–7, TDO, $\overline{RESET}$, SCLK	I_{IL}	—	—	1	µA
Input current (0 to 70)					
$\overline{IRQ}$, OSC1, TCAP1, TCAP2, RDI,	I_{IN}	—	—	5	µA
PD0/AN0-PD7/AN7 (channel not selected)			—	1	
Capacitance					
Ports (as input or output), $\overline{RESET}$, TDO, SCLK	C_{OUT}	—	—	12	pF
$\overline{IRQ}$, TCAP1, TCAP2, OSC1, RDI	C_{IN}	—	—	8	pF
PD0/AN0–PD7/AN7 (A/D off)	C_{IN}	—	12	TBD	pF
PD0/AN0–PD7/AN7 (A/D on)	C_{IN}	—	22	TBD	pF

(1) All I_{DD} measurements taken with suitable decoupling capacitors across the power supply to suppress the transient switching currents inherent in CMOS designs (see Section 2).

(2) Typical values are at mid point of voltage range and at 25 C only

(3) RUN and WAIT I_{DD}: measured using an external square-wave clock source (f_{OSC} = 8.0MHz); all inputs 0.2 V from rail; no DC loads; maximum load on outputs 50pF (20pF on OSC2).
STOP /WAIT I_{DD}: all ports configured as inputs; V_{IL} = 0.2 V and $V_{IH} = V_{DD}$ – 0.2 V: STOP I_{DD} measured with OSC1 = V_{DD}.
WAIT I_{DD} is affected linearly by the OSC2 capacitance.

H.2 A/D converter characteristics

Table H-3 A/D characteristics for 5V operation

(V_{DD} = 5.0 Vdc 10%, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H)

Characteristic	Parameter	Min	Max	Unit
Resolution	Number of bits resolved by the A/D	8	—	Bit
Non-linearity	Max deviation from the best straight line through the A/D transfer characteristics ($V_{RH} = V_{DD}$ and V_{RL} = 0V)	—	0.5	LSB
Quantization error	Uncertainty due to converter resolution	—	0.5	LSB
Absolute accuracy	Difference between the actual input voltage and the full-scale equivalent of the binary code output code for all errors	—	1	LSB
Conversion range	Analog input voltage range	V_{RL}	V_{RH}	V
V_{RH}	Maximum analog reference voltage	V_{RL}	V_{DD} + 0.1	V
V_{RL}	Minimum analog reference voltage	V_{SS} – 0.1	V_{RH}	V
V_R(1)	Minimum difference between V_{RH} and V_{RL}	3	—	V
Conversion time	Total time to perform a single analog to digital conversion a. External clock (OSC1, OSC2) b. Internal RC oscillator	 — —	 32 32	 t_{CYC} µs
Monotonicity	Conversion result never decreases with an increase in input voltage and has no missing codes	GUARANTEED		
Zero input reading	Conversion result when $V_{IN} = V_{RL}$	00	—	Hex
Full scale reading	Conversion result when $V_{IN} = V_{RH}$	—	FF	Hex
Sample acquisition time	Analog input acquisition sampling a. External clock (OSC1, OSC2) b. Internal RC oscillator(2)	 — —	 12 12	 t_{CYC} s
Sample/hold capacitance	Input capacitance on PD0/AN0–PD7/AN7	—	12	pF
Input leakage(3)	Input leakage on A/D pins PD0/AN0–PD7/AN7 VRL, VRH	— —	1 1	µA µA

(1) Performance verified down to 2.5V VR, but accuracy is tested and guaranteed at VR = 5V 10%.

(2) Source impedances greater than 10k will adversely affect internal charging time during input sampling.

(3) The external system error caused by input leakage current is approximately equal to the product of R source and input current. Input current to A/D channel will be dependent on external source impedance (see Figure 8-2).

H.3 Control timing for 5V operation

(V_{DD} = 5.0 Vdc ± 10%, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H)

Characteristic	Symbol	Min	Max	Unit
Frequency of operation				
Crystal option	f_{OSC}	—	8.0	MHz
External clock option	f_{OSC}	dc	8.0	MHz
Internal operating frequency (f_{OSC}/2)				
Crystal	f_{OP}	—	4.0	MHz
External clock	f_{OP}	dc	4.0	MHz
Cycle time (see Figure 9-1)	t_{CYC}	250	—	ns
Crystal oscillator start-up time (see Figure 9-1)	t_{OXOV}	—	100	ms
Stop recovery start-up time (crystal oscillator)	t_{ILCH}		100	ms
External RESET input pulse width	t_{RL}	1.5	—	t_{CYC}
Power-on RESET output pulse width				
4064 cycle	t_{PORL}	4064	—	t_{CYC}
16 cycle	t_{PORL}	16	—	t_{CYC}
Watchdog RESET output pulse width	t_{DOGL}	1.5	—	t_{CYC}
Watchdog time-out	t_{DOG}	6144	7168	t_{CYC}
EEPROM byte erase time				
0 to 70 (standard)	t_{ERA}	10	—	ms
– 40 to 85 (extended)	t_{ERA}	10	—	ms
EEPROM byte program time(1)				
0 to 70 (standard)	t_{PROG}	10	—	ms
– 40 to 85 (extended)	t_{PROG}	10	—	ms
Timer (see Figure H-1)				
Resolution(2)	t_{RESL}	4	—	t_{CYC}
Input capture pulse width	t_{TH}, t_{TL}	125	—	ns
Input capture pulse period	t_{TLTL}	—(3)	—	t_{CYC}
Interrupt pulse width (edge-triggered)	t_{ILIH}	125	—	ns
Interrupt pulse period	t_{ILIL}	—(4)	—	t_{CYC}
OSC1 pulse width	t_{OH}, t_{OL}	90	—	ns

(1) For bus frequencies less than 2 MHz, the internal RC oscillator should be used when programming the EEPROM.

(2) Since a 2-bit prescaler in the timer must count four external cycles (t_{cyc}), this is the limiting factor in determining the timer resolution.

(3) The minimum period t_{TLTL} should not be less than the number of cycle times it takes to execute the capture interrupt service routine plus 24 t_{cyc}.

(4) The minimum period t_{ILIL} should not be less than the number of cycle times it takes to execute the interrupt service routine plus 21 t_{cyc}.

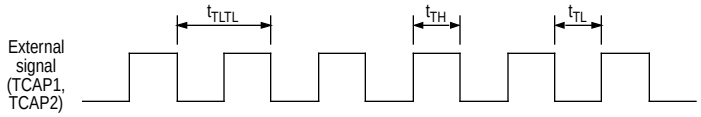

Figure H-1 Timer relationship

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CUSTOMER FEEDBACK QUESTIONNAIRE (MC68HC05B6)

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Understandability	☐	☐	☐	☐	Index	☐	☐	☐	☐
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SECTION 3	MEMORY AND REGISTERS	☐	☐	☐	☐	☐
SECTION 4	INPUT/OUTPUT PORTS	☐	☐	☐	☐	☐
SECTION 5	PROGRAMMABLE TIMER	☐	☐	☐	☐	☐
SECTION 6	SERIAL COMMUNICATIONS INTERFACE	☐	☐	☐	☐	☐
SECTION 7	PULSE LENGTH D/A CONVERTERS	☐	☐	☐	☐	☐
SECTION 8	ANALOG TO DIGITAL CONVERTER	☐	☐	☐	☐	☐
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