

SN54ALS640B, SN54AS640, SN74ALS640B, SN74AS640 OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SDAS122A – DECEMBER 1983 – REVISED JANUARY 1995

- Bidirectional Bus Transceivers in High-Density 20-Pin Packages
- Inverting Logic
- Package Options Include Plastic Small-Outline (DW) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs

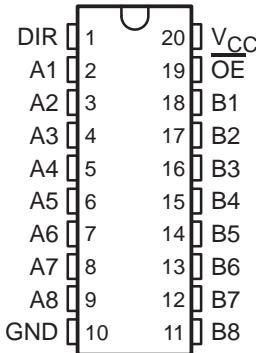
description

These octal bus transceivers are designed for asynchronous two-way communication between data buses. These devices transmit data from the A bus to the B bus or from the B bus to the A bus, depending upon the level at the direction-control (DIR) input. The output-enable (\overline{OE}) input can be used to disable the device so that the buses are effectively isolated.

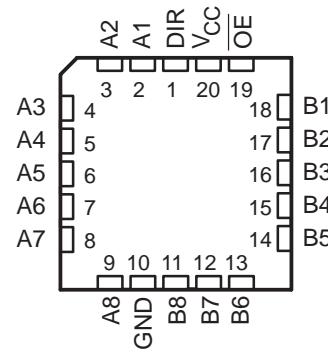
The -1 version of the SN74ALS640B is identical to the standard version, except that the recommended maximum I_{OL} for the -1 version is increased to 48 mA. There is no -1 version of the SN54ALS640B.

The SN54ALS640B and SN54AS640 are characterized for operation over the full military temperature range of -55°C to 125°C . The SN74ALS640B and SN74AS640 are characterized for operation from 0°C to 70°C .

SN54ALS640B, SN54AS640 . . . J PACKAGE
SN74ALS640B, SN74AS640 . . . DW OR N PACKAGE
(TOP VIEW)



SN54ALS640B, SN54AS640 . . . FK PACKAGE
(TOP VIEW)



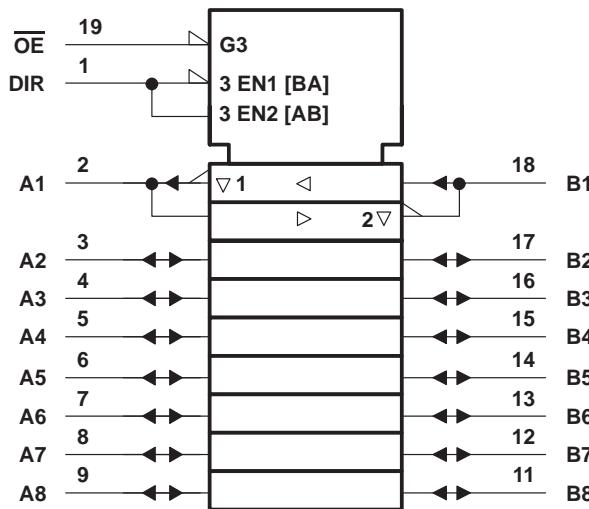
FUNCTION TABLE

INPUTS		OPERATION
\overline{OE}	DIR	
L	L	\overline{B} data to A bus
L	H	\overline{A} data to B bus
H	X	Isolation

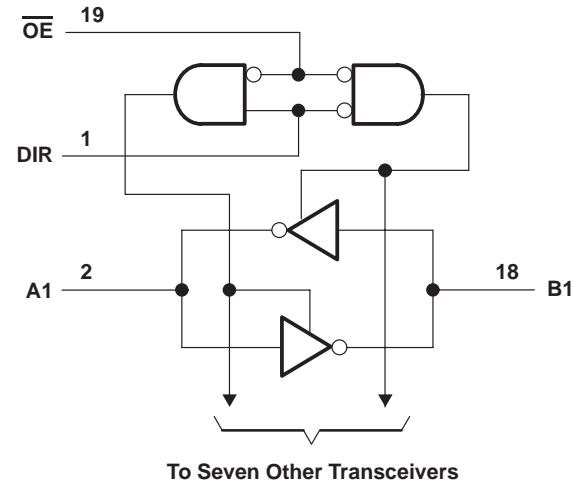
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logic symbol†



logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, V_{CC}	7 V
Input voltage, V_I : All inputs	7 V
I/O ports	5.5 V
Operating free-air temperature range, T_A : SN54ALS640B	-55°C to 125°C
SN74ALS640B	0°C to 70°C
Storage temperature range	-65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		SN54ALS640B			SN74ALS640B			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			-12			-15	mA
I_{OL}	Low-level output current			12			24	mA
							48§	
T_A	Operating free-air temperature	-55	125	0	0	70	70	°C

§ Applies only to the -1 version and only if V_{CC} is between 4.75 V and 5.25 V

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54ALS640B			SN74ALS640B			UNIT
		MIN	TYPT†	MAX	MIN	TYPT†	MAX	
V_{IK}	$V_{CC} = 4.5 \text{ V}$, $I_I = -18 \text{ mA}$			-1.5			-1.5	V
V_{OH}	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$, $I_{OH} = -0.4 \text{ mA}$	$V_{CC} - 2$		$V_{CC} - 2$				V
	$V_{CC} = 4.5 \text{ V}$	$I_{OH} = -3 \text{ mA}$	2.4	3.2	2.4	3.2		
		$I_{OH} = -12 \text{ mA}$	2					
		$I_{OH} = -15 \text{ mA}$				2		
V_{OL}	$V_{CC} = 4.5 \text{ V}$	$I_{OL} = 12 \text{ mA}$	0.25	0.4	0.25	0.4		V
		$I_{OL} = 24 \text{ mA}$			0.35	0.5		
		$I_{OL} = 48 \text{ mA}^{\ddagger}$			0.35	0.5		
I_I	Control inputs	$V_I = 7 \text{ V}$		0.1		0.1		mA
	A or B ports	$V_I = 5.5 \text{ V}$		0.1		0.1		
I_{IH}	Control inputs	$V_{CC} = 5.5 \text{ V}$, $V_I = 2.7 \text{ V}$		20		20		μA
	A or B ports \S			20		20		
I_{IL}	Control inputs	$V_{CC} = 5.5 \text{ V}$, $V_I = 0.4 \text{ V}$		-0.1		-0.1		mA
	A or B ports \S			-0.1		-0.1		
$I_{O\ddagger}$	$V_{CC} = 5.5 \text{ V}$, $V_O = 2.25 \text{ V}$	-20	-112	-30	-112			mA
I_{CC}	$V_{CC} = 5.5 \text{ V}$	Outputs high	19	50	19	45		mA
		Outputs low	27	60	27	55		
		Outputs disabled	28	55	28	50		

† All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

‡ Applies only to the -1 version and only if V_{CC} is between 4.75 V and 5.25 V

§ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

¶ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS} .

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$, $C_L = 50 \text{ pF}$, $R1 = 500 \Omega$, $R2 = 500 \Omega$, $T_A = \text{MIN to MAX}^{\#}$				UNIT	
			SN54ALS640B		SN74ALS640B			
			MIN	MAX	MIN	MAX		
t_{PLH}	A or B	B or A	2	14	2	11	ns	
t_{PHL}			2	13	2	10		
t_{PZH}	\overline{OE}	A or B	4	25	4	21	ns	
t_{PZL}			5	27	5	24		
t_{PHZ}	\overline{OE}	A or B	2	12	2	10	ns	
t_{PLZ}			3	20	3	15		

For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		SN54AS640			SN74AS640			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V _{IH}	High-level input voltage		2		2			V
V _{IL}	Low-level input voltage			0.8			0.8	V
I _{OH}	High-level output current			−12			−15	mA
I _{OL}	Low-level output current			48			64	mA
T _A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54AS640			SN74AS640			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	$V_{CC} = 4.5 \text{ V}$, $I_I = -18 \text{ mA}$			-1.2			-1.2	V
V_{OH}	$V_{CC} = 4.5 \text{ V}$, $I_{OH} = -2 \text{ mA}$	$V_{CC} - 2$						V
	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$, $I_{OH} = -2 \text{ mA}$				$V_{CC} - 2$			
	$V_{CC} = 4.5 \text{ V}$	$I_{OH} = -3 \text{ mA}$	2.4	3.2	2.4	3.2		
		$I_{OH} = -12 \text{ mA}$	2.4					
		$I_{OH} = -15 \text{ mA}$				2.4		
V_{OL}	$V_{CC} = 4.5 \text{ V}$	$I_{OL} = 48 \text{ mA}$	0.3	0.55				V
		$I_{OL} = 64 \text{ mA}$			0.35	0.55		
I_I	Control inputs	$V_{CC} = 5.5 \text{ V}$	$V_I = 7 \text{ V}$		0.1		0.1	mA
	A or B ports		$V_I = 5.5 \text{ V}$		0.1		0.1	
I_{IH}	Control inputs	$V_{CC} = 5.5 \text{ V}$	$V_I = 2.7 \text{ V}$		20		20	μA
	A or B ports\$				70		70	
I_{IL}	Control inputs	$V_{CC} = 5.5 \text{ V}$	$V_I = 0.4 \text{ V}$		-0.5		-0.5	mA
	A or B ports\$				-0.75		-0.75	
$I_O\parallel$	$V_{CC} = 5.5 \text{ V}$, $V_O = 2.25 \text{ V}$		-50	-150	-50	-150		mA
I_{CC}	$V_{CC} = 5.5 \text{ V}$	Outputs high		37	58		37	58
		Outputs low		78	123		78	123
		Outputs disabled		51	80		51	80

† All typical values are at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$.

§ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

¶ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS} .

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switching characteristics (see Figure 1)

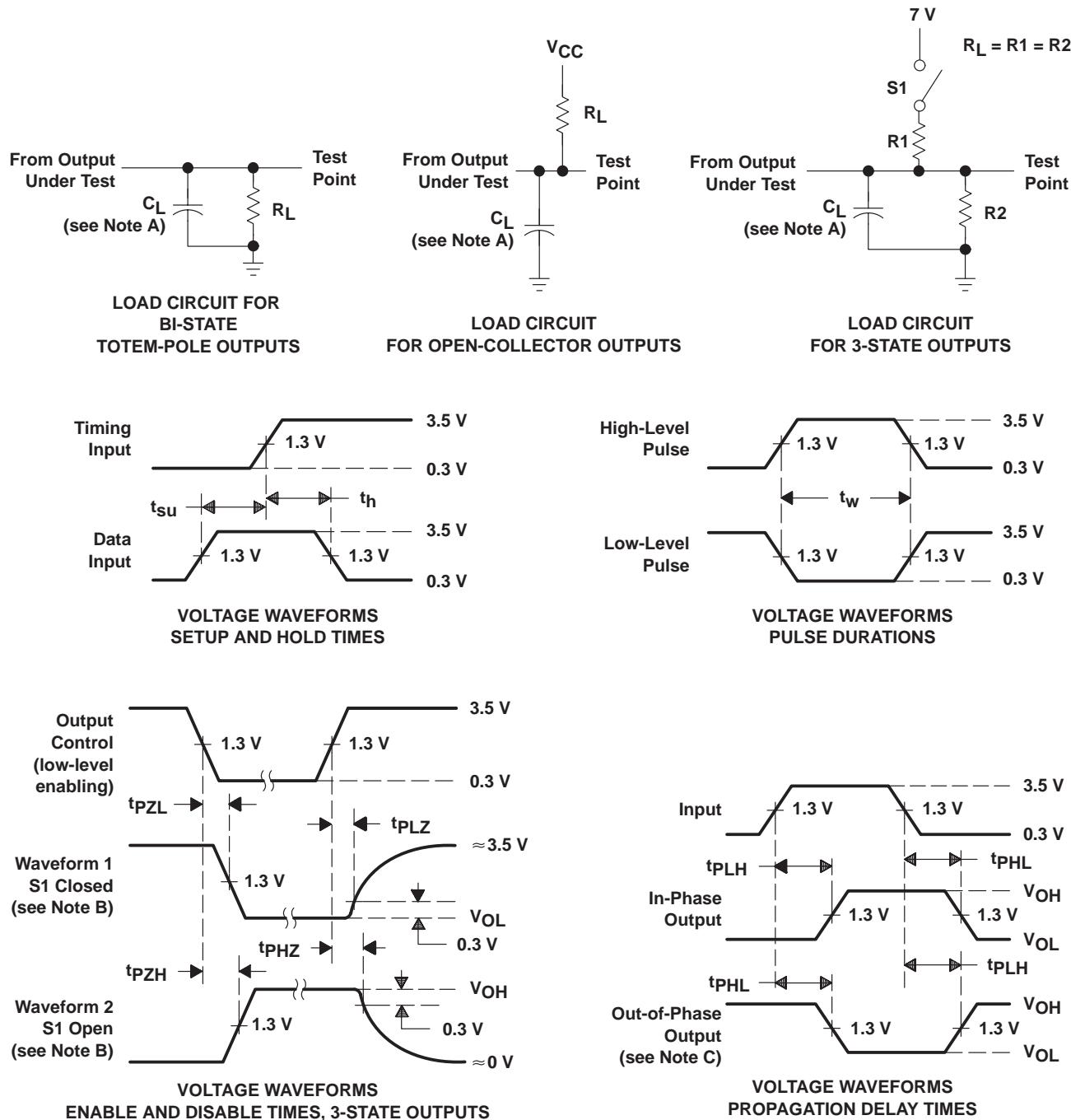
PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4.5\text{ V to }5.5\text{ V}$, $C_L = 50\text{ pF}$, $R1 = 500\text{ }\Omega$, $R2 = 500\text{ }\Omega$, $T_A = \text{MIN to MAX}^{\dagger}$				UNIT	
			SN54AS640		SN74AS640			
			MIN	MAX	MIN	MAX		
t_{PLH}	A or B	B or A	1	8	2	7	ns	
t_{PHL}			1	7	2	6		
t_{PZH}	\overline{OE}	A or B	2	10	2	8	ns	
t_{PZL}			2	12	2	10		
t_{PHZ}	\overline{OE}	A or B	2	9	2	8	ns	
t_{PLZ}			2	16	2	13		

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

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**PARAMETER MEASUREMENT INFORMATION
SERIES 54ALS/74ALS AND 54AS/74AS DEVICES**



NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. When measuring propagation delay items of 3-state outputs, switch S1 is open.
 D. All input pulses have the following characteristics: $PRR \leq 1 \text{ MHz}$, $t_r = t_f = 2 \text{ ns}$, duty cycle = 50%.
 E. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-88727012A	OBsolete	LCCC	FK	20		TBD	Call TI	Call TI	-55 to 125		
5962-8872701RA	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8872701RA SNJ54ALS640BJ	Samples
5962-8872701SA	ACTIVE	CFP	W	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8872701SA SNJ54ALS640BW	Samples
5962-89553012A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962- 89553012A SNJ54AS 640FK	Samples
5962-8955301RA	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8955301RA SNJ54AS640J	Samples
5962-8955301SA	OBsolete	CFP	W	20		TBD	Call TI	Call TI	-55 to 125		
SN54ALS640BJ	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	SN54ALS640BJ	Samples
SN54AS640J	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	SN54AS640J	Samples
SN74ALS640B-1DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS640B-1	Samples
SN74ALS640B-1DWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS640B-1	Samples
SN74ALS640B-1DWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS640B-1	Samples
SN74ALS640B-1N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74ALS640B-1N	Samples
SN74ALS640B-1N3	OBsolete	PDIP	N	20		TBD	Call TI	Call TI	0 to 70		
SN74ALS640B-1NE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74ALS640B-1N	Samples
SN74ALS640B-1NSR	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS640B-1	Samples
SN74ALS640BDW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS640B	Samples
SN74ALS640BDWE4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS640B	Samples
SN74ALS640BDWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS640B	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74ALS640BDWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS640B	Samples
SN74ALS640BDWRE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS640B	Samples
SN74ALS640BN	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74ALS640BN	Samples
SN74ALS640BNSR	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS640B	Samples
SN74ALS640BNSRG4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS640B	Samples
SN74AS640N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74AS640N	Samples
SN74AS640NSR	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	74AS640	Samples
SNJ54ALS640BFK	OBsolete	LCCC	FK	20		TBD	Call TI	Call TI	-55 to 125		
SNJ54ALS640BJ	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8872701RA SNJ54ALS640BJ	Samples
SNJ54ALS640BW	ACTIVE	CFP	W	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8872701SA SNJ54ALS640BW	Samples
SNJ54AS640FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-89553012A SNJ54AS640FK	Samples
SNJ54AS640J	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8955301RA SNJ54AS640J	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF SN54ALS640B, SN54AS640, SN74ALS640B, SN74AS640 :

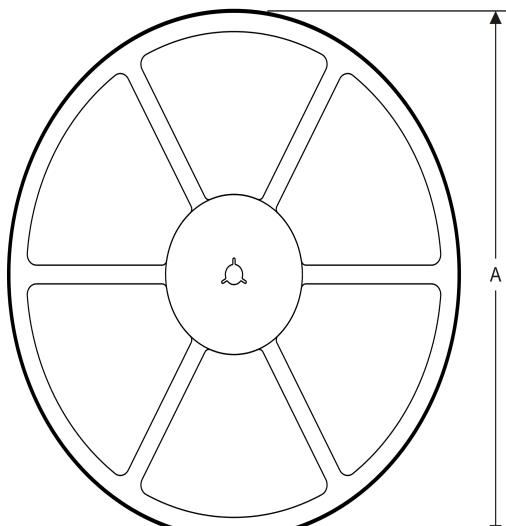
- Catalog: [SN74ALS640B](#), [SN74AS640](#)
- Military: [SN54ALS640B](#), [SN54AS640](#)

NOTE: Qualified Version Definitions:

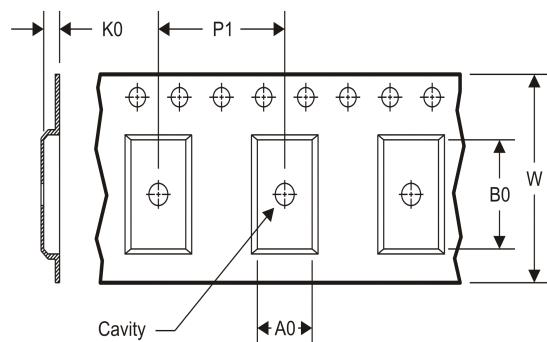
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

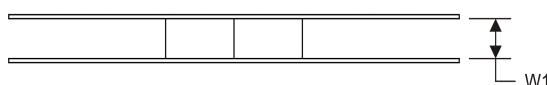
REEL DIMENSIONS



TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ALS640B-1DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1
SN74ALS640B-1NSR	SO	NS	20	2000	330.0	24.4	8.2	13.0	2.5	12.0	24.0	Q1
SN74ALS640BDWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1
SN74ALS640BNSR	SO	NS	20	2000	330.0	24.4	8.2	13.0	2.5	12.0	24.0	Q1
SN74AS640NSR	SO	NS	20	2000	330.0	24.4	8.2	13.0	2.5	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS

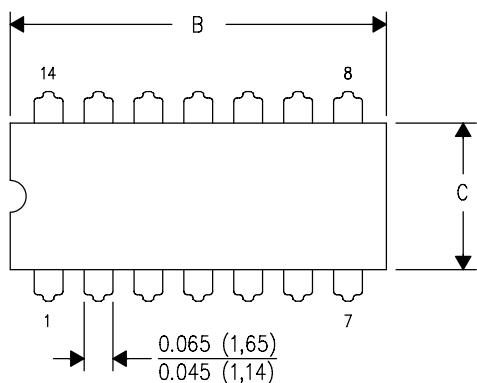

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ALS640B-1DWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN74ALS640B-1NSR	SO	NS	20	2000	367.0	367.0	45.0
SN74ALS640BDWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN74ALS640BNSR	SO	NS	20	2000	367.0	367.0	45.0
SN74AS640NSR	SO	NS	20	2000	367.0	367.0	45.0

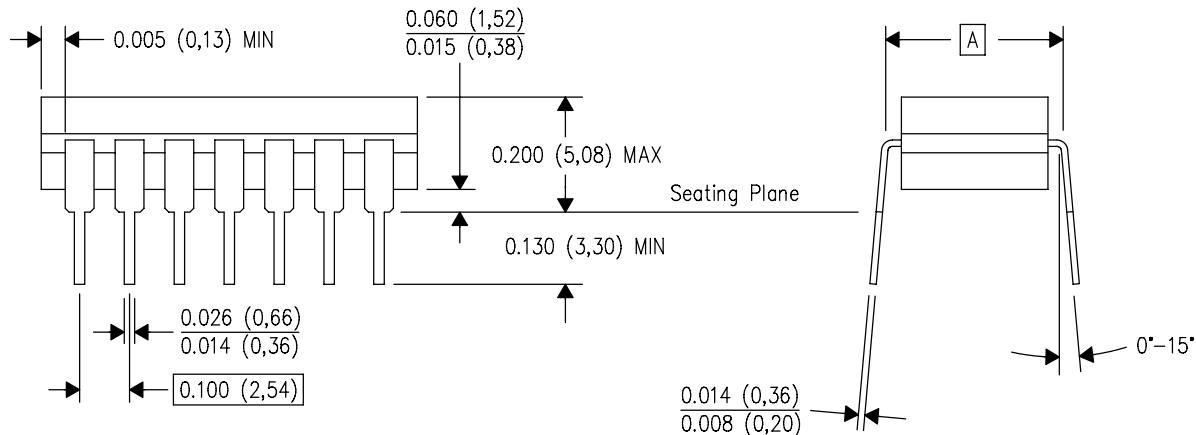
J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

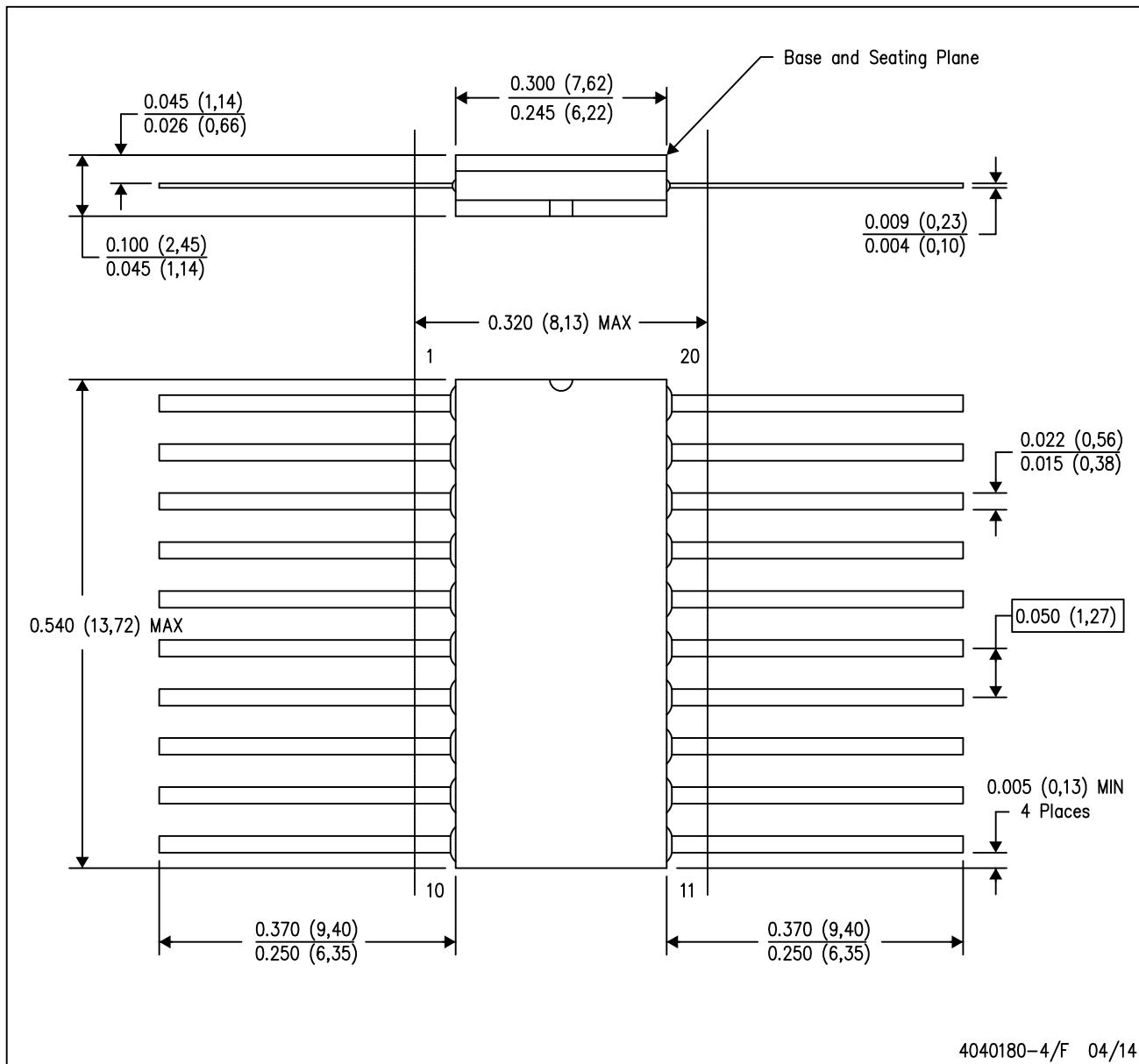


4040083/F 03/03

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F20)

CERAMIC DUAL FLATPACK



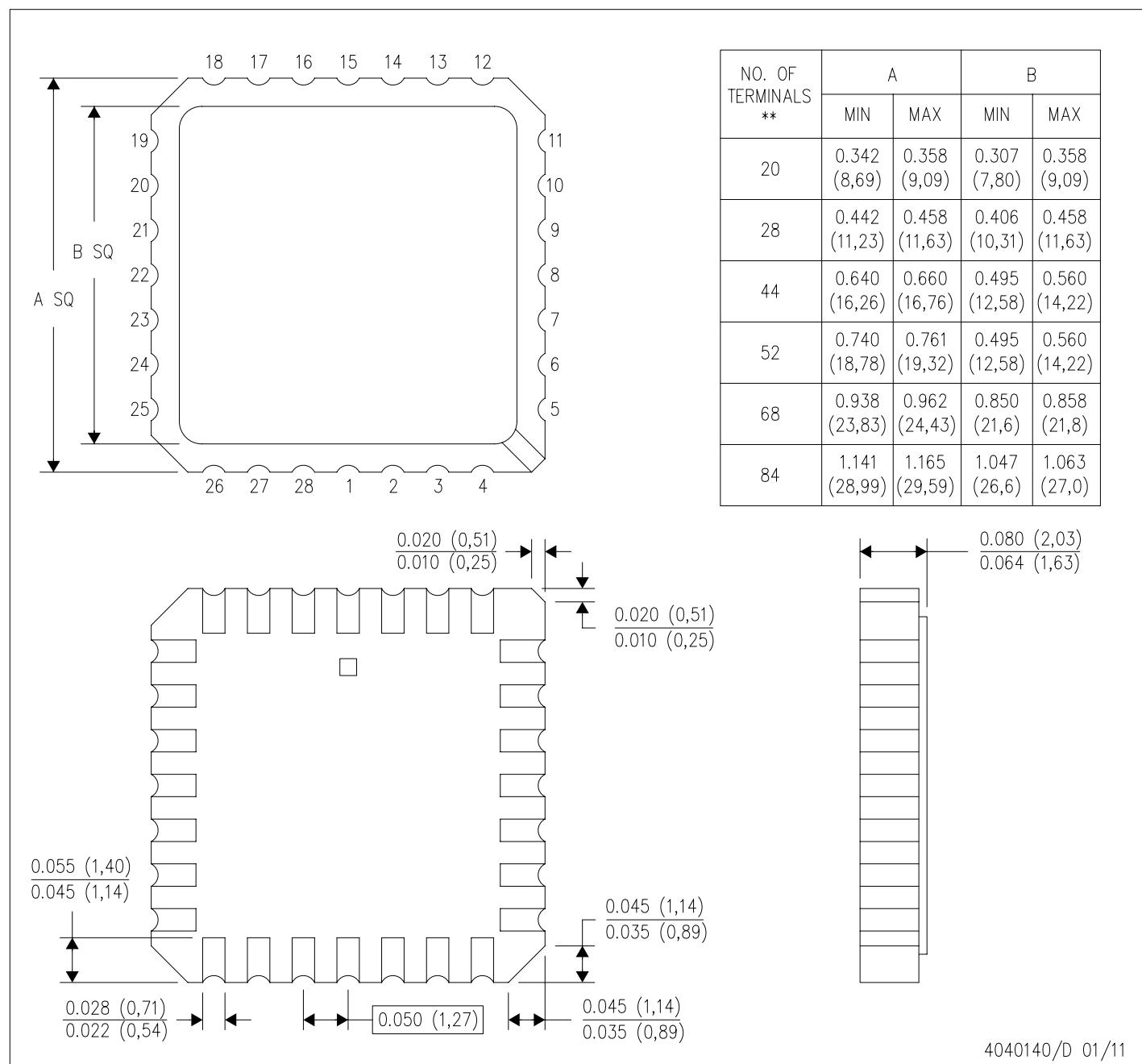
NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only.
- E. Falls within Mil-Std 1835 GDFP2-F20

FK (S-CQCC-N**)

28 TERMINAL SHOWN

LEADLESS CERAMIC CHIP CARRIER



NOTES:

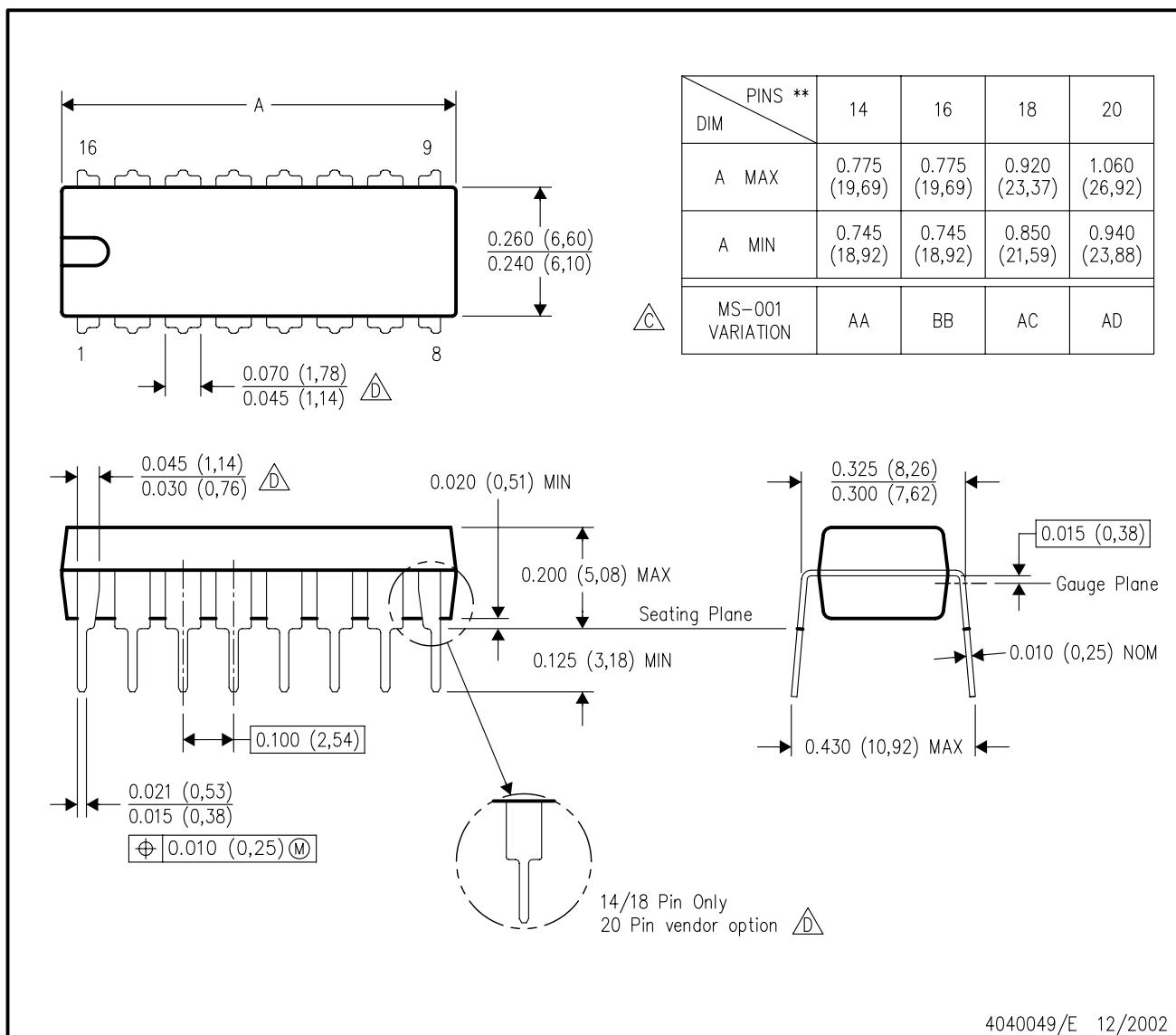
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a metal lid.
- D. Falls within JEDEC MS-004

4040140/D 01/11

N (R-PDIP-T**)

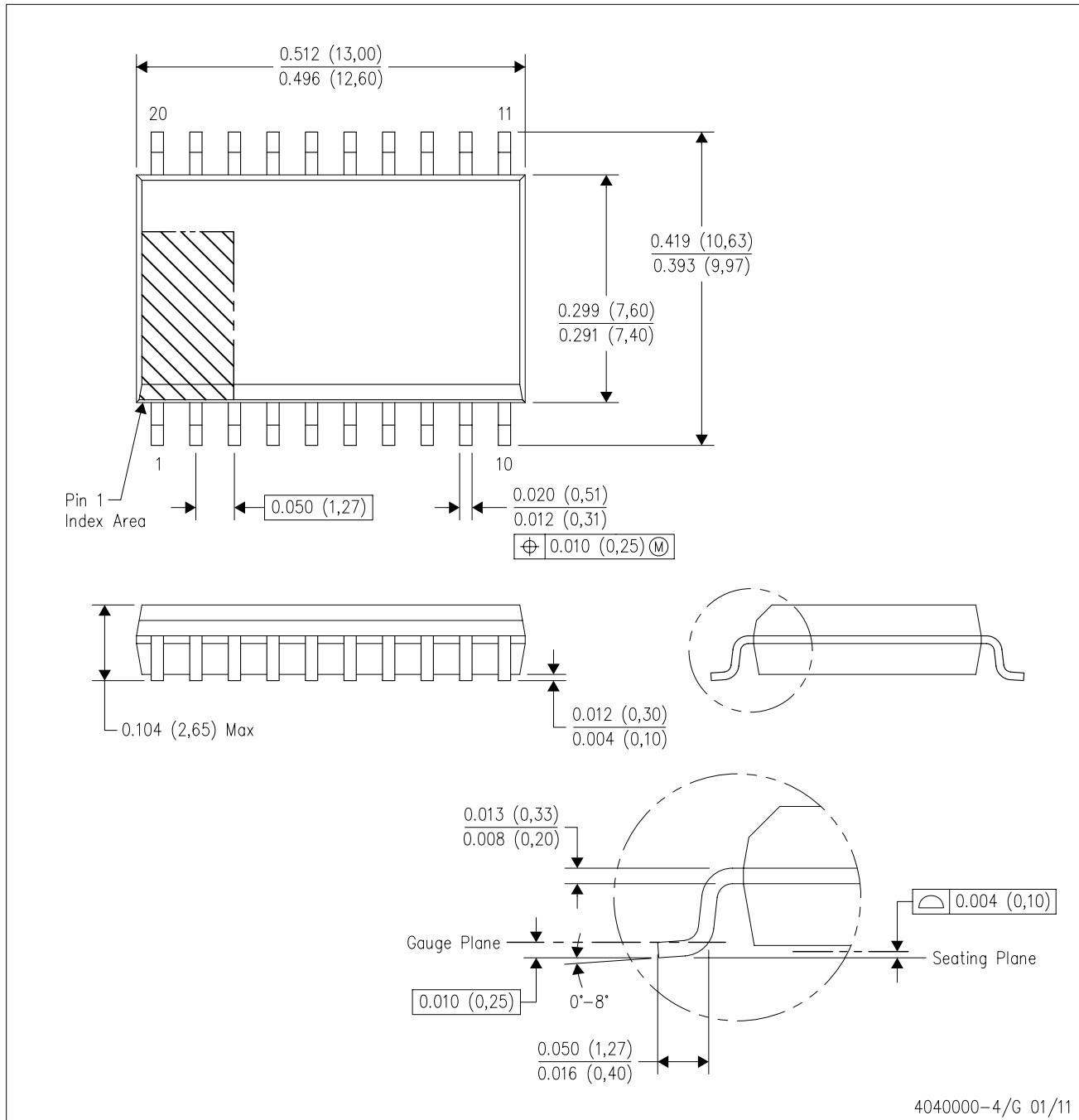
16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



DW (R-PDSO-G20)

PLASTIC SMALL OUTLINE

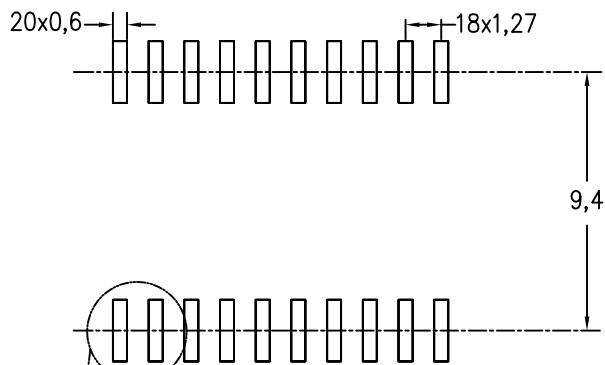
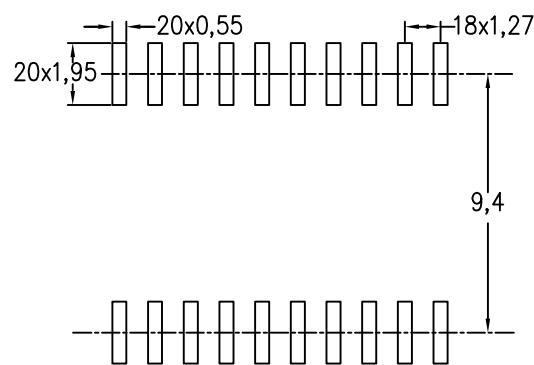


NOTES:

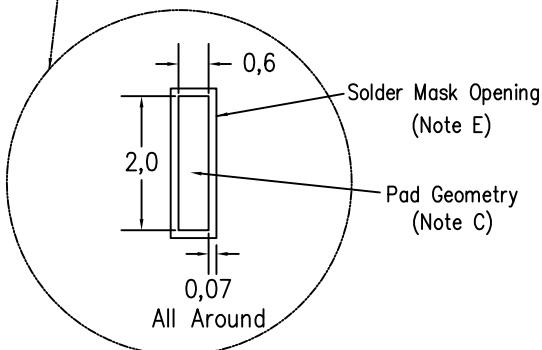
- All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
- This drawing is subject to change without notice.
- Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0.15).
- Falls within JEDEC MS-013 variation AC.

DW (R-PDSO-G20)

PLASTIC SMALL OUTLINE

Example Board Layout
(Note C)Stencil Openings
(Note D)

Non Solder Mask Define Pad



4209202-4/F 08/13

NOTES:

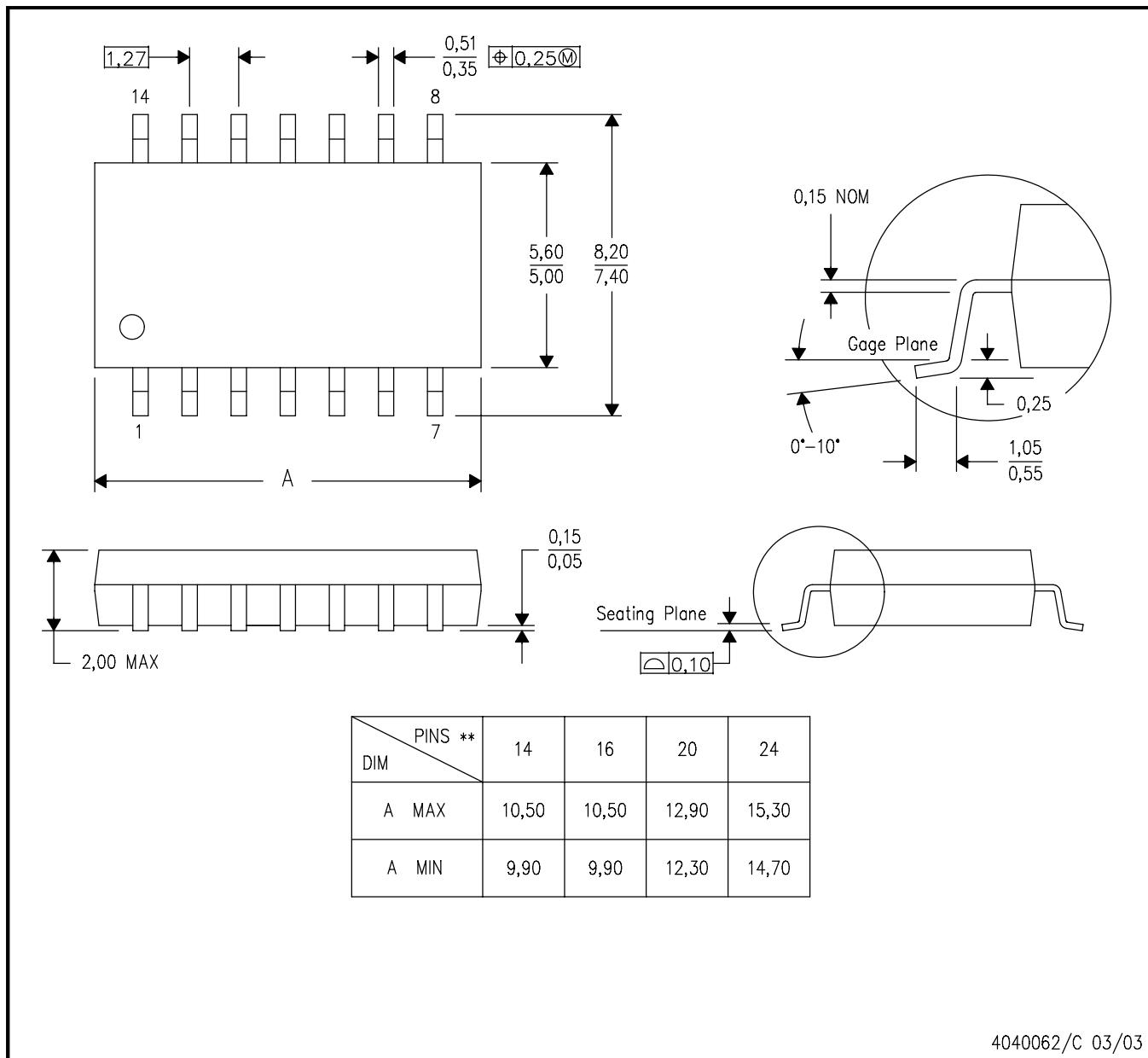
- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Refer to IPC7351 for alternate board design.
- Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
- Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MECHANICAL DATA

NS (R-PDSO-G)**

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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