

1-Mbit (64K x 16) Static RAM

Features

- **Temperature Ranges**
 - Industrial: -40°C to 85°C
 - Automotive: -40°C to 125°C
- **Very high speed: 45 ns**
- **Wide voltage range: 2.2V to 3.6V**
- **Pin compatible with CY62126BV**
- **Ultra-low active power**
 - Typical active current: 0.85 mA @ $f = 1\text{ MHz}$
 - Typical active current: 5 mA @ $f = f_{\text{MAX}}$
- **Ultra-low standby power**
- **Easy memory expansion with $\overline{\text{CE}}$ and $\overline{\text{OE}}$ features**
- **Automatic power-down when deselected**
- **Packages offered in a 48-ball FBGA, 56-lead QFN and a 44-lead TSOP Type II**
- **Also available in Lead-free packages**

Functional Description^[1]

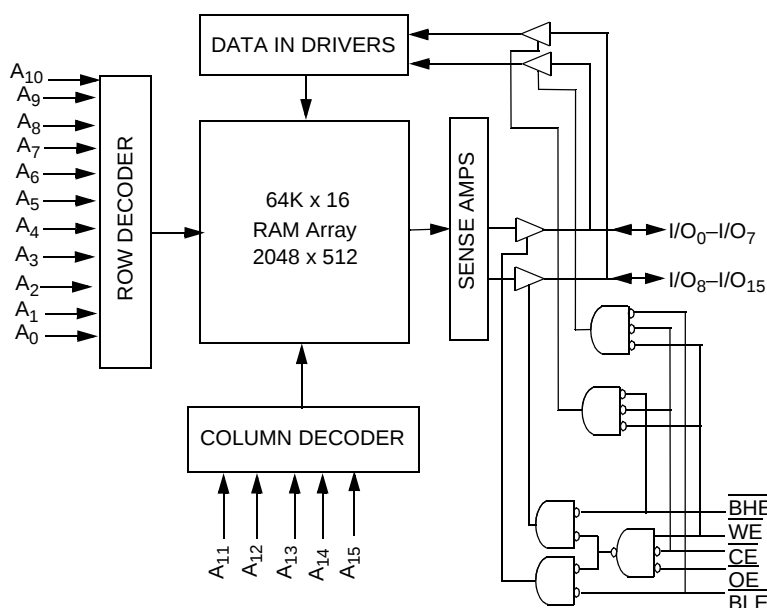
The CY62126DV30 is a high-performance CMOS static RAM organized as 64K words by 16 bits. This device features advanced circuit design to provide ultra-low active current.

This is ideal for providing More Battery Life™ (MoBL[®]) in portable applications such as cellular telephones. The device also has an automatic power-down feature that significantly reduces power consumption by 90% when addresses are not toggling. The device can be put into standby mode reducing power consumption by more than 99% when deselected ($\overline{\text{CE}}$ HIGH). The input/output pins (I/O_0 through I/O_{15}) are placed in a high-impedance state when: deselected ($\overline{\text{CE}}$ HIGH), outputs are disabled ($\overline{\text{OE}}$ HIGH), both Byte High Enable and Byte Low Enable are disabled ($\overline{\text{BHE}}$, $\overline{\text{BLE}}$ HIGH) or during a write operation ($\overline{\text{CE}}$ LOW and $\overline{\text{WE}}$ LOW).

Writing to the device is accomplished by taking Chip Enable ($\overline{\text{CE}}$) and Write Enable ($\overline{\text{WE}}$) inputs LOW. If Byte Low Enable ($\overline{\text{BLE}}$) is LOW, then data from I/O pins (I/O_0 through I/O_7), is written into the location specified on the address pins (A_0 through A_{15}). If Byte High Enable ($\overline{\text{BHE}}$) is LOW, then data from I/O pins (I/O_8 through I/O_{15}) is written into the location specified on the address pins (A_0 through A_{15}).

Reading from the device is accomplished by taking Chip Enable ($\overline{\text{CE}}$) and Output Enable ($\overline{\text{OE}}$) LOW while forcing the Write Enable ($\overline{\text{WE}}$) HIGH. If Byte Low Enable ($\overline{\text{BLE}}$) is LOW, then data from the memory location specified by the address pins will appear on I/O_0 to I/O_7 . If Byte High Enable ($\overline{\text{BHE}}$) is LOW, then data from memory will appear on I/O_8 to I/O_{15} . See the truth table at the back of this data sheet for a complete description of read and write modes.

Logic Block Diagram

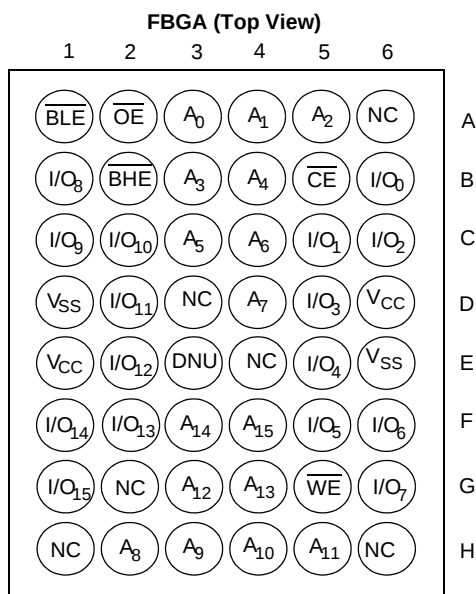


Note:

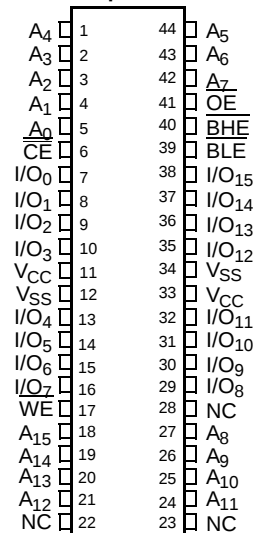
1. For best-practice recommendations, please refer to the Cypress application note "System Design Guidelines" on <http://www.cypress.com>.

Product Portfolio

Product	Range	V _{CC} Range (V)			Speed (ns)	Power Dissipation					
						Operating, I _{CC} (mA)				Standby, I _{SB2} (μA)	
						f = 1 MHz		f = f _{MAX}			
		Min.	Typ.	Max.		Typ. ^[2]	Max.	Typ. ^[2]	Max.	Typ. ^[2]	Max.
CY62126DV30L	Industrial	2.2	3.0	3.6	45	0.85	1.5	6.5	13	1.5	5
CY62126DV30LL	Industrial				45	0.85	1.5	6.5	13	1.5	4
CY62126DV30L	Industrial	2.2	3.0	3.6	55	0.85	1.5	5	10	1.5	5
CY62126DV30L	Automotive				55	0.85	1.5	5	10	1.5	15
CY62126DV30LL	Industrial				55	0.85	1.5	5	10	1.5	4
CY62126DV30L	Industrial	2.2	3.0	3.6	70	0.85	1.5	5	10	1.5	5
CY62126DV30LL	Industrial				70	0.85	1.5	5	10	1.5	4

Pin Configurations^[3, 4]


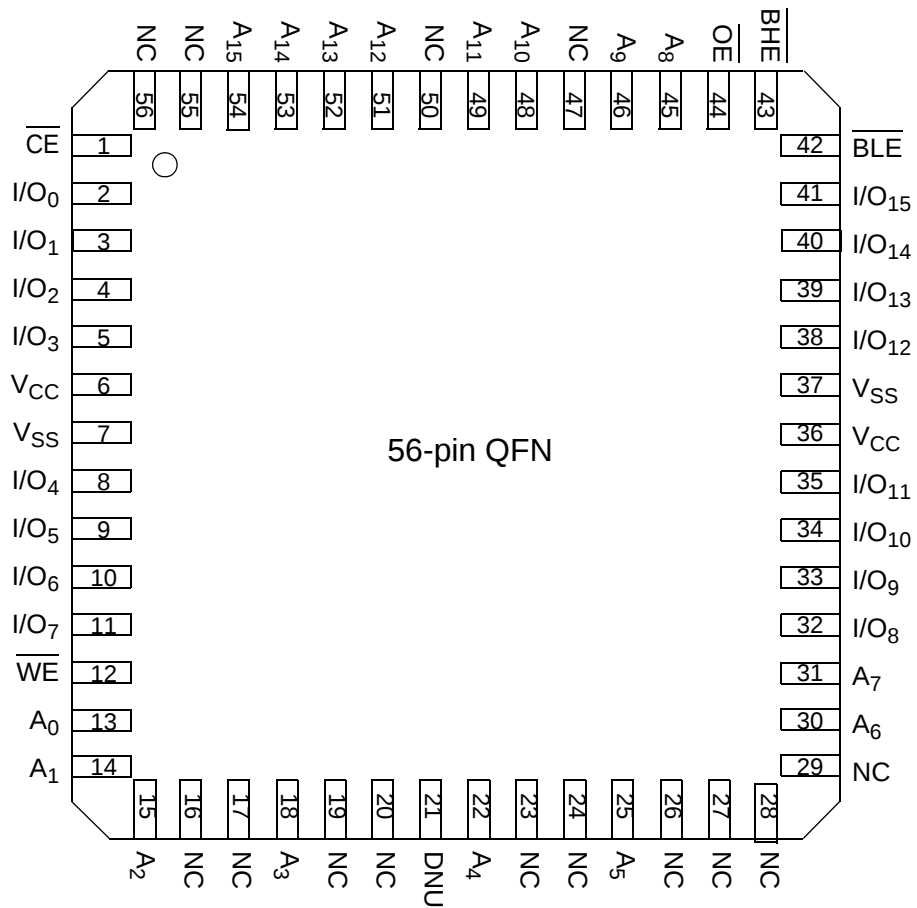
**TSOP II (Forward)
Top View**


Notes:

2. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = V_{CC(typ)}, T_A = 25°C.

3. NC pins are not connected to the die.

4. E3 (DNU) can be left as NC or V_{SS} to ensure proper operation. (Expansion Pins on FBGA Package: E4 - 2M, D3 - 4M, H1 - 8M, G2 - 16M, H6 - 32M).

Pin Configurations (continued)


**Maximum Ratings**

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature -65°C to +150°C

Ambient Temperature with
Power Applied -55°C to +125°C

Supply Voltage to Ground
Potential -0.3 to 3.9V

DC Voltage Applied to Outputs
in High-Z State^[6] -0.3V to $V_{CC} + 0.3V$

DC Input Voltage^[6] -0.3V to $V_{CC} + 0.3V$

Output Current into Outputs (LOW) 20 mA

Static Discharge Voltage > 2001V
(per MIL-STD-883, Method 3015)

Latch-up Current > 200 mA

Operating Range

Range	Ambient Temperature (T_A)	V_{CC} ^[7]
Industrial	-40°C to +85°C	2.2V to 3.6V
Automotive	-40°C to +125°C	2.2V to 3.6V

DC Electrical Characteristics (Over the Operating Range)

Parameter	Description	Test Conditions		CY62126DV30-45			CY62126DV30-55			CY62126DV30-70			Unit
				Min.	Typ. ^[5]	Max.	Min.	Typ. ^[5]	Max.	Min.	Typ. ^[5]	Max.	
V_{OH}	Output HIGH Voltage	$2.2 \leq V_{CC} \leq 2.7$	$I_{OH} = -0.1 \text{ mA}$	2.0			2.0			2.0			V
		$2.7 \leq V_{CC} \leq 3.6$	$I_{OH} = -1.0 \text{ mA}$	2.4			2.4			2.4			
V_{OL}	Output LOW Voltage	$2.2 \leq V_{CC} \leq 2.7$	$I_{OL} = 0.1 \text{ mA}$			0.4			0.4			0.4	V
		$2.7 \leq V_{CC} \leq 3.6$	$I_{OL} = 2.1 \text{ mA}$			0.4			0.4			0.4	
V_{IH}	Input HIGH Voltage	$2.2 \leq V_{CC} \leq 2.7$		1.8		$V_{CC} + 0.3$	1.8		$V_{CC} + 0.3$	1.8		$V_{CC} + 0.3$	V
		$2.7 \leq V_{CC} \leq 3.6$		2.2		$V_{CC} + 0.3$	2.2		$V_{CC} + 0.3$	2.2		$V_{CC} + 0.3$	
V_{IL}	Input LOW Voltage	$2.2 \leq V_{CC} \leq 2.7$		-0.3		0.6	-0.3		0.6	-0.3		0.6	V
		$2.7 \leq V_{CC} \leq 3.6$		-0.3		0.8	-0.3		0.8	-0.3		0.8	
I_{IX}	Input Leakage Current	$GND \leq V_I \leq V_{CC}$	Ind'l	-1		+1	-1		+1	-1		+1	μA
			Auto				-4		+4				μA
I_{OZ}	Output Leakage Current	$GND \leq V_O \leq V_{CC}$, Output Disabled	Ind'l	-1		+1	-1		+1	-1		+1	μA
			Auto				-4		+4				μA
I_{CC}	V_{CC} Operating Supply Current	$f = f_{MAX} = 1/t_{RC}$	$V_{CC} = 3.6V$, $I_{OUT} = 0 \text{ mA}$, CMOS level		6.5	13		5	10		5	10	mA
		$f = 1 \text{ MHz}$			0.85	1.5		0.85	1.5		0.85	1.5	
I_{SB1}	Automatic CE Power-down Current—CMOS Inputs	$\overline{CE} \geq V_{CC} - 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$, $V_{IN} \leq 0.2V$, $f = f_{MAX}$ (Address and Data Only), $f = 0$ (OE, WE, BHE and BLE)	L	Ind'l	1.5	5		1.5	5		1.5	5	μA
				Auto				1.5	15				
			LL		1.5	4		1.5	4		1.5	4	
I_{SB2}	Automatic CE Power-down Current—CMOS Inputs	$\overline{CE} \geq V_{CC} - 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$, $f = 0$, $V_{CC} = 3.6V$	L	Ind'l	1.5	5		1.5	5		1.5	5	μA
				Auto				1.5	15				
			LL		1.5	4		1.5	4		1.5	4	

Notes:

5. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$, $T_A = 25^\circ\text{C}$.

6. $V_{IL(min.)} = -2.0V$ for pulse durations less than 20 ns., $V_{IH(max.)} = V_{CC} + 0.75V$ for pulse durations less than 20 ns.

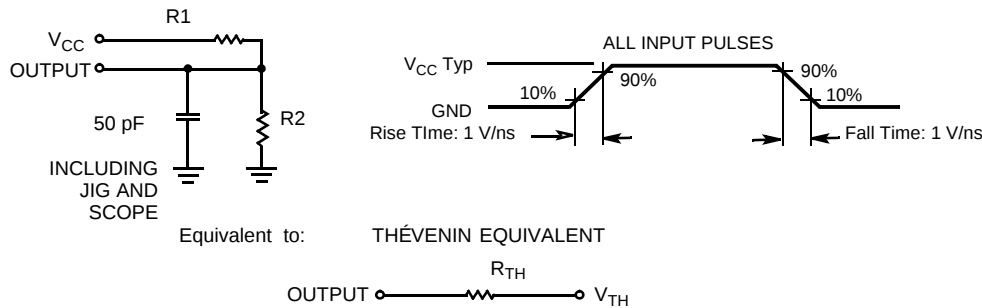
7. Full device operation requires linear ramp of V_{CC} from 0V to $V_{CC(min)}$ & V_{CC} must be stable at $V_{CC(min)}$ for 500 μs .

Capacitance^[8]

Parameter	Description	Test Conditions	Max.	Unit
C _{IN}	Input Capacitance	T _A = 25°C, f = 1 MHz V _{CC} = V _{CC(typ)}	8	pF
C _{OUT}	Output Capacitance		8	pF

Thermal Resistance

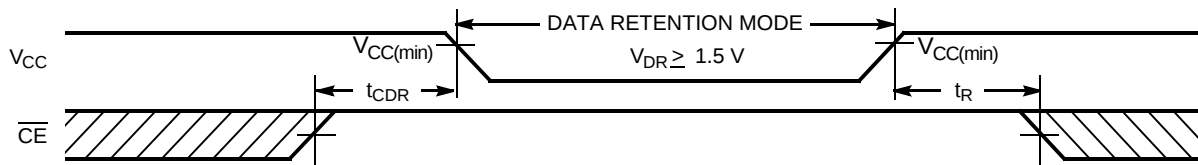
Parameter	Description	Test Conditions	QFN	TSOP	FBGA	Unit
θ _{JA}	Thermal Resistance (Junction to Ambient) ^[8]	Still Air, soldered on a 3 x 4.5 inch, two-layer printed circuit board	22.08	55	76	°C/W
θ _{JC}	Thermal Resistance (Junction to Case) ^[8]		5.03	12	11	°C/W

AC Test Loads and Waveforms^[9]


Parameters	2.5V	3.0V	Unit
R1	16600	1103	Ohms
R2	15400	1554	Ohms
R _{TH}	8000	645	Ohms
V _{TH}	1.2	1.75	Volts

Data Retention Characteristics

Parameter	Description	Conditions	Min.	Typ ^[2]	Max.	Unit
V _{DR}	V _{CC} for Data Retention		1.5			V
I _{CCDR}	Data Retention Current	V _{CC} =1.5V, $\overline{CE} \geq V_{CC} - 0.2V$, V _{IN} ≥ V _{CC} - 0.2V or V _{IN} ≤ 0.2V	L	Ind'l	4	μA
			L	Auto	10	
			LL	Ind'l	3	
t _{CDR} ^[8]	Chip Deselect to Data Retention Time		0			ns
t _R ^[10]	Operation Recovery Time		100			μs

Data Retention Waveform

Notes:

8. Tested initially and after any design or proces changes that may affect these parameters.
9. Test condition for the 45-ns part is a load capacitance of 30 pF.
10. Full device operation requires linear V_{CC} ramp from V_{DR} to V_{CC(min.)} >100 μs.

Switching Characteristics (Over the Operating Range)^[11]

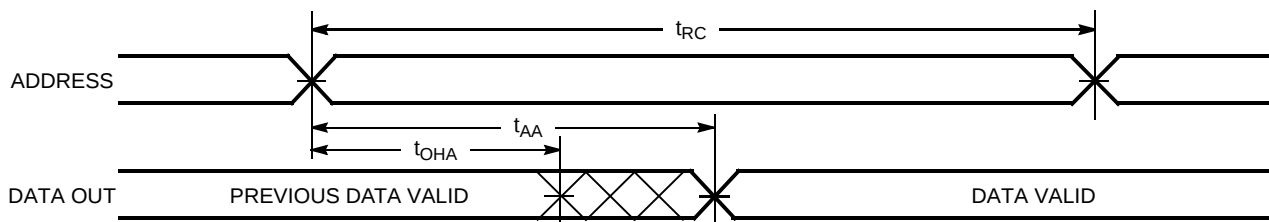
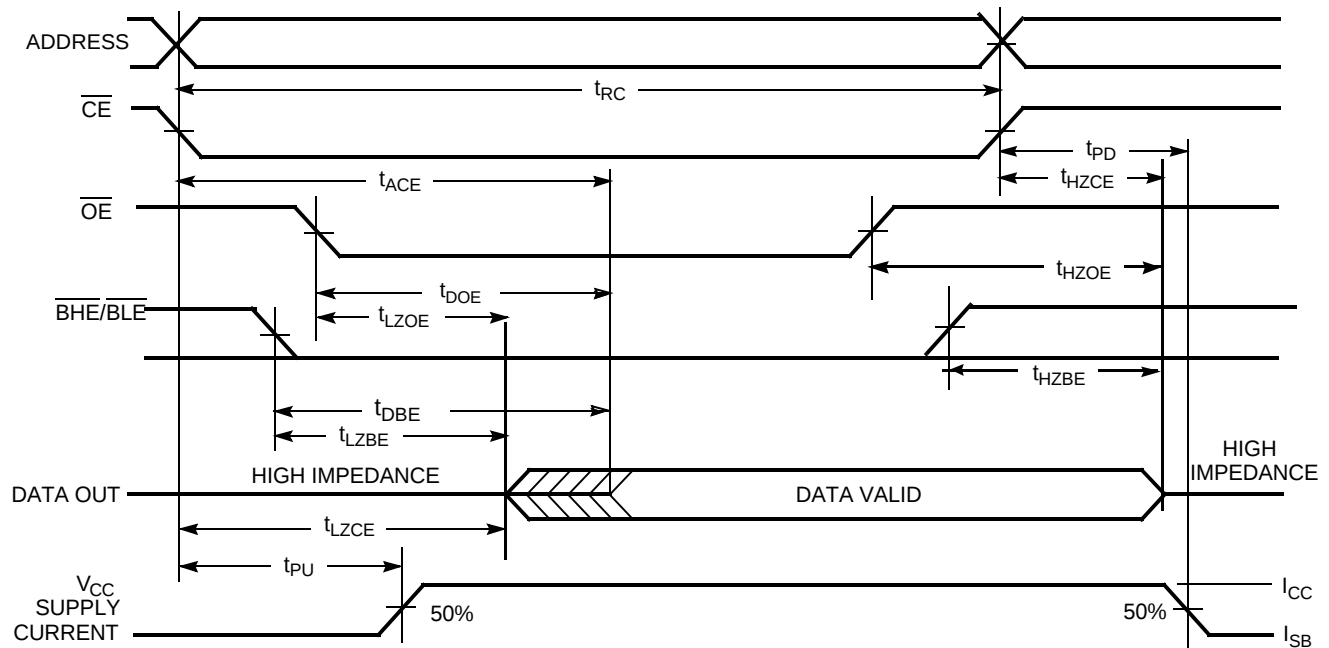
Parameter	Description	CY62126DV30-45 ^[9]		CY62126DV30-55		CY62126DV30-70		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle								
t _{RC}	Read Cycle Time	45		55		70		ns
t _{AA}	Address to Data Valid		45		55		70	ns
t _{OHA}	Data Hold from Address Change	10		10		10		ns
t _{ACE}	$\overline{\text{CE}}$ LOW to Data Valid		45		55		70	ns
t _{DOE}	$\overline{\text{OE}}$ LOW to Data Valid		25		25		35	ns
t _{LZOE}	$\overline{\text{OE}}$ LOW to Low Z ^[12]	5		5		5		ns
t _{HZOE}	$\overline{\text{OE}}$ HIGH to High Z ^[12, 13]		15		20		25	ns
t _{LZCE}	$\overline{\text{CE}}$ LOW to Low Z ^[12]	10		10		10		ns
t _{HZCE}	$\overline{\text{CE}}$ HIGH to High Z ^[12, 13]		20		20		25	ns
t _{PU}	$\overline{\text{CE}}$ LOW to Power-up	0		0		0		ns
t _{PD}	$\overline{\text{CE}}$ HIGH to Power-down		45		55		70	ns
t _{DBE}	$\overline{\text{BLE/BHE}}$ LOW to Data Valid		25		25		35	ns
t _{LZBE}	$\overline{\text{BLE/BHE}}$ LOW to Low Z ^[12]	5		5		5		ns
t _{HZBE}	$\overline{\text{BLE/BHE}}$ HIGH to High-Z ^[12, 13]		15		20		25	ns
Write Cycle ^[14]								
t _{WC}	Write Cycle Time	45		55		70		ns
t _{SCE}	$\overline{\text{CE}}$ LOW to Write End	40		40		60		ns
t _{AW}	Address Set-up to Write End	40		40		60		ns
t _{HA}	Address Hold from Write End	0		0		0		ns
t _{SA}	Address Set-up to Write Start	0		0		0		ns
t _{PWE}	$\overline{\text{WE}}$ Pulse Width	35		40		50		ns
t _{BW}	$\overline{\text{BLE/BHE}}$ LOW to Write End	40		40		60		ns
t _{SD}	Data Set-up to Write End	25		25		30		ns
t _{HD}	Data Hold from Write End	0		0		0		ns
t _{HZWE}	$\overline{\text{WE}}$ LOW to High Z ^[12, 13]		15		20		25	ns
t _{LZWE}	$\overline{\text{WE}}$ HIGH to Low Z ^[12]	10		10		5		ns

Notes:

11. Test conditions assume signal transition time of 1V/ns or less, timing reference levels of $V_{CC(typ.)}/2$, input pulse levels of 0 to $V_{CC(typ.)}$, and output loading of the specified I_{OL} .
12. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , t_{HZBE} is less than t_{LZBE} , t_{HZOE} is less than t_{LZOE} .
13. t_{HZOE} , t_{HZCE} , t_{HZBE} , and t_{HZWE} transitions are measured when the outputs enter a high-impedance state.
14. The internal Write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE} = V_{IL}$, $\overline{BHE}$ and/or $\overline{BLE} = V_{IL}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input set-up and hold timing should be referenced to the edge of the signal that terminates the write.

Switching Waveforms

Read Cycle No. 1 (Address Transition Controlled)^[15, 16]

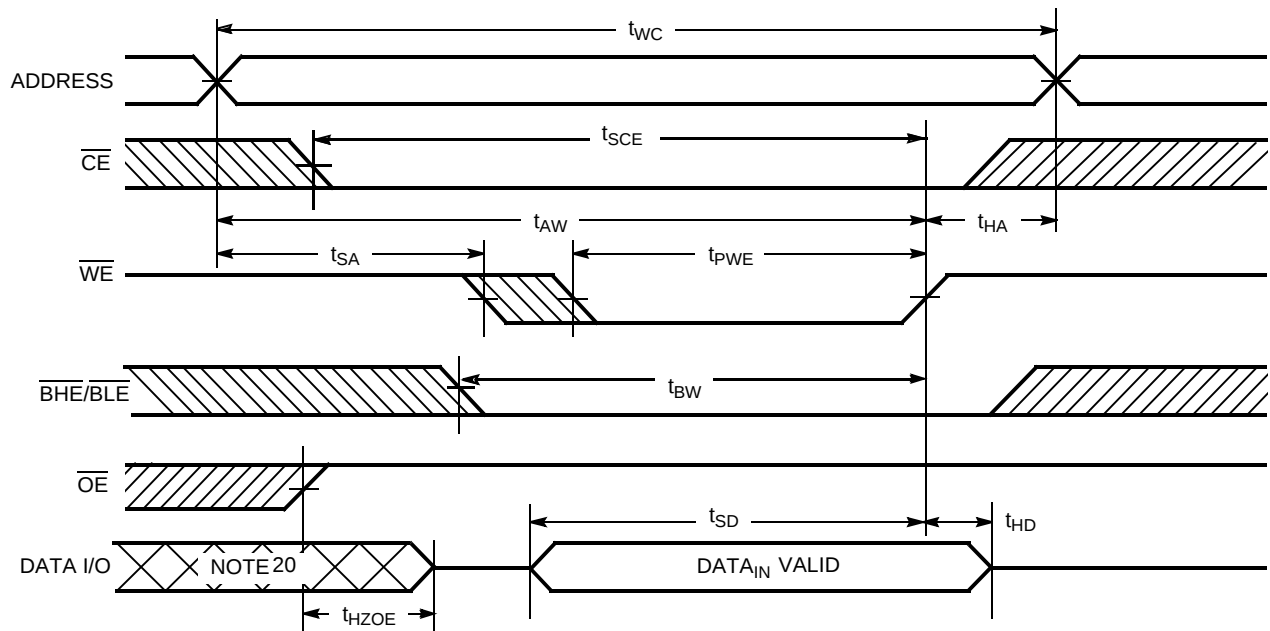
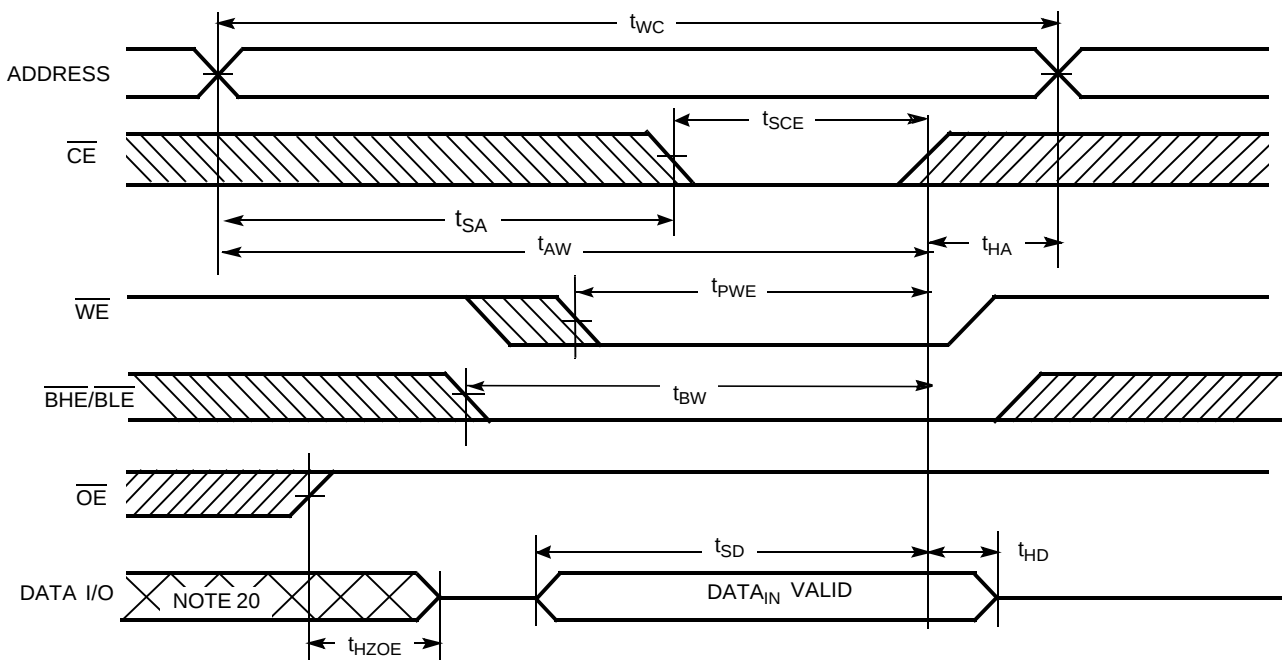
Read Cycle No. 2 ($\overline{\text{OE}}$ Controlled)^[16, 17]

Notes:

15. Device is continuously selected. $\overline{OE}, \overline{CE} = V_{IL}, \overline{BHE}, \overline{BLE} = V_{IL}$.

16. $\overline{WE}$ is HIGH for Read cycle.

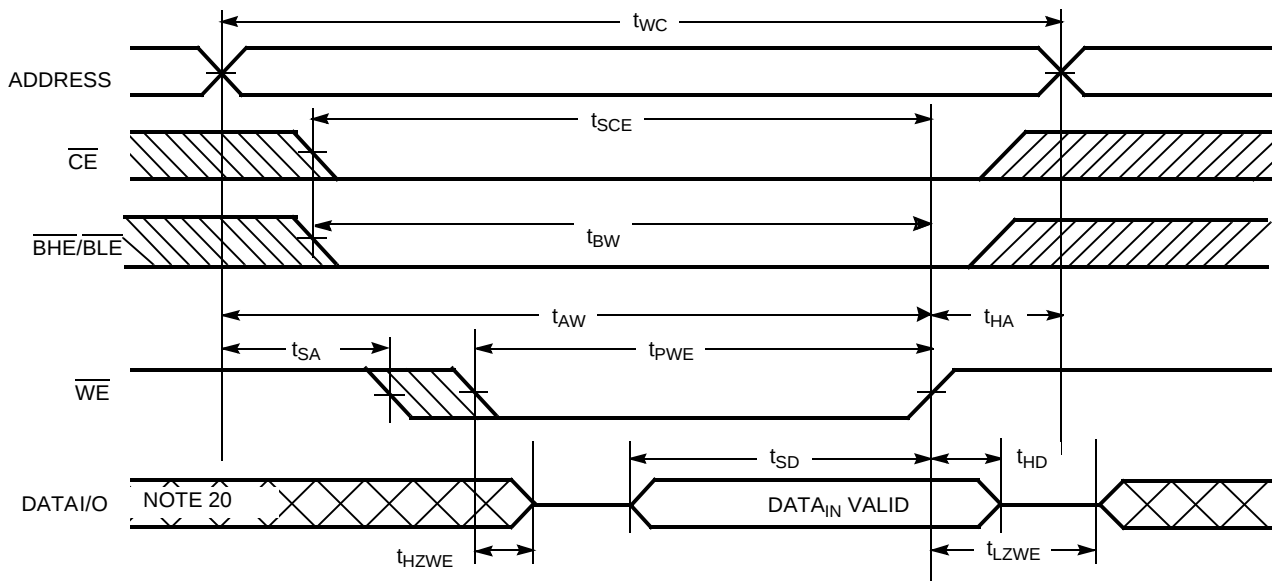
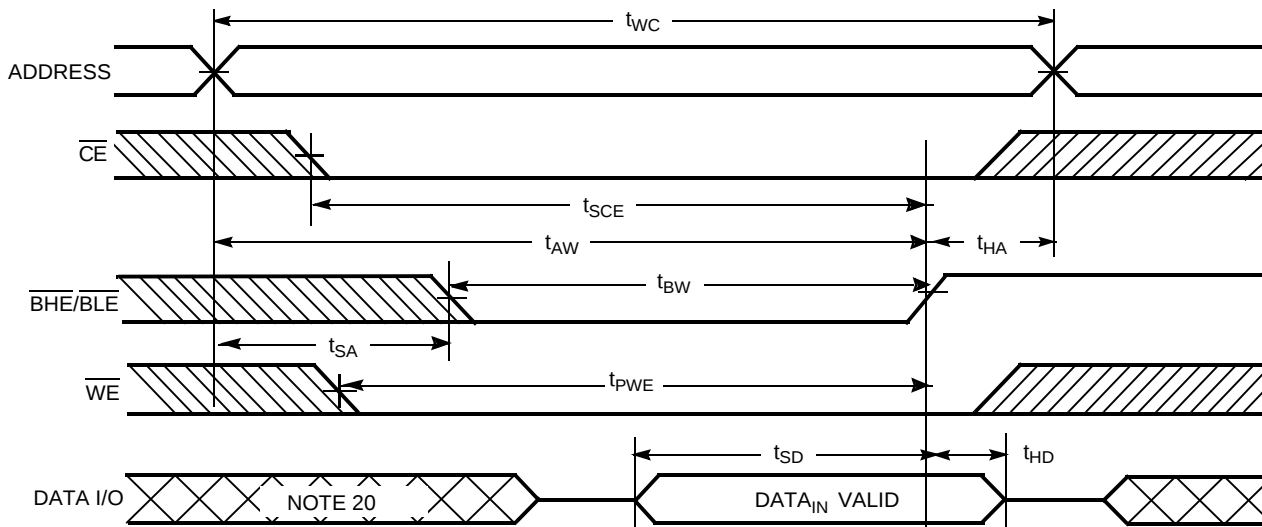
17. Address valid prior to or coincident with $\overline{\text{CE}}$, $\overline{\text{BHE}}$, $\overline{\text{BLE}}$ transition LOW.

Switching Waveforms(continued)
Write Cycle No. 1 ($\overline{WE}$ Controlled)^[13, 14, 17, 18, 19]

Write Cycle No. 2 ($\overline{CE}$ Controlled)^[13, 14, 17, 18, 19]

Notes:

18. Data I/O is high-impedance if $\overline{OE} = V_{IH}$.

19. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

20. During the DONT CARE period in the DATA I/O waveform, the I/Os are in output state and input signals should not be applied.

Switching Waveforms(continued)
Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW)^[18, 19]

Write Cycle No. 4 ($\overline{BHE}/\overline{BLE}$ -controlled, $\overline{OE}$ LOW)^[17, 18]


Truth Table

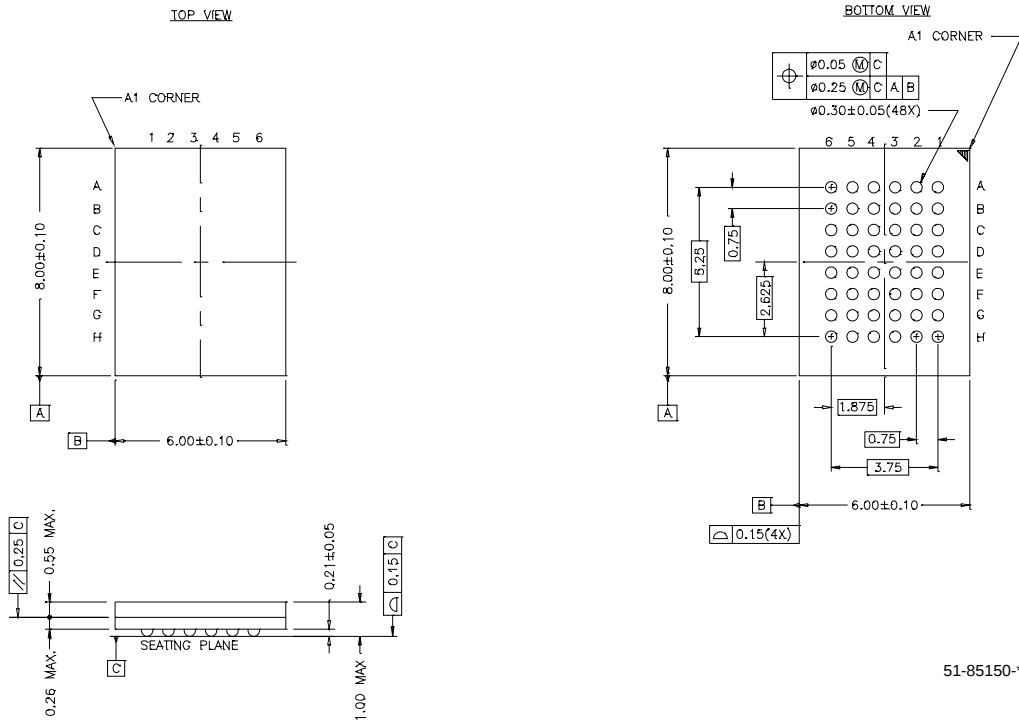
CE	WE	OE	BHE	BLE	Inputs/Outputs	Mode	Power
H	X	X	X	X	High Z	Deselect/Power-Down	Standby (I_{SB})
L	X	X	H	H	High Z	Output Disabled	Active (I_{CC})
L	H	L	L	L	Data Out (I/O_0 – I/O_{15})	Read	Active (I_{CC})
L	H	L	H	L	Data Out (I/O_0 – I/O_7); I/O_8 – I/O_{15} in High Z	Read	Active (I_{CC})
L	H	L	L	H	Data Out (I/O_8 – I/O_{15}); I/O_0 – I/O_7 in High Z	Read	Active (I_{CC})
L	H	H	L	L	High Z	Output Disabled	Active (I_{CC})
L	H	H	H	L	High Z	Output Disabled	Active (I_{CC})
L	H	H	L	H	High Z	Output Disabled	Active (I_{CC})
L	L	X	L	L	Data In (I/O_0 – I/O_{15})	Write	Active (I_{CC})
L	L	X	H	L	Data In (I/O_0 – I/O_7); I/O_8 – I/O_{15} in High Z	Write	Active (I_{CC})
L	L	X	L	H	Data In (I/O_8 – I/O_{15}); I/O_0 – I/O_7 in High Z	Write	Active (I_{CC})

Ordering Information

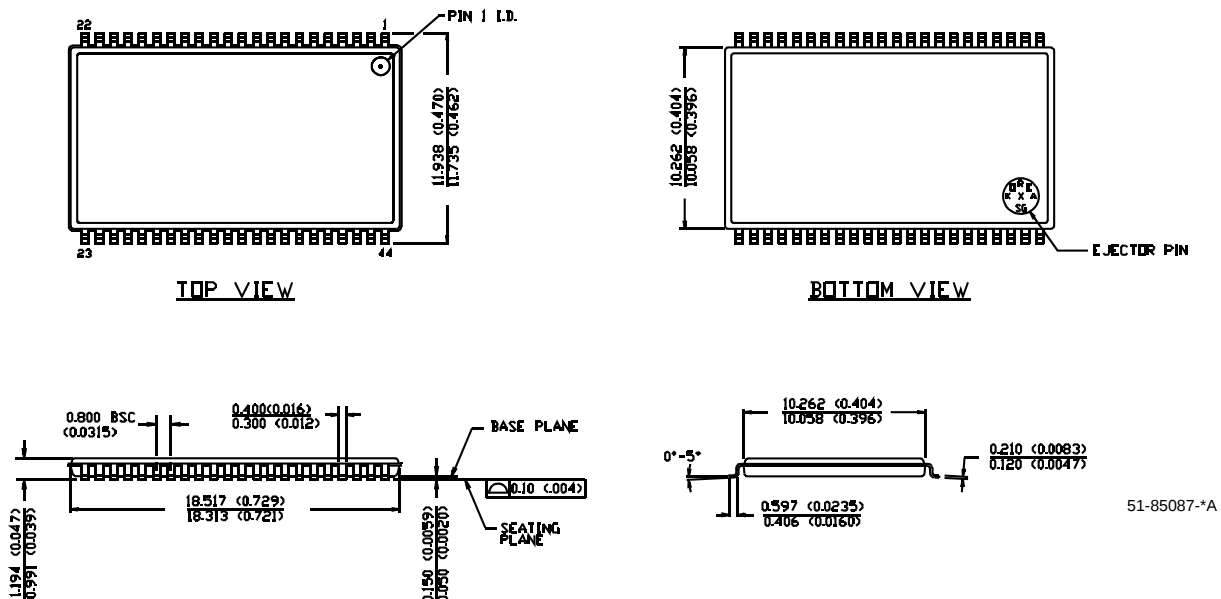
Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
45	CY62126DV30LL-45BVI	BV48A	48-ball Fine Pitch BGA (6 mm x 8 mm x 1 mm)	Industrial
	CY62126DV30LL-45BVXI	BV48A	48-ball Fine Pitch BGA (6 mm x 8 mm x 1 mm) (Pb-free)	
	CY62126DV30LL-45ZXI	Z44	44-Lead TSOP Type II (Pb-free)	
	CY62126DV30LL-45LFXI	LF56	56-pin QFN (Pb-free)	
55	CY62126DV30L-55BVI	BV48A	48-ball Fine Pitch BGA (6 mm x 8 mm x 1 mm)	Industrial
	CY62126DV30LL-55BVI	BV48A	48-ball Fine Pitch BGA (6 mm x 8 mm x 1 mm)	
	CY62126DV30LL-55BVXI	BV48A	48-ball Fine Pitch BGA (6 mm x 8 mm x 1 mm) (Pb-Free)	
	CY62126DV30L-55ZI	Z44	44-Lead TSOP Type II	
	CY62126DV30LL-55ZI	Z44	44-Lead TSOP Type II	
	CY62126DV30LL-55ZXI	Z44	44-Lead TSOP Type II (Pb-Free)	
	CY62126DV30L-55ZSE	Z44	44-Lead TSOP Type II	
	CY62126DV30L-55ZSXE	Z44	44-Lead TSOP Type II (Pb-Free)	Automotive
	CY62126DV30L-55BVXE	BV48A	48-ball Fine Pitch BGA (6 mm x 8 mm x 1 mm) (Pb-Free)	
	CY62126DV30LL-55LFXI	LF56	56-pin QFN (Pb-free)	Industrial
70	CY62126DV30L-70BVI	BV48A	48-ball Fine Pitch BGA (6 mm x 8 mm x 1 mm)	Industrial
	CY62126DV30LL-70BVI	BV48A	48-ball Fine Pitch BGA (6 mm x 8 mm x 1 mm)	
	CY62126DV30LL-70BVXI	BV48A	48-ball Fine Pitch BGA (6 mm x 8 mm x 1 mm) (Pb-Free)	
	CY62126DV30L-70ZI	Z44	44-Lead TSOP Type II	
	CY62126DV30LL-70ZI	Z44	44-Lead TSOP Type II	
	CY62126DV30LL-70ZXI	Z44	44-Lead TSOP Type II (Pb-Free)	
	CY62126DV30LL-70LFXI	LF56	56-pin QFN (Pb-free)	

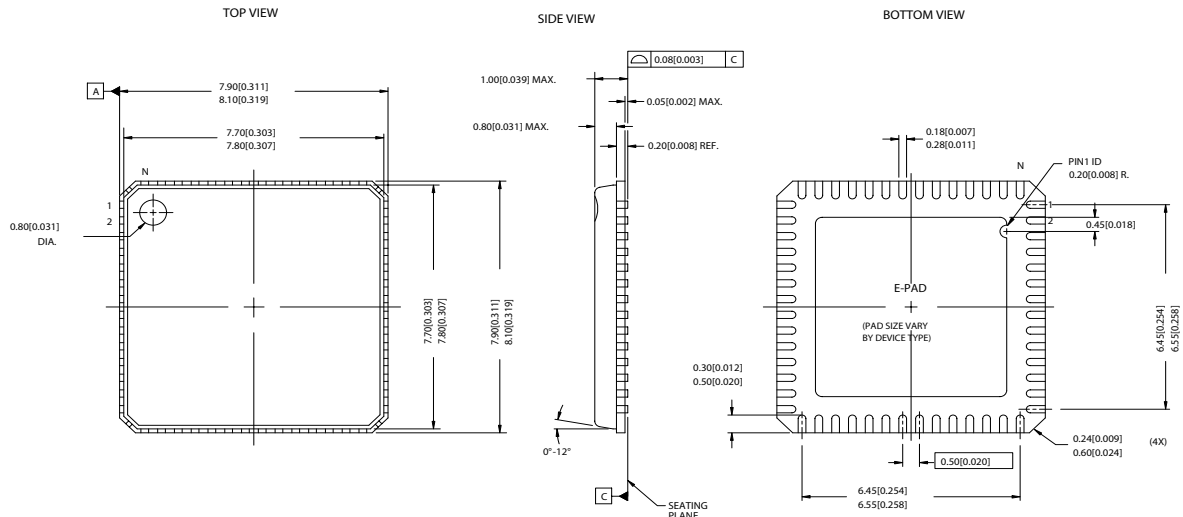
Package Diagrams

48-Lead VFBGA (6 x 8 x 1 mm) BV48A



44-pin TSOP II Z44



Package Diagrams (continued)
56-Lead QFN 8 x 8 MM LF56A


51-85144-*D

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Document History Page

Document Title: CY62126DV30 MoBL [®] 1- Mbit (64K x 16) Static RAM Document Number: 38-05230				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	117689	08/27/02	JUI	New Data Sheet
*A	127313	06/13/03	MPR	Changed From Advanced Status to Preliminary. Changed I _{SB2} to 5 μ A (L), 4 μ A (LL) Changed I _{CCDR} to 4 μ A (L), 3 μ A (LL) Changed C _{IN} from 6 pF to 8 pF
*B	128340	07/22/03	JUI	Changed from Preliminary to Final Add 70-ns speed, updated ordering information
*C	129002	08/29/03	CDY	Changed I _{CC} 1 MHz typ from 0.5 mA to 0.85 mA
*D	238050	See ECN	AJU	Fixed typo: Changed t _{DBE} from 70 ns to 35 ns
*E	316039	See ECN	PCI	Added 45-ns Speed Bin in AC, DC and Ordering Information tables Added Footnote #8 on page #4 Added Pb-Free package ordering information on page # 9 Changed 44-pin TSOP-II package name from Z44 to ZS44
*F	335861	See ECN	SYT	Added Temperature Ranges in the Features Section on Page # 1 Added Automotive Product Information for CY62126DV30-L for 55 ns Added I _{SB1} and I _{SB2} values for Automotive range of CY62126DV30-L for 55 ns Added Automotive Information for I _{CCDR} in the Data Retention Characteristics table Added Pb-Free packages in the ordering information Changed 44-pin TSOP-II package name from ZS44 to Z44
*G	357256	See ECN	PCI	Added Pin Configuration and Package Diagram for 56-Lead QFN Package Updated Thermal Characteristics and Ordering Information Table Added Automotive Specs for I _{IX} and I _{OZ} in the DC Electrical Characteristics table on Page# 4