TOSHIBA Field-Effect Transistor Silicon N-Channel MOS Type

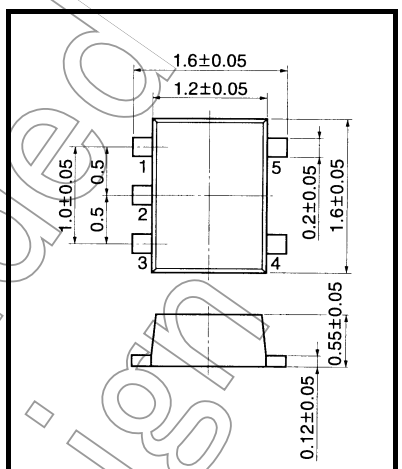
SSM5N03FE

High-Speed Switching Applications

Analog-Switch Applications

- Input impedance is high; driving current is extremely low.
- Can be directly driven by a CMOS device even at low voltage due to low gate threshold voltage.
- High-speed switching
- Housed in an ultra-small package suitable for high density mounting

Unit: mm



1: Gate 1 4. Drain 2
2. Source 5. Drain 1
3: Gate 2

ESV

JEDEC	—
JEITA	—
TOSHIBA	2-2P1B

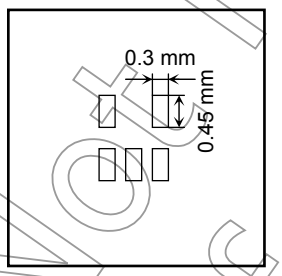
Weight: 0.003 g (typ.)

Absolute Maximum Ratings (Ta = 25°C) (Q1, Q2 Common)

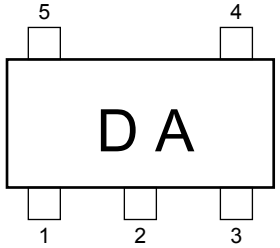
Characteristic	Symbol	Rating	Unit
Drain–source voltage	V_{DS}	20	V
Gate–source voltage	V_{GSS}	10	V
Drain current	I_D	100	mA
Drain power dissipation	P_D (Note 1)	150	mW
Channel temperature	T_{ch}	150	°C
Storage temperature	T_{stg}	−55 to 150	°C

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

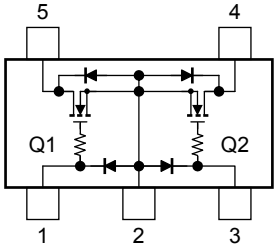
Note 1: Total rating, mounted on an FR4 board
(25.4 mm × 25.4 mm × 1.6 t, Cu Pad: 0.135 mm^2 × 5)



Marking



Equivalent Circuit (top view)

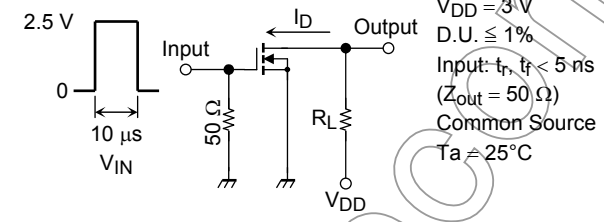


Electrical Characteristics (Ta = 25°C) (Q1, Q2 Common)

Characteristic		Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current		I_{GSS}	V_{GS} = 10 V, V_{DS} = 0 V	—	—	1	μA
Drain–source breakdown voltage		$V_{(BR)\ DSS}$	I_D = 100 μA, V_{GS} = 0 V	20	—	—	V
Drain cutoff current		I_{DSS}	V_{DS} = 20 V, V_{GS} = 0 V	—	—	1	μA
Gate threshold voltage		V_{th}	V_{DS} = 3 V, I_D = 0.1 mA	0.7	—	1.3	V
Forward transfer admittance		$\|Y_{fs}\|$	V_{DS} = 3 V, I_D = 10 mA	25	60	—	mS
Drain–source ON-resistance		$R_{DS\ (ON)}$	I_D = 10 mA, V_{GS} = 2.5 V	—	4	12	Ω
Input capacitance		C_{iss}	V_{DS} = 3 V, V_{GS} = 0 V, f = 1 MHz	—	11.0	—	pF
Reverse transfer capacitance		C_{rss}	V_{DS} = 3 V, V_{GS} = 0 V, f = 1 MHz	—	3.3	—	pF
Output capacitance		C_{oss}	V_{DS} = 3 V, V_{GS} = 0 V, f = 1 MHz	—	9.3	—	pF
Switching time	Turn-on time	t_{on}	V_{DD} = 3 V, I_D = 10 mA, V_{GS} = 0 to 2.5 V	—	0.16	—	μs
	Turn-off time	t_{off}	V_{DD} = 3 V, I_D = 10 mA, V_{GS} = 0 to 2.5 V	—	0.19	—	

Switching Time Test Circuit

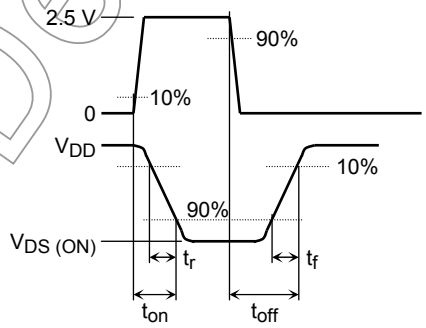
(a) Test circuit



V_{DD} = 3 V
D.U. ≦ 1%
Input: t_r, t_f < 5 ns
(Z_{out} = 50 Ω)
Common Source
Ta = 25°C

(b) V_{IN}
V_{GS}

(c) V_{OUT}
V_{DS}



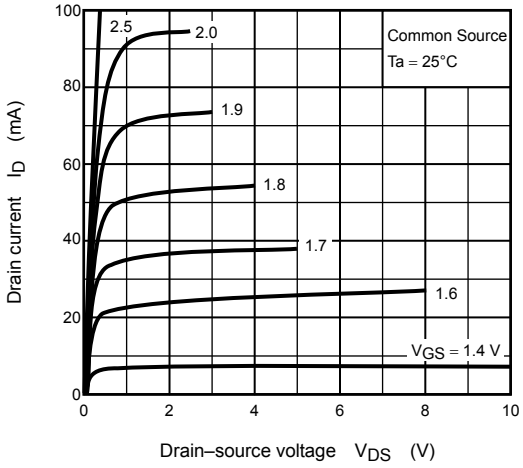
Precaution

V_{th} can be expressed as the voltage between gate and source when the low operating current value is I_D = 100 μA for this product. For normal switching operation, $V_{GS\ (on)}$ requires a higher voltage than V_{th}, and $V_{GS\ (off)}$ requires a lower voltage than V_{th}. (The relationship can be established as follows: $V_{GS\ (off)} < V_{th} < V_{GS\ (on)}$.)

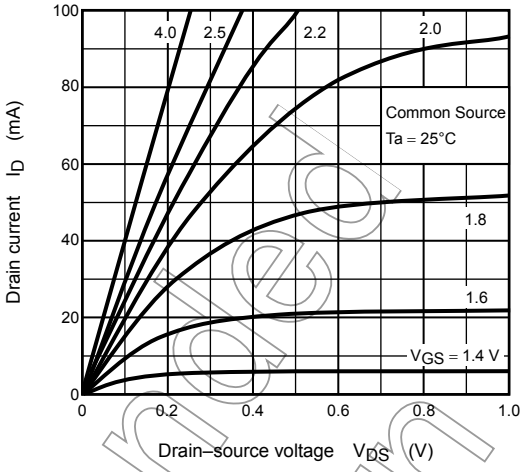
Take this into consideration when using the device.

(Q1, Q2 Common)

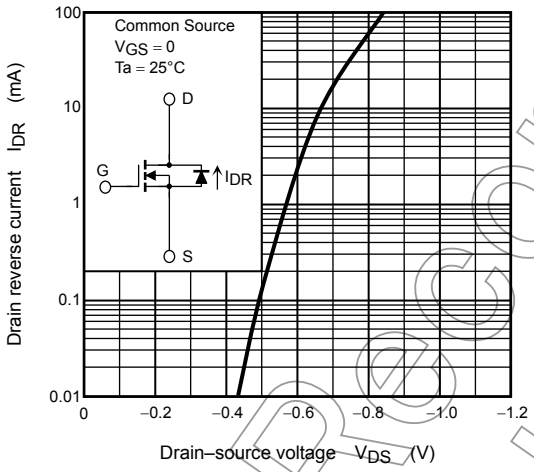
$I_D - V_{DS}$



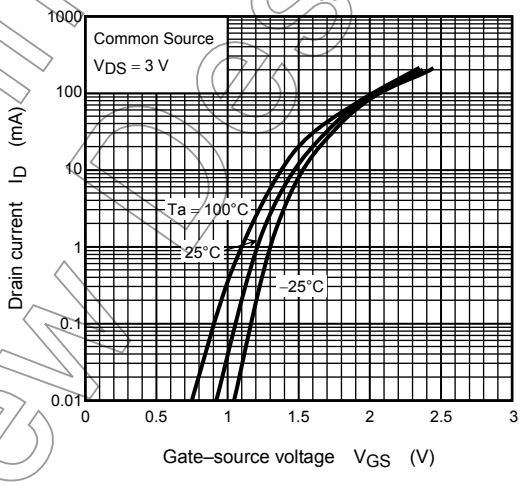
$I_D - V_{DS}$ (low-voltage region)



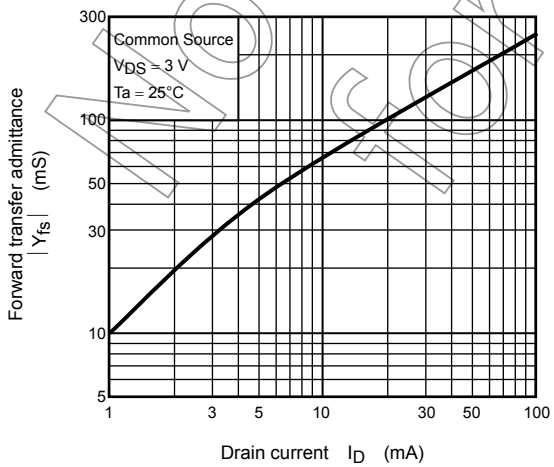
$I_{DR} - V_{DS}$



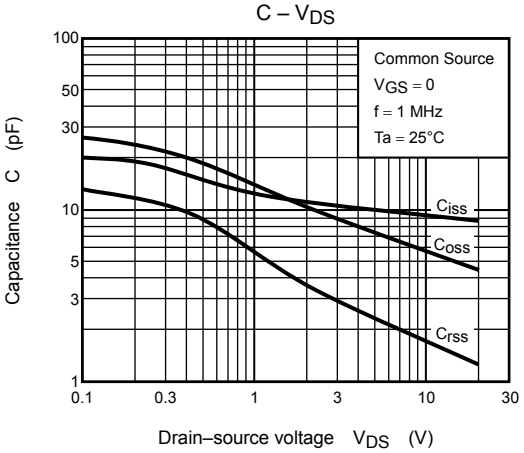
$I_D - V_{GS}$



$|Y_{fs}| - I_D$

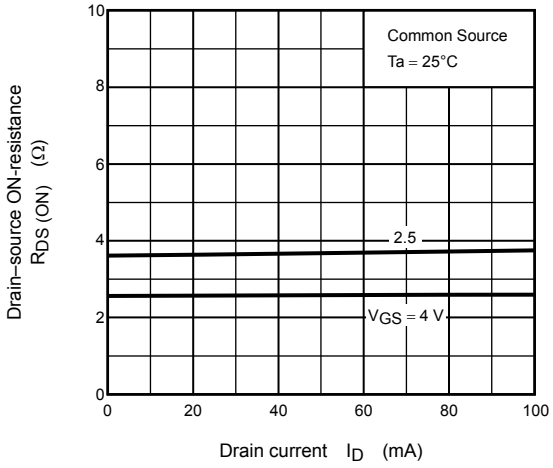


$C - V_{DS}$

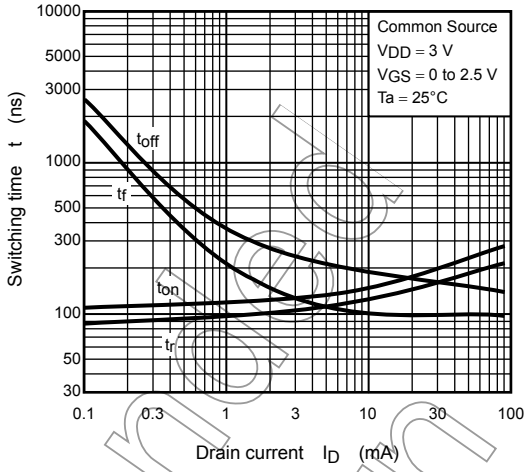


(Q1, Q2 Common)

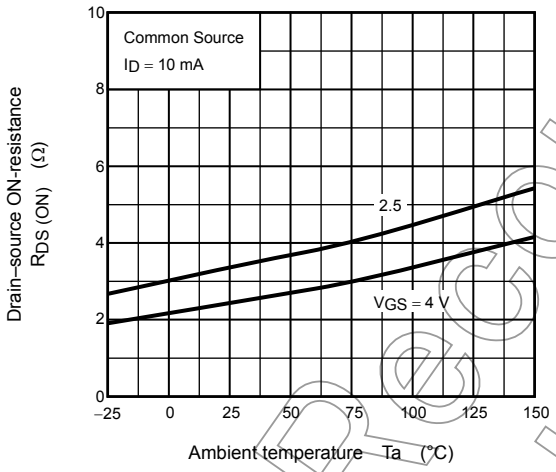
$R_{DS\ (ON)} - I_D$



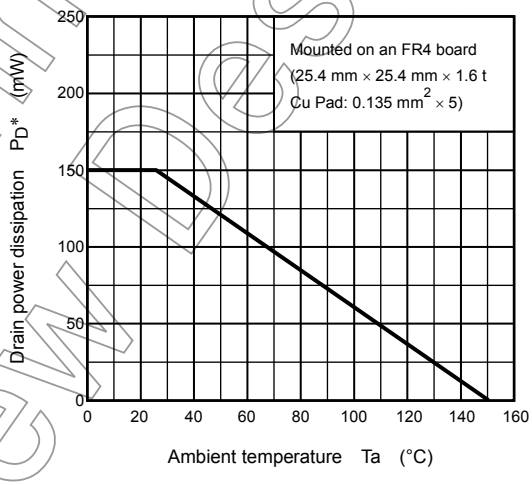
$t - I_D$



$R_{DS\ (ON)} - Ta$



$P_D^* - Ta$



*: Total rating

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