Serial 12-Bit/14-Bit, 3.5Msps Sampling ADCs with Shutdown

FEATURES

- **3.5Msps Conversion Rate**
- **74.1dB SINAD at 14-Bits, 71.1dB SINAD at 12-Bits**
- **Low Power Dissipation: 18mW**
- **3.3V Single Supply Operation**
- 2.5V Internal Bandgap Reference can be Overdriven
- 3-Wire SPI-Compatible Serial Interface
- Sleep (13µW) Shutdown Mode
- Nap (4mW) Shutdown Mode
- 80dB Common Mode Rejection
- ±1.25V Bipolar Input Range
- Tiny 10-Lead MSOP Package

APPLICATIONS

- Communications
- Data Acquisition Systems
- Uninterrupted Power Supplies
- Multiphase Motor Control
- Multiplexed Data Acquisition
- RFID

DESCRIPTION

The LTC®2356-12/LTC2356-14 are 12-bit/14-bit, 3.5Msps serial ADCs with differential inputs. The devices draw only 5.5mA from a single 3.3V supply and come in a tiny 10-lead MSOP package. A Sleep shutdown feature further reduces power consumption to 13µW. The combination of speed, low power and tiny package makes the LTC2356-12/LTC2356-14 suitable for high speed, portable applications.

The 80dB common mode rejection allows users to eliminate ground loops and common mode noise by measuring signals differentially from the source.

The devices convert –1.25V to 1.25V bipolar inputs differentially. The absolute voltage swing for A_{IN}^+ and A_{IN}^- extends from ground to the supply voltage.

The serial interface sends out the conversion results during the 16 clock cycles following a CONV rising edge for compatibility with standard serial interfaces. If two additional clock cycles for acquisition time are allowed after the data stream in between conversions, the full sampling rate of 3.5Msps can be achieved with a 63MHz clock.

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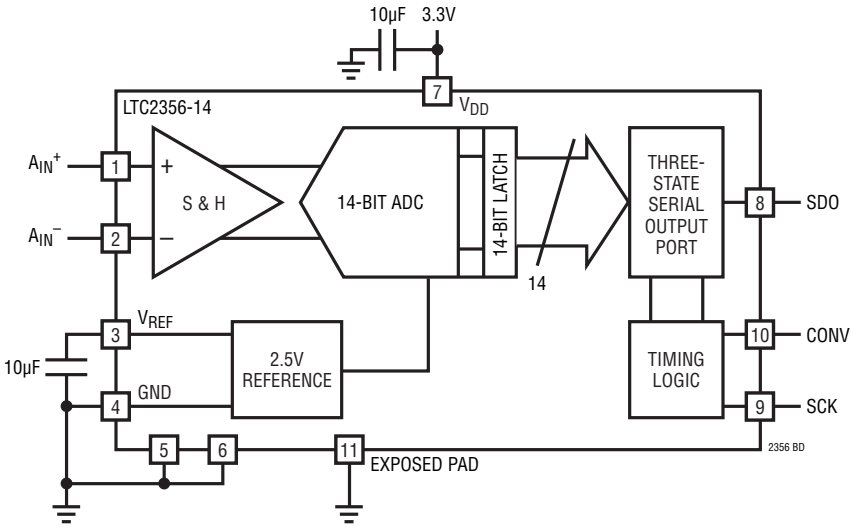
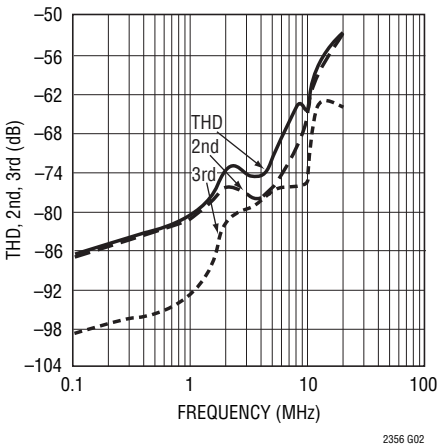
BLOCK DIAGRAM



THD, 2nd and 3rd vs Input Frequency for Differential Input Signals

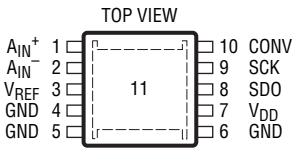


ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2)

Supply Voltage (V_{DD}) 4V
Analog and V_{REF} Input Voltages
(Note 3) ..... –0.3V to (V_{DD} + 0.3V)
Digital Input Voltages ..... – 0.3V to (V_{DD} + 0.3V)
Digital Output Voltage ..... –0.3V to (V_{DD} + 0.3V)
Power Dissipation 100mW
Operation Temperature Range
LTC2356C-12/LTC2356C-14 ..... 0°C to 70°C
LTC2356I-12/LTC2356I-14 ..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PIN CONFIGURATION



MSE PACKAGE
10-LEAD PLASTIC MSOP

T_{JMAX} = 125°C, θ_{JA} = 40°C/W
EXPOSED PAD (PIN 11) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC2356CMSE-12#PBF	LTC2356CMSE-12#TRPBF	LTCWN	10-Lead Plastic MSOP	0°C to 70°C
LTC2356IMSE-12#PBF	LTC2356IMSE-12#TRPBF	LTCWN	10-Lead Plastic MSOP	–40°C to 85°C
LTC2356CMSE-14#PBF	LTC2356CMSE-14#TRPBF	LTCVF	10-Lead Plastic MSOP	0°C to 70°C
LTC2356IMSE-14#PBF	LTC2356IMSE-14#TRPBF	LTCVF	10-Lead Plastic MSOP	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

CONVERTER CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. With internal reference. V_{DD} = 3.3V.

PARAMETER	CONDITIONS		LTC2356-12 MIN	LTC2356-12 TYP	LTC2356-12 MAX	LTC2356-14 MIN	LTC2356-14 TYP	LTC2356-14 MAX	UNITS
Resolution (No Missing Codes)		●	12			14			Bits
Integral Linearity Error	(Notes 4, 5, 18)	●	–2	±0.25	2	–4	±0.5	4	LSB
Offset Error	(Notes 4, 18)	●	–10	±1	10	–30	±2	30	LSB
Gain Error	(Note 4, 18)	●	–40	±5	40	–80	±10	80	LSB
Gain Tempco	Internal Reference (Note 4) External Reference			±15 ±1			±15 ±1		ppm/°C ppm/°C

ANALOG INPUT

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. With internal reference. V_{DD} = 3.3V.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}	Analog Differential Input Range (Notes 3, 8, 9)	3.1V ≤ V_{DD} ≤ 3.6V	●		–1.25 to 1.25		V
V_{CM}	Analog Common Mode + Differential Input Range (Note 10)				0 to V_{DD}		V
I_{IN}	Analog Input Leakage Current		●			1	µA
C_{IN}	Analog Input Capacitance	(Note 19)			13		pF
t_{ACQ}	Sample-and-Hold Acquisition Time	(Note 6)	●			39	ns
t_{AP}	Sample-and-Hold Aperture Delay Time				1		ns
t_{JITTER}	Sample-and-Hold Aperture Delay Time Jitter				0.3		ps
CMRR	Analog Input Common Mode Rejection Ratio	f_{IN} = 1MHz, V_{IN} = 0V to 3V f_{IN} = 100MHz, V_{IN} = 0V to 3V			–60 –15		dB dB

DYNAMIC ACCURACY

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C with external reference = 2.55V. V_{DD} = 3.3V. Single-ended A_{IN}^+ signal drive with A_{IN}^- = 1.5V DC. Differential signal drive with V_{CM} = 1.5V at A_{IN}^+ and A_{IN}^-

				LTC2356-12			LTC2356-14			
SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	MIN	TYP	MAX	UNITS
SINAD	Signal-to-Noise Plus Distortion Ratio	100kHz Input Signal (Note 19) 1.4MHz Input Signal (Note 19)	 ●	 68	71.1 71.1		 70	74.1 72.3		dB dB
THD	Total Harmonic Distortion	100kHz First 5 Harmonics (Note 19) 1.4MHz First 5 Harmonics (Note 19)	 ●		–86 –82	 –76		–86 –82	 –78	dB dB
SFDR	Spurious Free Dynamic Range	100kHz Input Signal (Note 19) 1.4MHz Input Signal (Note 19)			86 82			86 82		dB dB
IMD	Intermodulation Distortion	0.625V_{P-P} to 1.4MHz Summed with 0.625V_{P-P} 1.56MHz into A_{IN}^+ and Inverted into A_{IN}^-			–82			–82		dB
	Code-to-Code Transition Noise	V_{REF} = 2.5V (Note 18)			0.25			1		LSB_{RMS}
	Full Power Bandwidth	V_{IN} = 2.5V_{P-P}, SDO = 11585LSB_{P-P} (Note 15)			50			50		MHz
	Full Linear Bandwidth	S/(N + D) ≥ 68dB			5			5		MHz

INTERNAL REFERENCE CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{DD} = 3.3V.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{REF} Output Voltage	I_{OUT} = 0			2.5		V
V_{REF} Output Tempco				15		ppm/°C
V_{REF} Line Regulation	V_{DD} = 3.1V to 3.6V, V_{REF} = 2.5V			600		µV/V
V_{REF} Output Resistance	Load Current = 0.5mA			0.2		Ω
V_{REF} Settling Time	C_{REF} = 10µF			2		ms
External V_{REF} Input Range			2.55		V_{DD}	V

DIGITAL INPUTS AND DIGITAL OUTPUTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{DD} = 3.3V.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	High Level Input Voltage	V_{DD} = 3.6V	●	2.4			V
V_{IL}	Low Level Input Voltage	V_{DD} = 3.1V	●			0.6	V
I_{IN}	Digital Input Current	V_{IN} = 0V to V_{DD}	●			±10	µA
C_{IN}	Digital Input Capacitance				5		pF
V_{OH}	High Level Output Voltage	V_{DD} = 3.3V, I_{OUT} = –200µA	●	2.5	2.9		V
V_{OL}	Low Level Output Voltage	V_{DD} = 3.1V, I_{OUT}= 160µA V_{DD} = 3.1V, I_{OUT} = 1.6mA	 ●		0.05 0.10	 0.4	V V
I_{OZ}	Hi-Z Output Leakage D_{OUT}	V_{OUT} = 0V to V_{DD}	●			±10	µA
C_{OZ}	Hi-Z Output Capacitance D_{OUT}				1		pF
I_{SOURCE}	Output Short-Circuit Source Current	V_{OUT} = 0V, V_{DD} = 3.3V			20		mA
I_{SINK}	Output Short-Circuit Sink Current	V_{OUT} = V_{DD} = 3.3V			15		mA

POWER REQUIREMENTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 17)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{DD}	Supply Voltage			3.1	3.3	3.6	V
I_{DD}	Supply Current	Active Mode Nap Mode Sleep Mode (LTC2356-12) Sleep Mode (LTC2356-14)	● ●		5.5 1.1 4 4	8 1.5 15 12	mA mA µA µA
P_D	Power Dissipation	Active Mode with SCK in Fixed State (Hi or Lo)			18		mW

TIMING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{DD} = 3.3V.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$f_{SAMPLE(MAX)}$	Maximum Sampling Rate per Channel (Conversion Rate)		●	3.5			MHz
$t_{THROUGHPUT}$	Minimum Sampling Period (Conversion + Acquisiton Period)		●			286	ns
t_{SCK}	Clock Period	(Note 16)	●	15.872		10000	ns
t_{CONV}	Conversion Time	(Note 6)		16	18		SCLK cycles
t_1	Minimum High or Low SCLK Pulse Width	(Note 6)		2			ns
t_2	CONV to SCK Setup Time	(Notes 6, 10)		3			ns
t_3	Nearest SCK Edge Before CONV	(Note 6)		0			ns
t_4	Minimum High or Low CONV Pulse Width	(Note 6)		4			ns
t_5	SCK↑ to Sample Mode	(Note 6)		4			ns
t_6	CONV↑ to Hold Mode	(Notes 6, 11)		1.2			ns
t_7	16th SCK↑ to CONV≠ Interval (Affects Acquisition Period)	(Notes 6, 7, 13)		45			ns
t_8	Delay from SCK to Valid Data	(Notes 6, 12)				8	ns
t_9	SCK↑ to Hi-Z at SDO	(Notes 6, 12)				6	ns
t_{10}	Previous SDO Bit Remains Valid After SCK	(Notes 6, 12)		2			ns
t_{12}	V_{REF} Settling Time After Sleep-to-Wake Transition	(Note 14)			2		ms

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All voltage values are with respect to GND.

Note 3: When these pins are taken below GND or above V_{DD}, they will be clamped by internal diodes. This product can handle input currents greater than 100mA below GND or greater than V_{DD} without latchup.

Note 4: Offset and full-gain specifications are measured for a single-ended A_{IN}^+ input with A_{IN}^- grounded and using the internal 2.5V reference.

Note 5: Integral linearity is tested with an external 2.55V reference and is defined as the deviation of a code from the straight line passing through the actual endpoints of a transfer curve. The deviation is measured from the center of quantization band.

Note 6: Guaranteed by design, not subject to test.

Note 7: Recommended operating conditions.

Note 8: The analog input range is defined for the voltage difference between A_{IN}^+ and A_{IN}^-. Performance is specified with A_{IN}^- = 1.5V DC while driving A_{IN}^+.

Note 9: The absolute voltage at A_{IN}^+ and A_{IN}^- must be within this range.

Note 10: If less than 3ns is allowed, the output data will appear one clock cycle later. It is best for CONV to rise half a clock before SCK, when running the clock at rated speed.

Note 11: Not the same as aperture delay. Aperture delay is smaller (1ns) because the 2.2ns delay through the sample-and-hold is subtracted from the CONV to Hold mode delay.

Note 12: The rising edge of SCK is guaranteed to catch the data coming out into a storage latch.

Note 13: The time period for acquiring the input signal is started by the 16th rising clock and it is ended by the rising edge of convert.

Note 14: The internal reference settles in 2ms after it wakes up from Sleep mode with one or more cycles at SCK and a 10µF capacitive load.

Note 15: The full power bandwidth is the frequency where the output code swing drops to 3dB with a $2.5V_{P-P}$ input sine wave.

Note 16: Maximum clock period guarantees analog performance during conversion. Output data can be read with an arbitrarily long clock.

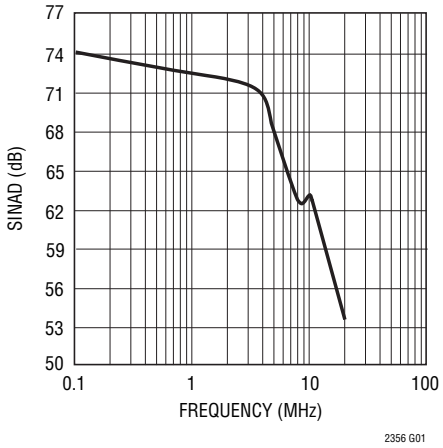
Note 17: V_{DD} = 3.3V, f_{SAMPLE} = 3.5Msps.

Note 18: The LTC2356-14 is measured and specified with 14-bit resolution (1LSB = 152µV) and the LTC2356-12 is measured and specified with 12-bit resolution (1LSB = 610µV).

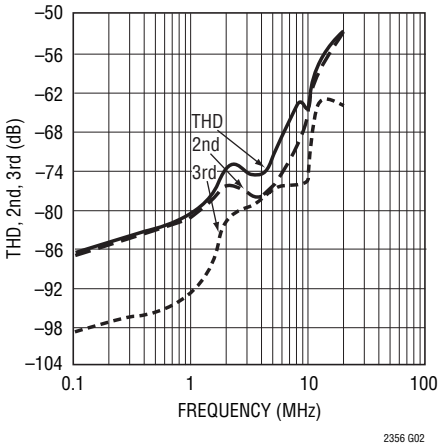
Note 19: The sampling capacitor at each input accounts for 4.1pF of the input capacitance.

TYPICAL PERFORMANCE CHARACTERISTICS $T_A = 25°C$, $V_{DD} = 3.3V$ (LTC2356-14)

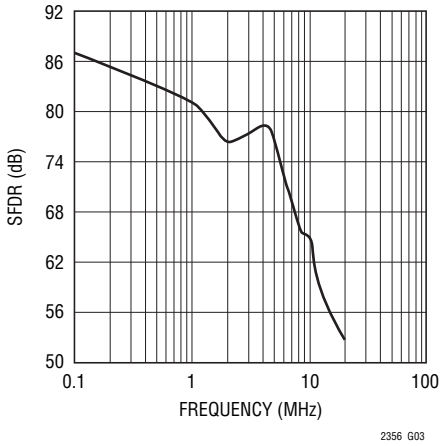
SINAD vs Input Frequency



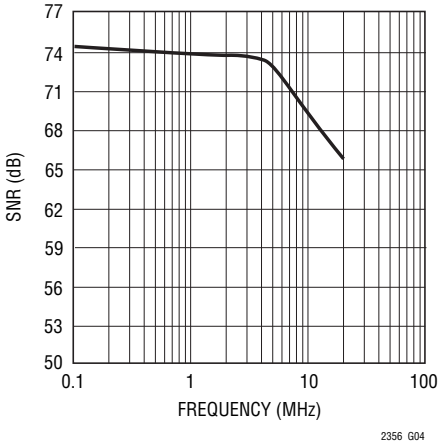
THD, 2nd and 3rd vs Input Frequency



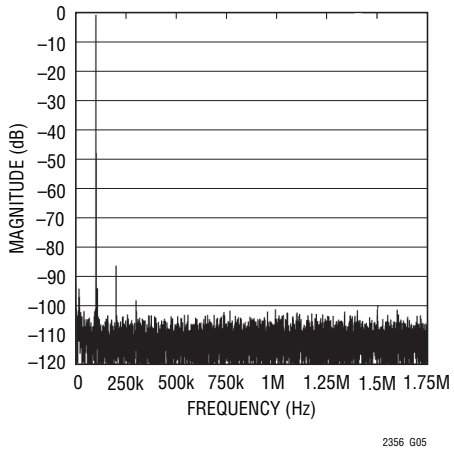
SFDR vs Input Frequency



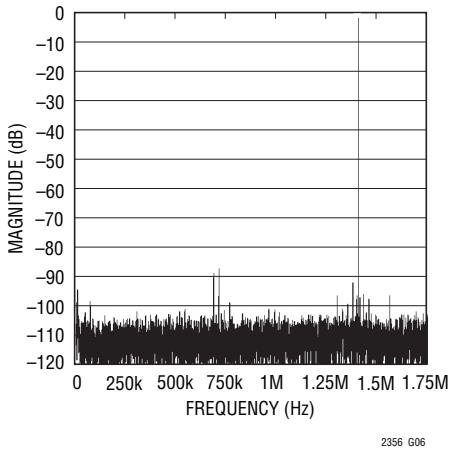
SNR vs Input Frequency



100kHz Sine Wave 8192 Point FFT Plot

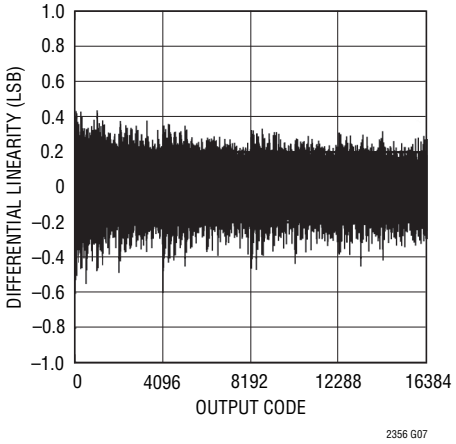


1.4MHz Sine Wave 8192 Point FFT Plot

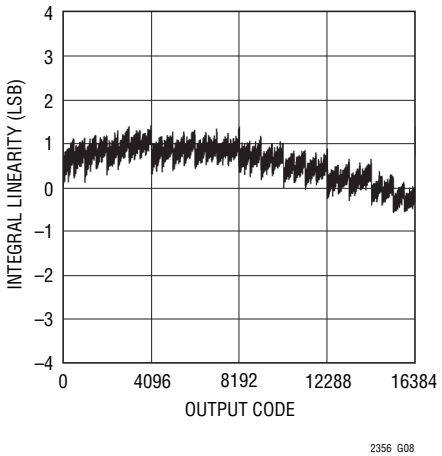


TYPICAL PERFORMANCE CHARACTERISTICS $T_A = 25°C$, $V_{DD} = 3.3V$ (LTC2356-14)

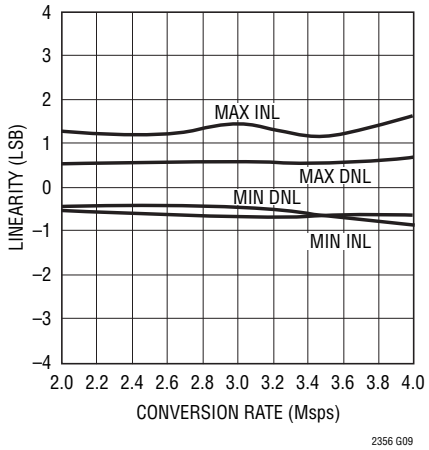
Differential Linearity vs Output Code



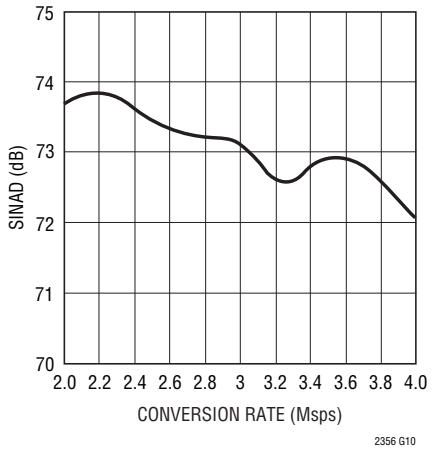
Integral Linearity vs Output Code



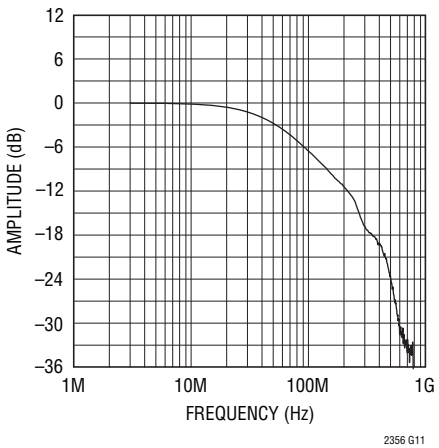
Differential and Integral Linearity vs Conversion Rate



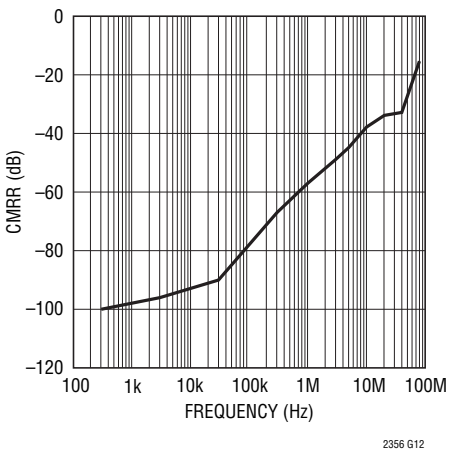
SINAD vs Conversion Rate, Input Frequency = 1.4MHz



2.5V_{P-P} Power Bandwidth

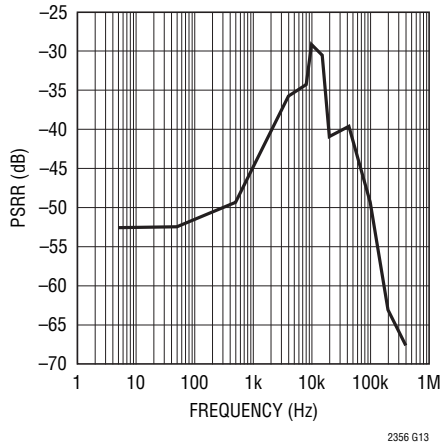


CMRR vs Frequency

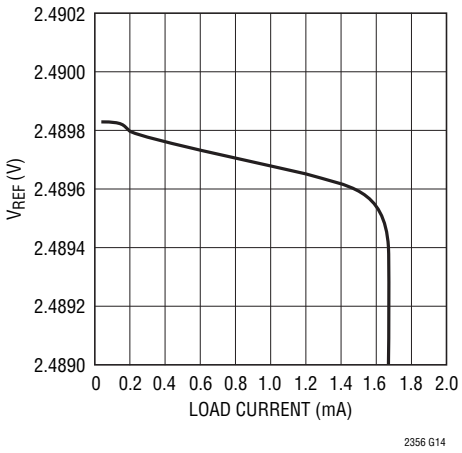


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, V_{DD} = 3.3V (LTC2356-12 and LTC2356-14)

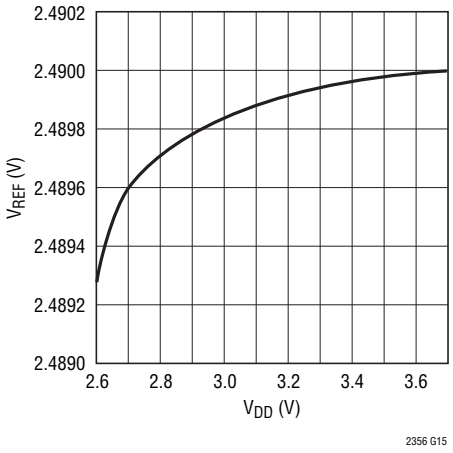
PSRR vs Frequency



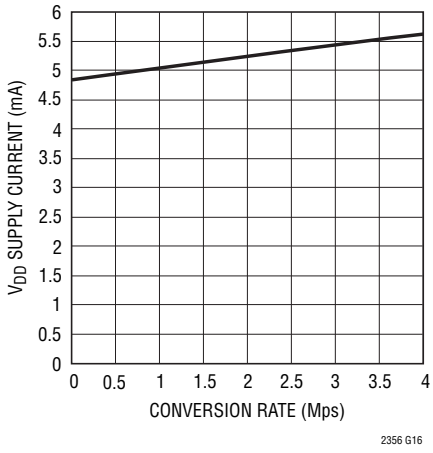
Internal Reference Voltage vs Load Current



Internal Reference Voltage vs V_{DD}



V_{DD} Supply Current vs Conversion Rate



PIN FUNCTIONS

A_{IN}^+ (Pin 1): Noninverting Analog Input. A_{IN}^+ operates fully differentially with respect to A_{IN}^- with a –1.25V to 1.25V differential swing with respect to A_{IN}^- and a 0V to V_{DD} common mode swing.

A_{IN}^- (Pin 2): Inverting Analog Input. A_{IN}^- operates fully differentially with respect to A_{IN}^+ with a 1.25V to –1.25V differential swing with respect to A_{IN}^+ and a 0V to V_{DD} common mode swing.

V_{REF} (Pin 3): 2.5V Internal Reference. Bypass to GND and to a solid analog ground plane with a 10µF ceramic capacitor (or 10µF tantalum in parallel with 0.1µF ceramic). Can be overdriven by an external reference between 2.55V and V_{DD}.

GND (Pins 4, 5, 6, 11): Ground and Exposed Pad. These ground pins and the exposed pad must be tied directly to the solid ground plane under the part. Keep in mind that analog signal currents and digital output signal currents flow through these pins.

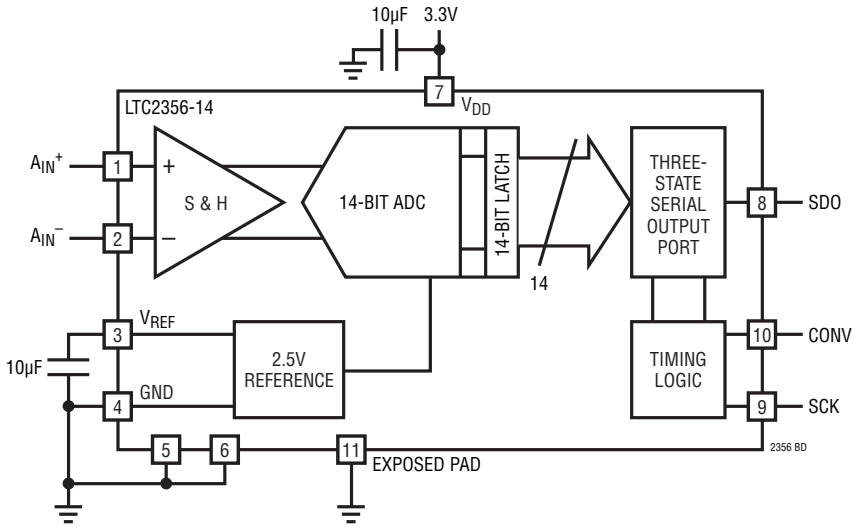
V_{DD} (Pin 7): 3.3V Positive Supply. This single power pin supplies 3.3V to the entire device. Bypass to GND and to a solid analog ground plane with a 10µF ceramic capacitor (or 10µF tantalum in parallel with 0.1µF ceramic). Keep in mind that internal analog currents and digital output signal currents flow through this pin. Care should be taken to place the 0.1µF bypass capacitor as close to Pins 6 and 7 as possible.

SDO (Pin 8): Three-State Serial Data Output. Each set of output data words represents the difference between A_{IN}^+ and A_{IN}^- analog inputs at the start of the previous conversion. The output format is 2's complement.

SCK (Pin 9): External Clock Input. Advances the conversion process and sequences the output data on the rising edge. Responds to TTL (≤3.3V) and 3.3V CMOS levels. One or more pulses wake from sleep.

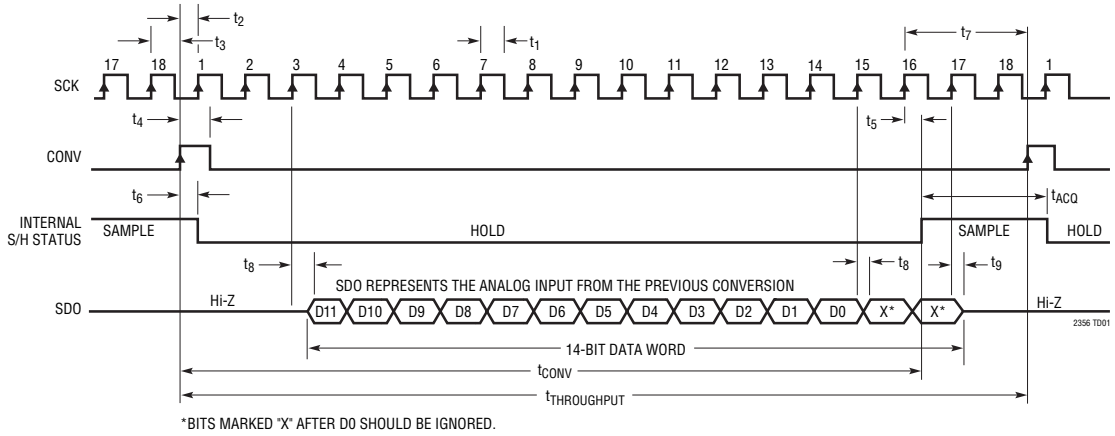
CONV (Pin 10): Convert Start. Holds the analog input signal and starts the conversion on the rising edge. Responds to TTL (≤3.3V) and 3.3V CMOS levels. Two CONV pulses with SCK in fixed high or fixed low state start Nap mode. Four or more CONV pulses with SCK in fixed high or fixed low state start Sleep mode.

BLOCK DIAGRAM



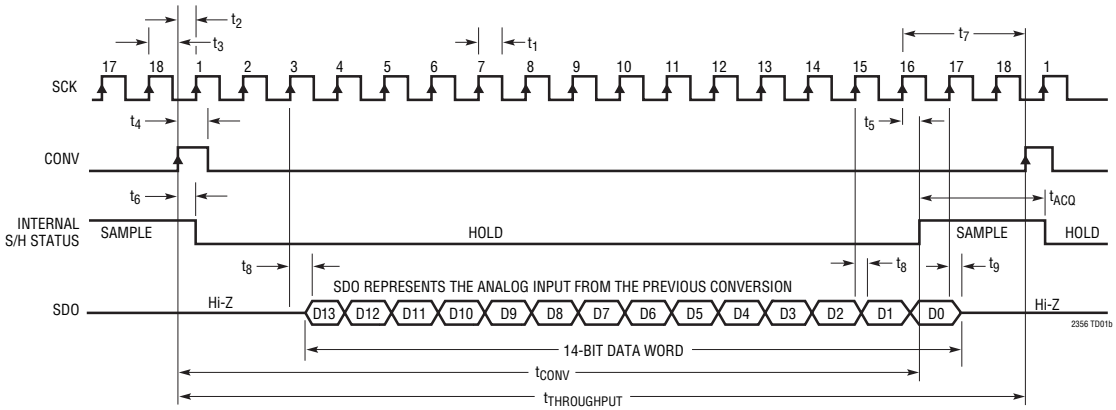
TIMING DIAGRAM

LTC2356-12 Timing Diagram

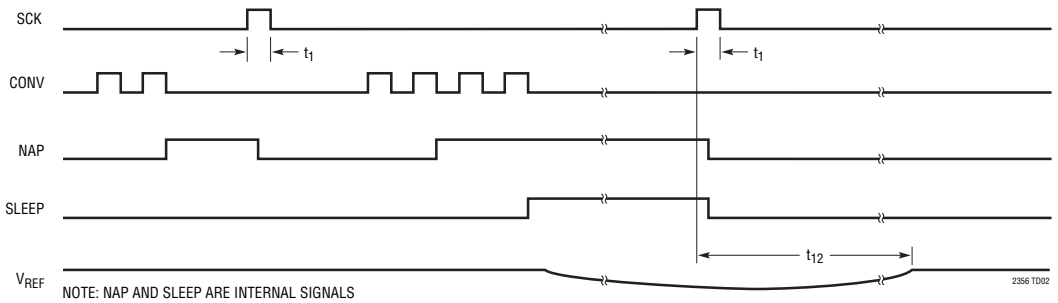


*BITS MARKED "X" AFTER D0 SHOULD BE IGNORED.

LTC2356-14 Timing Diagram

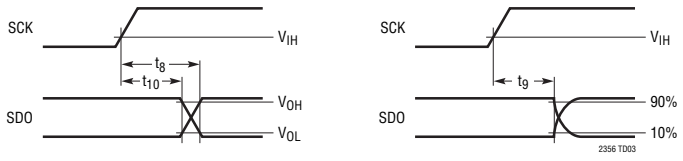


Nap Mode and Sleep Mode Waveforms



NOTE: NAP AND SLEEP ARE INTERNAL SIGNALS

SCK to SDO Delay



APPLICATIONS INFORMATION

DRIVING THE ANALOG INPUT

The differential analog inputs of the LTC2356-12/LTC2356-14 may be driven differentially or as a single-ended input (i.e., the A_{IN}^- input is set to V_{CM}). Both differential analog inputs, A_{IN}^+ and A_{IN}^-, are sampled at the same instant. Any unwanted signal that is common to both inputs of each input pair will be reduced by the common mode rejection of the sample-and-hold circuit. The inputs draw only one small current spike while charging the sample-and-hold capacitors at the end of conversion. During conversion, the analog inputs draw only a small leakage current. If the source impedance of the driving circuit is low, then the LTC2356-12/LTC2356-14 inputs can be driven directly. As source impedance increases, so will acquisition time. For minimum acquisition time with high source impedance, a buffer amplifier must be used. The main requirement is that the amplifier driving the analog input(s) must settle after the small current spike before the next conversion starts (settling time must be 39ns for full throughput rate). Also keep in mind while choosing an input amplifier the amount of noise and harmonic distortion added by the amplifier.

CHOOSING AN INPUT AMPLIFIER

Choosing an input amplifier is easy if a few requirements are taken into consideration. First, to limit the magnitude of the voltage spike seen by the amplifier from charging the sampling capacitor, choose an amplifier that has a low output impedance (<100Ω) at the closed-loop bandwidth frequency. For example, if an amplifier is used with a gain of 1 and has a unity-gain bandwidth of 50MHz, then the output impedance at 50MHz must be less than 100Ω. The second requirement is that the closed-loop bandwidth must be greater than 40MHz to ensure adequate small-signal settling for full throughput rate. If slower op amps are used, more time for settling can be provided by increasing the time between conversions. The best choice for an op amp to drive the LTC2356-12/LTC2356-14 will depend on the application. Generally, applications fall into two categories: AC applications where dynamic specifications are most critical and time domain applications where DC accuracy and settling time are most critical. The following list is a summary of the op amps that are suitable for driving the LTC2356-12/LTC2356-14. (More detailed information is available in the Linear Technology Databooks and our website at www.linear.com.)

LTC1566-1: Low Noise 2.3MHz Continuous Time Low-Pass Filter.

LT®1630: Dual 30MHz Rail-to-Rail Voltage FB Amplifier. 2.7V to ±15V supplies. Very high A_{VOL}, 500µV offset and 520ns settling to 0.5LSB for a 4V swing. THD and noise are –93dB to 40kHz and below 1LSB to 320kHz (A_V = 1, $2V_{P-P}$ into 1kΩ, V_S = 5V), making the part excellent for AC applications (to 1/3 Nyquist) where rail-to-rail performance is desired. Quad version is available as LT1631.

LT1632: Dual 45MHz Rail-to-Rail Voltage FB Amplifier. 2.7V to ±15V supplies. Very high A_{VOL}, 1.5mV offset and 400ns settling to 0.5LSB for a 4V swing. It is suitable for applications with a single 5V supply. THD and noise are –93dB to 40kHz and below 1LSB to 800kHz (A_V = 1, $2V_{P-P}$ into 1kΩ, V_S = 5V), making the part excellent for AC applications where rail-to-rail performance is desired. Quad version is available as LT1633.

LT1813: Dual 100MHz 750V/µs 3mA Voltage Feedback Amplifier. 5V to ±5V supplies. Distortion is –86dB to 100kHz and –77dB to 1MHz with ±5V supplies ($2V_{P-P}$ into 500Ω). Excellent part for fast AC applications with ±5V supplies.

LT1801: 80MHz GBWP, –75dBc at 500kHz, 2mA/Amplifier, 8.5nV/√Hz.

LT1806/LT1807: 325MHz GBWP, –80dBc Distortion at 5MHz, Unity-Gain Stable, R-R In and Out, 10mA/Amplifier, 3.5nV/√Hz.

LT1810: 180MHz GBWP, –90dBc Distortion at 5MHz, Unity-Gain Stable, R-R In and Out, 15mA/Amplifier, 16nV/√Hz.

LT1818/LT1819: 400MHz, 2500V/µs,9mA, Single/Dual Voltage Mode Operational Amplifier.

LT6200: 165MHz GBWP, –85dBc Distortion at 1MHz, Unity-Gain Stable, R-R In and Out, 15mA/Amplifier, 0.95nV/√Hz.

LT6203: 100MHz GBWP, –80dBc Distortion at 1MHz, Unity-Gain Stable, R-R In and Out, 3mA/Amplifier, 1.9nV/√Hz.

LT6600-10: Amplifier/Filter Differential In/Out with 10MHz Cutoff.

APPLICATIONS INFORMATION

INPUT FILTERING AND SOURCE IMPEDANCE

The noise and the distortion of the input amplifier and other circuitry must be considered since they will add to the LTC2356-12/LTC2356-14 noise and distortion. The small-signal bandwidth of the sample-and-hold circuit is 50MHz. Any noise or distortion products that are present at the analog inputs will be summed over this entire bandwidth. Noisy input circuitry should be filtered prior to the analog inputs to minimize noise. A simple 1-pole RC filter is sufficient for many applications. For example, Figure 1 shows a 47pF capacitor from A_{IN}^+ to ground and a 51Ω source resistor to limit the input bandwidth to 47MHz. The 47pF capacitor also acts as a charge reservoir for the input sample-and-hold and isolates the ADC input from sampling-glitch sensitive circuitry. High quality capacitors and resistors should be used since these components can add distortion. NPO and silvermica type dielectric capacitors have excellent linearity. Carbon surface mount resistors can generate distortion from self heating and from damage that may occur during soldering. Metal film surface mount resistors are much less susceptible to both problems. When high amplitude unwanted signals are close in frequency to the desired signal frequency, a multiple pole filter is required. High external source resistance, combined with the 13pF of input capacitance, will reduce the rated 50MHz bandwidth and increase acquisition time beyond 39ns.

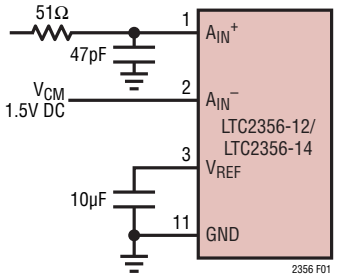


Figure 1. RC Input Filter

INPUT RANGE

The analog inputs of the LTC2356-12/LTC2356-14 may be driven fully differentially with a single supply. Each input may swing up to $2.5V_{P-P}$ individually. When using the internal reference, the non-inverting input should never be more than 1.25V more positive or more negative than the inverting input. The ±1.25V range is also ideally suited for AC-coupled signals in single supply applications. Figure 2 shows how to AC couple signals in a single supply system without needing a mid-supply 1.5V external reference. The DC common mode level is supplied by the previous stage that is already bounded by the single supply voltage of the system. The common mode range of the inputs extend from ground to the supply voltage V_{DD}. If the difference between the A_{IN}^+ and A_{IN}^- inputs exceeds 1.25V, the output code will stay fixed at zero and all ones and if this difference goes below –1.25V, the output code will stay fixed at one and all zeros.

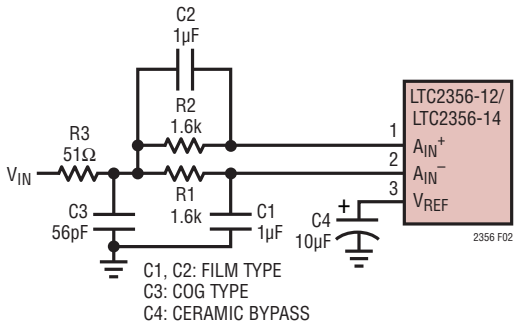


Figure 2. AC Coupling of AC Signals with 1kHz Low Cutoff Frequency

INTERNAL REFERENCE

The LTC2356-12/LTC2356-14 has an on-chip, temperature compensated, bandgap reference that is factory trimmed to 2.5V to obtain a bipolar ±1.25V input span. The reference amplifier output V_{REF}, (Pin 3) must be bypassed with a capacitor to ground. The reference amplifier is stable with capacitors of 1µF or greater. For the best noise performance, a 10µF ceramic or a 10µF tantalum in parallel with a 0.1µF ceramic is recommended. The V_{REF} pin can be overdriven with an external reference as shown in

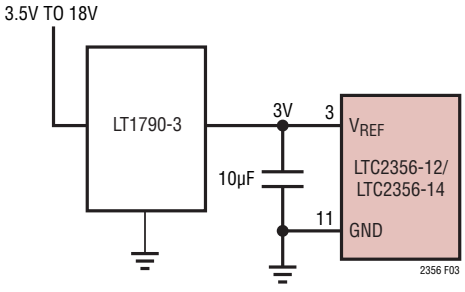


Figure 3. Overdriving V_{REF} Pin with an External Reference

APPLICATIONS INFORMATION

Figure 3. The voltage of the external reference must be higher than the 2.5V output of the internal reference. The recommended range for an external reference is 2.55V to V_{DD}. An external reference at 2.55V will see a DC quiescent load of 0.75mA and as much as 3mA during conversion.

INPUT SPAN VERSUS REFERENCE VOLTAGE

The differential input range has a bipolar ± V_{REF}/2 voltage span that equals the difference between the voltage at the reference buffer output V_{REF} at Pin 3, and the voltage at the ground (Exposed Pad Ground). The differential input range of the ADC is ±1.25V when using the internal reference. The internal ADC is referenced to these two nodes. This relationship also holds true with an external reference.

DIFFERENTIAL INPUTS

The LTC2356-12/LTC2356-14 have a unique differential sample-and-hold circuit that measures input voltages from ground to V_{DD}. The ADC will always convert the bipolar difference of $A_{IN}^+ – A_{IN}^–$, independent of the common mode voltage at the inputs. The common mode rejection holds up at extremely high frequencies, see Figure 4. The only requirement is that both inputs not go below ground or exceed V_{DD}. Integral nonlinearity errors (INL) and differential nonlinearity errors (DNL) are largely independent of the common mode voltage. However, the offset error will vary. The change in offset error is typically less than 0.1% of the common mode voltage.

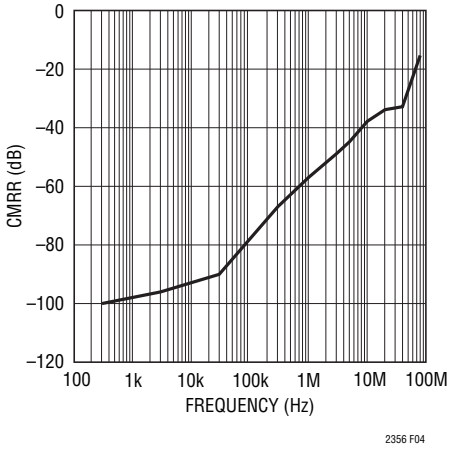


Figure 4. CMRR vs Frequency

Figure 5 shows the ideal input/output characteristics for the LTC2356-12/LTC2356-14. The code transitions occur midway between successive integer LSB values (i.e., 0.5LSB, 1.5LSB, 2.5LSB, FS – 1.5LSB). The output code is 2's complement with 1LSB = 2.5V/16384 = 153µV for the LTC2356-14, and 1LSB = 2.5V/4096 = 610µV for the LTC2356-12. The LTC2356-14 has 1LSB RMS of random white noise. Figure 6a shows the LTC1819 converting a single ended input signal to differential input signals for optimum THD and SFDR performance as shown in the FFT plot (Figure 6b).

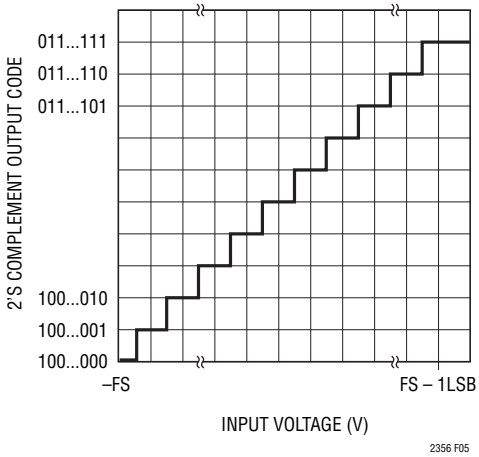


Figure 5. LTC2356-12/LTC2356-14 Transfer Characteristic

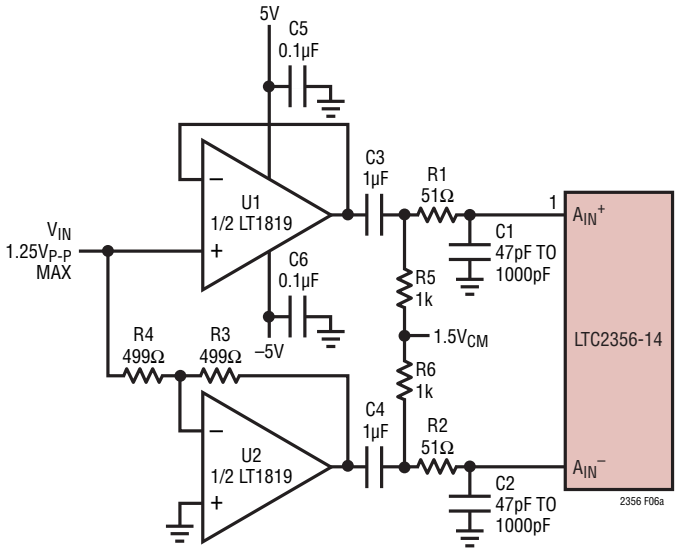


Figure 6a. The LT1819 Driving the LTC2356-14 Differentially

APPLICATIONS INFORMATION

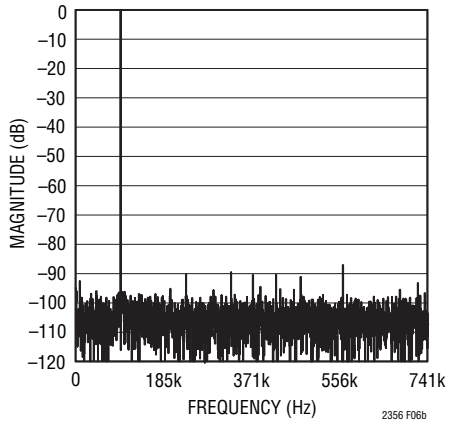


Figure 6b. LTC2356-12 6MHz Sine Wave 4096 Point FFT Plot with the LT1819 Driving the Inputs Differentially

Board Layout and Bypassing

Wire wrap boards are not recommended for high resolution and/or high speed A/D converters. To obtain the best performance from the LTC2356-12/LTC2356-14, a printed circuit board with ground plane is required. Layout for the printed circuit board should ensure that digital and analog signal lines are separated as much as possible. In particular, care should be taken not to run any digital track alongside an analog signal track. If optimum phase match between the inputs is desired, the length of the two input wires should be kept matched.

High quality tantalum and ceramic bypass capacitors should be used at the V_{DD} and V_{REF} pins as shown in the Block Diagram on the first page of this data sheet. For optimum performance, a 10µF surface mount Tantalum capacitor with a 0.1µF ceramic is recommended for the V_{DD} and V_{REF} pins. Alternatively, 10µF ceramic chip capacitors such as Murata GRM219R60J106M may be used. The capacitors must be located as close to the pins as possible. The traces connecting the pins and the bypass capacitors must be kept short and should be made as wide as possible.

Figure 7 shows the recommended system ground connections. All analog circuitry grounds should be terminated at the LTC2356-12/LTC2356-14 GND (Pins 4, 5, 6 and exposed pad). The ground return from the LTC2356-12/LTC2356-14 (Pins 4, 5, 6 and exposed pad) to the power supply should be low impedance for noise free operation. In applications where the ADC data outputs

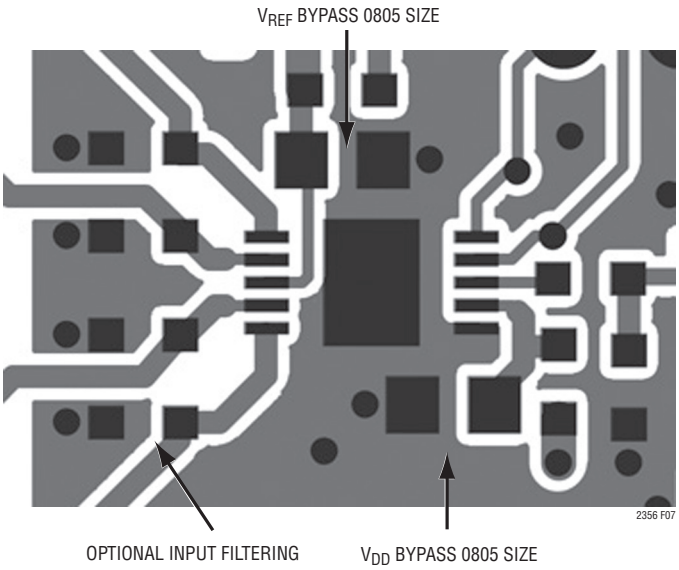


Figure 7. Recommended Layout

and control signals are connected to a continuously active microprocessor bus, it is possible to get errors in the conversion results. These errors are due to feedthrough from the microprocessor to the successive approximation comparator. The problem can be eliminated by forcing the microprocessor into a Wait state during conversion or by using three-state buffers to isolate the ADC data bus.

POWER-DOWN MODES

Upon power-up, the LTC2356-12/LTC2356-14 is initialized to the active state and is ready for conversion. The Nap and Sleep mode waveforms show the power-down modes for the LTC2356-12/LTC2356-14. The SCK and CONV inputs control the power-down modes (see Timing Diagrams). Two rising edges at CONV, without any intervening rising edges at SCK, put the LTC2356-12/LTC2356-14 in Nap mode and the power consumption drops from 18mW to 4mW. The internal reference remains powered in Nap mode. One or more rising edges at SCK wake up the LTC2356-12/LTC2356-14 very quickly, and CONV can start an accurate conversion within a clock cycle. Four rising edges at CONV, without any intervening rising edges at SCK, put the LTC2356-12/LTC2356-14 in Sleep mode and the power consumption drops from 18mW to 13µW. One or more rising edges at SCK wake up the LTC2356-12/LTC2356-14 for operation. The internal reference (V_{REF}) takes 2ms to slew and settle with a 10µF load.

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Note that, using sleep mode more frequently than every 2ms, compromises the settled accuracy of the internal reference. Note that, for slower conversion rates, the Nap and Sleep modes can be used for substantial reductions in power consumption.

DIGITAL INTERFACE

The LTC2356-12/LTC2356-14 has a 3-wire SPI-compatible (Serial Protocol Interface) interface. The SCK and CONV inputs and SDO output implement this interface. The SCK and CONV inputs accept swings from 3.3V logic and are TTL compatible, if the logic swing does not exceed V_{DD}. A detailed description of the three serial port signals follows.

Conversion Start Input (CONV)

The rising edge of CONV starts a conversion, but subsequent rising edges at CONV are ignored by the LTC2356-12/LTC2356-14 until the following 16 SCK rising edges have occurred. It is necessary to have a minimum of 16 rising edges of the clock input SCK between rising edges of CONV. But to obtain maximum conversion speed (with a 63MHz SCK), it is necessary to allow two more clock periods between conversions to allow 39ns of acquisition time for the internal ADC sample-and-hold circuit. With 16 clock periods per conversion, the maximum conversion rate is limited to 3.5Msps to allow 39ns for acquisition time. In either case, the output data stream comes out within the first 16 clock periods to ensure compatibility with processor serial ports. The duty cycle of CONV can be arbitrarily chosen to be used as a frame sync signal for the processor serial port. A simple approach to generate CONV is to create a pulse that is one SCK wide to drive the LTC2356-12/LTC2356-14 and then buffer this signal with the appropriate number of inverters to ensure the correct delay driving the frame sync input of the processor serial port. It is good practice to drive the LTC2356-12/LTC2356-14 CONV input first to avoid digital noise interference during the sample-to-hold transition triggered by CONV at the start of conversion. It is also good practice to keep the width of the low portion of the CONV signal greater than 15ns to avoid introducing glitches in the front end of the ADC just before the sample-and-hold goes into hold mode at the rising edge of CONV.

Minimizing Jitter on the CONV Input

In high speed applications where high amplitude sine waves above 100kHz are sampled, the CONV signal must have as little jitter as possible (10ps or less). The square wave output of a common crystal clock module usually meets this requirement . The challenge is to generate a CONV signal from this crystal clock without jitter corruption from other digital circuits in the system. A clock divider and any gates in the signal path from the crystal clock to the CONV input should not share the same integrated circuit with other parts of the system. As shown in Figure 8, the SCK and CONV inputs should be driven first, with digital buffers used to drive the serial port interface. Also note that the master clock in the DSP may already be corrupted with jitter, even if it comes directly from the DSP crystal. Another problem with high speed processor clocks is that they often use a low cost, low speed crystal (i.e., 10MHz) to generate a fast, but jittery, phase-locked-loop system clock (i.e., 40MHz). The jitter in these PLL-generated high speed clocks can be several nanoseconds. Note that if you choose to use the frame sync signal generated by the DSP port, this signal will have the same jitter of the DSP's master clock.

The Typical Application Figure on page 16 shows a circuit for level-shifting and squaring the output from an RF signal generator or other low-jitter source. A single D-type flip flop is used to generate the CONV signal to the LTC2356-12/LTC2356-14. Re-timing the master clock signal eliminates clock jitter introduced by the controlling device (DSP, FPGA, etc.) Both the inverter and flip flop must be treated as analog components and should be powered from a clean analog supply.

Serial Clock Input (SCK)

The rising edge of SCK advances the conversion process and also udpates each bit in the SDO data stream. After CONV rises, the third rising edge of SCK starts clocking out the 12/14 data bits with the MSB sent first. A simple approach is to generate SCK to drive the LTC2356-12/LTC2356-14 first and then buffer this signal with the appropriate number of inverters to drive the serial clock input of the processor serial port. Use the falling edge of the clock to latch data from the Serial Data Output (SDO)

APPLICATIONS INFORMATION

into your processor serial port. The 14-bit serial data will be received right justified, in a 16-bit word with 16 or more clocks per frame sync. It is good practice to drive the LTC2356-12/LTC2356-14 SCK input first to avoid digital noise interference during the internal bit comparison decision by the internal high speed comparator. Unlike the CONV input, the SCK input is not sensitive to jitter because the input signal is already sampled and held constant.

Serial Data Output (SDO)

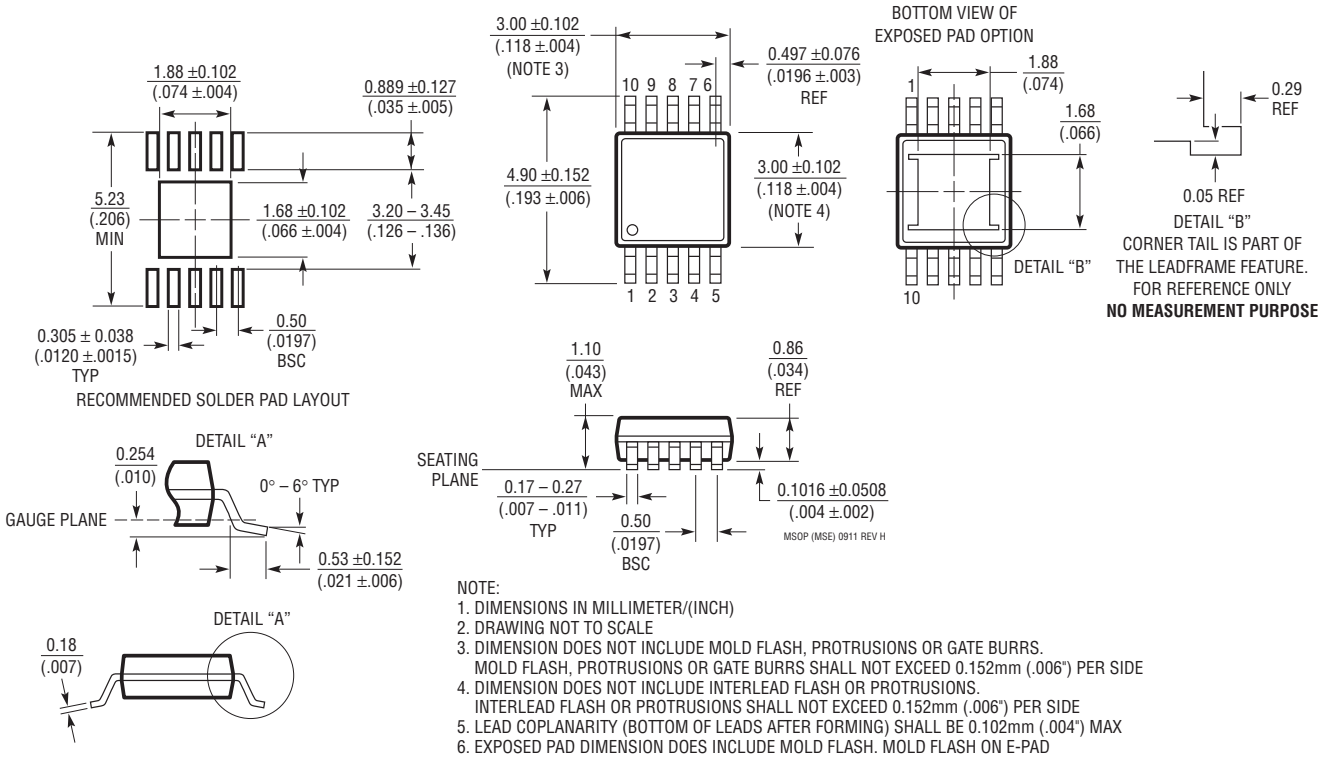
Upon power-up, the SDO output is automatically reset to the high impedance state. The SDO output remains in high impedance until a new conversion is started. SDO sends out 12/14 bits in 2's complement format in the output data stream beginning at the third rising edge of SCK after the rising edge of CONV. SDO is always in high impedance mode when it is not sending out data bits. Please note the delay specification from SCK to a valid SDO. SDO is always guaranteed to be valid by the next rising edge of SCK. The 16-bit output data stream is compatible with the 16-bit or 32-bit serial port of most processors.

Loading on the SDO line must be minimized. SDO can directly drive most fast CMOS logic inputs directly. However, the general purpose I/O pins on many programmable logic devices (FPGAs, CPLDs) and DSPs have excessive capacitance. In these cases, a 100Ω resistor in series with SDO can isolate the input capacitance of the receiving device. If the receiving device has more than 10pF of input capacitance or is located far from the LTC2356-12/LTC2356-14, an NC7SVU04P5X inverter can be used to provide more drive.

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

MSE Package
10-Lead Plastic MSOP, Exposed Die Pad
(Reference LTC DWG # 05-08-1664 Rev H)



NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX
6. EXPOSED PAD DIMENSION DOES INCLUDE MOLD FLASH. MOLD FLASH ON E-PAD SHALL NOT EXCEED 0.254mm (.010") PER SIDE.

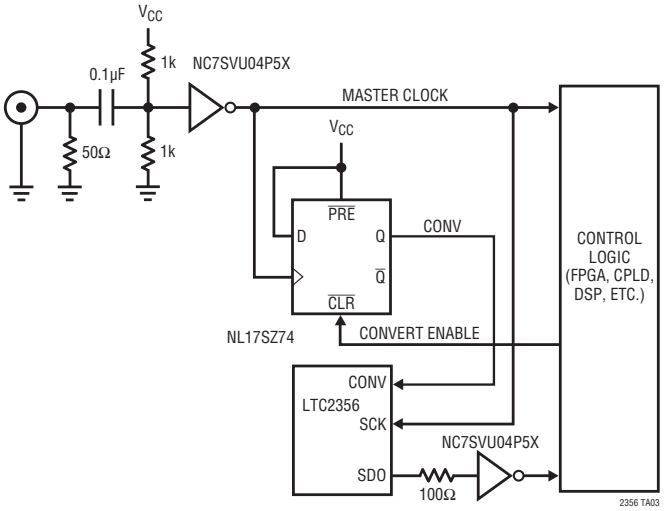
REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	01/10	Revise Values in Pin Configuration Section	2
B	06/12	Changed straight binary to 2's complement	13

Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

TYPICAL APPLICATION

Low-Jitter Clock Timing with RF Sine Generator Using Clock Squaring/Level Shifting Circuit and Re-Timing Flip-Flop



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
ADCs		
LTC1402	12-Bit, 2.2Msps Serial ADC	5V or ±5V Supply, 4.096V or ±2.048V Span
LTC1403/LTC1403A	12-/14-Bit, 2.8Msps Serial ADC	3V, 14mW, Unipolar Inputs, MSOP Package
LTC1403-1/LTC1403A-1	12-/14-Bit, 2.8Msps Serial ADC	3V, 14mW, Bipolar Inputs, MSOP Package
LTC1405	12-Bit, 5Msps Parallel ADC	5V, Selectable Spans, 115mW
LTC1407/LTC1407A	12-/14-Bit, 3Msps Simultaneous Sampling ADC	3V, 2-Channel Differential, Unipolar Inputs, 14mW, MSOP Package
LTC1407-1/LTC1407A-1	12-/14-Bit, 3Msps Simultaneous Sampling ADC	3V, 2-Channel Differential, Bipolar Inputs, 14mW, MSOP Package
LTC1411	14-Bit, 2.5Msps Parallel ADC	5V, Selectable Spans, 80dB SINAD
LTC1412	12-Bit, 3Msps Parallel ADC	±5V Supply, ±2.5V Span, 72dB SINAD
LCT1414	14-Bit, 2.2Msps Parallel ADC	±5V Supply, ±2.5V Span, 78dB SINAD
LTC1420	12-Bit, 10Msps Parallel ADC	5V, Selectable Spans, 71dB SINAD
LTC1604	16-Bit, 333ksps Parallel ADC	±5V Supply, ±2.5V Span, 90dB SINAD
LTC1608	16-Bit, 500ksps Parallel ADC	±5V Supply, ±2.5V Span, 90dB SINAD
LTC1609	16-Bit, 200ksps Serial ADC	5V, Configurable Bipolar/Unipolar Inputs
LTC1864/LTC1865	16-Bit, 250ksps Serial ADCs	5V Supply, 1 and 2 Channel, 4.3mW, MSOP Package
LTC2355-12/LTC2355-14	12-/14-Bit, 3.5Msps Serial ADC	3.3V 14mW, 0V to 2.5V Span, MSOP Package
DACs		
LTC1666/LTC1667/LTC1668	12-/14-/16-Bit, 50Msps DACs	87dB SFDR, 20ns Settling Time
LTC1592	16-Bit, Serial SoftSpan™ I_{OUT} DAC	±1LSB INL/DNL, Software Selectable Spans
References		
LT1790-2.5	Micropower Series Reference in SOT-23	0.05% Initial Accuracy, 10ppm Drift
LT1461-2.5	Precision Voltage Reference	0.04% Initial Accuracy, 3ppm Drift
LT1460-2.5	Micropower Series Voltage Reference	0.075% Initial Accuracy, 10ppm Drift

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