

# R2A20121SP

## Synchronous Phase Shift Full-Bridge Control IC

REJ03D0914-0100

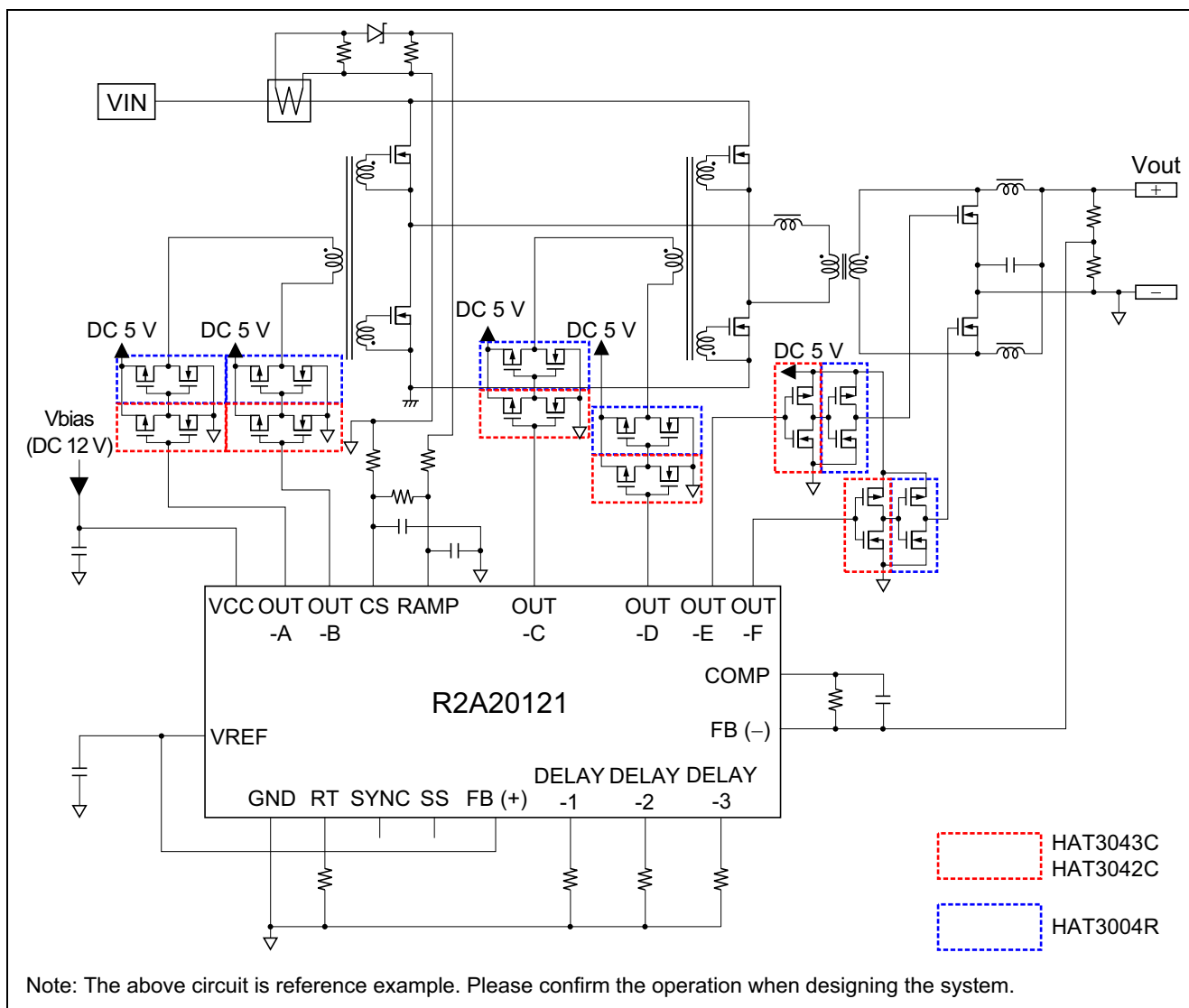
Rev.1.00

Sep 29, 2008

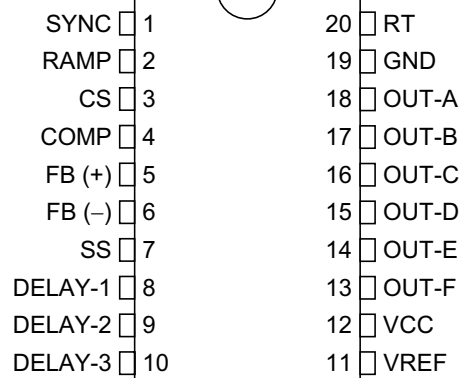
### Features

- High frequency operation; oscillator frequency = 2 MHz Max
- Full-bridge phase-shift switching circuit with adjustable delay times
- Integrated secondary synchronous rectification control with adjustable delay times
- Pulse by pulse current limit
- Package: TSSOP-20

### Illustrative Circuit



## Pin Arrangement

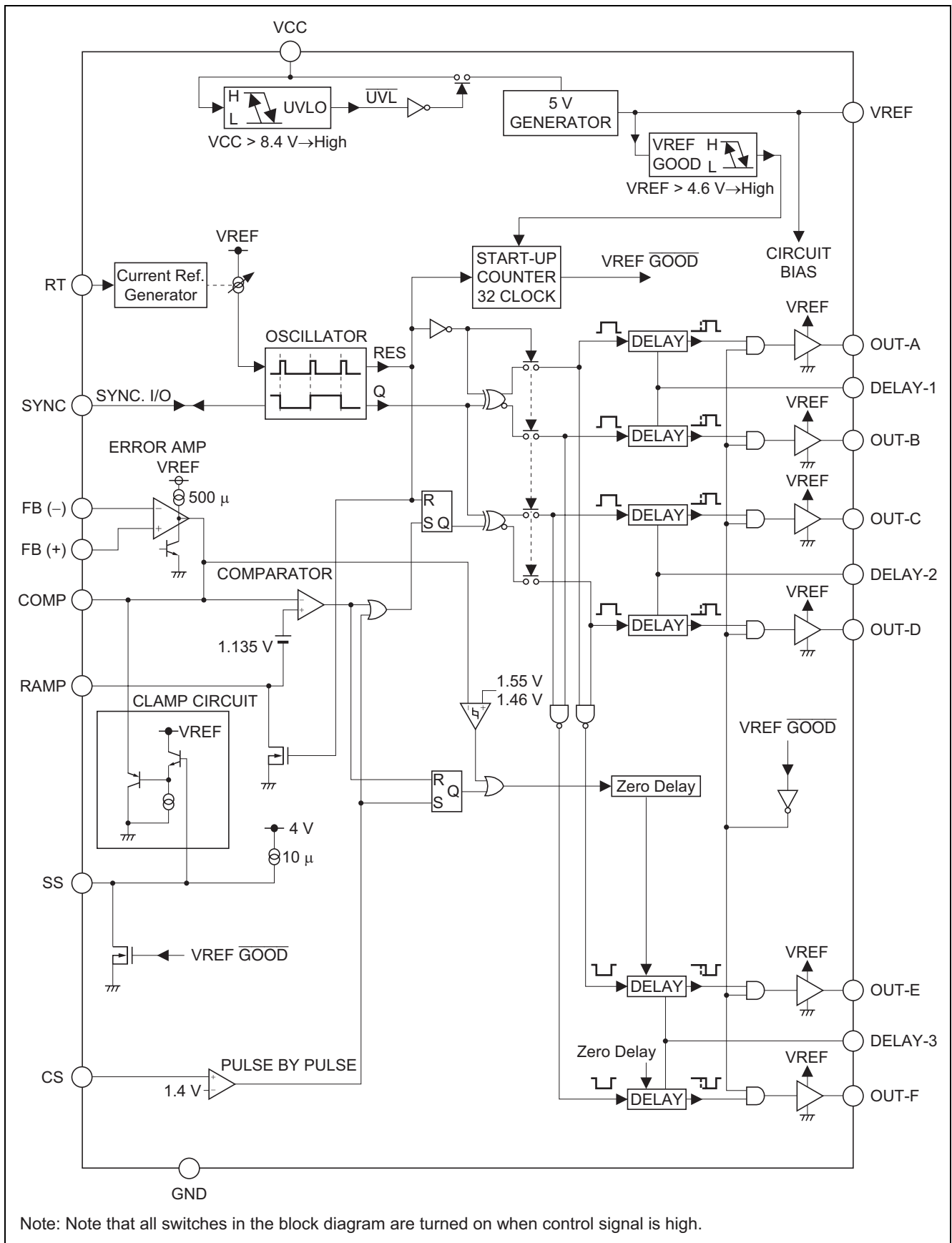


(Top view)

## Pin Functions

Pin No.	Pin Name	Function
1	SYNC	Synchronization I/O for the oscillator
2	RAMP	Current sense signal input for the full-bridge control loop
3	CS	Current sense signal input for OCP
4	COMP	Error amplifier output
5	FB (+)	Error amplifier plus input
6	FB (-)	Error amplifier minus input
7	SS	Timing capacitor for soft-start
8	DELAY-1	Delay time adjustor for the full-bridge control signal (OUT-A and B)
9	DELAY-2	Delay time adjustor for the full-bridge control signal (OUT-C and D)
10	DELAY-3	Delay time adjustor for the secondary control signal (OUT-E and F)
11	VREF	5 V/20 mA Output
12	VCC	IC power supply input
13	OUT-F	Secondary control signal
14	OUT-E	Secondary control signal
15	OUT-D	Full-bridge control signal
16	OUT-C	Full-bridge control signal
17	OUT-B	Full-bridge control signal
18	OUT-A	Full-bridge control signal
19	GND	Ground level for the IC
20	RT	Timing resistor for the oscillator

## Block Diagram



## Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Ratings	Unit	Notes
Power supply voltage	Vcc	20	V	1
Peak output current	Ip <sub>k-out</sub>	±50	mA	2, 3
DC output current	Id <sub>c-out</sub>	±5	mA	3
VREF output current	I <sub>ref-out</sub>	−20	mA	3
COMP sink current	I <sub>sink-comp</sub>	2	mA	3
DELAY set current	I <sub>set-delay</sub>	0.3	mA	3
RT set current	I <sub>set-rt</sub>	0.3	mA	3
VREF terminal voltage	V <sub>ter-ref</sub>	−0.3 to 6	V	1, 4
Terminal group 1 voltage	V <sub>ter-1</sub>	−0.3 to (V <sub>ref</sub> + 0.3)	V	1, 5
Operating junction temperature	T <sub>j-opr</sub>	−40 to +125	°C	6
Storage temperature	T <sub>stg</sub>	−55 to +150	°C	

- Notes:
1. Rated voltages are with reference to the GND pin.
  2. Shows the transient current when driving a capacitive load.
  3. For rated currents, inflow to the IC is indicated by (+), and outflow by (−).
  4. VREF pin voltage must not exceed VCC pin voltage.
  5. Terminal group 1 is defined the pins;  
CS, RAMP, COMP, FB (+), FB (−), SS, RT, SYNC, DELAY-1 to 3, OUT-A to F
  6.  $\theta_{ja}$ ; 228°C/W  
Board condition; Glass epoxy 55 mm × 45 mm × 1.6 mm, 10% wiring density.

## Electrical Characteristics

(Ta = 25°C, Vcc = 12 V, RT = 33 kΩ, Rdelay = 51 kΩ, unless otherwise specified.)

	Item	Symbol	Min	Typ	Max	Unit	Test Conditions
SUPPLY	Start threshold	VH	7.7	8.4	9.1	V	
	Shutdown threshold	VL	7.4	8.0	8.6	V	
	UVLO hysteresis	dVUVL	0.3	0.4	0.5	V	
	Start-up current	Is	—	90	150	μA	Vcc = 7.5 V
	Operating current	Icc	—	7	10	mA	No load on VREF pin
VREF	Output voltage	Vref	4.9	5.0	5.1	V	
	Line regulation	Vref-line	—	0	10	mV	Vcc = 10 V to 16 V
	Load regulation	Vref-load	—	6	20	mV	Iref = -1 mA to -20 mA
	Temperature stability	dVref/dTa	—	±80 * <sup>1</sup>	—	ppm/°C	Ta = -40 to 105°C
OSCILLATOR	Oscillator frequency	fosc	—	960 * <sup>1</sup>	—	kHz	
	Switching frequency	fsw	412	480	547	kHz	Measured on OUT-A, -B
	Line stability	fsw-line	-1.5	0	1.5	%	Vcc = 10 V to 16 V
	Temperature stability	dfsw/dTa	—	±0.1 * <sup>1</sup>	—	%/°C	Ta = -40 to 105°C
	RT voltage	VRT	2.5	2.7	2.9	V	
SYNC	Input threshold	VTH-SYNC	2.5	2.85	3.2	V	
	Output high	VOH-SYNC	3.5	4.0	—	V	RSYNC = 33 kΩ to GND
	Output low	VOL-SYNC	—	0.05	0.15	V	RSYNC = 33kΩ to VREF
	Minimum input pulse	TI-MIN	50	—	—	ns	
	Output pulse width	TO-SYNC	—	500	—	ns	

Note: 1. Reference values for design. Not 100% tested in production.

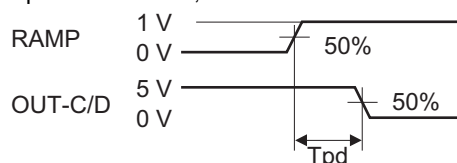
## Electrical Characteristics (cont.)

(Ta = 25°C, Vcc = 12 V, RT = 33 k, Rdelay = 51 k, unless otherwise specified.)

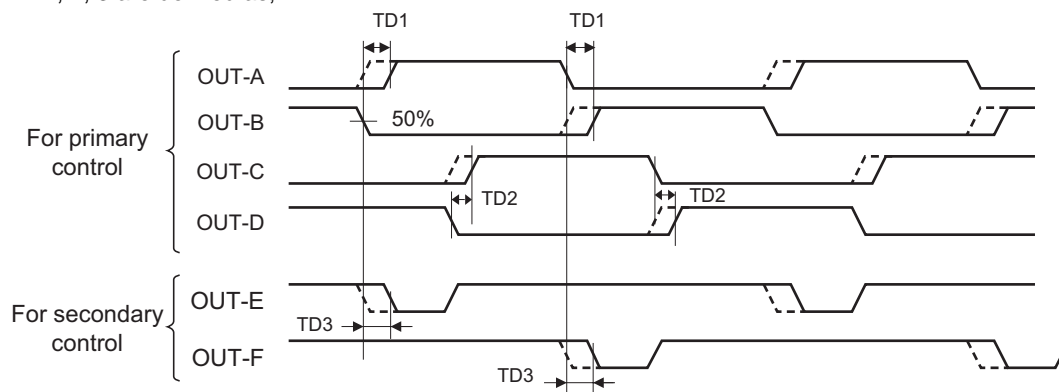
	Item	Symbol	Min	Typ	Max	Unit	Test Conditions
ERROR AMPLIFIER	Input offset voltage	Vos	-2	3	8	mV	FB (-) and COMP are shorted. VFB (+) = 1.25 V
	FB (+) input current	IFB (+)	-2.0	0	2.0	μA	FB (+) = FB (-) = 1.25 V
	FB (-) input current	IFB (-)	-2.0	0	2.0	μA	FB (+) = FB (-) = 1.25 V
	Open-loop DC gain	Av	—	80 * <sup>1</sup>	—	dB	
	Unity gain bandwidth	BW	—	2 * <sup>1</sup>	—	MHz	
	Output source current	ISOURCE	-650	-500	-390	μA	FB (+) = 1.25 V, FB (-) = 0.75 V, COMP = 2 V
	Output sink current	ISINK	2.0	6.5	—	mA	FB (+) = 1.25 V, FB (-) = 1.75 V, COMP = 2 V
	Output high voltage	VOH-EO	3.7	3.9	—	V	FB (+) = 1.25 V, FB (-) = 0.75 V, COMP; Open
	Output low voltage	VOL-EO	—	0.1	0.4	V	FB (+) = 1.25 V, FB (-) = 1.75 V, COMP; Open
	Output clamp voltage * <sup>4</sup>	VCLAMP-EO	-0.16	-0.07	0.0	V	FB (+) = 1.25 V, FB (-) = 0.75 V, COMP; Open, SS = 1 V
PHASE MODULATOR	RAMP offset voltage	VRAMP	1.035	1.135	1.235	V	
	RAMP bias current	IRAMP	-5	-0.8	5	μA	RAMP = 0.3 V
	RAMP sink current * <sup>1</sup>	ISINK-RAMP	8	26	—	mA	RAMP = 1 V, COMP = 0 V
	Minimum phase shift	Dmin	—	0 * <sup>1</sup> * <sup>5</sup>	—	%	RAMP = 1 V, COMP = 0 V
	Maximum phase shift	Dmax	—	97.0 * <sup>1</sup> * <sup>5</sup>	—	%	RAMP = 0 V, COMP = 2.1 V
	Delay to OUT-C, -D * <sup>2</sup>	Tpd	—	30	60	ns	COMP = 1.6 V
	RAMP discharge time * <sup>1</sup>	Tdis	40	80	120	ns	
DELAY	DELAY-1, -2, -3 * <sup>3</sup>	TD1, 2, 3	22	33.5	45	ns	Delay set R = 51 k
	DELAY2-1, -2, -3 * <sup>1</sup> * <sup>3</sup>	TD2_1, _2, _3	70	100	130	ns	Delay set R = 180 k
	Terminal voltage	VD1, 2, 3	1.9	2.0	2.1	V	Delay set R = 51 k

Notes: 1. Reference values for design. Not 100% tested in production.

2. Tpd is defined as;



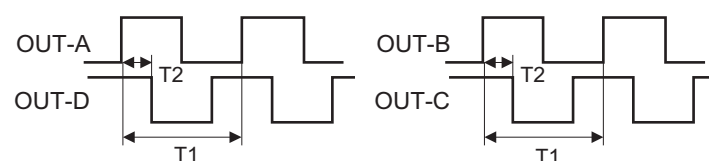
3. TD1, 2, 3 are defined as;



4. VCLAMP-EO = VCOMP - SS voltage (1 V)

5. Maximum/Minimum phase shift is defined as;

$$D = \frac{T_2}{T_1} \times 2 \times 100 \text{ (%)}$$



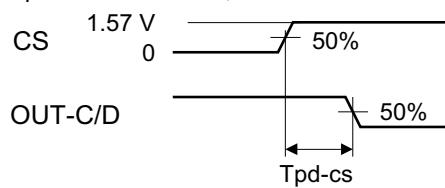
## Electrical Characteristics (cont.)

(Ta = 25°C, Vcc = 12 V, RT = 33 k, Rdelay = 51 k, unless otherwise specified.)

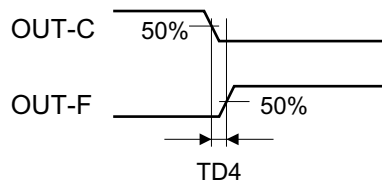
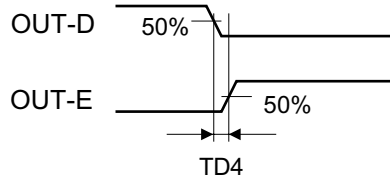
	Item	Symbol	Min	Typ	Max	Unit	Test Conditions
SOFT START	Source current	ISS	-14	-10	-6	μA	SS = 1 V
	SS high voltage	VOH-SS	3.9	4.0	4.1	V	
OVER CURRENT PROTECTION	Pulse-by-pulse current limit threshold	VCS-PP	1.26	1.4	1.54	V	
	Delay to OUT pins * <sup>2</sup>	Tpd-cs	—	40	80	ns	CS = 0 V to 1.57 V
OUTPUT	High voltage	VOH-OUT	4.3	4.8	—	V	IOUT = -5 mA
	Low voltage	VOL-OUT	—	0.1	0.4	V	IOUT = 5 mA
	Rise time	tr	—	5	15	ns	COUT = 33 pF
	Fall time	tf	—	5	15	ns	COUT = 33 pF
	Timing offset * <sup>3</sup>	TD4	—	3	20	ns	

Notes: 1. Reference values for design. Not 100% tested in production.

2. Tpd-cs is defined as;



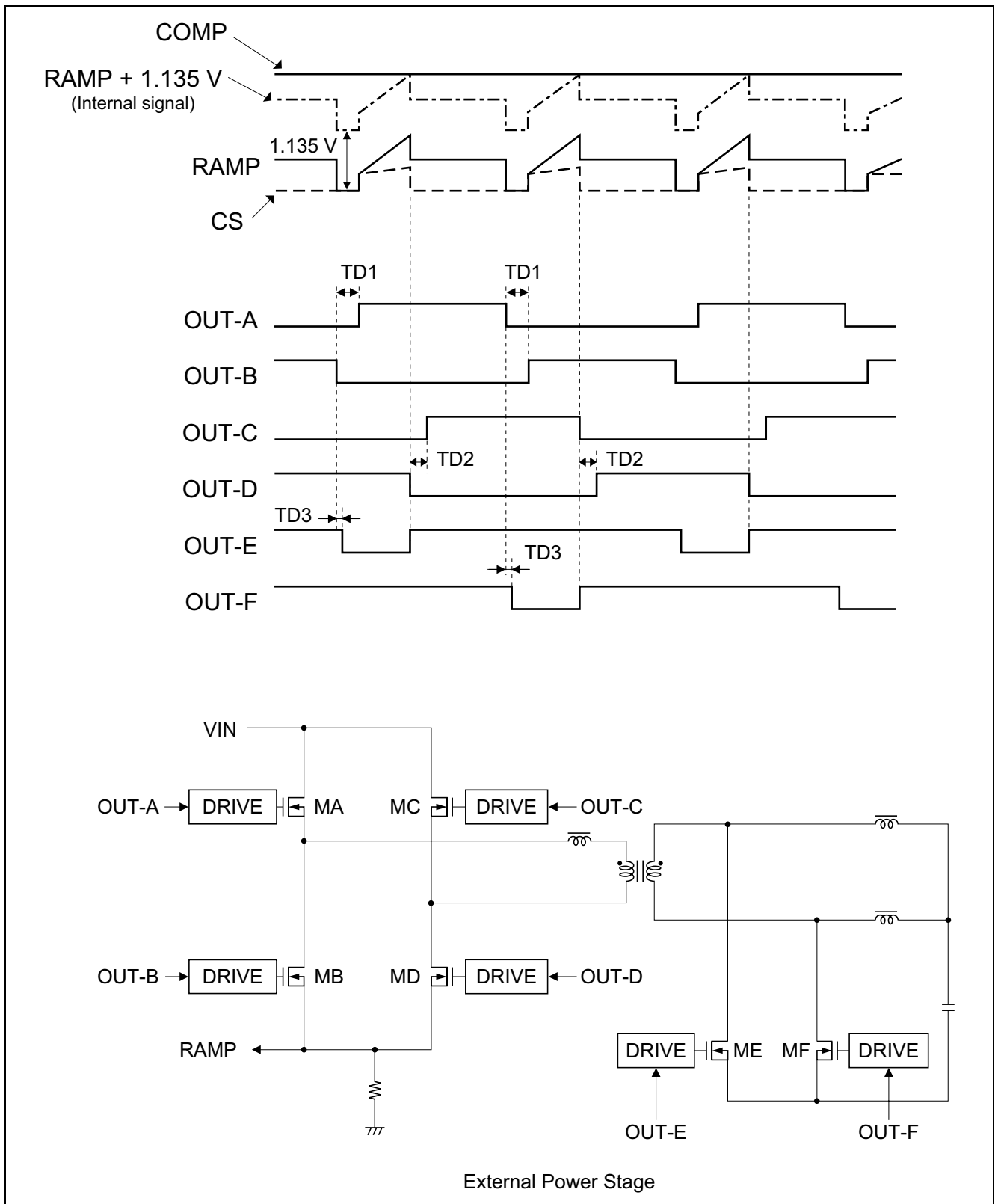
3. TD4 is defined as;



## Timing Diagram

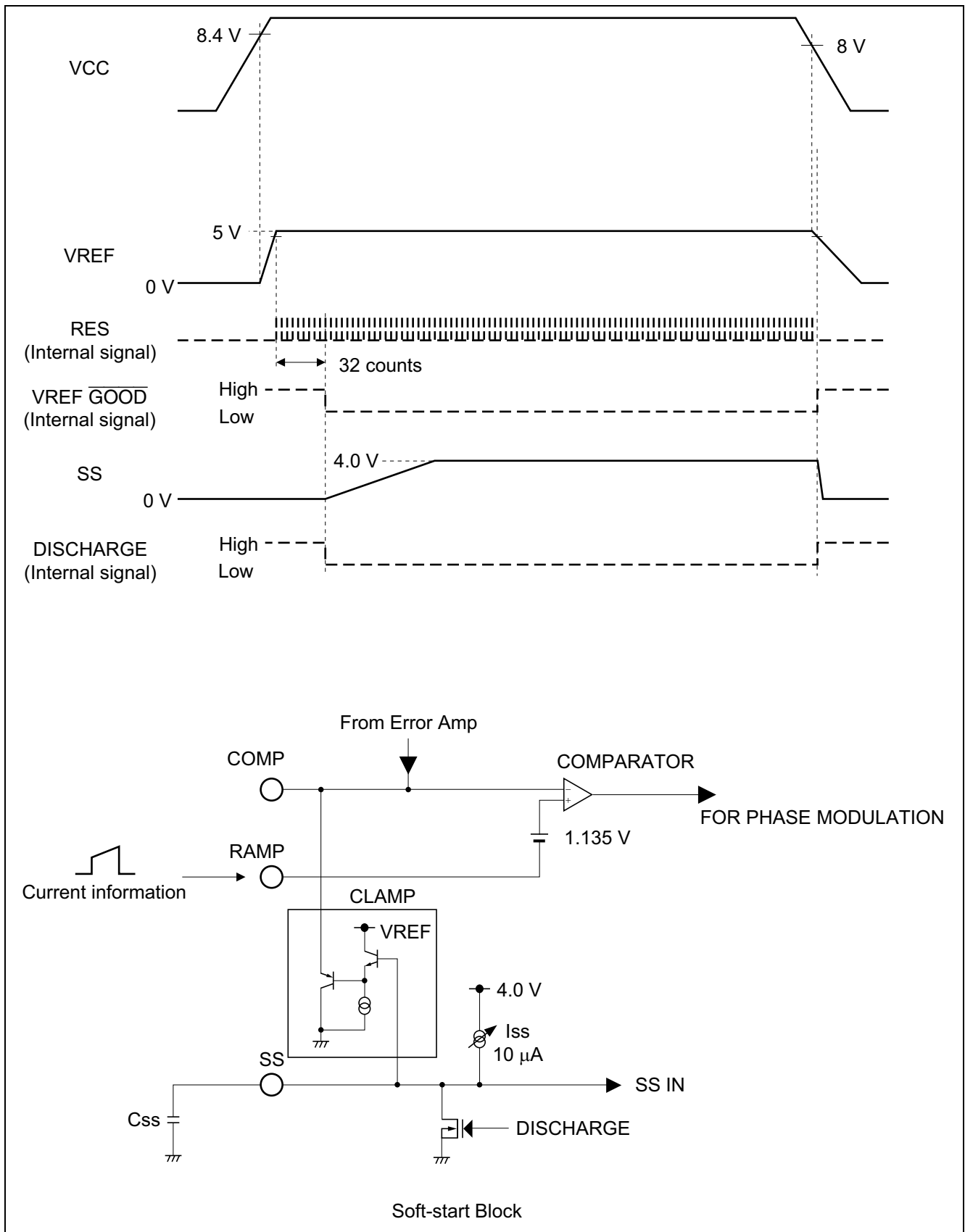
Note: All voltage, current, time shown in the diagram is typical value.

### Full Bridge and Secondary Control





## Start-up and Shutdown



## Functional Description

Note: All voltage, current, time shown in the diagram is typical value unless otherwise noted.

### UVLO

UVLO (Under Voltage Lockout Operation) is a function that halts operation of the IC in the event of a low IC power supply voltage. When IC operation is halted, the 5 V internal voltage generation circuit (VREF) halts, and therefore operation of circuitry using VREF as the operating power supply halts.

Circuit blocks other than UVLO use VREF as their operating power supply. Therefore, the power supply current of the IC becomes equal to the current dissipated by the UVLO circuit. The following graphs show the relationship between the VCC input current and VCC input voltage, and between VREF and the VCC input voltage.

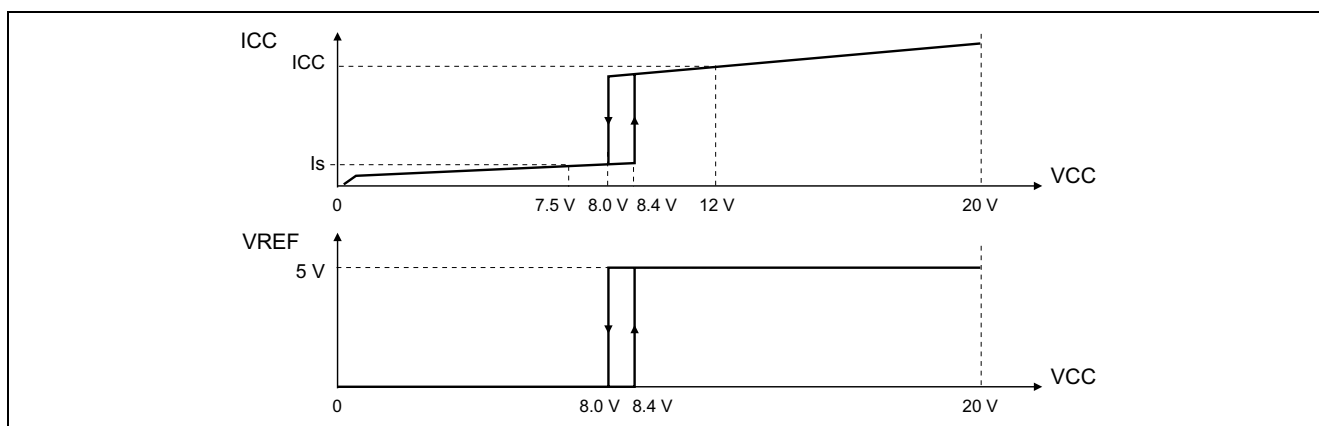


Figure 1

### Start-up Counter

When the  $\overline{\text{VREFGOOD}}$  signal (internal signal) goes to the logic low level, the R2A20121 starts operating as a controller. The  $\overline{\text{VREFGOOD}}$  signal is created from VREFGOOD circuit output via a 32-clock startup counter.

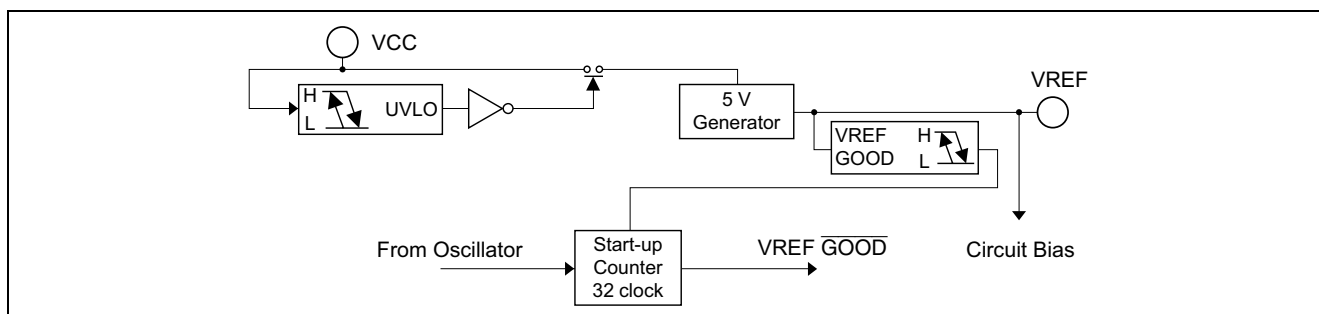


Figure 2

Therefore, the start of IC operation is a 32-count later than UVLO release. When the oscillator frequency is set to 1 MHz, this represents a delay of 32  $\mu\text{s}$ . This delay enables operation to be halted until VREF (5 V) stabilizes when UVLO is released. Note that the start-up counter operates when VREF rises is performed, but does not operate when VREF falls is performed (there is no logic delay due to the start-up counter).

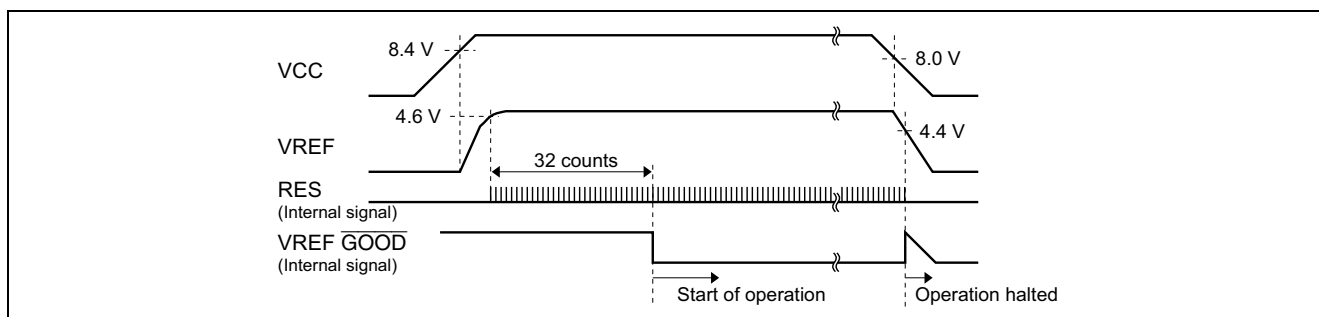


Figure 3

## Oscillator

The oscillation frequency of the oscillator is set by means of a resistance connected between the RT pin and GND. The following graph shows the relationship between the external resistance and the oscillation frequency. The typical value of the oscillation frequency is given by the following equation.

$$f_{osc} = \frac{1}{25 \text{ [pF]} \times RT \text{ [\Omega]} + 150 \text{ [ns]}} \quad [\text{Hz}]$$

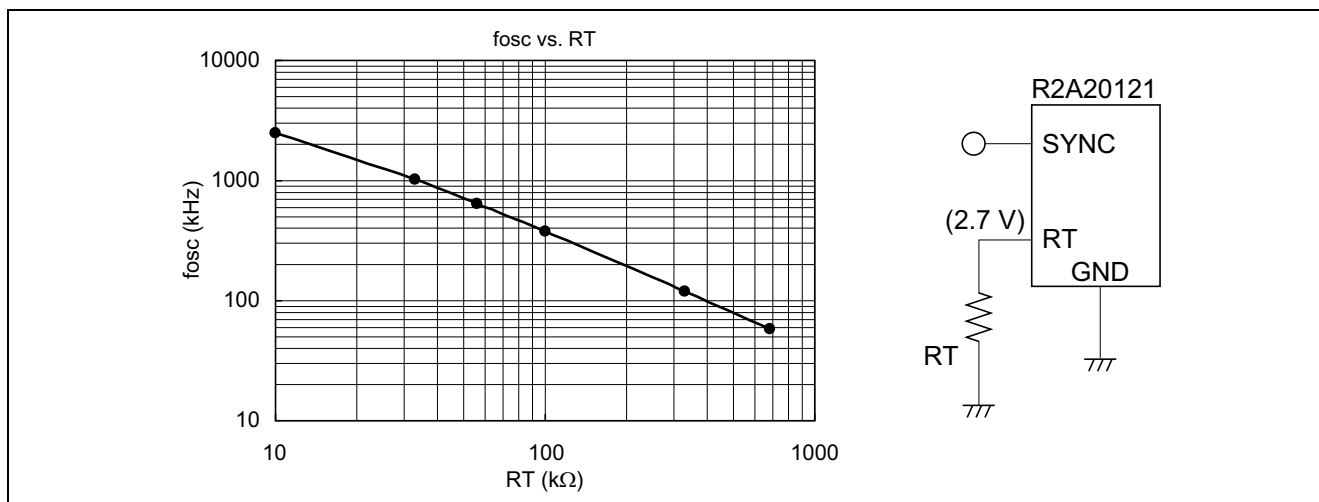


Figure 4

Place the resistor for connection to the RT pin as close to the pin as is possible. Please design the pattern so that the level of cross-talk from other signals is minimized.

## Synchronized Operation

Parallel synchronized operation is possible by connecting the SYNC pins of R2A20121s. In this case, up to four slave ICs can be connected to one master IC. A value of at least twice the master RT value should be set for the slave IC RT values.

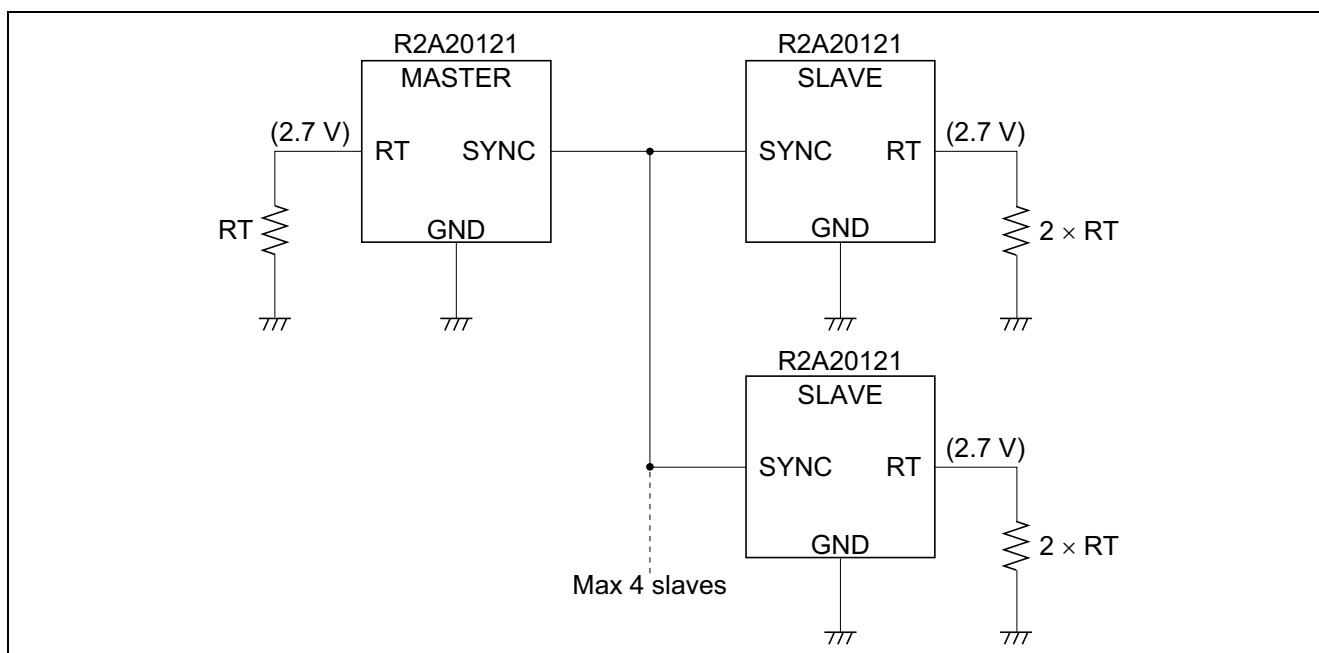


Figure 5 Parallel Synchronized Operation

External synchronized operation is possible by supplying a synchronization signal to the SYNC pins of R2A20121s. In this case, a frequency not exceeding 1/2 that of the master clock should be set for the R2A20121s.

A maximum master clock frequency of 2 MHz should be used. See the figure below for the input waveform conditions.

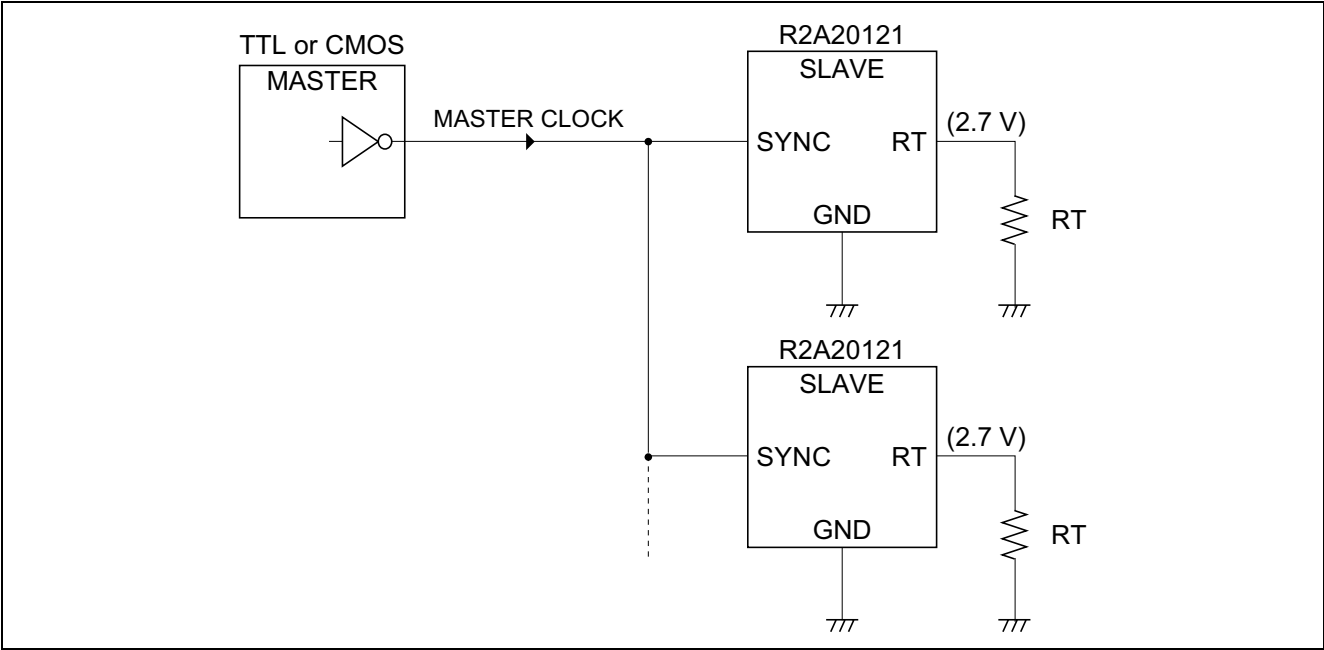


Figure 6 External Synchronized Operation

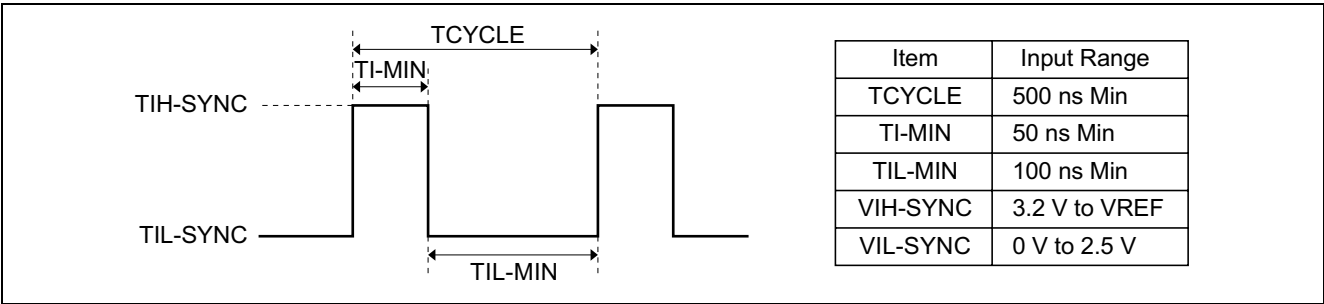


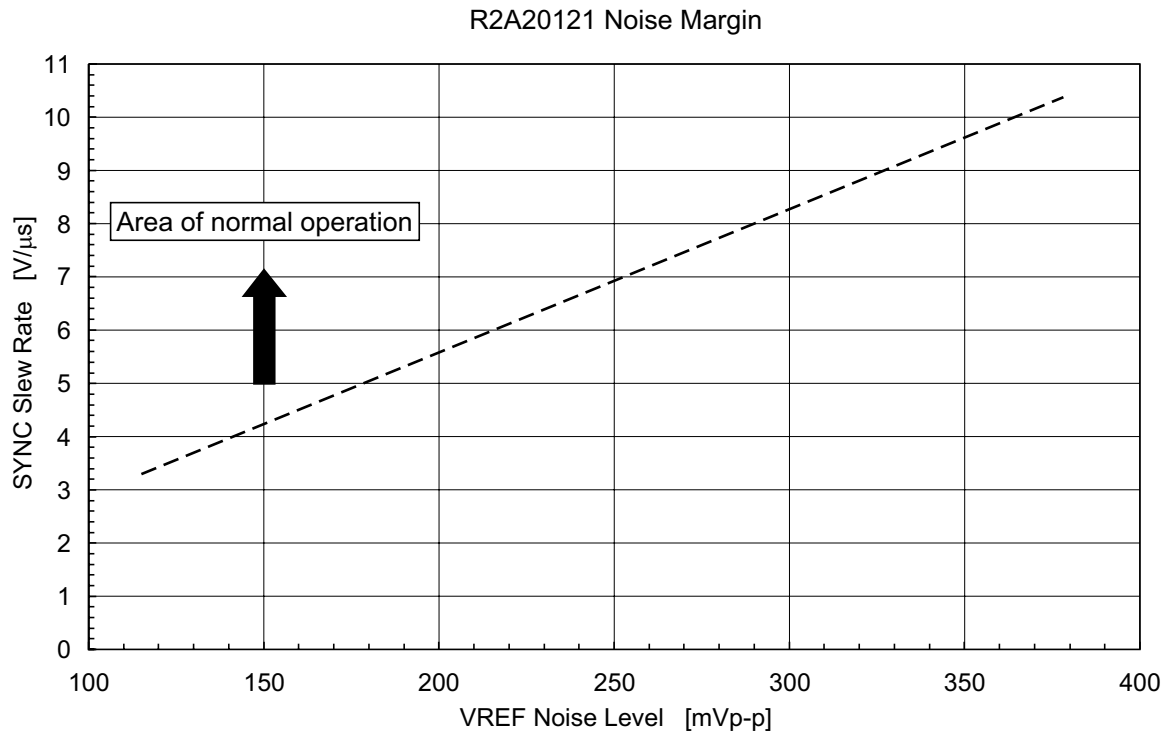
Figure 7 SYNC Pin Input Conditions

## Noise Margin

When a synchronization signal is given to an SYNC terminal of the R2A20121, the oscillation frequency of the IC may occur abnormality by the slew rate of the synchronization signal and the noise level of the VREF terminal.

The following graph shows the relationship between the slew rate of the synchronization signal and the VREF noise level.

In the case of synchronized operation, a VREF capacitor should be chosen with reference to the following graph.

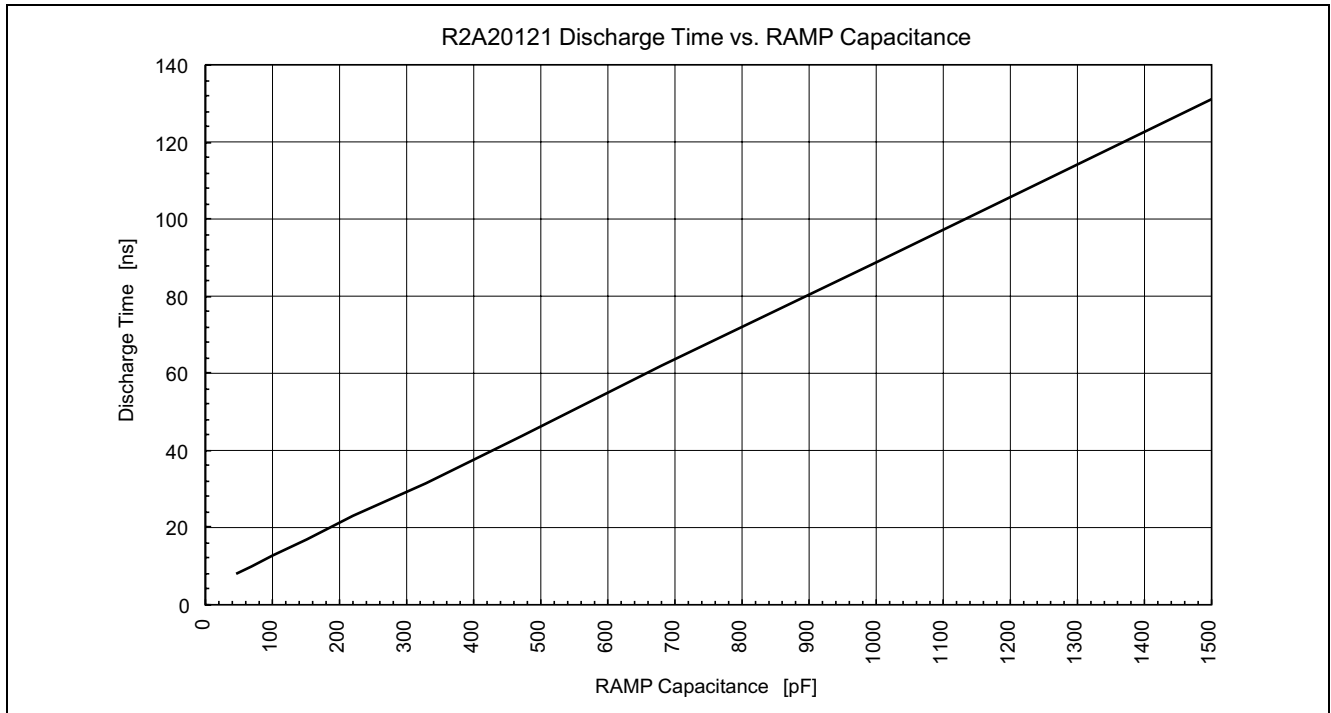


Note: The upper graph is a measurement result by our evaluation jig.  
Please confirm enough evaluation because the influence of the noise is different with each board.

### RAMP Capacitance Setting Method

The following graph shows the relationship between the RAMP capacitance and discharge time.

A RAMP capacitance should be chosen with reference to the following graph.



## Synchronous Phase Shift Full-Bridge Control

The R2A20121 is provided with full-bridge control outputs OUT-A through OUT-D, and secondary-side synchronous rectification control outputs OUT-E and OUT-F. ZVS (Zero Voltage Switching) can be performed by adjusting timing delays TD1 and TD2 between the OUT-A through OUT-D outputs by means of an external resistance. OUT-E and OUT-F have an output timing suitable for secondary-side full-wave rectification, and so can be used in either current doubler or center tap applications. The following figure shows full-bridge ZVS + current doubler operation using an ideal model.

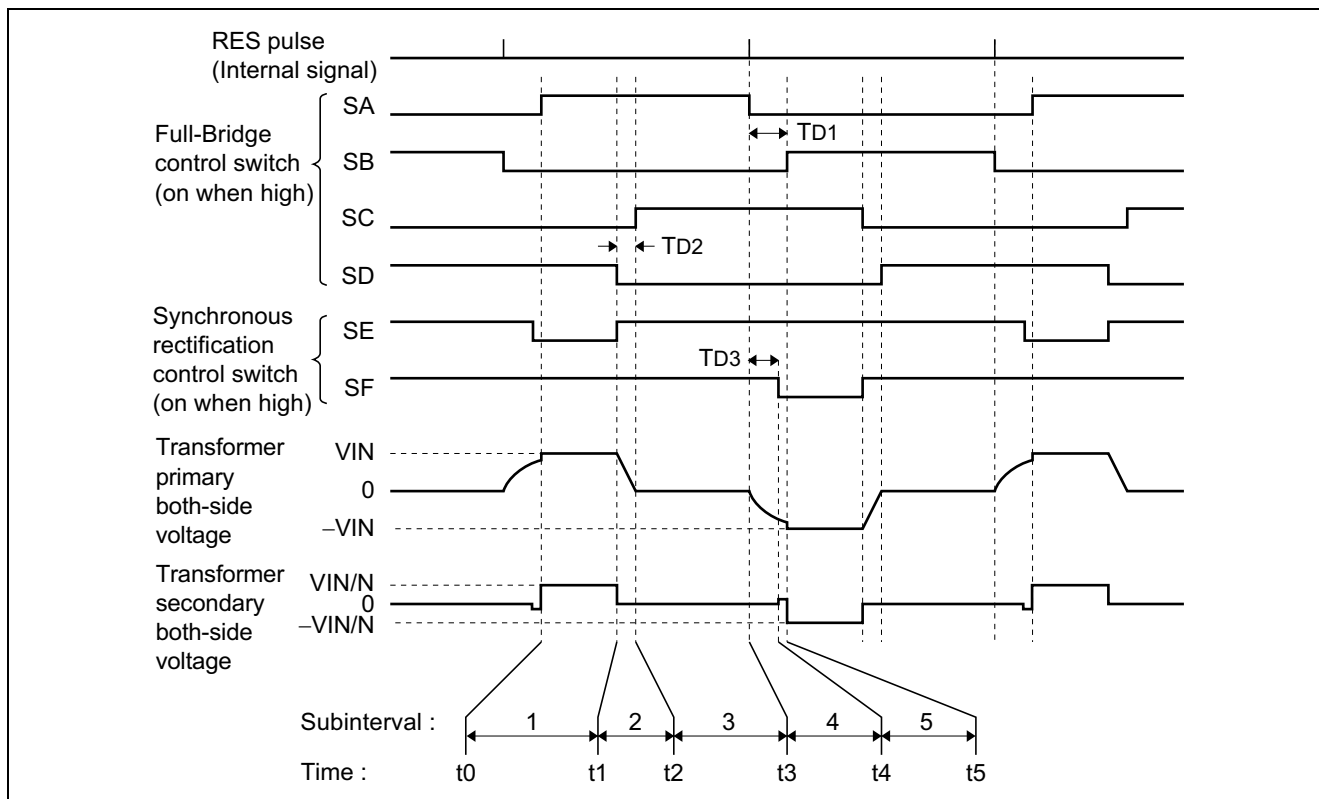
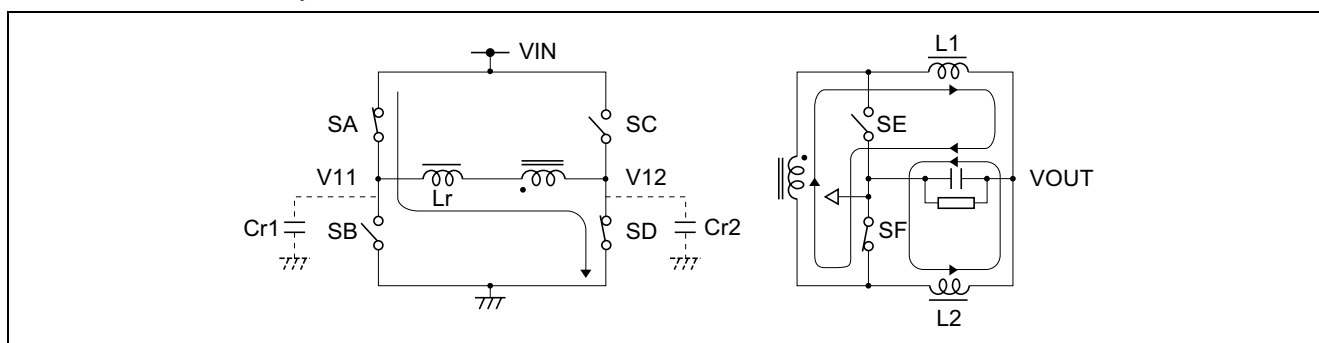


Figure 8

- Subinterval: 1

In interval 1, SA and SD are turned on, and  $V_{IN}$  is generated on the transformer primary side. On the transformer secondary side, a value proportional to the winding ratio is generated, and the primary-side power is transmitted to the load side.

At this time, secondary-side switch SE is off and SF is on.



Subinterval: 1

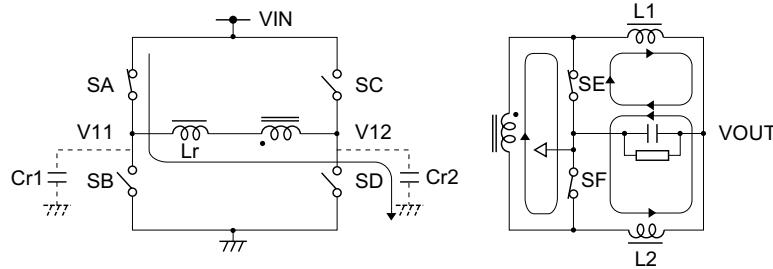
- Subinterval: 2

As SD is turned off at point t1, the primary-side current flows into resonant capacitance Cr2. At this time Cr2 is charged, and therefore the potential of V12 rises. Considering that the exciting current and the L1 and L2 ripple currents are considerable smaller than Io, the following is an approximate equation for the slope of V12.

$$\frac{dV_{12}}{dt} = \frac{0.5 I_o}{N} \cdot \frac{1}{Cr2} \quad [V/s] \quad \dots\dots\dots (1)$$

Here, N is the ratio of the primary coil to the secondary coil ( $N = N_1/N_2$ ), and Io is the output current.

As SE and SF are on, the transformer secondary side is in the shorted state, and the value of the current flowing up to that time is retained.



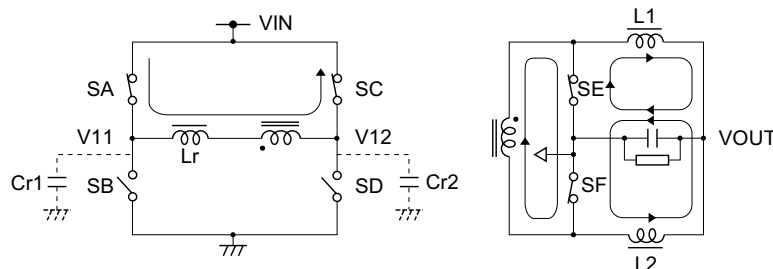
Subinterval: 2

- Subinterval: 3

SC is turned on at point t2. ZVS operation can be attained by setting the SD off (t1) → SC on (t2) delay to the optimal value. This delay time can be expressed by equation (2).

$$TD2 = \frac{N}{0.5 I_o} \cdot Cr2 \cdot VIN \quad [s] \quad \dots\dots\dots (2)$$

After SC is turned on, the transformer primary side is in the shorted state, and therefore the current value immediately after SC was turned on is retained.

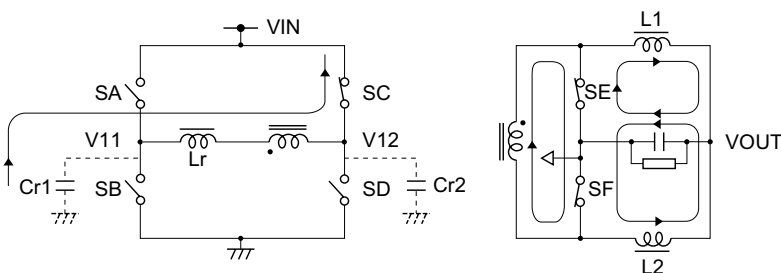


Subinterval: 3

- Subinterval: 4

As SA is turned off at point t3, the primary-side current discharges resonant capacitance Cr1, and the potential of V11 falls. A negative potential is applied to resonant inductor Lr, and a flux reset starts. At this time, since the series resonance circuit is composed of Cr1 and Lr, the V11 waveform changes to a sine wave. The resonance frequency is given by equation (3).

$$f_r = \frac{1}{2\pi\sqrt{Cr1 \cdot Lr}} \quad [Hz] \quad \dots\dots\dots (3)$$



Subinterval: 4



- Subinterval: 5

When synchronous switch SF is turned off at point t4, the current flowing in SF up to that time continues to flow through the SF body diode. SF turn-off must be performed before completion of the resonant inductor Lr flux reset. If SF is not off on completion of the Lr flux reset, power transmission will be performed with the transformer secondary-side shorted, and therefore an excessive current will flow in the transformer primary and secondary sides, and parts may be damaged.

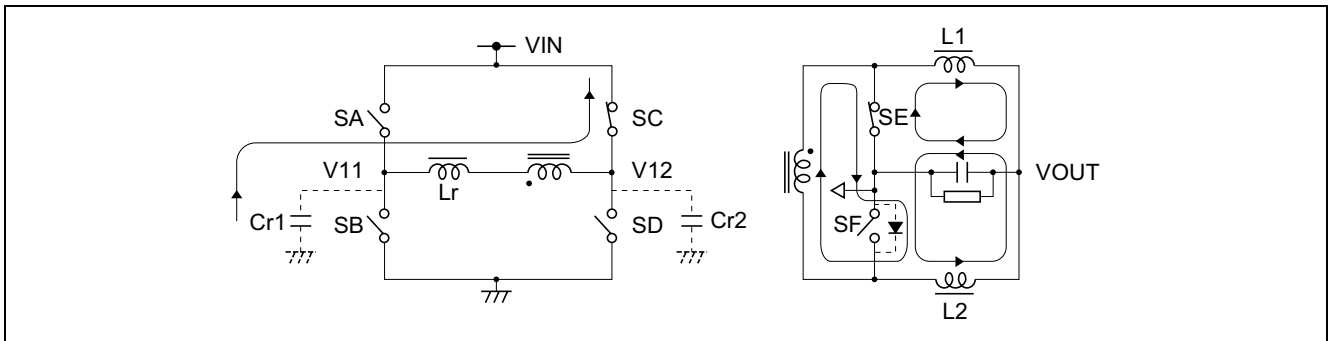
Also, if the SF body diode is on for a long period, loss will be high. Therefore, optimal timing should be set by means of the R2A20121's delay adjustment pin, DELAY-3.

Lr reset time tr is given by equation (4) when the resonance voltage peak value is within the input voltage.

$$\begin{aligned} T_{\text{reset}}(L_r) \mid v_{pp} \leq V_{IN} &= \frac{1}{4} \cdot \frac{1}{f_r} \\ &= 0.5 \pi \sqrt{L_r \cdot C r_1} \quad [\text{s}] \dots\dots\dots (4) \end{aligned}$$

Here, vpp is the resonance voltage peak value.

$$v_{pp} = \frac{I_o}{2} \cdot \frac{1}{N} \cdot \sqrt{L_r / C r_1} \quad [\text{V}] \dots\dots\dots (5)$$

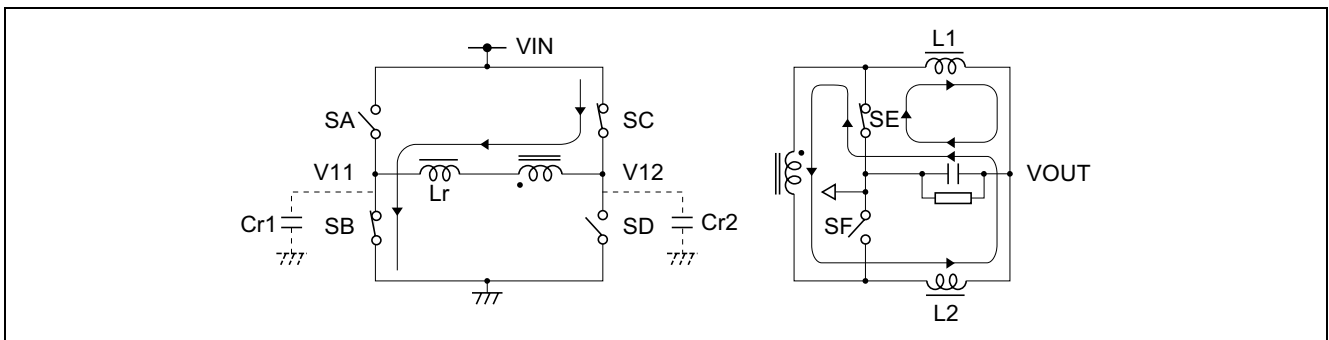


**Subinterval: 5**

- Time: t5

SB is turned on at point t5. The SB switching loss can be minimized by turning on SB when the SB both-side voltages are at a minimum (when the resonance voltage is at a peak). The SB turn-on timing can be set with TD1 of the R2A20121. The time when the resonance voltage is at a peak is given by equation (4).

From t5 onward, operation is on the same principle as in Subinterval 1 through Subinterval 5.



**Time: t5**

## Delay Setting

Inter-output delays (TD1, TD2, TD3) are set by means of a resistance connected between the DELAY-1 (-2, -3) pin and GND. The following graph shows the relationship between the external resistance and delay. The typical value of the delay set time is given by the following equation.

$$TD = 0.5 \text{ [pF]} \times RD \text{ [\Omega]} + 8 \text{ [ns]} \quad [\text{s}]$$

When the RD value is small, the set time will be larger than the above calculated value due to the effect of internal delay, etc., and therefore a constant setting should be made with reference to the following graph.

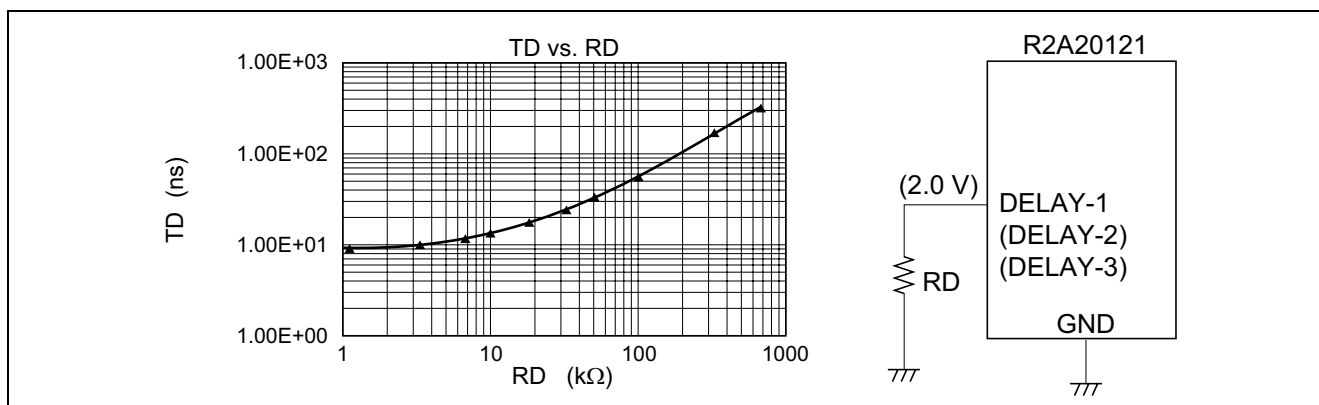


Figure 9

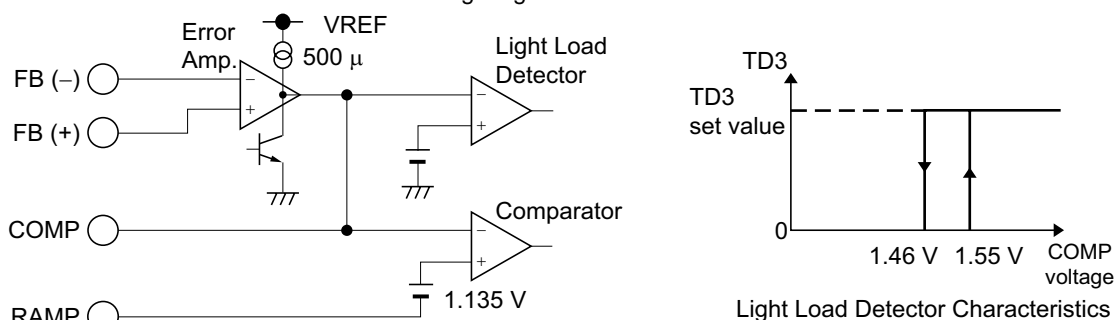
Place the resistor for connection to the DELAY-1,2,3 pin as close to the pin as is possible. Please design the pattern so that the level of cross-talk from other signals is minimized.

## DELAY-3 (TD3)

There is a condition that secondary-side control output OUT-E and OUT-F delay TD3 is 0 s (typical) in order to prevent shorting of the transformer secondary side. The relationship between TD3 and the IC operating state is shown in the following table.

Mode	Definition	Operation of OUT-E, OUT-F	Notes
Light load	COMP < 1.55 V	TD3 = 0	1, 3
Pulse by pulse OCL	CS ≥ 1.4 V	TD3 = 0	2, 3

Notes: 1. Light-load detection is performed by means of the error amplifier output voltage. Light-load detection characteristics are as shown in the following diagram.



- TD3 of the next OUT-E or OUT-F after the pulse-by-pulse current limiter (PBP OCL) operates is 0 s (typical). When OUT-C and OUT-D are subsequently inverted by the Phase Shift Comparator, not the PBP OCL, TD3 is restored to the value set by means of the DELAY-3 pin.
- If once the SS terminal is not exceed 3.9 V after an IC started, the IC continues maintaining a state in TD3 = 0. When an external part is attached to the SS terminal, please be careful.

## Application

Note: All voltage, current, time shown in the diagram are typical value.

Sample application circuits are given here. Confirmatory experiments should be carried out when applying these examples to products.

## Slope Compensation

In order to improve the unstable operation characteristic of current mode, voltage slopes in a current sense signal can be superimposed. The following is a possible slope compensation method.

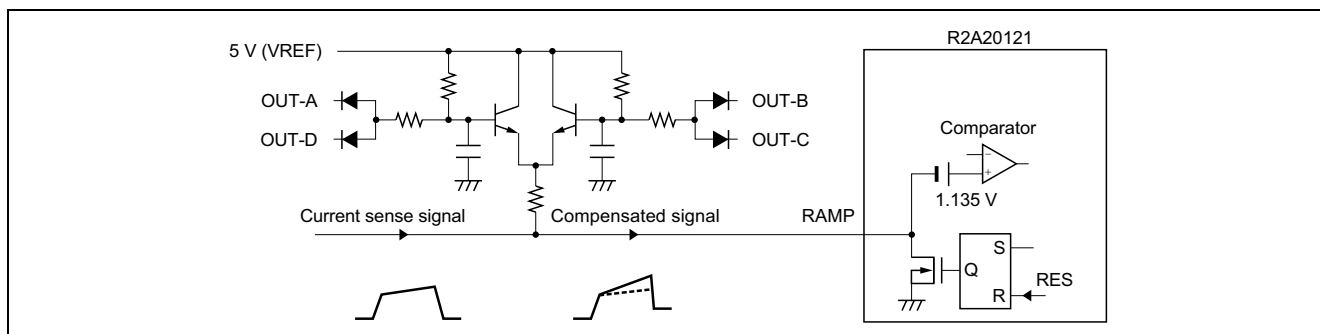


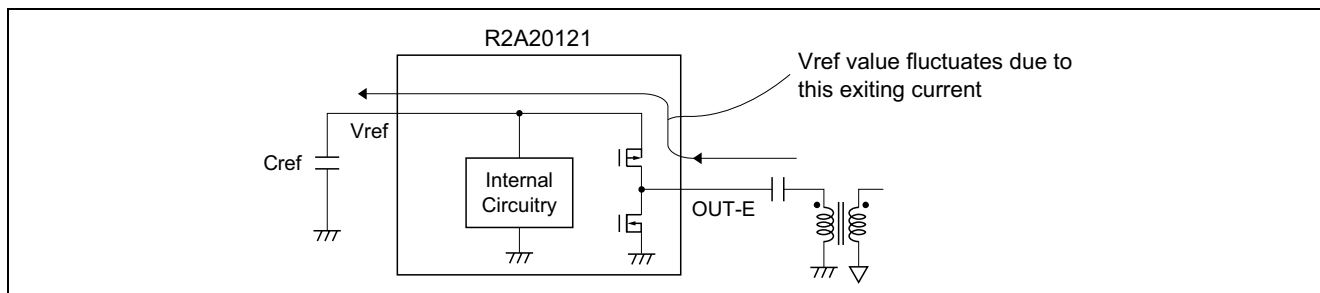
Figure 10

## Driving a Pulse Transformer

OUT-A through OUT-F of this IC are CMOS outputs that use Vref as their power supply. When directly driving a pulse transformer, the Vref voltage fluctuates according to the exciting current. As Vref fluctuation may make internal circuit operation unstable, direct drive of a pulse transformer should be avoided.

- Case 1 (NG)

The figure below shows a case where a pulse transformer is driven directly. Vref voltage fluctuation occurs due to the exciting current.

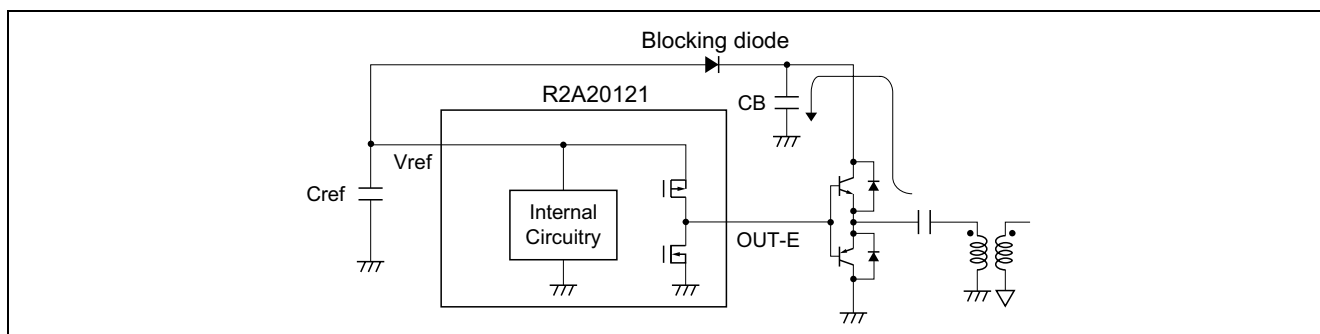


Case 1 (NG)

- Case 2

The figure below shows an example in which a current amplifier is added by means of transistors. A reverse current due to the exciting current is prevented by a blocking diode, and therefore capacitance CB is charged. In this way, fluctuation of the Cref potential is suppressed and stable operation can be achieved.

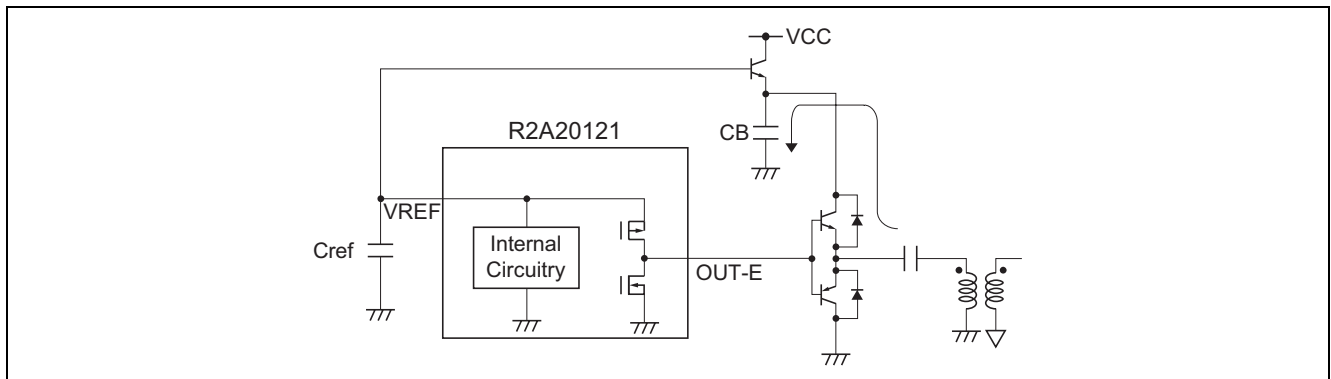
As well as a buffer implemented by means of a transistor, standard logic IC or buffer IC connection is also possible. The buffer circuit power supply method should be implemented in the same way.



Case 2

- Case 3

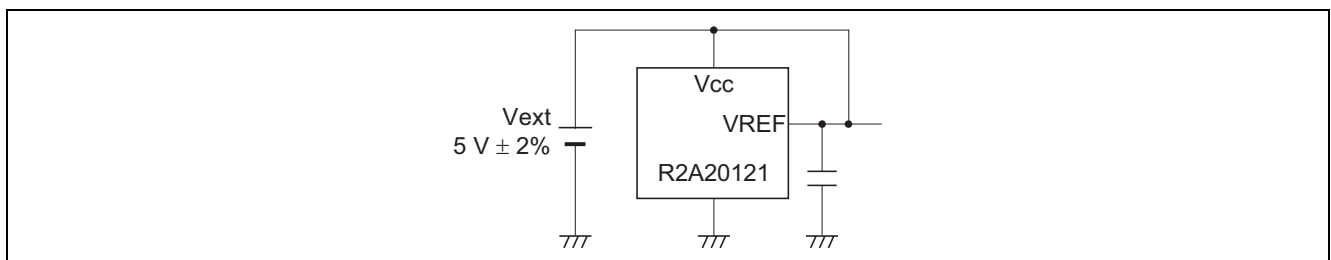
The figure below shows an example of a drive power supply method using emitter following. For the same reason as described above, fluctuation of the Cref potential is suppressed and stable operation can be achieved.



**Case 3**

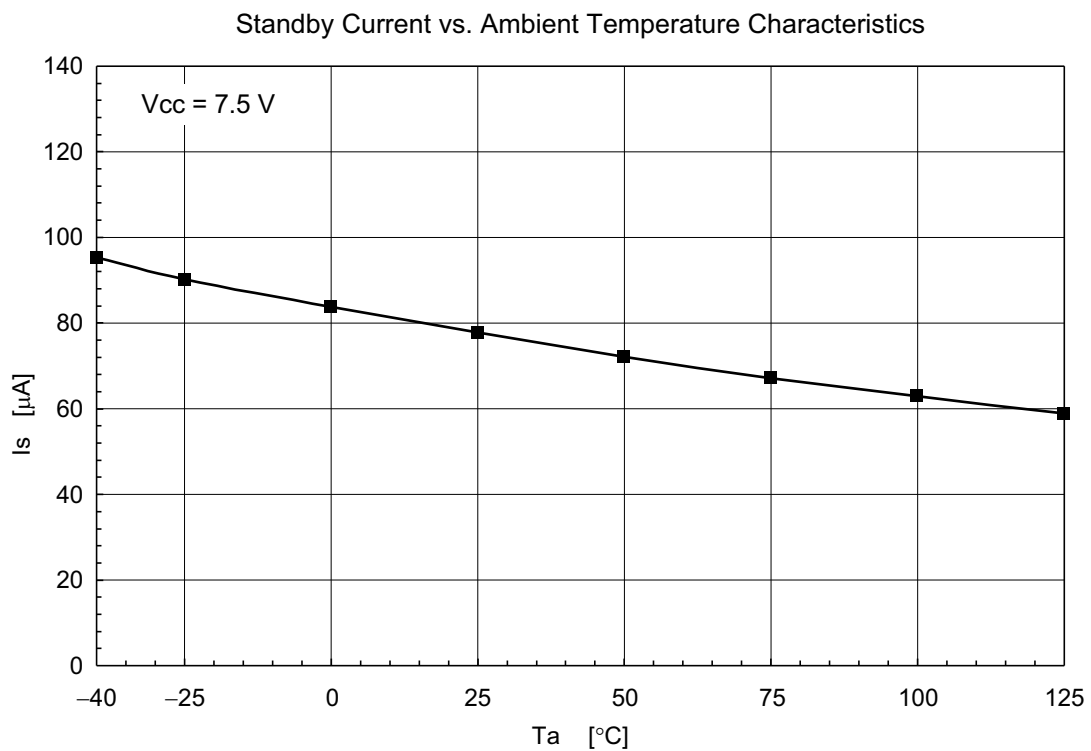
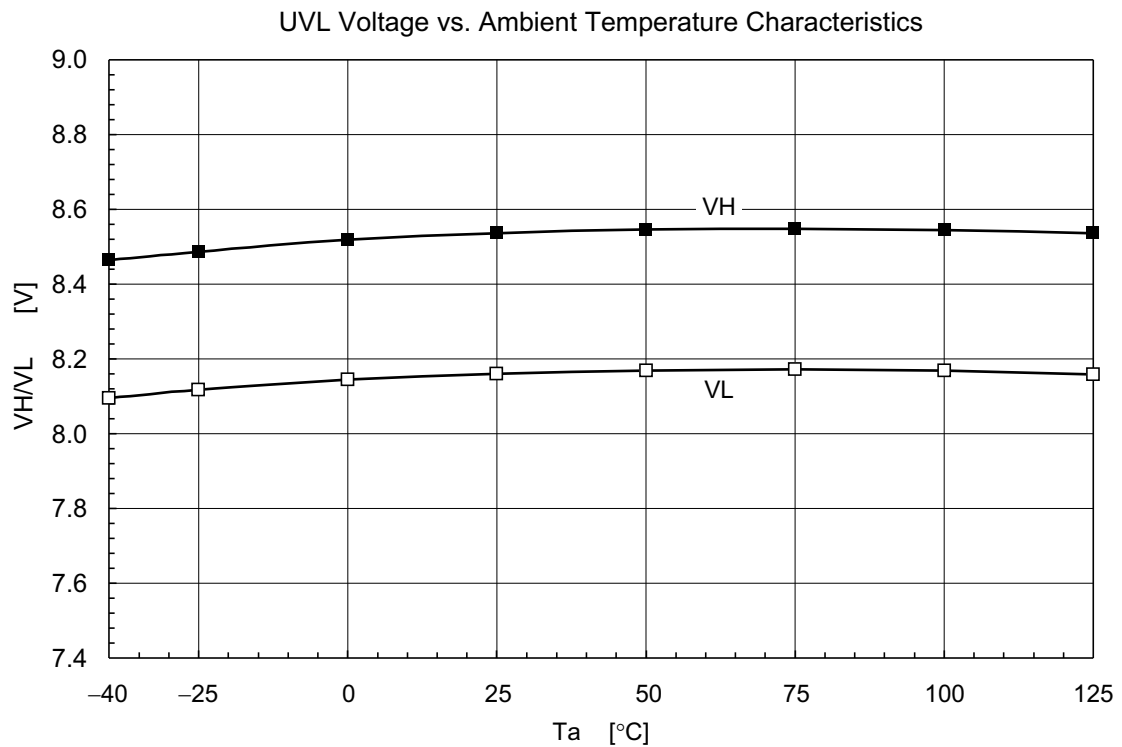
### Supplying Power from an External Power Supply

It is also possible to use an external source as the power supply for the R2A20121 as shown in figure 11. The VREFGOOD circuit controls whether the IC is operating or stopped. The threshold voltage of the VREFGOOD circuit is 4.6 V (typ.) on the rising edge and 4.4 V on the falling edge. Since the IC's characteristics vary with the value of the external voltage, this voltage must be provided by a high-precision 5-V source.

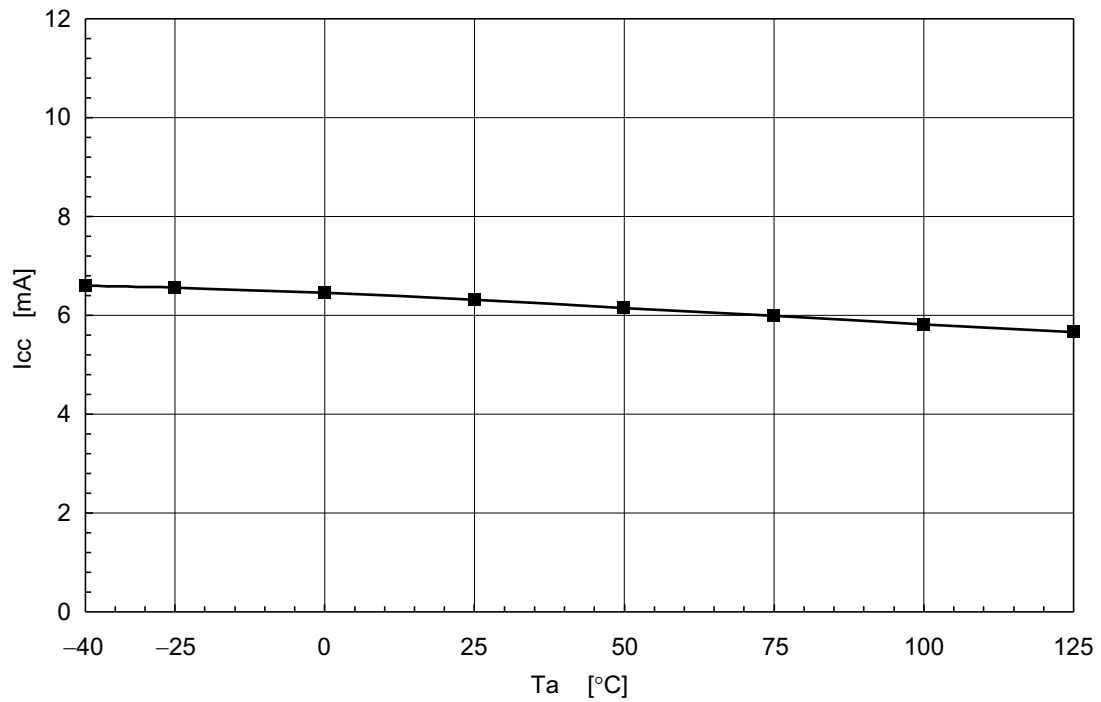


**Figure 11**

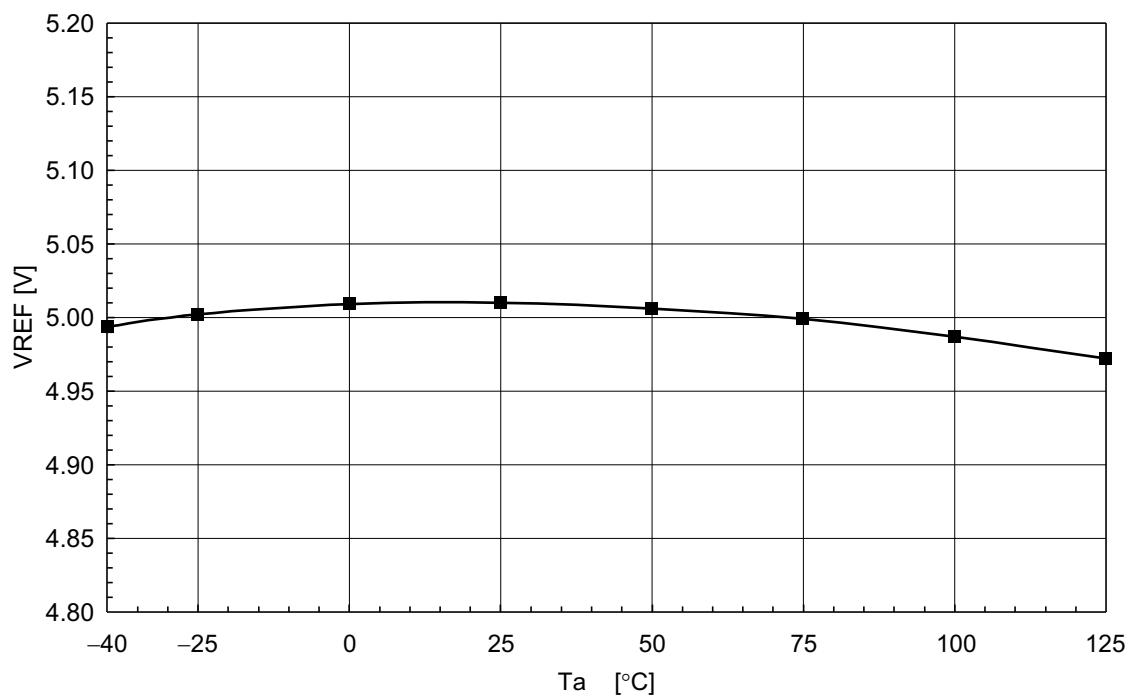
## Characteristic Curves



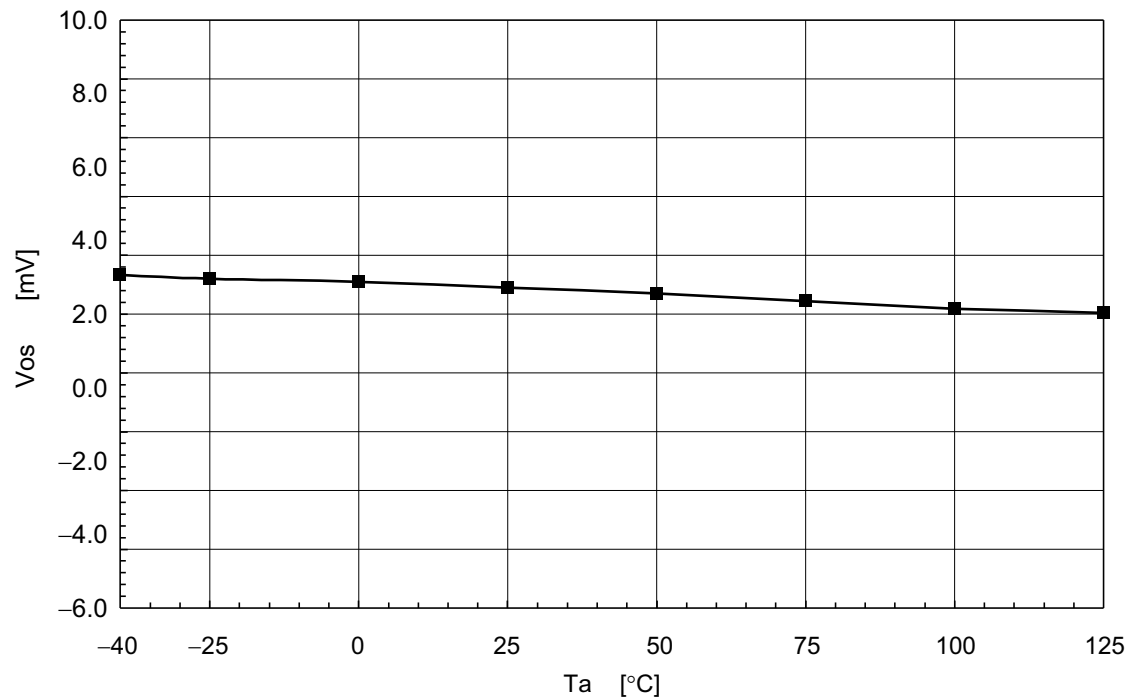
Operating Current vs. Ambient Temperature Characteristics



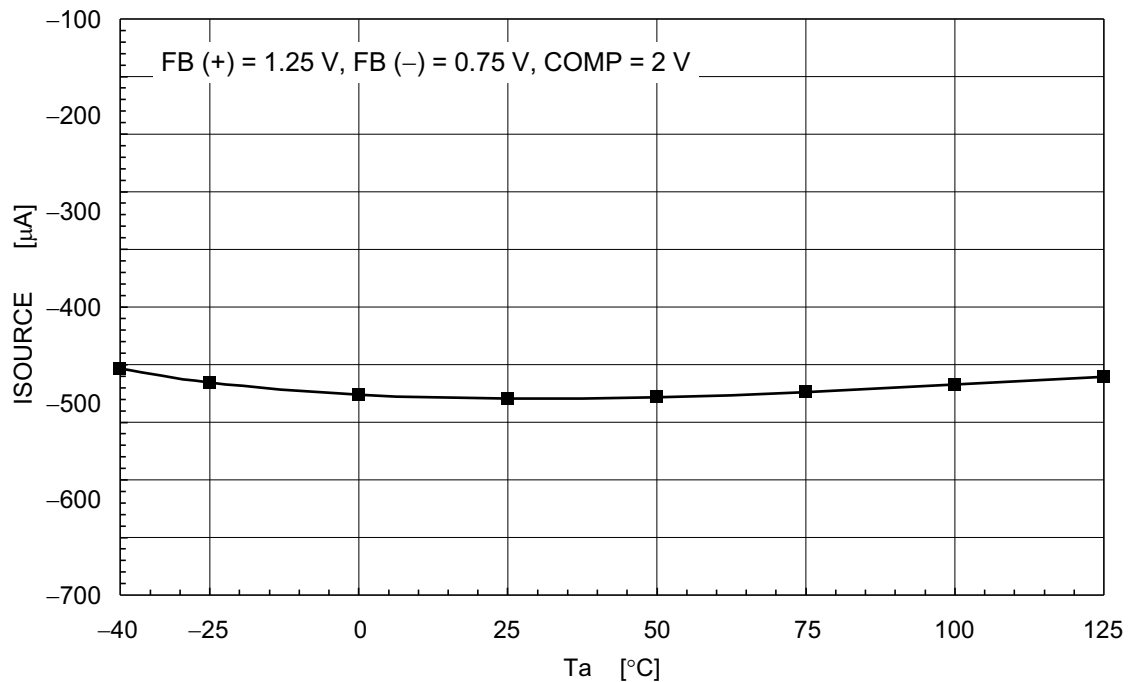
VREF Output Voltage vs. Ambient Temperature Characteristics

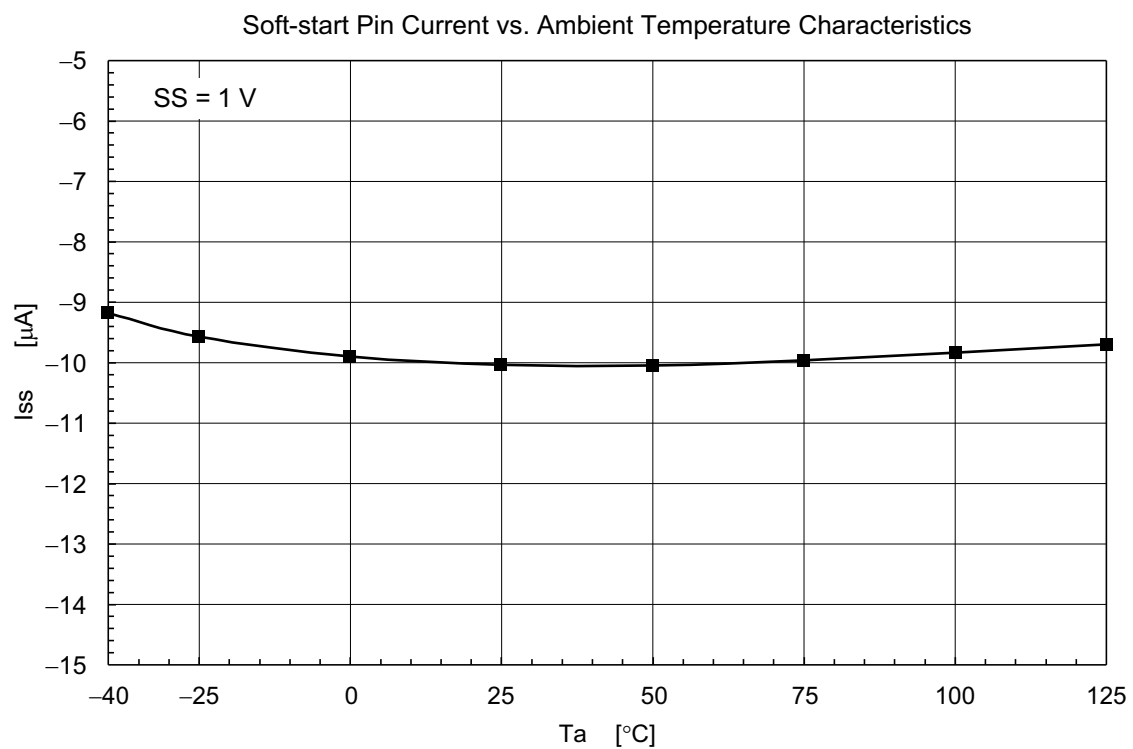
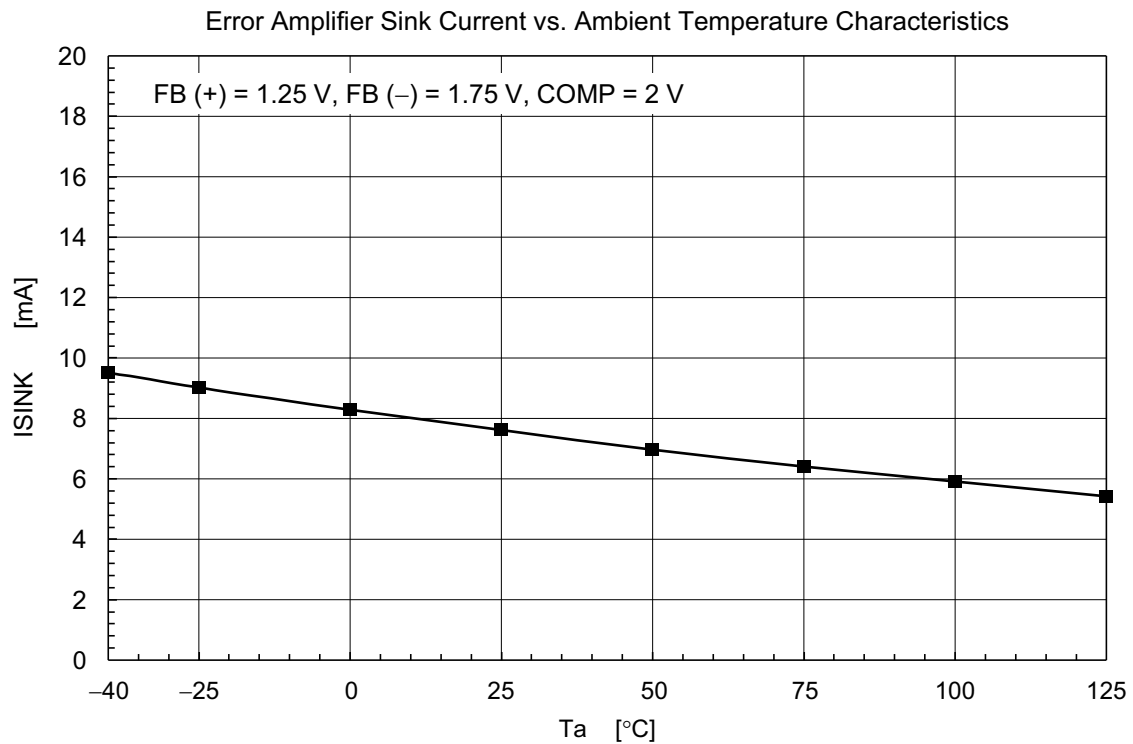


Error Amplifier Offset Voltage vs. Ambient Temperature Characteristics



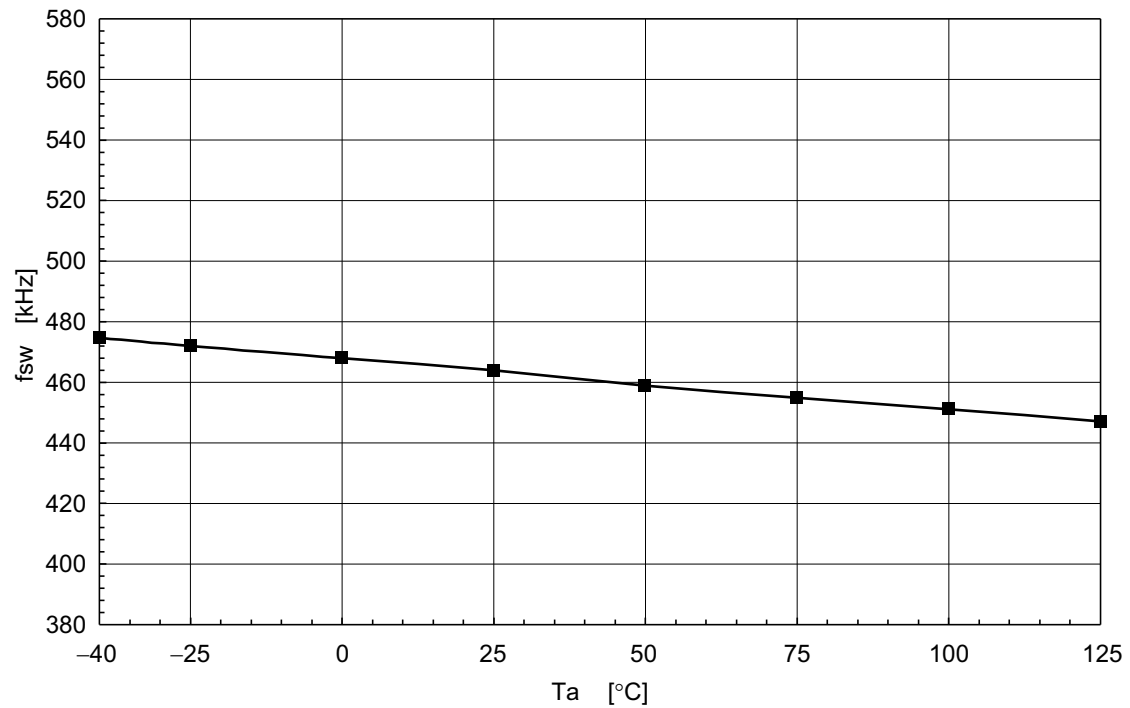
Error Amplifier Source Current vs. Ambient Temperature Characteristics



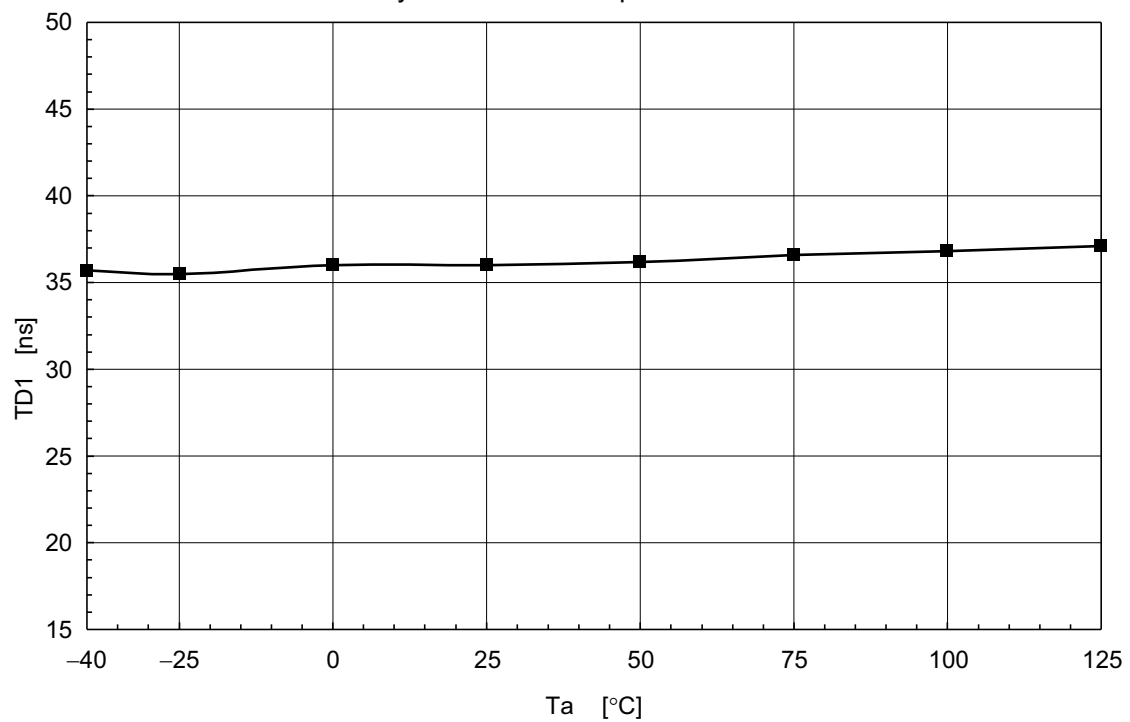


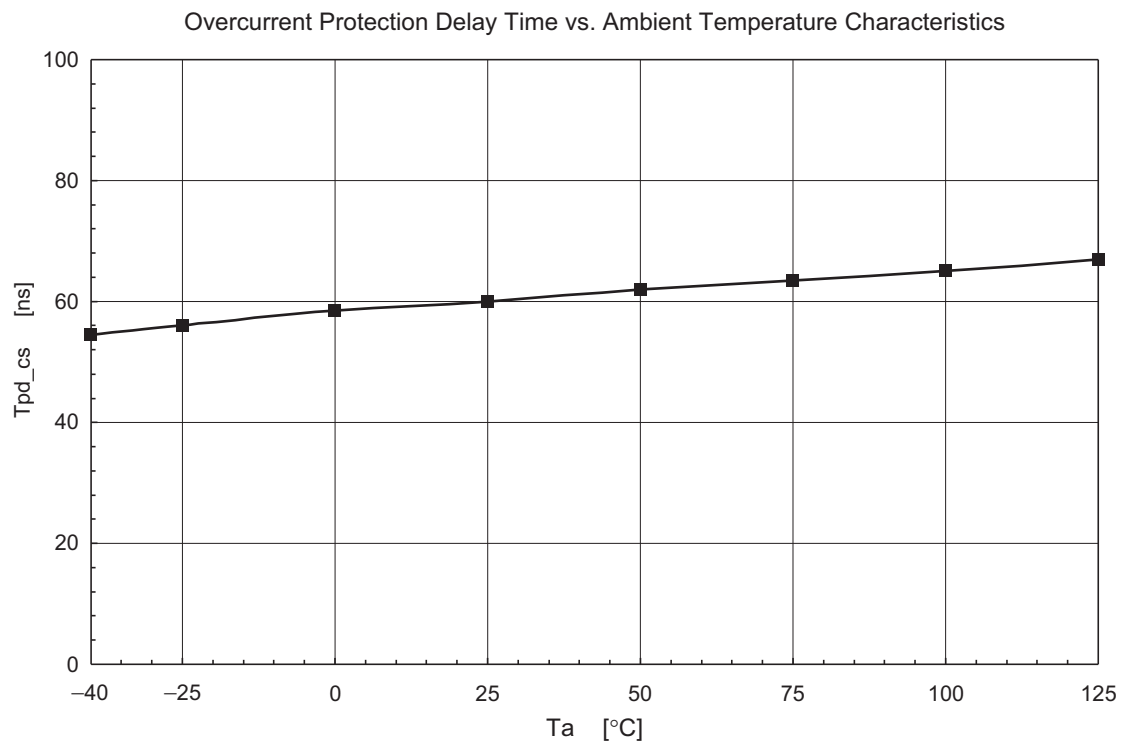
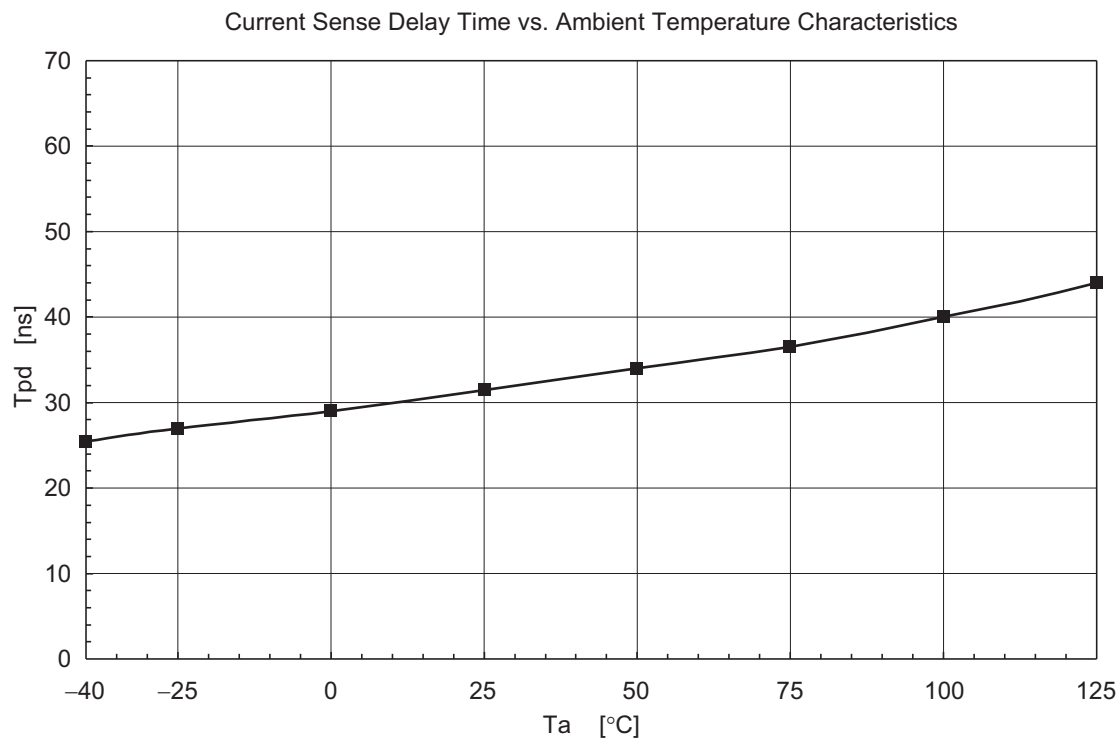


Switching Frequency vs. Ambient Temperature Characteristics



TD1 Delay vs. Ambient Temperature Characteristics







Notes:

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