



Description

The LX7178 is a digitally controlled step-down regulator IC with an integrated 40mΩ high-side P-channel MOSFET and a 14mΩ low-side N-channel MOSFET. It features Microsemi's proprietary constant-frequency hysteretic control engine for near-instantaneous correction to line/load transients. It does not require high-ESR output capacitors and incorporates energy-saving "PSM" (Power Save or Pulse Skip Mode) at light loads, to extend battery life in mobile applications.

The LX7178 has an I²C serial interface port for output voltage margining and monitoring if required (it can also operate in default mode). In addition it includes robust fault monitoring functions.

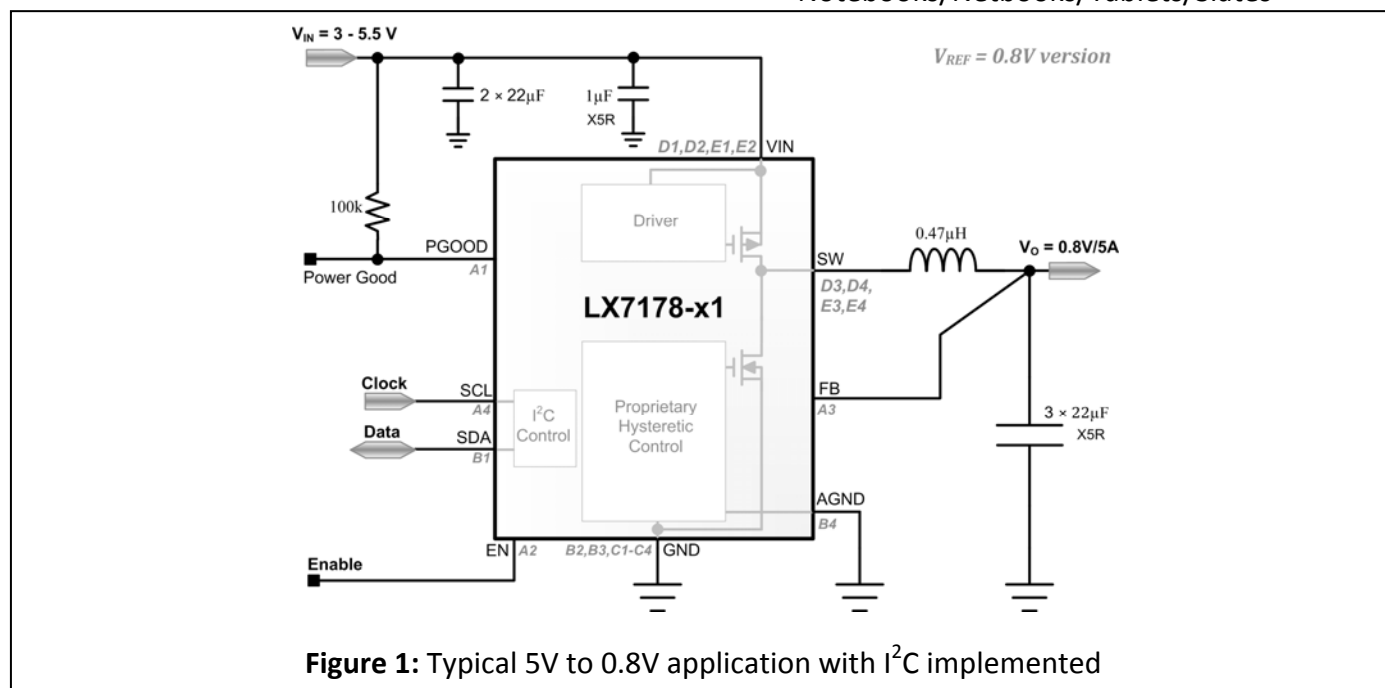
The LX7178 will operate from 3V to 5.5V, and is available in 0.8V fixed output voltage option (no voltage divider is necessary). The output voltage can also be adjusted with an external voltage divider up to 3.3V.

Features

- ◆ Constant Frequency Hysteretic Control
- ◆ Extremely Fast Line/Load Transient Response
- ◆ I²C for Output Adjustment (3.4Mbps)
- ◆ 1.875 MHz Switching Frequency
- ◆ Extremely Low-R_{DS(on)} MOSFETS
- ◆ Input Voltage Rail 3.3V to 5V
- ◆ Greater than 5A Output Current
- ◆ I²C Selectable Power Save Mode for Light-Load Efficiency
- ◆ UVLO, OVP, OCP
- ◆ 0°C to +85°C Ambient Temperature
- ◆ Available in WLCSP-20 (0.4mm pitch)
- ◆ RoHS Compliant

Applications

- High Performance HDD
- Notebooks/Netbooks/Tablets/Slates





Other Application Diagrams

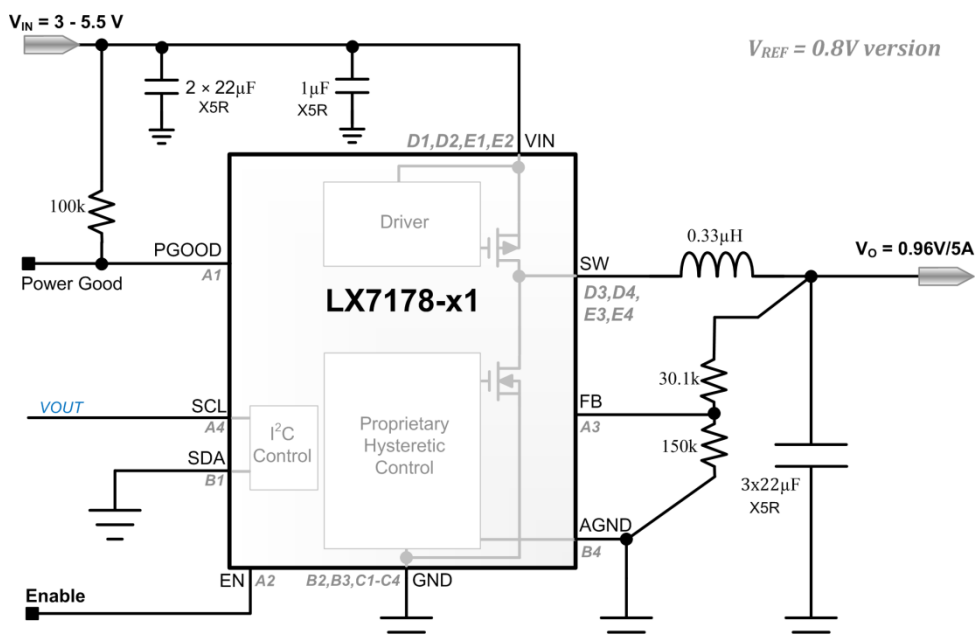


Figure 2: Typical 5V to 0.96V application without I²C implemented

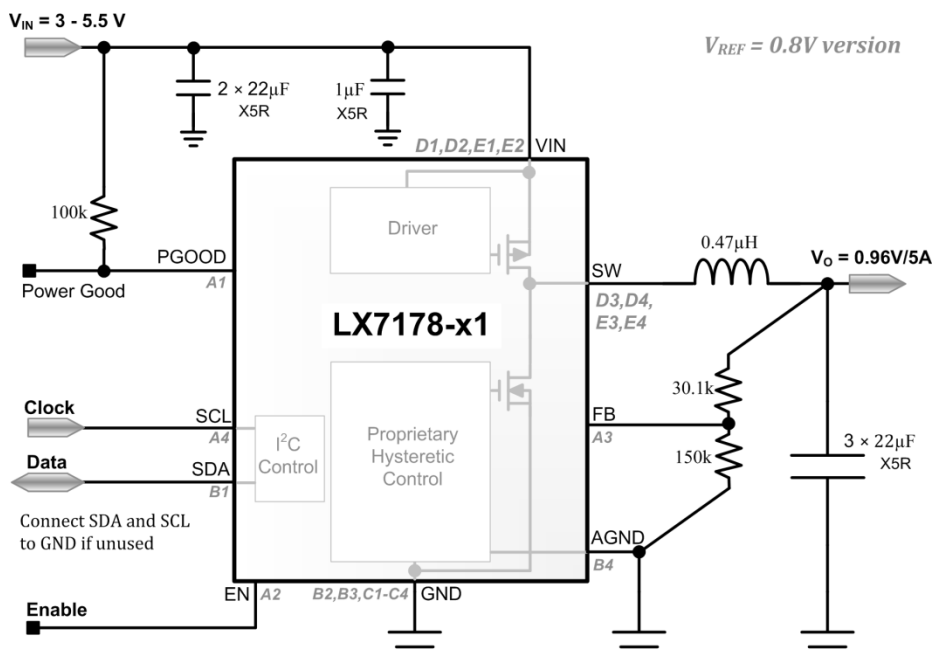
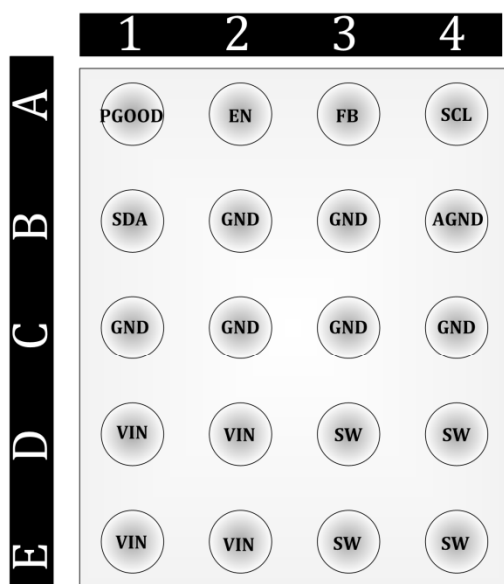


Figure 3: Typical 5V to 0.96V application with I²C implemented

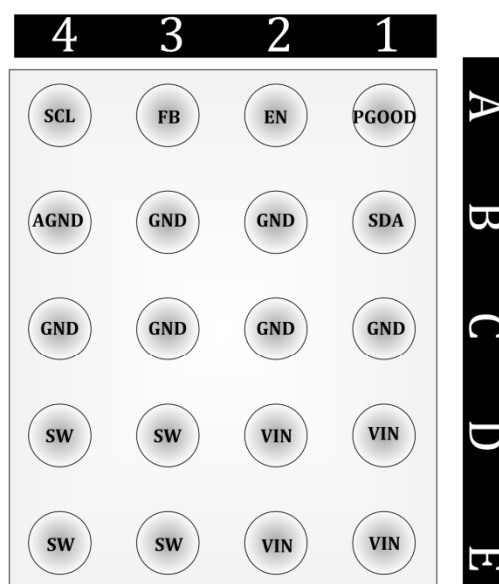


Pin/Ball Configuration



LX7178

Top View
(Ball Side Down)
20-ball Wafer Scale Package



LX7178

Bottom View
(Ball Side Up)
20-ball Wafer Scale Package

Part Marking:

| | | |
|------|-------------------------|-------------------------|
| MSC | XXXX=Device Number | YWWA |
| XXXX | | |
| YWWA | E.g.: 7801=LX7178-01CSP | Year/Work Week/Lot Code |

Figure 4: Pinout

Ordering Information

| Ambient Temperature | Type | Package | Set Output Voltage | Part Number | Packaging Type |
|---------------------|-------------------------|------------------------|--------------------|-------------------------------------|----------------|
| 0°C to 85°C | RoHS compliant, Pb-free | WLCSP-20 (0.4mm pitch) | 0.8V | LX7178-01CSP LX7178-xyCSP* | Bulk |
| | | | 0.8V | LX7178-01CSP-TR LX7178-xyCSP-TR* | Tape and Reel |

* Consult factory for other I²C slave address and set output voltage options.

"x" is the 2 LSB bits of the binary I²C slave address (0 to 3);

"y" is the set output voltage (0 is 0.6V, 1 is 0.8V, 2 is 0.9V, 3 is 0.975V)

3V to 5.5V, 5A Constant Frequency Hysteretic Synchronous Buck Regulator with I²C Production Datasheet



Pin/Ball Description

| Pin/Ball Number | Pin/Ball Designator | Description |
|----------------------------|---------------------|--|
| A1 | PGOOD | Open Drain status output, requires external pull up resistor. This pin will go low when VOUT is outside the defined power good range, when the die is hotter than the thermal shutdown threshold, when PVIN is above the over voltage threshold, or when PVIN is below the under voltage threshold. |
| A2 | EN | Enable for switching regulator. Force high to enable, force low to disable the IC. |
| A3 | FB | Feedback Voltage sense – Analog Input – This voltage is compared with the internal V _{REF} voltage to control the hysteretic converter. Normally this is connected to VOUT via a resistor divider network. |
| A4 | SCL | Serial Data Clock – Logic Input – Clock for the serial interface. Glitches shorter than 50nS will be ignored. If the serial interface is not used, connect to GND or VIN. This pin can also be connect to VOUT if required by the layout. |
| B1 | SDA | Serial Data – Bi-Directional Logic – This I ² C pin is used to receive clocked serial data from the host and to send clocked serial data to the host. Glitches shorter than 50nS will be ignored. If the serial interface is not used in the application, this pin should be connected to VIN or GND. |
| B2, B3, C1 – C4 | GND | Ground. Connect to ground plane. |
| B4 | AGND | Analog Ground. Connect to ground plane. |
| D1, D2 E1, E2 | VIN | Input of IC and buck stage. Connect to input rail VIN (between 3V and 5.5V). A minimum input capacitance of one 1μF and one 22μF of X5R or better multilayer ceramic, should be placed very close to IC between this node and GND. |
| D3, D4 E3, E4 | SW | Switching Node. Drives the external L-C low pass filter. |



Functional Block Diagram

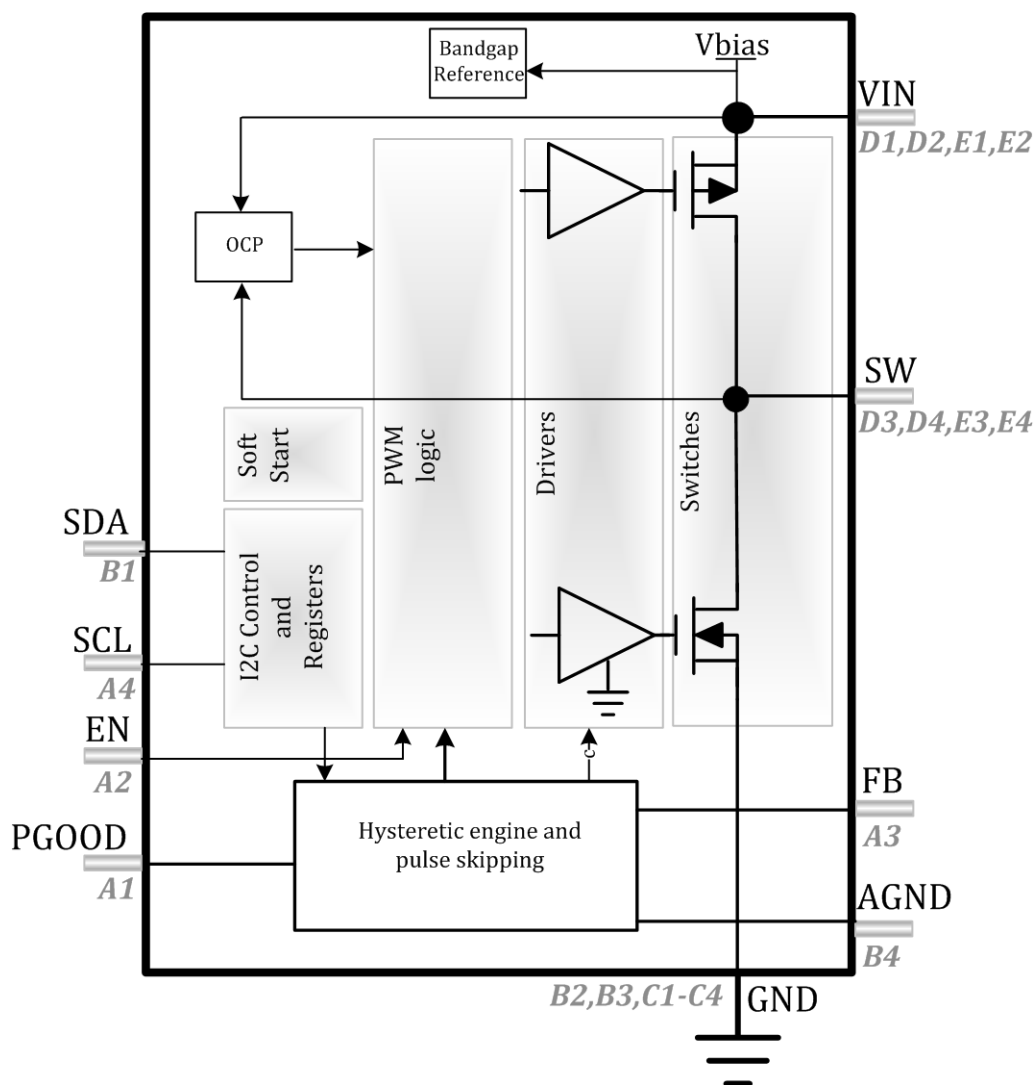


Figure 5: Block Diagram

3V to 5.5V, 5A Constant Frequency Hysteretic Synchronous Buck Regulator with I²C Production Datasheet



Absolute Maximum Ratings

Performance is not necessarily guaranteed over this entire range. These are maximum stress ratings only. Exceeding these ratings, even momentarily, can cause immediate damage, or negatively impact long-term operating reliability.

| | Min | Max | Units |
|--|------|--------------|-------|
| VIN, SW to GND | -0.3 | 7 | V |
| EN, FB, SDA, SCL, PGOOD to GND | -0.3 | 7 | V |
| SW to GND (Shorter than 50ns) | -2 | 7 | V |
| Maximum Junction Temperature | | 150 | °C |
| Lead Soldering Temperature (40s, reflow) | | 260 (+0, -5) | °C |
| Storage Temperature | -65 | 150 | °C |

Operating Ratings

Performance is generally guaranteed over this range as further detailed below under Electrical Characteristics.

| | Min | Max | Units |
|---------------------|-----|-----|-------|
| VIN | 3 | 5.5 | V |
| Ambient Temperature | 0 | 85 | °C |
| Output Current | | 5 | A |

Note: Corresponding Absolute Max Junction Temperature is 150°C.

Thermal Properties

| Thermal Resistance | Typical | Units |
|--------------------|---------|-------|
| θ_{JA} | 38 | °C/W |

Note: The θ_{JA} number assume no forced airflow. Junction Temperature is calculated using $T_J = T_A + (P_D \times \theta_{JA})$. In particular, θ_{JA} is a function of the PCB construction. The stated number above is for a four-layer board in accordance with JESD-51 (JEDEC).

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Electrical Characteristics

Unless otherwise specified under conditions, the Min and Max ratings stated below apply over the entire specified operating ratings of the device. Typ values stated, are either by design or by production testing at 25°C ambient.

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|--------------------------------|--|--|-------|-------|-------|-------------------|
| Input Voltage | | | | | | |
| I _Q | Input current | I _{LOAD} = 0, PSM enabled | 200 | 440 | 600 | μA |
| I _{IN} | Input current at shut down | EN = GND, T _A = 25°C | | 0.1 | 3 | μA |
| I _{IN_I²C} | Input current I ² C shut down | VSEL(7) = low, EN = high | | 100 | 120 | μA |
| UVLO | Under voltage rising threshold | VIN rising | | 2.6 | 2.8 | V |
| UVLO _{HYST} | UVLO hysteresis | | | 0.26 | | V |
| OVP _R | Over voltage rising threshold | VIN_OVP: Ctrl1(1) = 1 | 6.25 | | 6.75 | V |
| OVP _F | Over voltage falling threshold | VIN_OVP: Ctrl1(1) = 1 | 5.75 | | 6.2 | V |
| Reference Voltage | | | | | | |
| V _{REFMIN} | Minimum reference voltage | VSEL(6:0) = 00h | 0.588 | 0.6 | 0.612 | V |
| V _{REFMEAN} | Mean reference voltage | VSEL(6:0) = 40h | 0.888 | 0.9 | 0.912 | V |
| V _{REFMAX} | Maximum reference voltage | VSEL(6:0) = 7Fh | 1.184 | 1.195 | 1.206 | V |
| T _{SS} | V _{REF} slew rate | SLEW: Ctrl2(2:0) = 011 | 3 | 4 | 5.5 | mV/μs |
| T _{HICUP} | Hiccup time | VOUT = 0.2V | | 1.5 | | ms |
| Output Voltage | | | | | | |
| VOUT | Default VOUT | Target based on option: 01 = 0.8. Measured with respect to target voltage. | -1.5 | 0 | 1.5 | % |
| | Line regulation | VIN from 3V to 5.5V, I _{LOAD} = 1A. Note 1 | | 0.1 | | % |
| | Load regulation | I _{LOAD} = 0A to 5A. Note 1 | | -0.17 | | %/A |
| | VOUT input current | | | 0 | 1 | μA |
| V _{ouv} | VOUT under voltage threshold | VOUT below this threshold will initiate a hiccup sequence | 77 | 82 | 85 | %V _{REF} |

3V to 5.5V, 5A Constant Frequency Hysteretic Synchronous Buck Regulator with I²C Production Datasheet



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| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|--------------------------------|-----------------------------|--|-----|-------|------|-------------------|
| SW | | | | | | |
| R _{DS(on)_H} | High side on resistance | | | 40 | | mΩ |
| R _{DS(on)_L} | Low side on resistance | | | 14 | | mΩ |
| OCP | Current limit | Note 1 | 6.5 | 7.5 | 9 | A |
| T _{SH} | Thermal shut down threshold | Note 1 | | 150 | | °C |
| T _H | Hysteresis | Note 1 | | 20 | | °C |
| F _{SW} | PWM switching frequency | | 1.5 | 1.875 | 2.25 | MHz |
| R _{SWDISC} | SW discharge resistance | EN = low; Discharge: Ctrl2(4) = 1; | 80 | 200 | 1400 | Ω |
| EN, SDA (as input), SCL | | | | | | |
| V _{IH} | Input high | | 1.1 | | | V |
| V _{IL} | Input low | | | | 0.4 | V |
| V _H | Hysteresis | | | 0.1 | | V |
| I _{II} | Input current | | | 0.01 | 1 | μA |
| PGOOD | | | | | | |
| V _{PG90} | PGOOD VOUT lower threshold | VOUT rising, percentage of V _{REF} | 85 | 90 | 95 | %V _{REF} |
| V _{PG110} | PGOOD VOUT upper threshold | VOUT falling, percentage of V _{REF} | 105 | 110 | 115 | %V _{REF} |
| V _{PGHY} | Hysteresis | Percentage of V _{REF} | | 5 | | %V _{REF} |
| PG _{RDS(on)} | PGOOD pull down resistance | | | 100 | 300 | Ω |
| | PGOOD leakage current | | | 0 | 1 | μA |
| | PGOOD delay | PGOOD rising edge delay (only when enabled by setting CTRL 1:5 to 0). By default, this delay is not enabled. | 30 | 45 | 65 | ms |
| 7 Bit DAC | | | | | | |
| | Differential linearity | Monotonicity assured by design | | | 0.8 | LSB |

Note 1: Guaranteed by design.

3V to 5.5V, 5A Constant Frequency Hysteretic Synchronous Buck Regulator with I²C Production Datasheet


Microsemi

Application Specifics

| | | |
|---------------------------------|---|--------------|
| Efficiency | $I_{OUT} = 1.5A$, $VCC = 5V$, $VOUT = 3.3V$ | 95% |
| | $I_{OUT} = 5.0A$, $VCC = 5V$, $VOUT = 3.3V$ | 90% |
| VOUT Min Transient | 0.5 A to 2.5 A load step slews in 900ns, $C_{LOAD} = 3 \times 22\mu F$ ceramic caps, 0.47 μH inductor | 31.6mV |
| VOUT Max transient | 2.5 A to 0.5 A load step slews in 1.46 μs , $C_{LOAD} = 3 \times 22\mu F$ ceramic caps, $L = 0.47\mu H$ inductor | 34.8mV |
| Typical Load Inductance | DCR = 6.7m Ω , IDC = 12.2A, ISAT = 16A. | 0.47 μH |
| Typical Load Capacitance | 6.3V, X5R | 3x22 μF |



Layout Recommendations

The LX7178 EVAL Board is a 4-layer board, the thickness of the board is 63mil in total. The second layer to top layer is 7mil, the third layer to the bottom layer is 7mil. The recommended BGA PCB layout shown below requires no microvias or blind vias. Each signal trace can exit the LX7178 directly without any vias under the device. Also, with the bypass capacitors C2, C3 and C8 implemented as shown it can lower the ESL. Please see LX7178 User Guide for additional details.

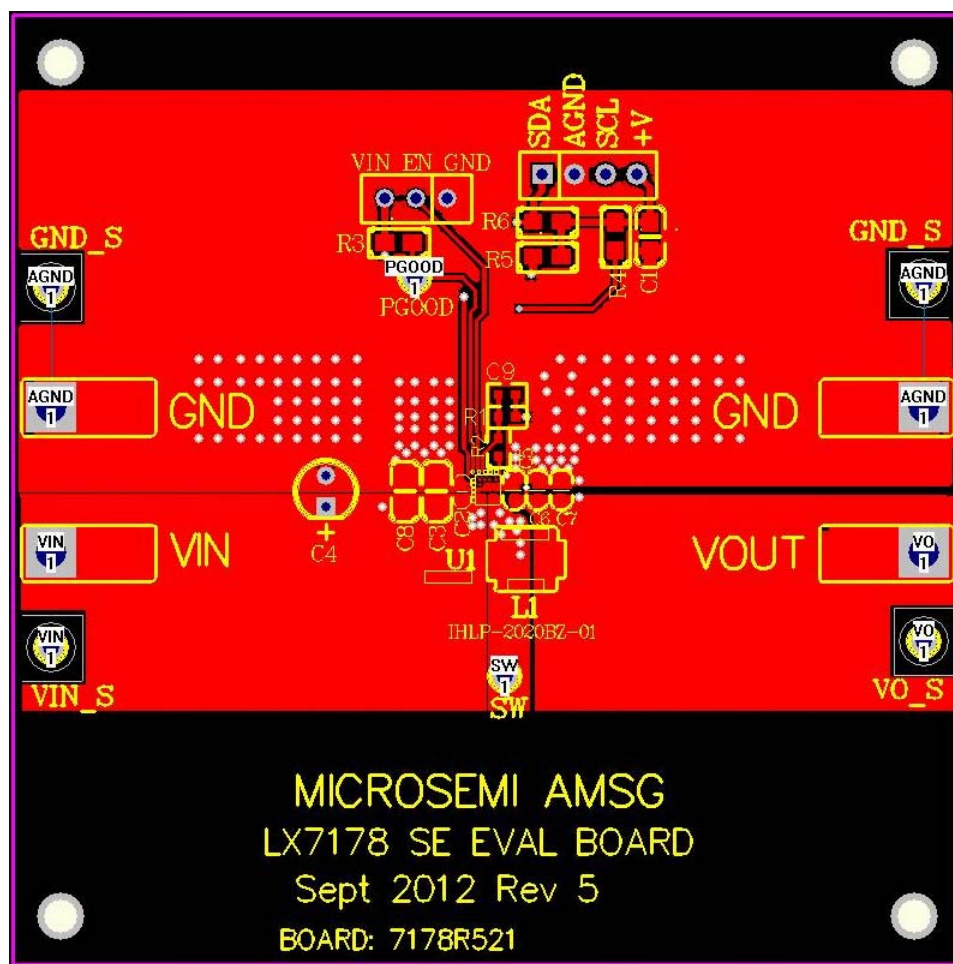


Figure 6: Layout recommendation (TOP layer)

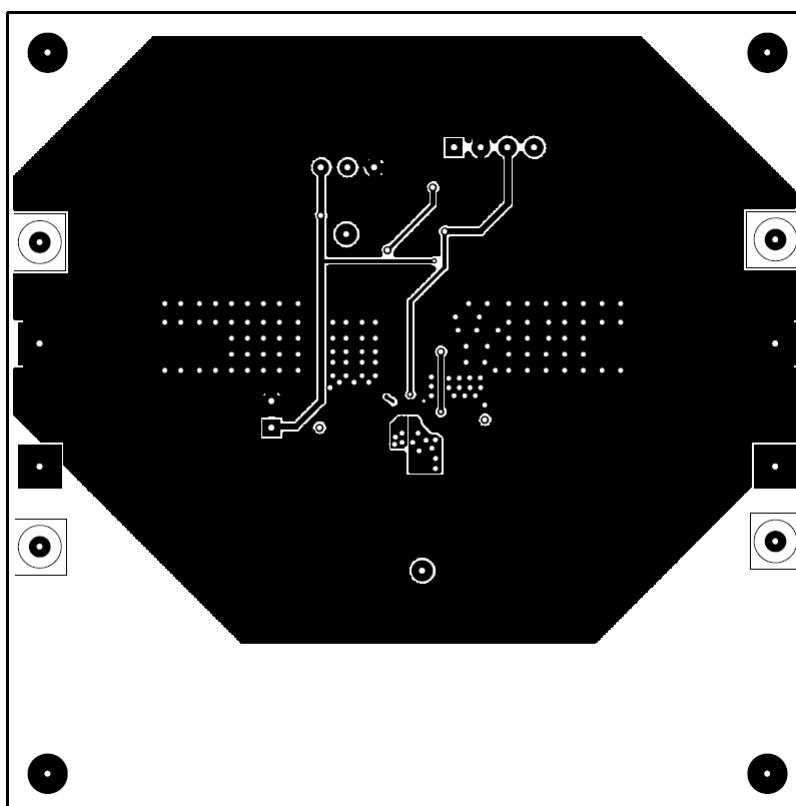


Figure 7: Layout recommendation (BOTTOM layer)

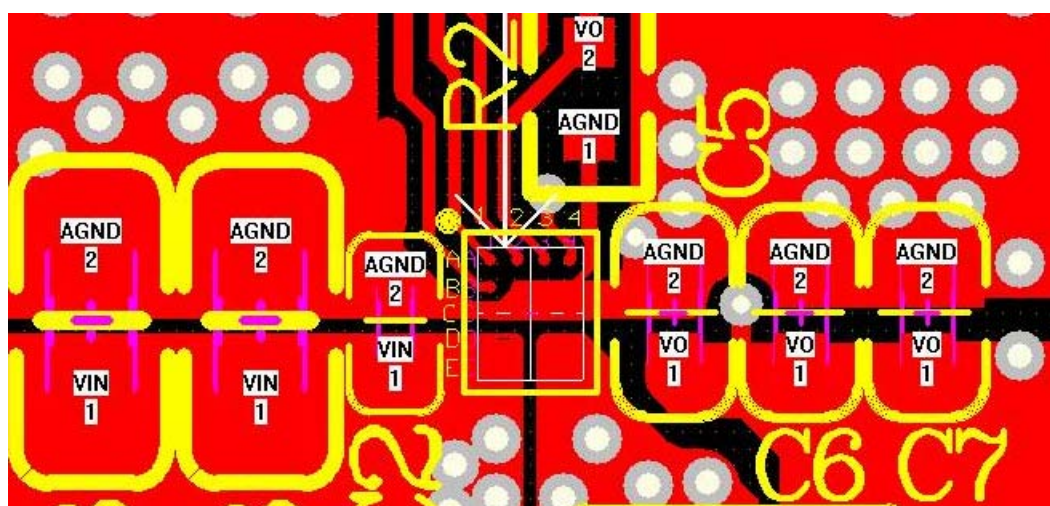


Figure 8: Closeup of Layout in Region of BGA (note Ground gull-wings and via Stitching to BOTTOM)



Typical Performance Curves

Dynamic Response

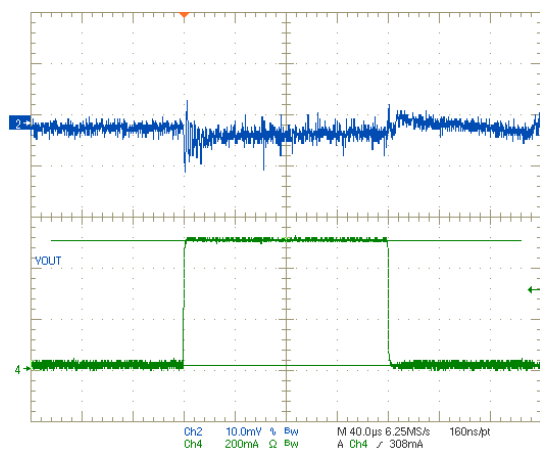


Figure 9: No load to 0.5A PWM
CH2: VOUT, CH4: I_{LOAD}

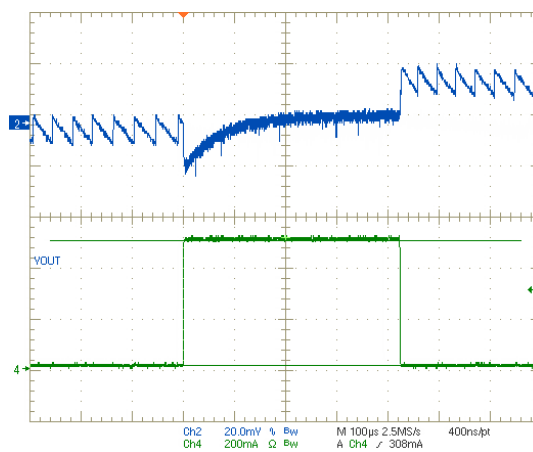


Figure 10: No load to 0.5A PSM
CH2: VOUT, CH4: I_{LOAD}

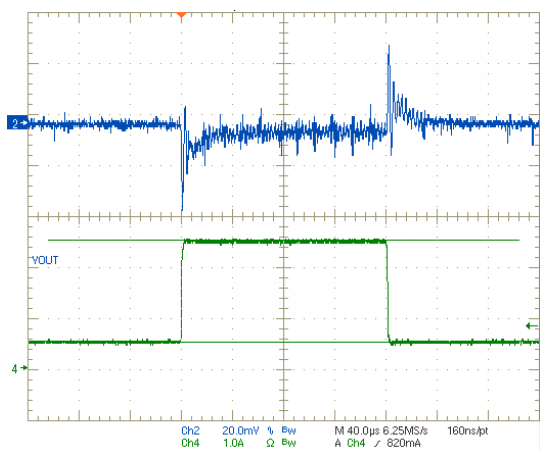


Figure 11: 0.5A to 2.5A PWM
CH2: VOUT, CH4: I_{LOAD}

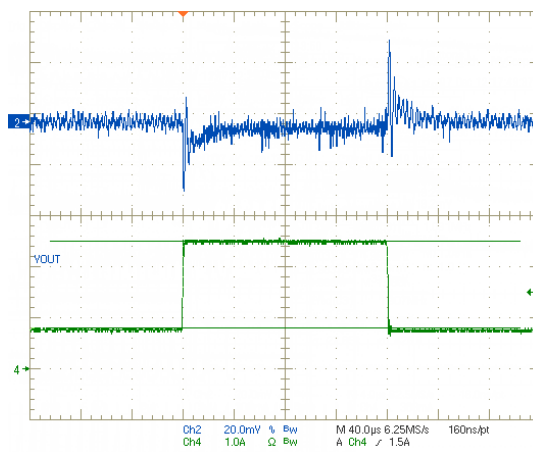


Figure 12: 0.8A to 2.5A PWM
CH2: VOUT, CH4: I_{LOAD}

3V to 5.5V, 5A Constant Frequency Hysteretic Synchronous Buck Regulator with I²C Production Datasheet



Typical Performance Curves (Continued)

Dynamic Response (Continued)

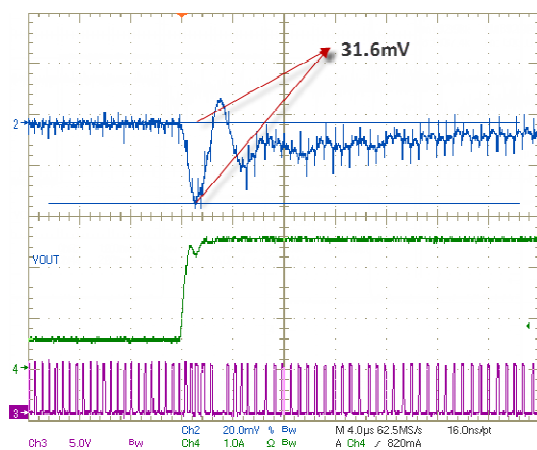


Figure 13: 0.5A to 2.5A PWM Rising Edge
CH2: VOUT, CH3: SW, CH4: I_{LOAD}

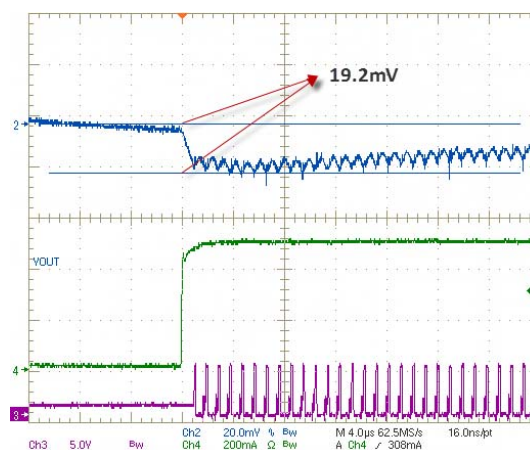


Figure 14: No load to 0.5A PSM Rising Edge
CH2: VOUT, CH3: SW, CH4: I_{LOAD}

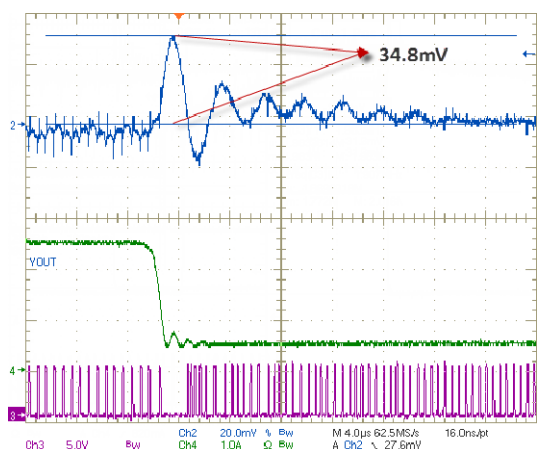


Figure 15: 0.5A to 2.5A PWM Falling Edge
CH2: VOUT, CH3: SW, CH4: I_{LOAD}

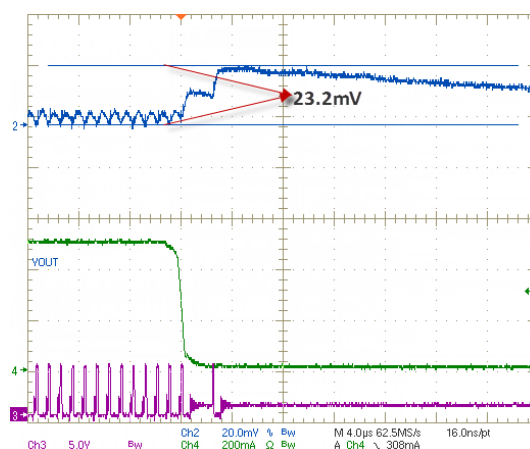


Figure 16: No load to 0.5A PSM Falling Edge
CH2: VOUT, CH3: SW, CH4: I_{LOAD}



Typical Performance Curves (Continued)

Efficiency

LX7178 5V VIN Efficiency

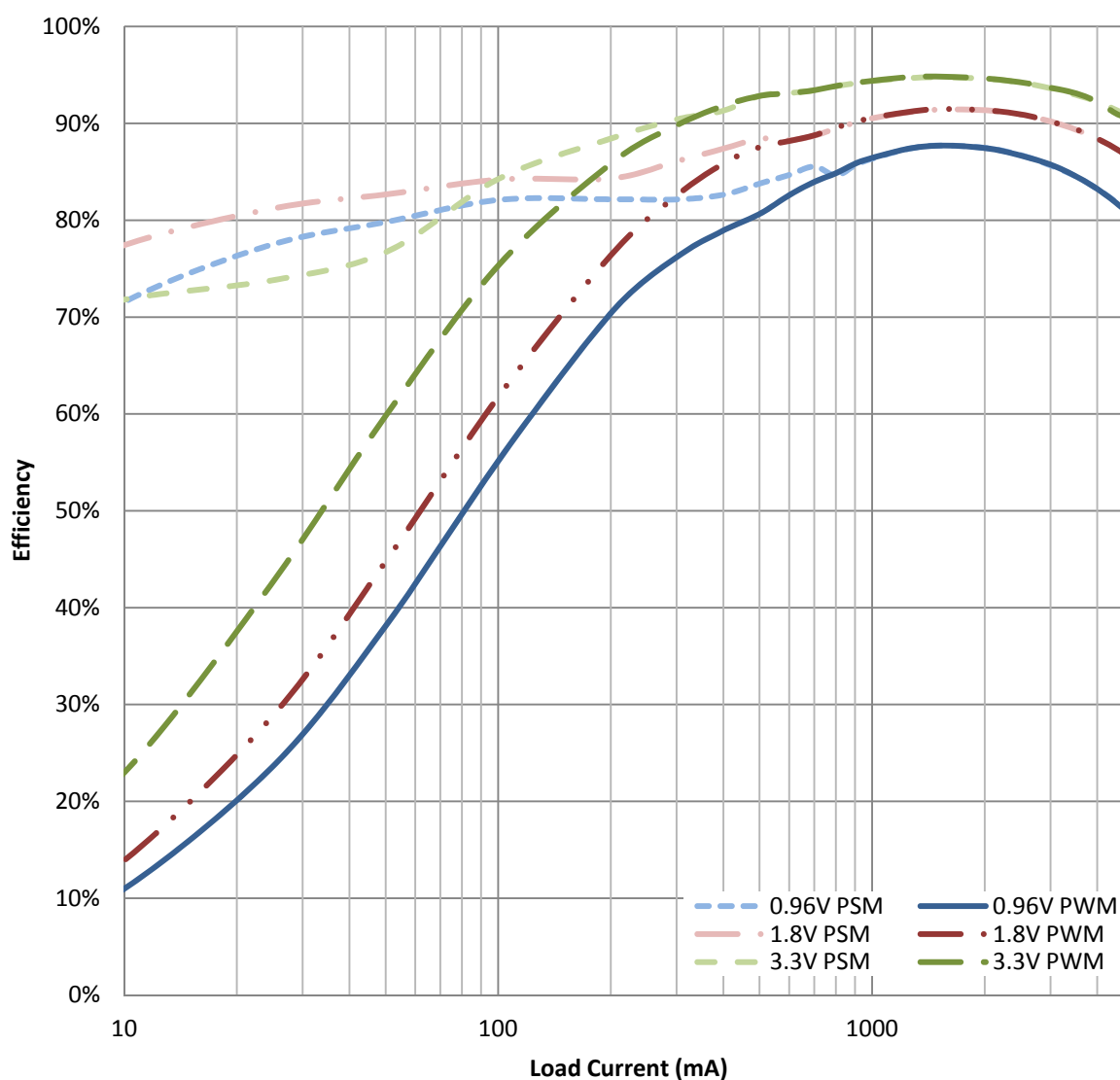


Figure 17: Efficiency Curves for 5V input

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I²C Timing Specifications

| Symbol | Parameter | Conditions | C _b = 100 pF (max) (*Note2) | | C _b = 400 pF | | Unit |
|---------------------|---|-------------------|---|-----|-------------------------|-----|------|
| | | | Min | Max | Min | Max | |
| f _{SCHL} | SCL clock frequency | | 0 | 3.4 | 0 | 0.4 | MHz |
| t _{SU;STA} | Set-up time for a repeated START condition | | 160 | - | 600 | - | ns |
| t _{HD;STA} | Hold time (repeated) START condition | | 160 | - | 600 | - | ns |
| t _{LOW} | LOW period of the SCL clock | | 160 | - | 1300 | - | ns |
| t _{HIGH} | HIGH period of the SCL clock | | 60 | - | 600 | - | ns |
| t _{SU;DAT} | Data set-up time | | 10 | - | 100 | - | ns |
| t _{HD;DAT} | Data hold time | | 0 | 70 | 0 | - | ns |
| t _{rCL} | Rise time of SCL signal | | 10 | 40 | 20*0.1C _b | 300 | ns |
| t _{rCL1} | Rise time of SCL signal after a repeated START condition and after an acknowledge bit | | 10 | 80 | 20*0.1C _b | 300 | ns |
| t _{fCL} | Fall time of SCL signal | | 10 | 40 | 20*0.1C _b | 300 | ns |
| t _{rDA} | Rise time of SDA signal | | 10 | 80 | 20*0.1C _b | 300 | ns |
| t _{fDA} | Fall time of SDA signal | | 10 | 80 | 20*.01C _b | 300 | ns |
| t _{SU;STO} | Set-up time for STOP condition | | 160 | - | 600 | - | ns |
| t _{BUF} | Bus free time between a STOP and START condition | | 160 | - | 1300 | - | ns |
| t _{VD;DAT} | Data valid time | | - | 160 | - | 900 | ns |
| t _{VD;ACK} | Data valid acknowledge time | | - | 160 | - | 900 | ns |
| C _b | Capacitive load for each bus line | SDA and SCL lines | - | 100 | - | 400 | pF |

Note 1: All values referred to V_{IH}(min) and V_{IL}(max) levels of I/O stages table.

Note 2: Loads in excess of 100pf will restrict bus operation speed below 3.4MHz

**3V to 5.5V, 5A Constant Frequency Hysteretic
Synchronous Buck Regulator with I²C
Production Datasheet**

Operation Theory

Basic Operation

The LX7178 compares VOUT voltage to an internal reference, V_{REF}. When VOUT is lower than V_{REF}, the upper switch turns on and the lower switch turns off. When VOUT is higher than V_{REF}, the upper switch turns off and the lower switch turns on. An internal ramp helps to keep the switching frequency constant over a wide range of output capacitor values and parasitic components (i.e. ESR, ESL). In addition, a frequency control loop keeps the switching frequency constant during continuous conduction mode.

At light loads, if enabled, the converter automatically reduces the switching frequency and enters discontinuous conduction to optimize efficiency while ensuring low VOUT ripple voltage.

An integrated I²C bus interface, operating up to 3.4Mbps, adds the following use programmability to the converter:

1. On the fly programming of the output voltage in 4.7mV increments.
2. Enable / Disable the regulator.
3. Allow PSM or limit operation to only PWM mode.
4. Set the V_{REF} slew rate.
5. Switch node slew rate control.

Setting the Output Voltage

The reference voltage is programmed with the I²C bus VSEL register value.

$$V_{REF} = 0.6V + N_{SEL} \cdot 0.0046875 V \quad (2)$$

Where N_{SEL} is the decimal value of the 7 VSEL bits.

Startup

If the LX7178 is enabled, when VIN rises above the UVLO threshold, the regulator will initiate a startup sequence. The serial port registers are initialized to their default values and all internal bias voltages and currents are allowed to stabilize. V_{REF} then ramps up from 0V to the default voltage at the default slew rate. At the end of the ramp time, PGOOD is allowed to go high 45ms after VOUT has reached the PGOOD rising threshold. During the ramp time, the LX7178 switches to PSM to allow discontinuous operation. This switchover is independent of the MODE bit setting.

3V to 5.5V, 5A Constant Frequency Hysteretic Synchronous Buck Regulator with I²C

Production Datasheet



Operation Theory (Continued)

Over Current Protection

The LX7178 protects against all types of short circuit conditions. Cycle by cycle over current protection turns off the upper switch when the current exceeds the OCP threshold. When this occurs, the upper switch is held off for at least 200ns before being allowed to turn on again. After startup, if VOUT drops below the VOUT under voltage threshold, a hiccup sequence will be initiated where both output switches are shut off for 1.5ms before initiating another soft start cycle. This protects against a crowbar short circuit. The VOUT under voltage detection is not active during start up.

Positive Voltage Transitions

After the initial start up sequence, the output voltage can be programmed to a new value by programming the VSEL register bits and then asserting the GO bit. V_{REF} will transition to the new value at the programmed slew rate. The PGOK monitor bit is deasserted during the V_{REF} ramp time, or when VOUT is outside the error envelope.

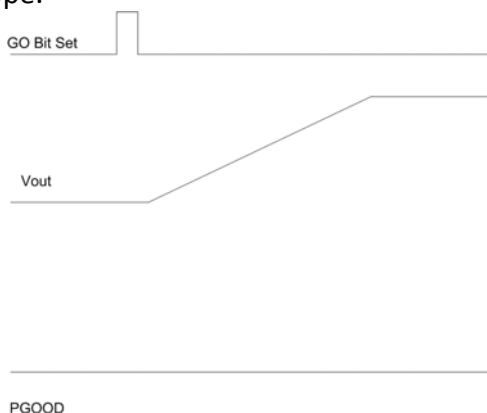


Figure 18: Positive Voltage Transition

Negative Voltage Transitions

A negative voltage transition occurs when a lower output voltage is programmed into the VSEL register, and initiated by asserting the GO bit. In PSM, the LX7178 will not discharge the output filter capacitor.

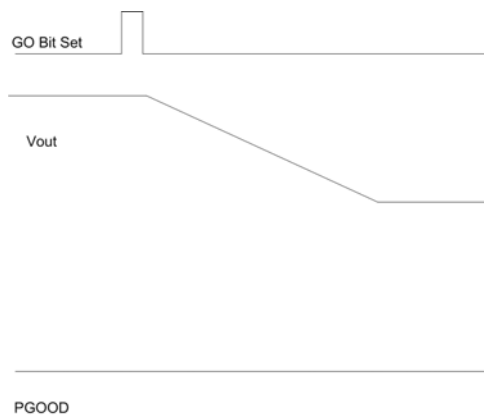


Figure 19: Negative Voltage Transition

Enabling Regulator from I²C Bus

In addition to the EN pin, the regulator can be enabled and disabled via the I²C bus by programming the control register. During disable, the regulator and most of the support circuitry is turned off. However, the I²C bus circuitry is still active and may be programmed.

Switch Node Rise Rate Adjustment

The LX7178 can be programmed to operate in a lower emissions mode by slowing down the switch node rise rate. In this mode, the switch node rise rate will slow down 25%, reducing the switching frequency harmonic content.

3V to 5.5V, 5A Constant Frequency Hysteretic Synchronous Buck Regulator with I²C Production Datasheet



I²C Interface

I²C Port Functional Description

- Simple two wire, bidirectional, serial communication port.
- Multiple devices on same bus speeds from 400Kbps (FS-Mode) to 3.4Mbps (HS-Mode).
- SOC Master controls bus.
- Device listens for the unique address that precedes data.

General I²C Port Description

The LX7178 includes an I²C compatible serial interface, using two dedicated pins: SCL and SDA for I²C clock and data respectively. Each line is externally pulled up to a logic voltage when they are not being controlled by a device on the bus. The LX7178 interface acts as a I²C slave that is clocked by the incoming SCL clock. The LX7178 I²C port will support both the Fast mode (400kHz max) and typically the High Speed mode (3.4MHz max). The data on the SDA line must be stable during the HIGH period of the clock signal (SCL). The state of the SDA line can only be changed when SCL is LOW (except for start, stop, and restart).

Register Map

The LX7178 has five 8-bit user-accessible registers. See Control Register Bit Definition.

Slave Address

In the table below, the A1 and A0 are the binary value of the address given in the ordering information shown on page 3.

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|----|----|-----|
| 0 | 0 | 0 | 1 | 1 | A1 | A0 | R/W |

Table 1: I²C Slave Address

START and STOP Commands

When the bus is idle, both SCL and SDA must be high except in the power up case where they may be held high or low during the system power up sequence.

The STX SOC (bus master) signals START and STOP bits signify the beginning and the end of the I²C transfer. The START condition is defined as the SDA signal transitioning from HIGH to LOW while the SCL line is HIGH. The STOP condition is defined as the SDA transitioning from LOW to HIGH while the SCL is HIGH. The STX SOC acts as the I²C masters and always generates the START and STOP bits. The I²C bus is considered to be busy after START condition and free after STOP condition. During data transfer, STX SOC master can generate repeated START conditions. The START and the repeated START conditions are functionally equivalent.

3V to 5.5V, 5A Constant Frequency Hysteretic Synchronous Buck Regulator with I²C Production Datasheet



I²C Interface (Continued)

Data Transfers

Data is transferred in 8 bit bytes by SDA with the MSB transferred first. Each byte of data has to be followed by an acknowledge (ACK) bit. The acknowledged related clock pulse is generated by the master. The acknowledge occurs when the transmitter master releases the SDA line to a high state during the acknowledge clock. The SDA line must be pulled down by the receiver slave during the 9th clock pulse to signify acknowledgment. A receiver slave which has been addressed must generate an acknowledgement ("ACK") after each byte has been received.

After the START condition, the STX SOC (I²C) master sends a chip address. The standard I²C address is seven bits long. Making the eighth bit a data direction bit (R/W). For the eighth bit (LSB), a "0" indicates a WRITE and a "1" indicates a READ. (For clarification, communications are broken up into 9-bit segments, one byte followed by one bit for acknowledging.) The second byte selects the register to which the data will be written. The third byte contains data to write to the selected register.

When a receiver slave doesn't acknowledge the slave address, the data line must be left HIGH by the slave. The master can then generate a STOP command to abort the transfer. If a slave receiver does acknowledge the slave address but, sometime later in the transfer cannot receive any more data bytes, the master must again abort the transfer. This is indicated by the slave generating the not acknowledge on the first byte to follow.

The slave leaves the data line HIGH and the master generates the STOP command. The data line is also left high by the slave and master after a slave has transmitted a byte of data to the master in a read operation, but this is a not acknowledge that indicates that the data transfer is successful.

Data Transfer Timing for Write Commands

In order to help assure that bad data is not written into the part, data from a write command is only stored after a valid STOP command has been performed.

I²C Electrical Characteristics

The minimum HIGH and LOW periods of the SCL clock specified the I²C Timing Specification table determine the maximum bit transfer rates of, 400 kbit/s for Fast-mode devices, and 3.4 Mbits/s for HS-mode Plus. Devices must be able to follow transfers at their own maximum bit rates, either by being able to transmit or receive at that speed or by applying the I²C clock synchronization procedure, which will force the master into a wait state and stretch the LOW period of the SCL signal. Of course, in the latter case the bit transfer rate is reduced.

Figures 22 and Figure 23 show all timing parameters for the HS & FS-mode timing. The 'normal' START condition S does not exist in HS-mode. Timing parameters for Address bits, R/W bit, Acknowledge bit and DATA bits are all the same. Only the rising edge of the first SCL clock signal after an acknowledge bit has a larger value because the external Rp has to pull-up SCL without the help of the internal current-source.

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I²C Interface (Continued)

The HS & FS-mode timing parameters for the bus lines are specified in the I²C Timing Specification Table. The minimum HIGH and LOW periods and the maximum rise and fall times of the SCL clock signal determine the highest bit rate.

With an internally generated SCL signal with LOW and HIGH level periods of 200ns and 100ns respectively, an HS-mode master fulfills the timing requirements for the external SCL clock pulses (taking the rise and fall times into account) for the maximum bit rate of 3.4Mbit/s. So a basic frequency of 10MHz, or a multiple of 10MHz, can be used by an HS-mode master to generate the SCL signal. There are no limits for maximum HIGH and LOW periods of the SCL clock, and there is no limit for a lowest bit rate.

Timing parameters are independent for capacitive load up to 100pF for each bus line allowing the maximum possible bit rate of 3.4Mbit/s. At a higher capacitive load on the bus lines, the bit rate decreases gradually. The timing parameters for a capacitive bus load of 400pF are specified in I²C Timing Specification Table, allowing a maximum bit rate of 1.7Mbit/s. For capacitive bus loads between 100pF and 400pF, the timing parameters must be interpolated linearly. Rise and fall times are in accordance with the maximum propagation time of the transmission lines SDA and SCL to prevent reflections of the open ends.

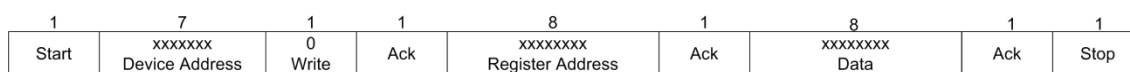


Figure 20: Write Protocol

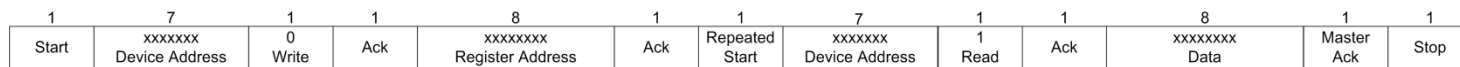


Figure 21: Read Protocol



I²C Interface (Continued)

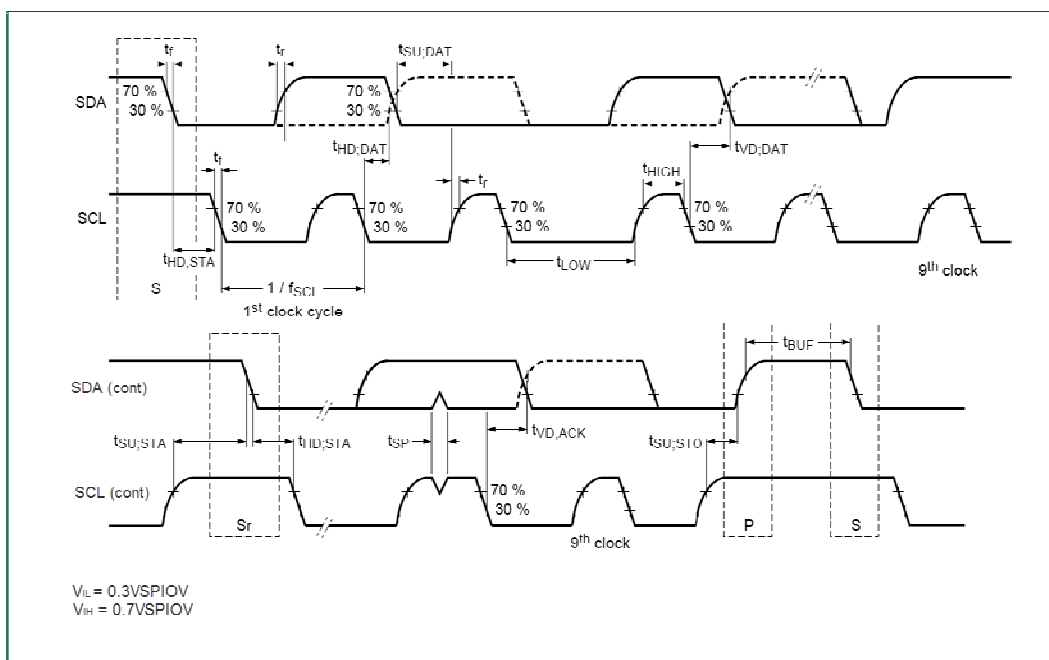


Figure 22: Definition for FS-Mode devices on the I²C Port

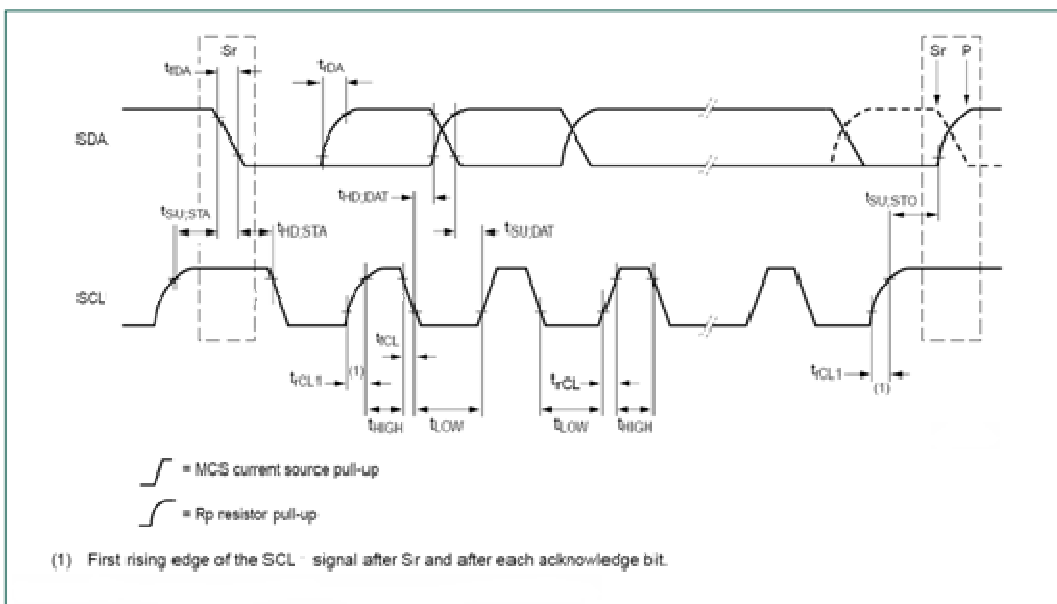


Figure 23: Timing definition for HS-mode devices on the I²C Port

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I²C Interface (Continued)

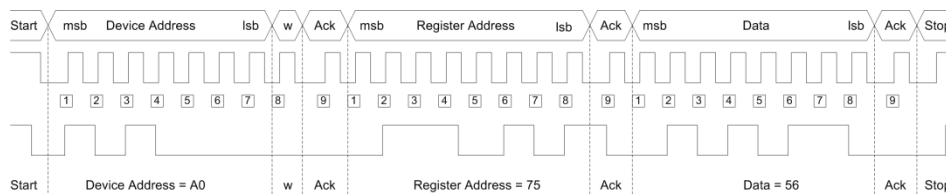


Figure 24: Write Cycle Diagram

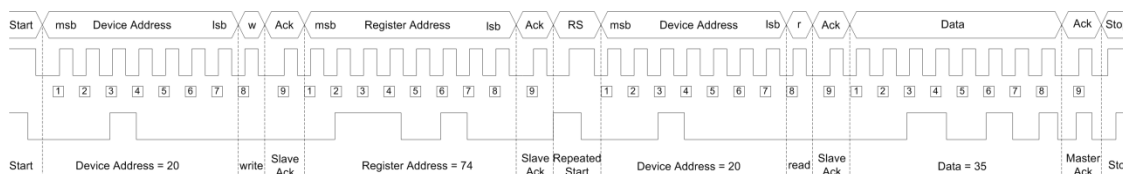


Figure 25: Read Cycle Diagram

Control Register Bit Definition

| Bit | Name | Value | Description |
|-------------------------------------|-----------|-------|--|
| Status, Address 00h | | | |
| 7:3 | Reserved | | |
| 2 | OCP | | Latched to 1 if the over current limit is reached. Write a "1" to reset the status flag. |
| 1 | OTP | | Latched to 1 if an over temperature event occurs. Write a "1" to reset the status flag. |
| 0 | FB_UVLO | | Latched to 1 if a FB_UVLO event occurs. Write a "1" to reset the status flag. |
| Vsel, Address 01h, (aka dac) | | | |
| 7 | EN | 1-d | Device enabled. |
| | | 0 | Device disabled. |
| 6:0 | VSEL[6:0] | | 7-bit DAC value to set V _{REF} . The default value is determined by the part ordering code. |

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Microsemi

| Bit | Name | Value | Description |
|------------------------------------|---------------------|-------|---|
| Ctrl1, Address 02h, (aka reg2) | | | |
| 7:6 | Reserved | 00-d | |
| 5 | DLY_DIS | 1-d | Disable 45ms delay on PGOOD. |
| | | 0 | 45ms delay on PGOOD is enabled. |
| 4 | ctrl1 | 0-d | TBD |
| 3 | SW_RATE | 1-d | Normal high efficiency rise rate. |
| | | 0 | Reduced switch node rise rate. |
| 2 | Reserved | 1-d | |
| | | 0 | |
| 1 | Reserved | 1-d | |
| | | 0 | |
| 0 | MODE | 1-d | PWM mode only – NO PSM. |
| | | 0 | Power Save Mode – allows discontinuous conduction. |
| Vendor ID, Address 03h (Read Only) | | | |
| 7:4 | VID[7:0] | 0010 | Microsemi Vendor ID . |
| 3:2 | A1A0 | 00 | Designates the slave address version. These bits will correspond to the two LSB bits. |
| 1:0 | VOUT | 00 | Designates the default output voltage version, 00=0.6V, 01=0.8V, 10=0.9V, 11=0.975V. |
| Ctrl2, Address 04h, (aka reg4) | | | |
| 7:6 | Reserved | | |
| 5 | GO | 1 | Writing to this bit starts a VOUT transition regardless of its initial value. |
| | | 0-d | The VOUT is ramped to the default VSEL Value. |
| 4 | Discharge | 1 | When the regulator is disabled, the output voltage is discharged through the SW pin. |
| | | 0-d | When the regulator is disabled, the output voltage Is not discharged. |
| 3 | PGOK (read only) | 1 | Is high when output is in regulation and V _{REF} has stabilized. |
| | | 0 | Is low during a output voltage transition or when the output is not in regulation. |
| 2:0 | SLEW | 000 | Reserved. |
| | | 001 | Reserved. |
| | | 010 | VOUT slews at 2mv/μs. |
| | | 011-d | VOUT Slews at 4mV/μs; this is the default setting. |
| | | 100 | VOUT slews at 8mV/μs. |
| | | 101 | VOUT slews at 16mv/μs. |
| | | 110 | VOUT slews at 32mv/μs. |
| | | 111 | VOUT slews at 64mV/μs. |

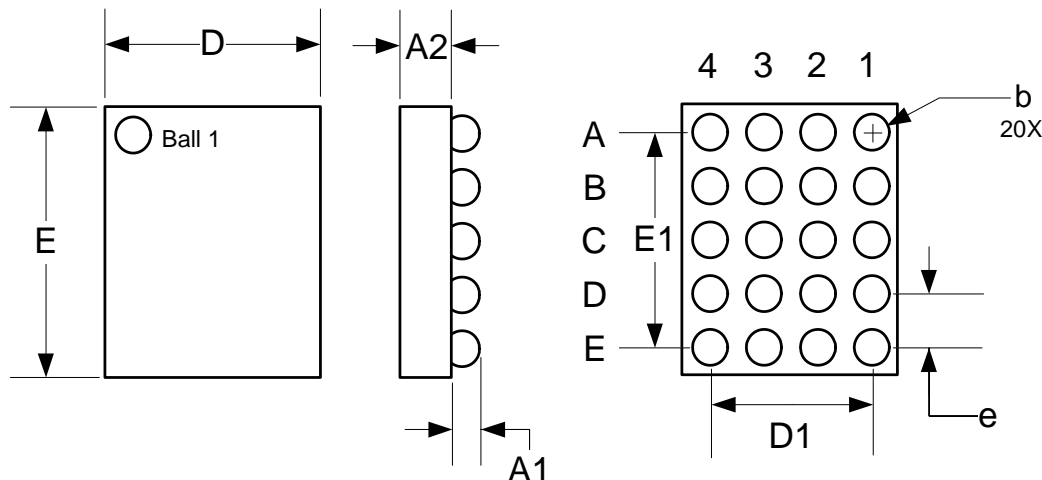
Note: -d is the default value at startup.

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Package Dimensions

WLCSP 20 Ball 0.4mm Pitch



| Dim | MILLIMETERS | | INCHES | |
|-----|-------------|-------|------------|--------|
| | MIN | MAX | MIN | MAX |
| A1 | 0.186 | 0.226 | 0.0073 | 0.0089 |
| A2 | 0.360 | 0.400 | 0.0142 | 0.0157 |
| b | 0.240 | 0.280 | 0.0094 | 0.0110 |
| D1 | 1.20 BSC | | 0.0472 BSC | |
| D | 1.630 | | 0.0642 | |
| e | 0.40 BSC | | 0.0157 BSC | |
| E1 | 1.60 BSC | | 0.0630 BSC | |
| E | 2.045 | | 0.0805 | |

Note:

1. Solder ball composition SnAgCu

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