

N-Channel Power MOSFET

600V, 1A, 10Ω

FEATURES

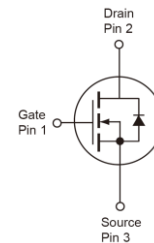
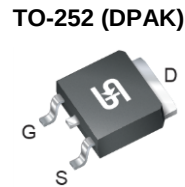
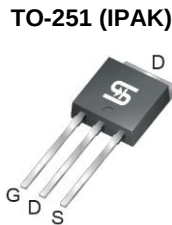
- Advanced planar process
- 100% avalanche tested
- Low $R_{DS(ON)}$ 8Ω (Typ.)
- Low gate charge typical @ 6.1 nC (Typ.)
- Low Crss typical @4.2pF (Typ.)

KEY PERFORMANCE PARAMETERS

PARAMETER	VALUE	UNIT
V_{DS}	600	V
$R_{DS(on)}$ (max)	10	Ω
Q_g	6.1	nC

APPLICATION

- Power Supply
- Lighting
- Charger



Notes: MSL 3 (Moisture Sensitivity Level) for TO-252 (D-PAK), SOT-223 per J-STD-020

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

PARAMETER	SYMBOL	IPAK/DPAK	SOT-223	UNIT
Drain-Source Voltage	V_{DS}	600		V
Gate-Source Voltage	V_{GS}	±30		V
Continuous Drain Current ^(Note 1)	I_D	1		A
		0.7		
Pulsed Drain Current ^(Note 2)	I_{DM}	4		A
Total Power Dissipation @ $T_C = 25^\circ\text{C}$	P_{DTOT}	39	2.1	W
Single Pulsed Avalanche Energy ^(Note 3)	E_{AS}	5		mJ
Single Pulsed Avalanche Current ^(Note 3)	I_{AS}	1		A
Peak Diode Recovery dv/dt ^(Note 4)	dv/dt	4.5		V/ns
Operating Junction and Storage Temperature Range	T_J, T_{STG}	- 55 to +150		°C

THERMAL PERFORMANCE

PARAMETER	SYMBOL	IPAK/DPAK	SOT-223	UNIT
Junction to Case Thermal Resistance	$R_{\theta JC}$	2.87	--	°C/W
Junction to Ambient Thermal Resistance	$R_{\theta JA}$	110	60	°C/W

Notes: $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistances. The case thermal reference is defined at the solder mounting surface of the drain pins. $R_{\theta JA}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design. $R_{\theta JA}$ shown below for single device operation on FR-4 PCB in still air.

ELECTRICAL SPECIFICATIONS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNIT
Static ^(Note 5)						
Drain-Source Breakdown Voltage	V _{GS} = 0V, I _D = 250μA	BV _{DSS}	600	--	--	V
Drain-Source On-State Resistance	V _{GS} = 10V, I _D = 0.5A	R _{DS(ON)}	--	8	10	Ω
Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 250μA	V _{GS(TH)}	2.5	3.5	4.5	V
Zero Gate Voltage Drain Current	V _{DS} = 600V, V _{GS} = 0V	I _{DSS}	--	--	10	μA
Gate Body Leakage	V _{GS} = ±30V, V _{DS} = 0V	I _{GSS}	--	--	±100	nA
Forward Transfer Conductance	V _{DS} = 10V, I _D = 0.5A	g _{fs}	--	0.8	--	S
Dynamic ^(Note 6)						
Total Gate Charge	V _{DS} = 480V, I _D = 1A, V _{GS} = 10V	Q _g	--	6.1	--	nC
Gate-Source Charge		Q _{gs}	--	1.4	--	
Gate-Drain Charge		Q _{gd}	--	3.3	--	
Input Capacitance	V _{DS} = 25V, V _{GS} = 0V, f = 1.0MHz	C _{iss}	--	138	--	pF
Output Capacitance		C _{oss}	--	17.1	--	
Reverse Transfer Capacitance		C _{rss}	--	4.2	--	
Gate Resistance	F = 1MHz, open drain	R _g	--	12.5	--	Ω
Switching ^(Note 7)						
Turn-On Delay Time	V _{DD} = 300V, R _G =25Ω I _D = 1A, V _{GS} = 10V	t _{d(on)}	--	7.7	--	ns
Turn-On Rise Time		t _r	--	6.8	--	
Turn-Off Delay Time		t _{d(off)}	--	15.3	--	
Turn-Off Fall Time		t _f	--	14.9	--	
Source-Drain Diode ^(Note 5)						
Diode Forward Voltage	I _S = 1A, V _{GS} = 0V	V _{SD}	--	0.9	1.4	V
Source Current	Integral reverse diode In the MOSFET	I _S	--	--	1	A
Source Current (Pulse)		I _{SM}	--	--	4	

Notes:

- Current limited by package.
- Pulse width limited by the maximum junction temperature.
- $L = 10\text{mH}, I_{AS} = 1A, V_{DD} = 50V, R_G = 25\Omega$, Starting $T_J = 25^\circ\text{C}$.
- $I_{SD} \leq 1A, V_{DD} \leq BV_{DSS}, di/dt \leq 200A/\mu s$, Starting $T_J = 25^\circ\text{C}$.
- Pulse test: $PW \leq 300\mu s$, duty cycle $\leq 2\%$.
- For DESIGN AID ONLY, not subject to production testing.
- Switching time is essentially independent of operating temperature.

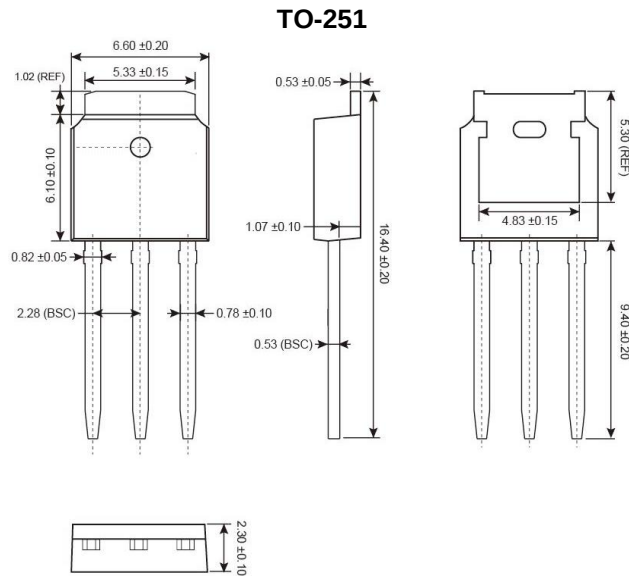
ORDERING INFORMATION

PART NO.	PACKAGE	PACKING
TSM1NB60CH C5G	TO-251	75 pcs / Tube
TSM1NB60CP ROG	TO-252	2,500 pcs / 13" Reel
TSM1NB60CW RPG	SOT-223	2,500 pcs / 13" Reel

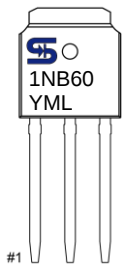
Note:

1. Compliant to RoHS Directive 2011/65/EU and in accordance to WEEE 2002/96/EC
2. Halogen-free according to IEC 61249-2-21 definition

PACKAGE OUTLINE DIMENSIONS (Unit: Millimeters)



MARKING DIAGRAM



Y = Year Code

M = Month Code for Halogen Free Product

O =Jan **P** =Feb **Q** =Mar **R** =Apr

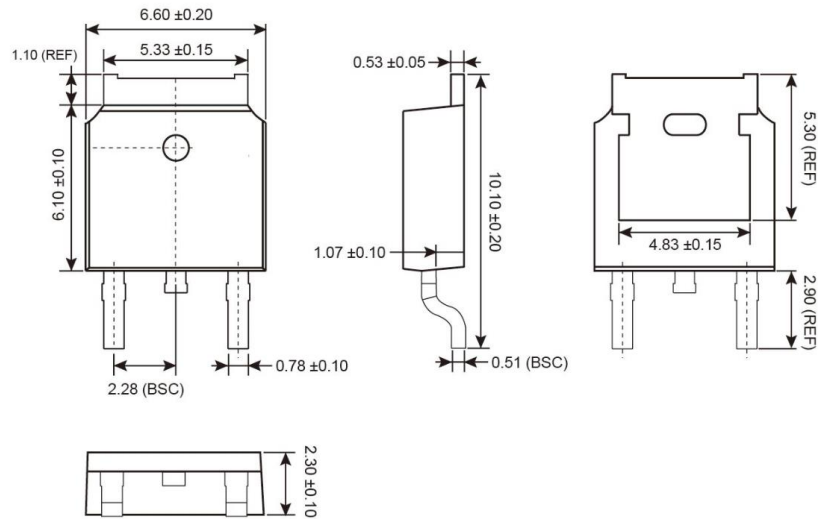
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W =Sep **X** =Oct **Y** =Nov **Z** =Dec

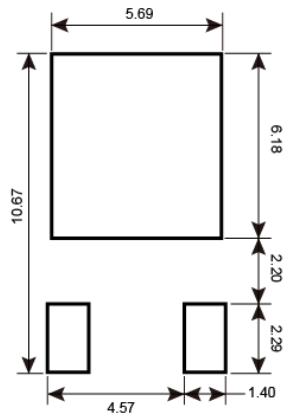
L = Lot Code (1~9, A~Z)

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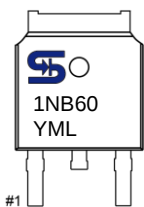
TO-252



SUGGESTED PAD LAYOUT



MARKING DIAGRAM



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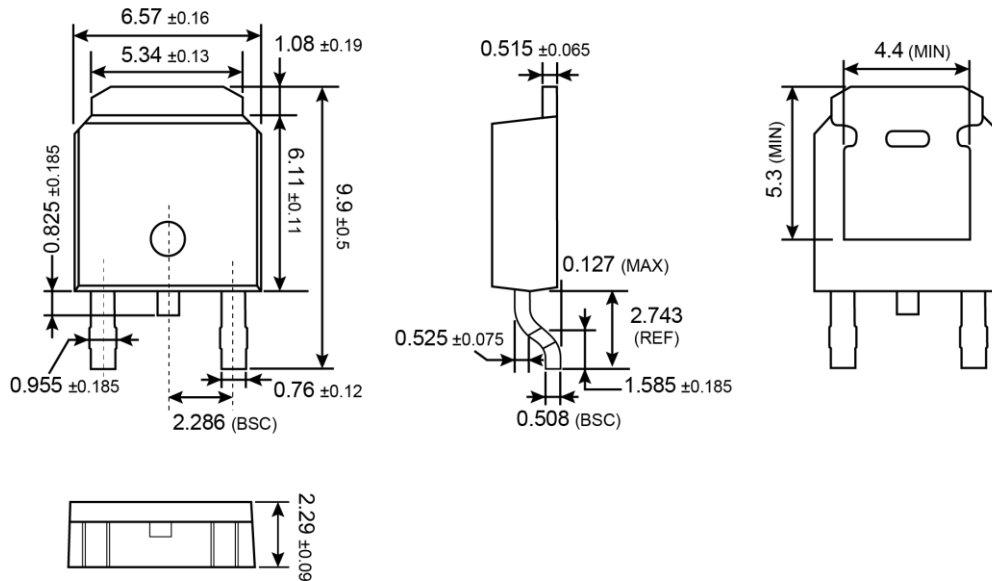
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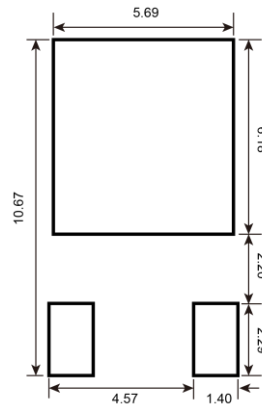
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PACKAGE OUTLINE DIMENSIONS (Unit: Millimeters)

TO-252



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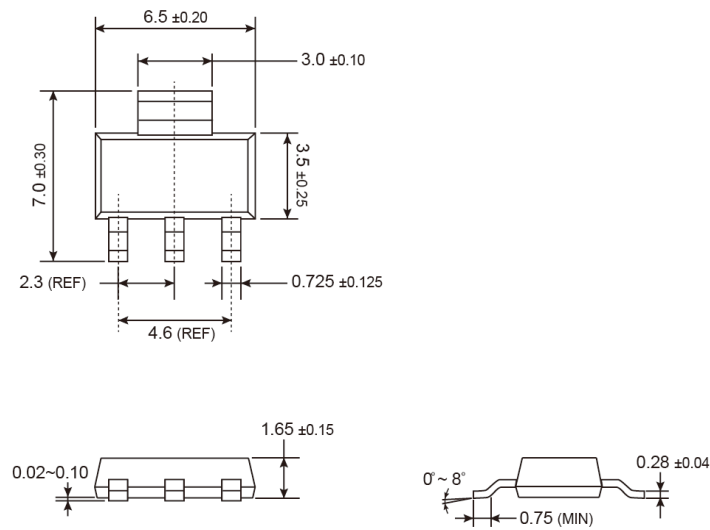
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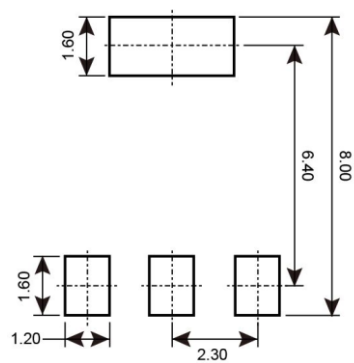
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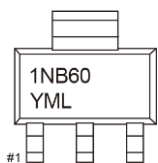
SOT-223



SUGGESTED PAD LAYOUT



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