

74AHC595-Q100; 74AHCT595-Q100

8-bit serial-in/serial-out or parallel-out shift register with output latches

Rev. 1 — 12 July 2012

Product data sheet

1. General description

The 74AHC595-Q100; 74AHCT595-Q100 are high-speed Si-gate CMOS devices and are pin compatible with Low-power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard No. 7A.

The 74AHC595-Q100; 74AHCT595-Q100 are 8-stage serial shift registers with a storage register and 3-state outputs. The registers have separate clocks.

Data is shifted on the positive-going transitions of the shift register clock input (SHCP). The data in each register is transferred to the storage register on a positive-going transition of the storage register clock input (STCP). If both clocks are connected together, the shift register is always one clock pulse ahead of the storage register.

The shift register has a serial input (DS) and a serial standard output (Q7S) for cascading. It is also provided with asynchronous reset (active LOW) for all 8 shift register stages. The storage register has 8 parallel 3-state bus driver outputs. Data in the storage register appears at the output whenever the output enable input ($\overline{OE}$) is LOW.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
 - ◆ Specified from $-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$ and from $-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$
- Balanced propagation delays
- All inputs have Schmitt trigger action
- Inputs accept voltages higher than V_{CC}
- Input levels:
 - ◆ The 74AHC595-Q100 operates with CMOS input levels
 - ◆ The 74AHCT595-Q100 operates with TTL input levels
- ESD protection:
 - ◆ MIL-STD-883, method 3015 exceeds 2000 V
 - ◆ HBM JESD22-A114F exceeds 2000 V
 - ◆ MM JESD22-A115-A exceeds 200 V ($C = 200\text{ pf}$, $R = 0\text{ }\Omega$)
- Multiple package options

3. Applications

- Serial-to-parallel data conversion
- Remote control holding register

4. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74AHC595-Q100				
74AHC595D-Q100	–40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74AHC595PW-Q100	–40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
74AHC595BQ-Q100	–40 °C to +125 °C	DHVQFN16	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 × 3.5 × 0.85 mm	SOT763-1
74AHCT595-Q100				
74AHCT595D-Q100	–40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74AHCT595PW-Q100	–40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
74AHCT595BQ-Q100	–40 °C to +125 °C	DHVQFN16	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 × 3.5 × 0.85 mm	SOT763-1

5. Functional diagram

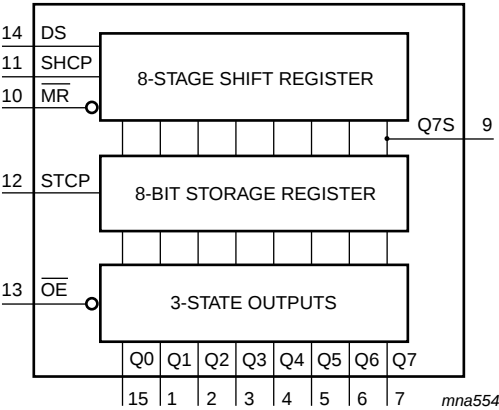


Fig 1. Functional diagram

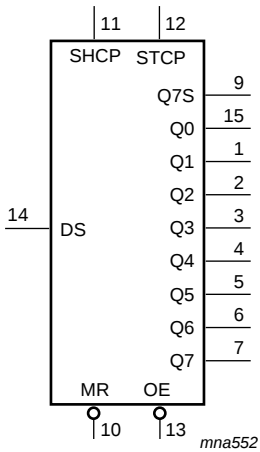


Fig 2. Logic symbol

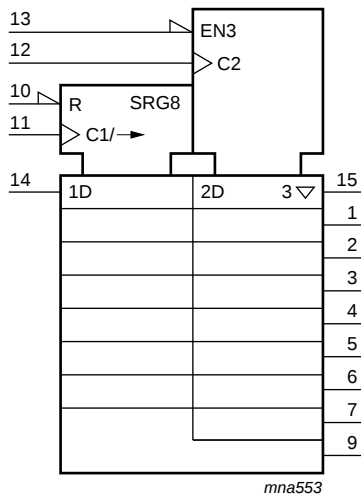


Fig 3. IEC logic symbol

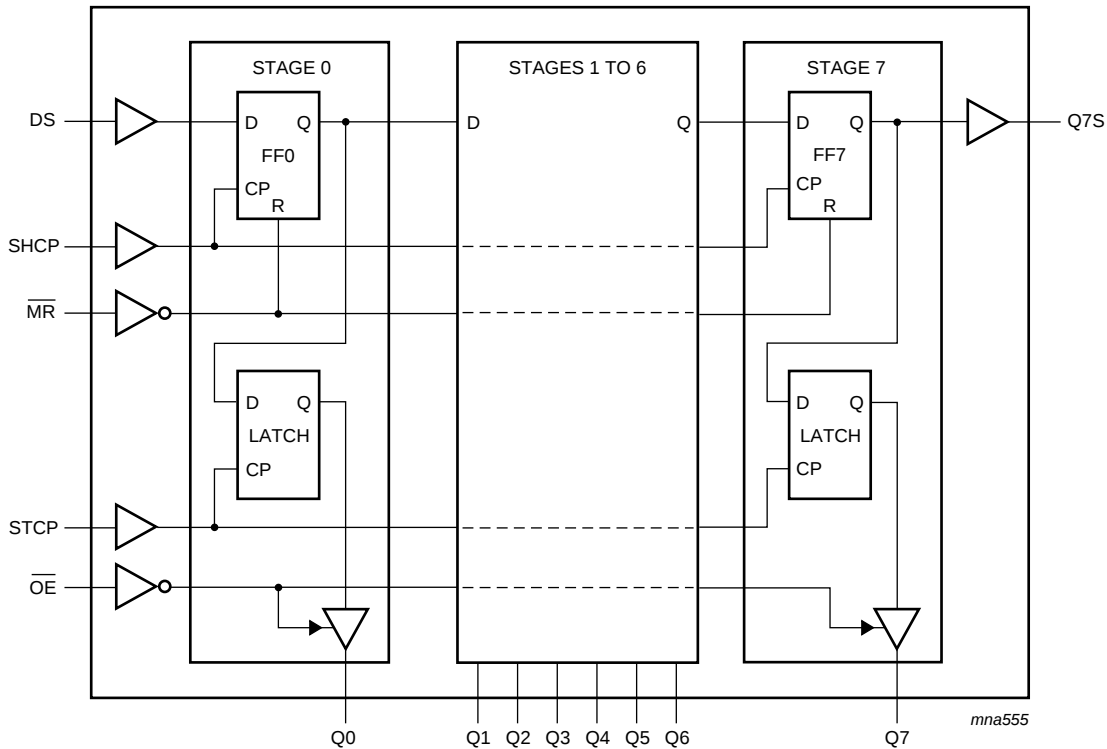
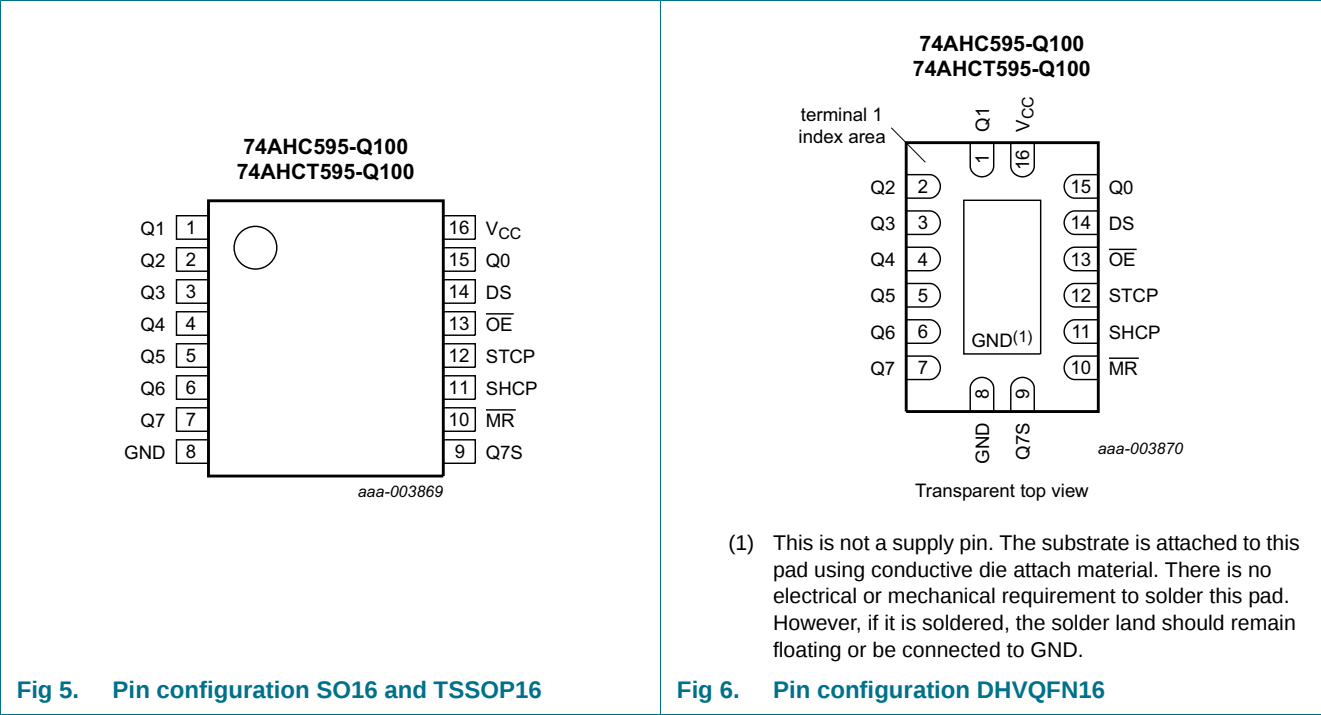


Fig 4. Logic diagram

6. Pinning information

6.1 Pinning



6.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
Q1	1	parallel data output 1
Q2	2	parallel data output 2
Q3	3	parallel data output 3
Q4	4	parallel data output 4
Q5	5	parallel data output 5
Q6	6	parallel data output 6
Q7	7	parallel data output 7
GND	8	ground (0 V)
Q7S	9	serial data output
MR	10	master reset (active LOW)
SHCP	11	shift register clock input
STCP	12	storage register clock input
OE	13	output enable input (active LOW)
DS	14	serial data input
Q0	15	parallel data output 0
V _{CC}	16	supply voltage

7. Functional description

Table 3. Function table^[1]

Control				Input	Output		Function
SHCP	STCP	$\overline{OE}$	$\overline{MR}$	DS	Q7S	Qn	
X	X	L	L	X	L	NC	a LOW-level on $\overline{MR}$ only affects the shift registers
X	↑	L	L	X	L	L	empty shift register loaded into storage register
X	X	H	L	X	L	Z	shift register clear; parallel outputs in high-impedance OFF-state
↑	X	L	H	H	Q6S	NC	logic HIGH-level shifted into shift register stage 0. Contents of all shift register stages shifted through, e.g. previous state of stage 6 (internal Q6S) appears on the serial output (Q7S).
X	↑	L	H	X	NC	QnS	contents of shift register stages (internal QnS) are transferred to the storage register and parallel output stages
↑	↑	L	H	X	Q6S	QnS	contents of shift register shifted through; previous contents of the shift register is transferred to the storage register and the parallel output stages

- [1] H = HIGH voltage state;
 L = LOW voltage state;
 ↑ = LOW-to-HIGH transition;
 X = don't care;
 NC = no change;
 Z = high-impedance OFF-state.

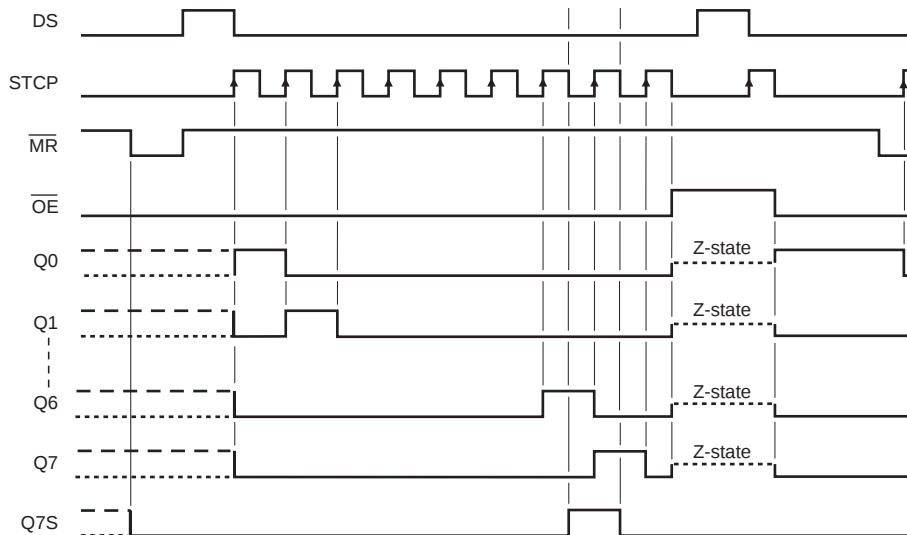


Fig 7. Timing diagram

8. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+7.0	V
V_I	input voltage		-0.5	+7.0	V
I_{IK}	input clamping current	$V_I < -0.5$ V	[1] -20	-	mA
I_{OK}	output clamping current	$V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V	[1] -20	+20	mA
I_O	output current	$V_O = -0.5$ V to $(V_{CC} + 0.5)$ V	-25	+25	mA
I_{CC}	supply current		-	+75	mA
I_{GND}	ground current		-75	-	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation	$T_{amb} = -40$ °C to +125 °C	[2] -	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SO16 packages: above 70 °C the value of P_{tot} derates linearly at 8 mW/K.

For TSSOP16 packages: above 60 °C the value of P_{tot} derates linearly at 5.5 mW/K.

For DHVQFN16 packages: above 60 °C the value of P_{tot} derates linearly at 4.5 mW/K.

9. Recommended operating conditions

Table 5. Operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
74AHC595-Q100						
V_{CC}	supply voltage		2.0	5.0	5.5	V
V_I	input voltage		0	-	5.5	V
V_O	output voltage		0	-	V_{CC}	V
T_{amb}	ambient temperature		-40	+25	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 3.0$ V to 3.6 V	-	-	100	ns/V
		$V_{CC} = 4.5$ V to 5.5 V	-	-	20	ns/V
74AHCT595-Q100						
V_{CC}	supply voltage		4.5	5.0	5.5	V
V_I	input voltage		0	-	5.5	V
V_O	output voltage		0	-	V_{CC}	V
T_{amb}	ambient temperature		-40	+25	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 4.5$ V to 5.5 V	-	-	20	ns/V

10. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74AHC595-Q100										
V _{IH}	HIGH-level input voltage	V _{CC} = 2.0 V	1.5	-	-	1.5	-	1.5	-	V
		V _{CC} = 3.0 V	2.1	-	-	2.1	-	2.1	-	V
		V _{CC} = 5.5 V	3.85	-	-	3.85	-	3.85	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 2.0 V	-	-	0.5	-	0.5	-	0.5	V
		V _{CC} = 3.0 V	-	-	0.9	-	0.9	-	0.9	V
		V _{CC} = 5.5 V	-	-	1.65	-	1.65	-	1.65	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}								
		I _O = –50 μA; V _{CC} = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I _O = –50 μA; V _{CC} = 3.0 V	2.9	3.0	-	2.9	-	2.9	-	V
		I _O = –50 μA; V _{CC} = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I _O = –4.0 mA; V _{CC} = 3.0 V	2.58	-	-	2.48	-	2.40	-	V
		I _O = –8.0 mA; V _{CC} = 4.5 V	3.94	-	-	3.80	-	3.70	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}								
		I _O = 50 μA; V _{CC} = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 50 μA; V _{CC} = 3.0 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 50 μA; V _{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 4.0 mA; V _{CC} = 3.0 V	-	-	0.36	-	0.44	-	0.55	V
		I _O = 8.0 mA; V _{CC} = 4.5 V	-	-	0.36	-	0.44	-	0.55	V
I _I	input leakage current	V _I = 5.5 V or GND; V _{CC} = 0 V to 5.5 V	-	-	0.1	-	1.0	-	2.0	μA
I _{OZ}	OFF-state output current	V _I = V _{IH} or V _{IL} ; V _O = V _{CC} or GND; V _{CC} = 5.5 V	-	-	±0.25	-	±2.5	-	±10	μA
I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 5.5 V	-	-	4.0	-	40	-	80	μA
C _I	input capacitance		-	3	10	-	10	-	10	pF
74AHCT595-Q100										
V _{IH}	HIGH-level input voltage	V _{CC} = 4.5 V to 5.5 V	2.0	-	-	2.0	-	2.0	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 4.5 V to 5.5 V	-	-	0.8	-	0.8	-	0.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V								
		I _O = –50 μA	4.4	4.5	-	4.4	-	4.4	-	V
		I _O = –8.0 mA	3.94	-	-	3.80	-	3.70	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V								
		I _O = 50 μA	-	0	0.1	-	0.1	-	0.1	V
		I _O = 8.0 mA	-	-	0.36	-	0.44	-	0.55	V

Table 6. Static characteristics ...continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
I_I	input leakage current	$V_I = 5.5 \text{ V}$ or GND; $V_{CC} = 0 \text{ V}$ to 5.5 V	-	-	0.1	-	1.0	-	2.0	μA
I_{OZ}	OFF-state output current	$V_I = V_{IH}$ or V_{IL} ; $V_O = V_{CC}$ or GND per input pin; other inputs at V_{CC} or GND; $I_O = 0 \text{ A}$; $V_{CC} = 5.5 \text{ V}$	-	-	± 0.25	-	± 2.5	-	± 10	μA
I_{CC}	supply current	$V_I = V_{CC}$ or GND; $I_O = 0 \text{ A}$; $V_{CC} = 5.5 \text{ V}$	-	-	4.0	-	40	-	80	μA
ΔI_{CC}	additional supply current	per input pin; $V_I = V_{CC} - 2.1 \text{ V}$; other inputs at V_{CC} or GND; $I_O = 0 \text{ A}$; $V_{CC} = 4.5 \text{ V}$ to 5.5 V	-	-	1.35	-	1.5	-	1.5	mA
C_I	input capacitance		-	3	10	-	10	-	10	pF

11. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see [Figure 13](#).

Symbol	Parameter	Conditions	25 °C			−40 °C to +85 °C		−40 °C to +125 °C		Unit		
			Min	Typ ^[1]	Max	Min	Max	Min	Max			
74AHC595-Q100												
t _{pd}	propagation delay	SHCP to Q7S; see Figure 8 ^[2]										
		V _{CC} = 3.0 V to 3.6 V										
		C _L = 15 pF	-	5.7	13.0	1.0	15.0	1.0	16.5	ns		
		C _L = 50 pF	-	7.7	16.5	1.0	18.5	1.0	20.1	ns		
		V _{CC} = 4.5 V to 5.5 V										
		C _L = 15 pF	-	4.0	8.2	1.0	9.4	1.0	10.5	ns		
		C _L = 50 pF	-	5.4	10.0	1.0	11.4	1.0	12.5	ns		
		STCP to Qn; see Figure 9 ^[2]										
		V _{CC} = 3.0 V to 3.6 V										
		C _L = 15 pF	-	5.9	11.9	1.0	13.5	1.0	15.0	ns		
		C _L = 50 pF	-	7.7	15.4	1.0	17.0	1.0	18.5	ns		
		V _{CC} = 4.5 V to 5.5 V										
		C _L = 15 pF	-	4.2	7.4	1.0	8.5	1.0	9.5	ns		
		C _L = 50 pF	-	5.5	9.0	1.0	10.5	1.0	11.5	ns		
		t _{en}	enable time	$\overline{\text{MR}}$ to Q7S; see Figure 11 ^[3]								
				V _{CC} = 3.0 V to 3.6 V								
C _L = 15 pF	-			5.9	12.8	1.0	13.7	1.0	15.0	ns		
C _L = 50 pF	-			7.4	16.3	1.0	17.2	1.0	18.7	ns		
V _{CC} = 4.5 V to 5.5 V												
C _L = 15 pF	-			4.4	8.0	1.0	9.1	1.0	10.0	ns		
C _L = 50 pF	-			5.6	10.0	1.0	11.1	1.0	12.0	ns		
t _{dis}	disable time			$\overline{\text{OE}}$ to Qn; see Figure 12 ^[4]								
				V _{CC} = 3.0 V to 3.6 V								
				C _L = 15 pF	-	5.6	11.5	1.0	13.5	1.0	15.0	ns
		C _L = 50 pF	-	7.4	15.0	1.0	17.0	1.0	18.5	ns		
		V _{CC} = 4.5 V to 5.5 V										
C _L = 15 pF	-	4.0	8.6	1.0	10.0	1.0	11.0	ns				
C _L = 50 pF	-	5.3	10.6	1.0	12.0	1.0	13.0	ns				
t _{dis}	disable time	$\overline{\text{OE}}$ to Qn; see Figure 12 ^[5]										
		V _{CC} = 3.0 V to 3.6 V										
		C _L = 15 pF	-	5.4	11.0	1.0	13.0	1.0	14.5	ns		
		C _L = 50 pF	-	8.7	15.7	1.0	16.2	1.0	17.5	ns		
		V _{CC} = 4.5 V to 5.5 V										
C _L = 15 pF	-	3.8	8.0	1.0	9.5	1.0	10.5	ns				
C _L = 50 pF	-	5.8	10.3	1.0	11.0	1.0	12.0	ns				

Table 7. Dynamic characteristics ...continuedVoltages are referenced to GND (ground = 0 V); for test circuit see [Figure 13](#).

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	Min	Max	
f _{max}	maximum frequency	SHCP or STCP; see Figure 8 and 9								
		V _{CC} = 3.0 V to 3.6 V	80	125	-	60	-	40	-	MHz
		V _{CC} = 4.5 V to 5.5 V	130	170	-	110	-	90	-	MHz
t _w	pulse width	SHCP HIGH or LOW; see Figure 8								
		V _{CC} = 3.0 V to 3.6 V	5.0	-	-	5.0	-	5.0	-	ns
		V _{CC} = 4.5 V to 5.5 V	5.0	-	-	5.0	-	5.0	-	ns
		STCP HIGH or LOW; see Figure 9								
		V _{CC} = 3.0 V to 3.6 V	5.0	-	-	5.0	-	5.0	-	ns
		V _{CC} = 4.5 V to 5.5 V	5.0	-	-	5.0	-	5.0	-	ns
		MR LOW; see Figure 11								
		V _{CC} = 3.0 V to 3.6 V	5.0	-	-	5.0	-	5.0	-	ns
t _{su}	set-up time	DS to SHCP; see Figure 9								
		V _{CC} = 3.0 V to 3.6 V	3.5	-	-	3.5	-	3.5	-	ns
		V _{CC} = 4.5 V to 5.5 V	3.0	-	-	3.0	-	3.0	-	ns
		SHCP to STCP; see Figure 10								
		V _{CC} = 3.0 V to 3.6 V	8.5	-	-	8.5	-	8.5	-	ns
		V _{CC} = 4.5 V to 5.5 V	5.0	-	-	5.0	-	5.0	-	ns
t _h	hold time	DS to SHCP; see Figure 10								
		V _{CC} = 3.0 V to 3.6 V	1.5	-	-	1.5	-	1.5	-	ns
		V _{CC} = 4.5 V to 5.5 V	2.0	-	-	2.0	-	2.0	-	ns
t _{rec}	recovery time	MR to SHCP; see Figure 11								
		V _{CC} = 3.0 V to 3.6 V	3.0	-	-	3.0	-	3.0	-	ns
		V _{CC} = 4.5 V to 5.5 V	2.5	-	-	2.5	-	2.5	-	ns
C _{PD}	power dissipation capacitance	f _i = 1 MHz; V _I = GND to V _{CC} [6] [7]	-	180	-	-	-	-	-	pF

74AHCT595-Q100; V_{CC} = 4.5 V to 5.5 V

t _{pd}	propagation delay	SHCP to Q7S; see Figure 8 [2]								
		C _L = 15 pF	-	3.8	8.2	1.0	9.0	1.0	10.0	ns
		C _L = 50 pF	-	5.2	10.0	1.0	11.0	1.0	12.0	ns
		STCP to Qn; see Figure 9 [2]								
		C _L = 15 pF	-	4.0	7.4	1.0	8.5	1.0	9.5	ns
		C _L = 50 pF	-	5.3	9.0	1.0	10.5	1.0	11.5	ns
		MR to Q7S; see Figure 11 [3]								
		C _L = 15 pF	-	4.6	8.2	1.0	9.5	1.0	10.5	ns
		C _L = 50 pF	-	5.8	10.5	1.0	11.5	1.0	12.5	ns

Table 7. Dynamic characteristics ...continuedVoltages are referenced to GND (ground = 0 V); for test circuit see [Figure 13](#).

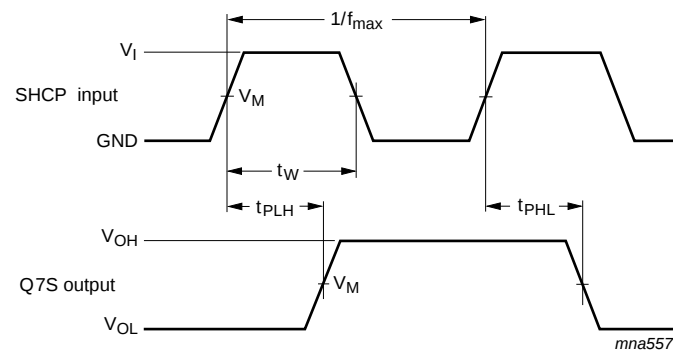
Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	Min	Max	
t _{en}	enable time	$\overline{\text{OE}}$ to Qn; see Figure 12 ^[4]								
		C _L = 15 pF	-	4.8	9.0	1.0	11.0	1.0	12.0	ns
		C _L = 50 pF	-	6.2	11.6	1.0	13.0	1.0	14.5	ns
t _{dis}	disable time	$\overline{\text{OE}}$ to Qn; see Figure 12 ^[5]								
		C _L = 15 pF	-	3.6	6.9	1.0	8.0	1.0	9.0	ns
		C _L = 50 pF	-	5.8	10.3	1.0	11.0	1.0	12.0	ns
f _{max}	maximum frequency	SHCP and STCP; see Figure 8 and Figure 9	130	170	-	110	-	90	-	MHz
t _w	pulse width	SHCP HIGH or LOW; see Figure 8	5.0	-	-	5.0	-	5.0	-	ns
		STCP HIGH or LOW; see Figure 9	5.0	-	-	5.0	-	5.0	-	ns
		$\overline{\text{MR}}$ LOW; see Figure 11	5.0	-	-	5.0	-	5.0	-	ns
t _{su}	set-up time	DS to SHCP; see Figure 9	3.0	-	-	3.0	-	3.0	-	ns
		SHCP to STCP; see Figure 10	5.0	-	-	5.0	-	5.0	-	ns
t _h	hold time	DS to SHCP; see Figure 10	2.0	-	-	2.0	-	2.0	-	ns
t _{rec}	recovery time	$\overline{\text{MR}}$ to SHCP; see Figure 11	3.0	-	-	3.0	-	3.0	-	ns
C _{PD}	power dissipation capacitance	f _i = 1 MHz; V _I = GND to V _{CC} ^[6] ^[7]	-	190	-	-	-	-	-	pF

[1] Typical values are measured at nominal supply voltage.

[2] t_{pd} is the same as t_{PHL} and t_{PLH}.[3] t_{pd} is the same as t_{PHL} only.[4] t_{en} is the same as t_{PZL} and t_{PZH}.[5] t_{dis} is the same as t_{PLZ} and t_{PHZ}.[6] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).P_D = C_{PD} × V_{CC}² × f_i + Σ(C_L × V_{CC}² × f_o) where:f_i = input frequency in MHz;f_o = output frequency in MHz;Σ(C_L × V_{CC}² × f_o) = sum of outputs;C_L = output load capacitance in pF;V_{CC} = supply voltage in V.

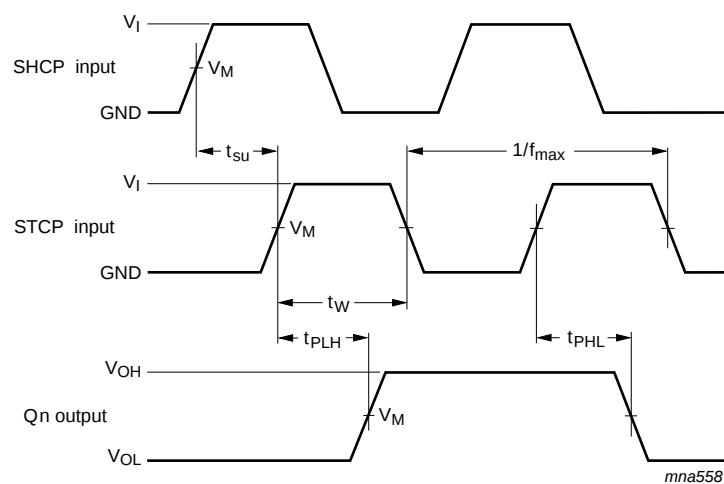
[7] All 9 outputs switching.

12. Waveforms



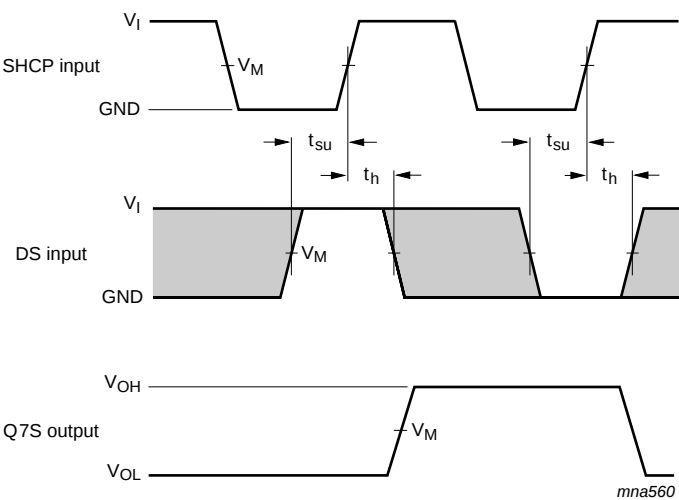
Measurement points are given in [Table 8](#).
 V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 8. Shift clock pulse, maximum frequency and input to output propagation delays



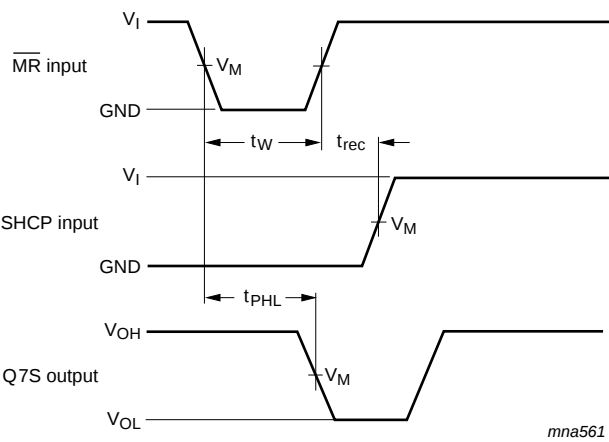
Measurement points are given in [Table 8](#).
 V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 9. Storage clock to output propagation delays



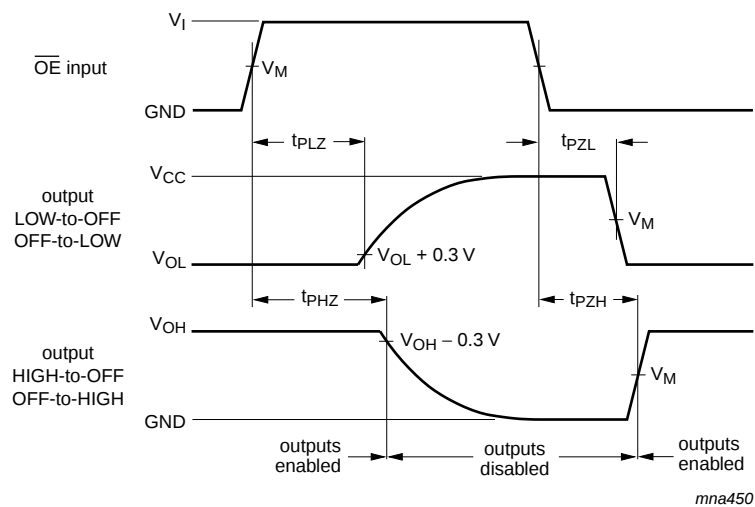
Measurement points are given in [Table 8](#).
The shaded areas indicate when the input is permitted to change for predictable output performance.
 V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 10. Data set-up and hold times



Measurement points are given in [Table 8](#).
 V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 11. Master reset to output propagation delays



Measurement points are given in [Table 8](#).
 V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 12. Enable and disable times

Table 8. Measurement points

Type	Input	Output
	V_M	V_M
74AHC595-Q100	$0.5V_{CC}$	$0.5V_{CC}$
74AHCT595-Q100	1.5 V	$0.5V_{CC}$

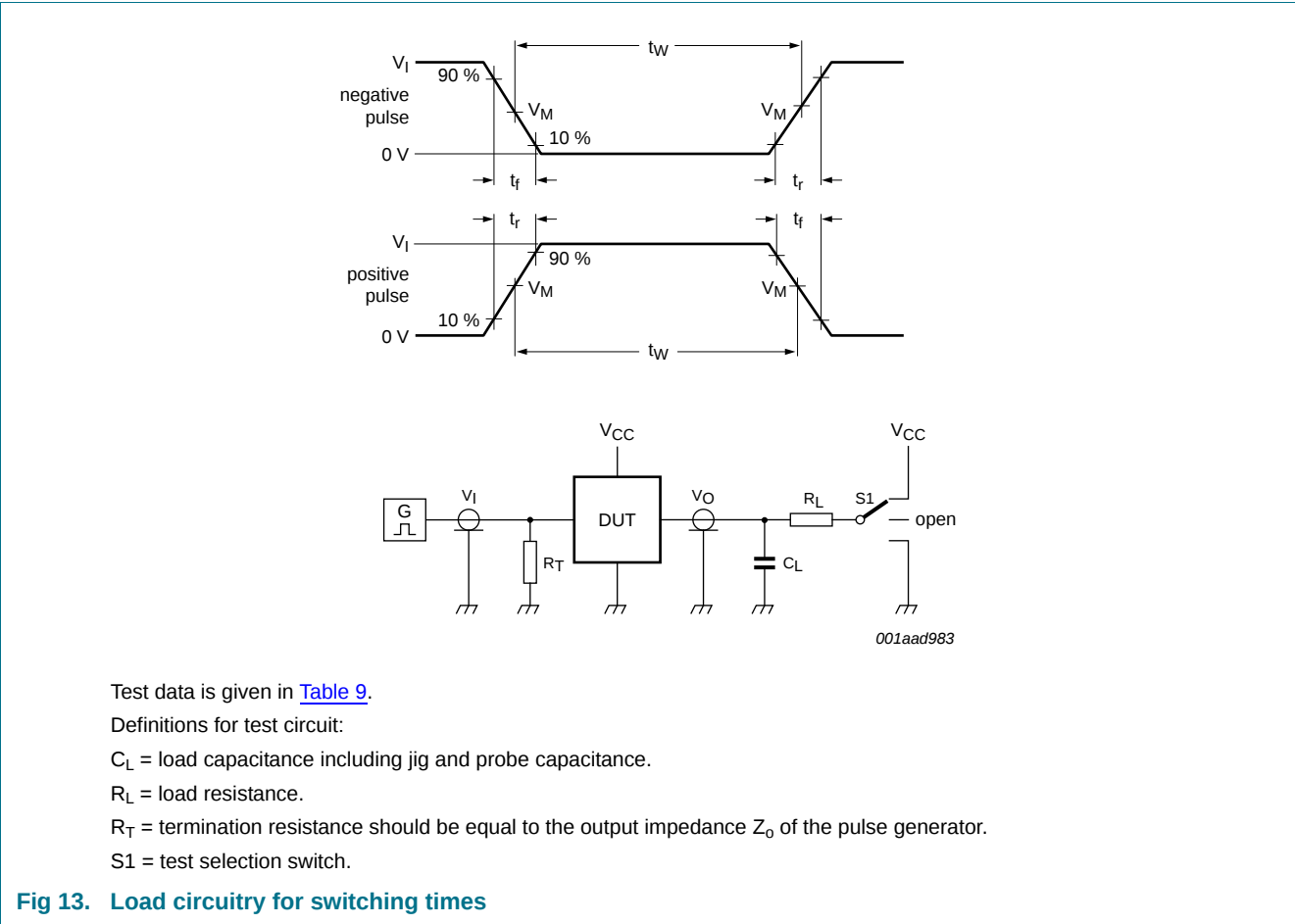
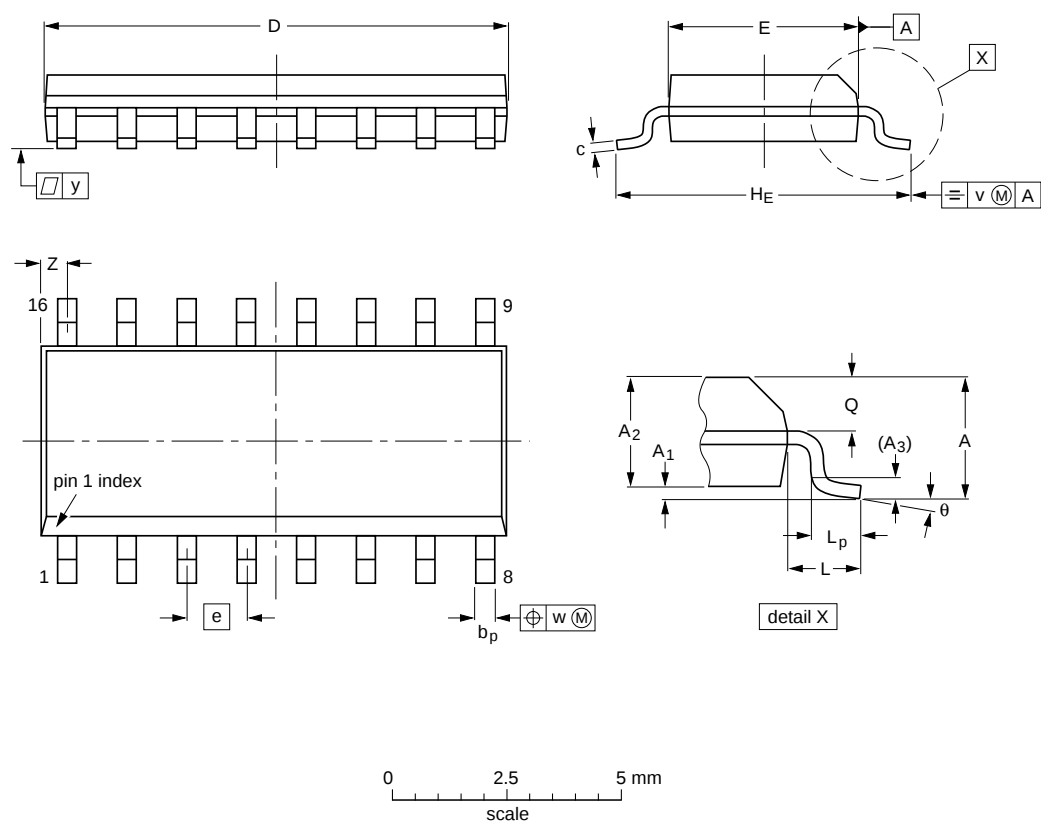


Table 9. Test data

Type	Input		Load		S1 position		
	V_I	t_r, t_f	C_L	R_L	t_{PHL}, t_{PLH}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
74AHC595-Q100	V_{CC}	≤ 3.0 ns	15 pF, 50 pF	1 k Ω	open	GND	V_{CC}
74AHCT595-Q100	3.0 V	≤ 3.0 ns	15 pF, 50 pF	1 k Ω	open	GND	V_{CC}

13. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mmSOT109-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	z ⁽¹⁾	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

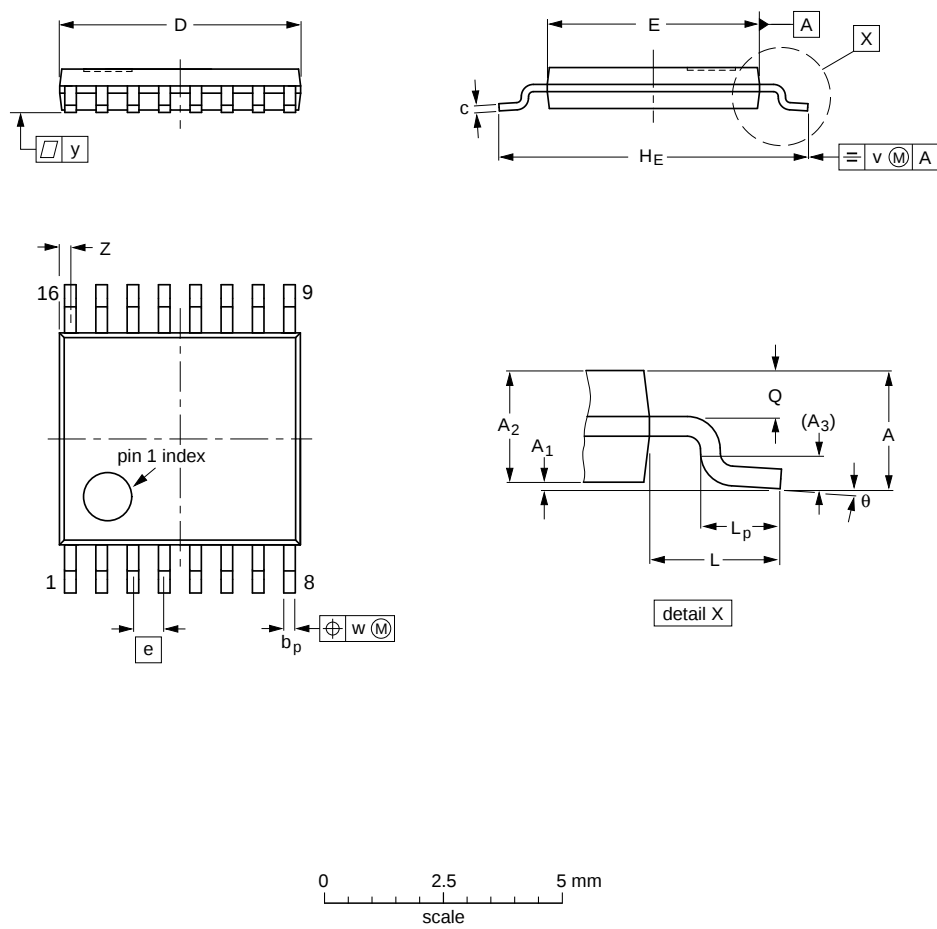
Note
1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT109-1	076E07	MS-012				99-12-27 03-02-19

Fig 14. Package outline SOT109-1 (SO16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽²⁾	e	H _E	L	L _p	Q	v	w	y	z ⁽¹⁾	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8° 0°

Notes

- 1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
- 2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT403-1		MO-153				99-12-27 03-02-18

Fig 15. Package outline SOT403-1 (TSSOP16)

DHVQFN16: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads;
16 terminals; body 2.5 x 3.5 x 0.85 mm

SOT763-1

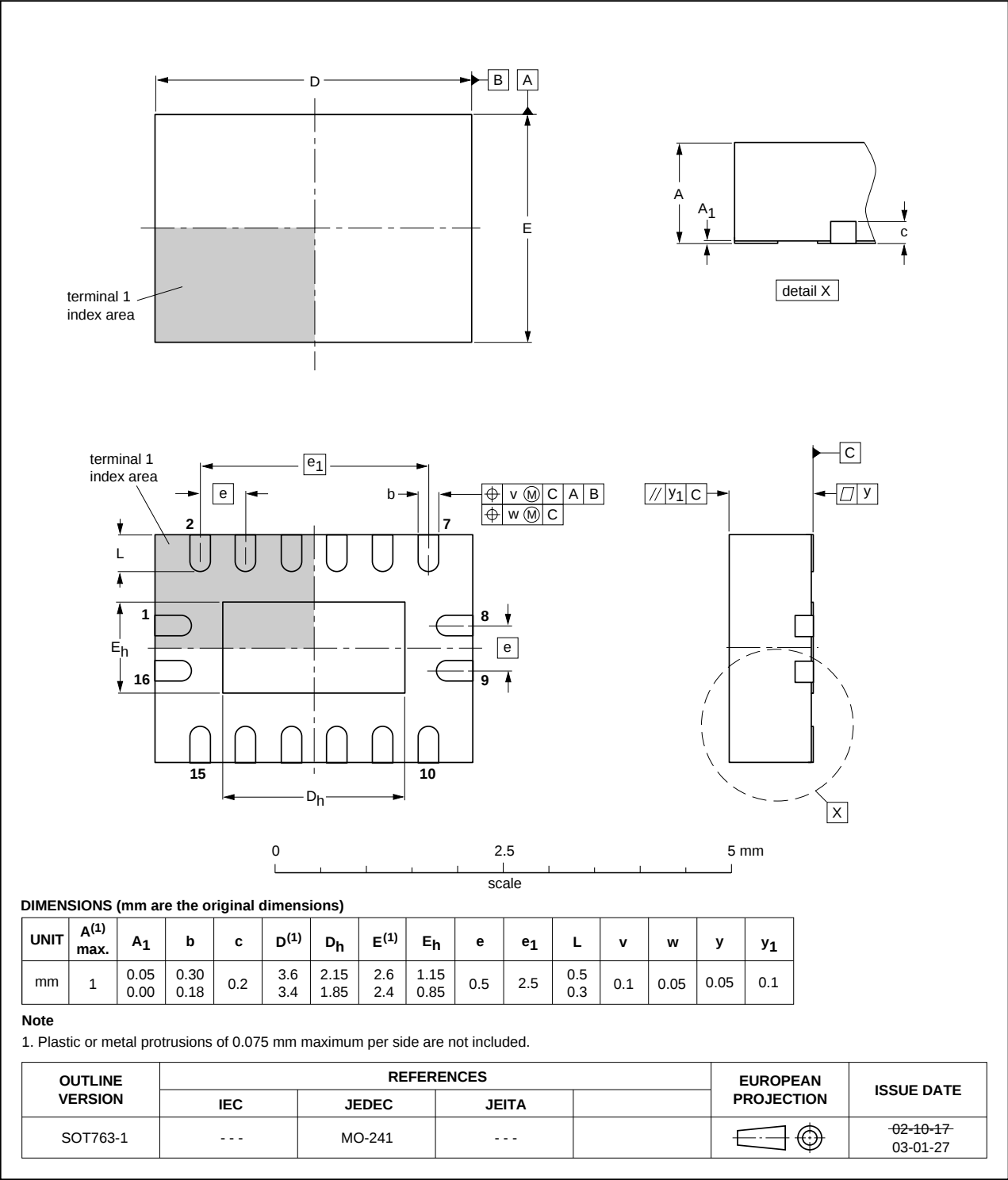


Fig 16. Package outline SOT763-1 (DHVQFN16)

14. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic
MIL	Military

15. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74AHC_AHCT595_Q100 v.1	20120712	Product data sheet	-	-

16. Legal information

16.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nexperia.com>.

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18. Contents

1	General description	1
2	Features and benefits	1
3	Applications	2
4	Ordering information	2
5	Functional diagram	2
6	Pinning information	4
6.1	Pinning	4
6.2	Pin description	4
7	Functional description	5
8	Limiting values	6
9	Recommended operating conditions	6
10	Static characteristics	7
11	Dynamic characteristics	9
12	Waveforms	12
13	Package outline	16
14	Abbreviations	19
15	Revision history	19
16	Legal information	20
16.1	Data sheet status	20
16.2	Definitions	20
16.3	Disclaimers	20
16.4	Trademarks	21
17	Contact information	21
18	Contents	22