HARRIS SEMICONDUCTOR

HFA3724

400MHz Quadrature IF Modulator/Demodulator

August 1997

Features

- **Integrates all IF Transmit and Receive Functions**
- **Broad Frequency Range . . . . . 10MHz to 400MHz**
- **I/Q Amplitude and Phase Balance . . . . . 0.2dB, 2^{o}**
- **5th Order Programmable Low Pass Filter. . . . . 2.2MHz - 17.6MHz**
- **400MHz Limiting IF Gain Strip with RSSI 84dB**
- **Low LO Drive Level . . . . . -15dBm**
- **Fast Transmit-Receive Switching. 1μs**
- **Power Management/Standby Mode**
- **Single Supply 2.7V to 5.5V Operation**

Applications

- **Systems Targeting IEEE 802.11 Standard**
- **TDD Quadrature-Modulated Communication Systems**
- **Wireless Local Area Networks**
- **PCMCIA Wireless Transceivers**
- **ISM Systems**
- **TDMA Packet Protocol Radios**
- **PCS/Wireless PBX**
- **Wireless Local Loop**

Description

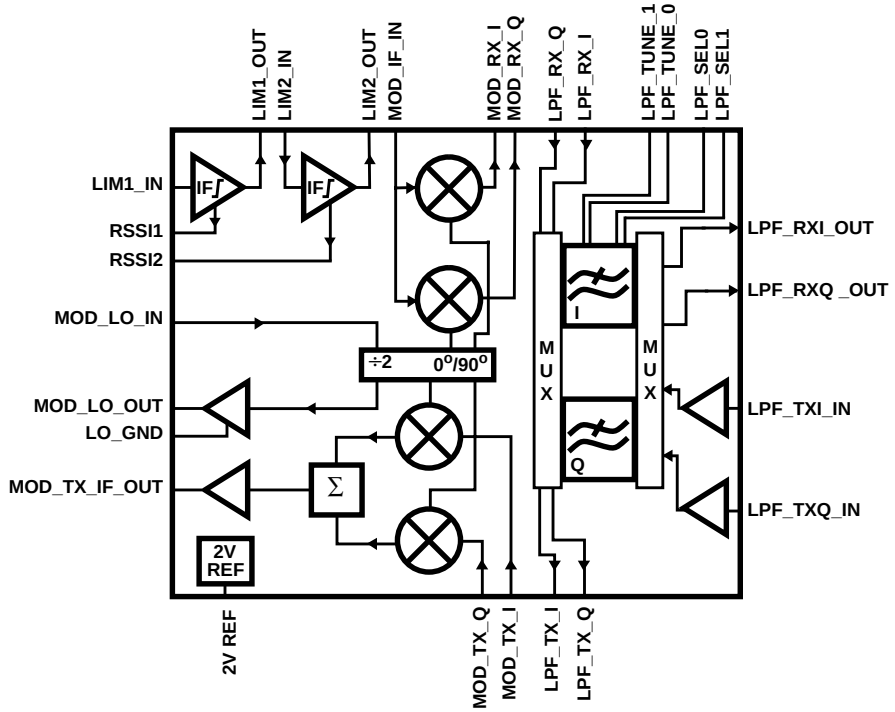
The Harris 2.4GHz PRISM™ chip set is a highly integrated five-chip solution for RF modems employing Direct Sequence Spread Spectrum (DSSS) signaling. The HFA3724 400MHz Quadrature IF Modulator/Demodulator is one of the five chips in the PRISM™ chip set (see the Typical Application Diagram).

The HFA3724 is a highly integrated baseband converter for quadrature modulation applications. It features all the necessary blocks for baseband modulation and demodulation of I and Q signals. It has a two stage integrated limiting IF amplifier with 84db of gain with a built in Receive Signal Strength Indicator (RSSI). Baseband antialiasing and shaping filters are integrated in the design. Four filter bandwidths are programmable via a two bit digital control interface. In addition, these filters are continuously tunable over a ±20% frequency range via one external resistor. The modulator channel receives digital I and Q data for processing. To achieve broadband operation, the Local Oscillator frequency input is required to be twice the desired frequency of modulation/demodulation. A selectable buffered divide by 2 LO output and a stable reference voltage are provided for convenience of the user. The device is housed in a thin 80 lead TQFP package well suited for PCMCIA board applications.

Ordering Information

PART NUMBER	TEMP. RANGE (^{o}C)	PACKAGE	PKG. NO.
HFA3724IN	-40 to 85	80 Ld TQFP	Q80.14x14
HFA3724IN96	-40 to 85	Tape and Reel	

Simplified Block Diagram



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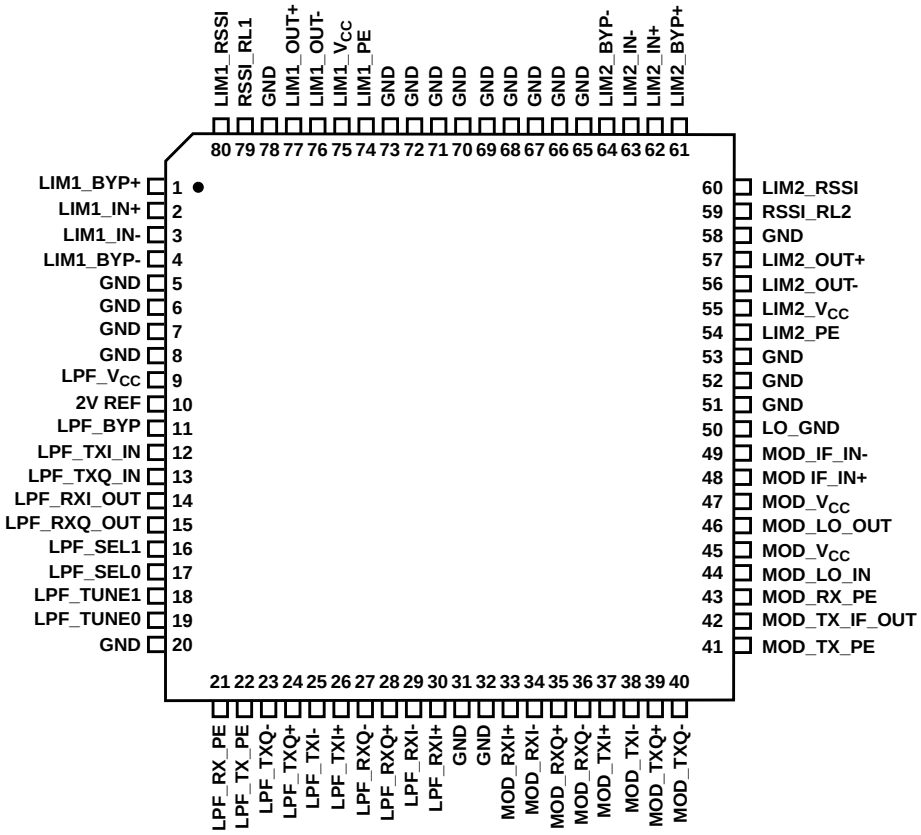
CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

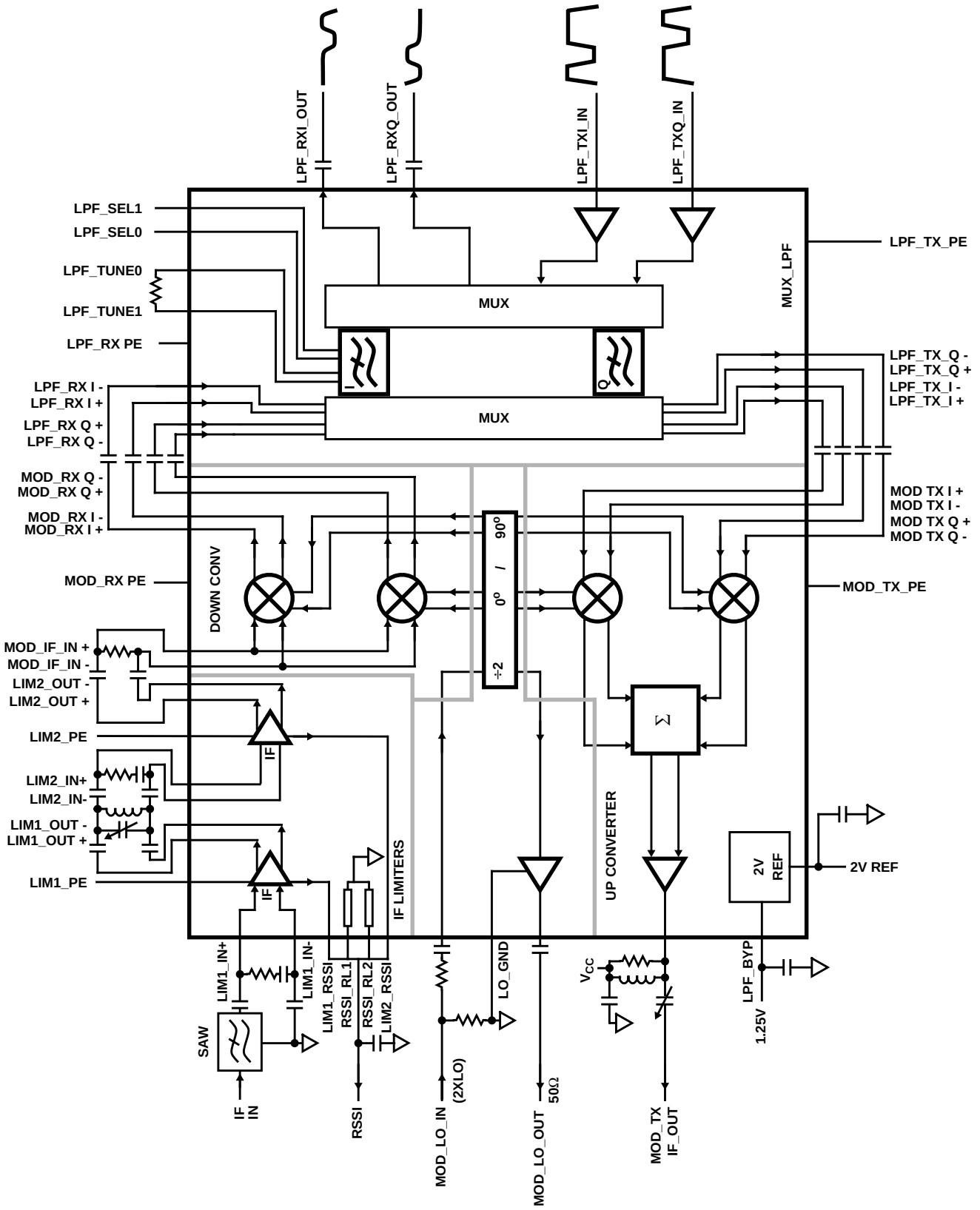
File Number **4067.5**

Pinout

80 LEAD TQFP
TOP VIEW

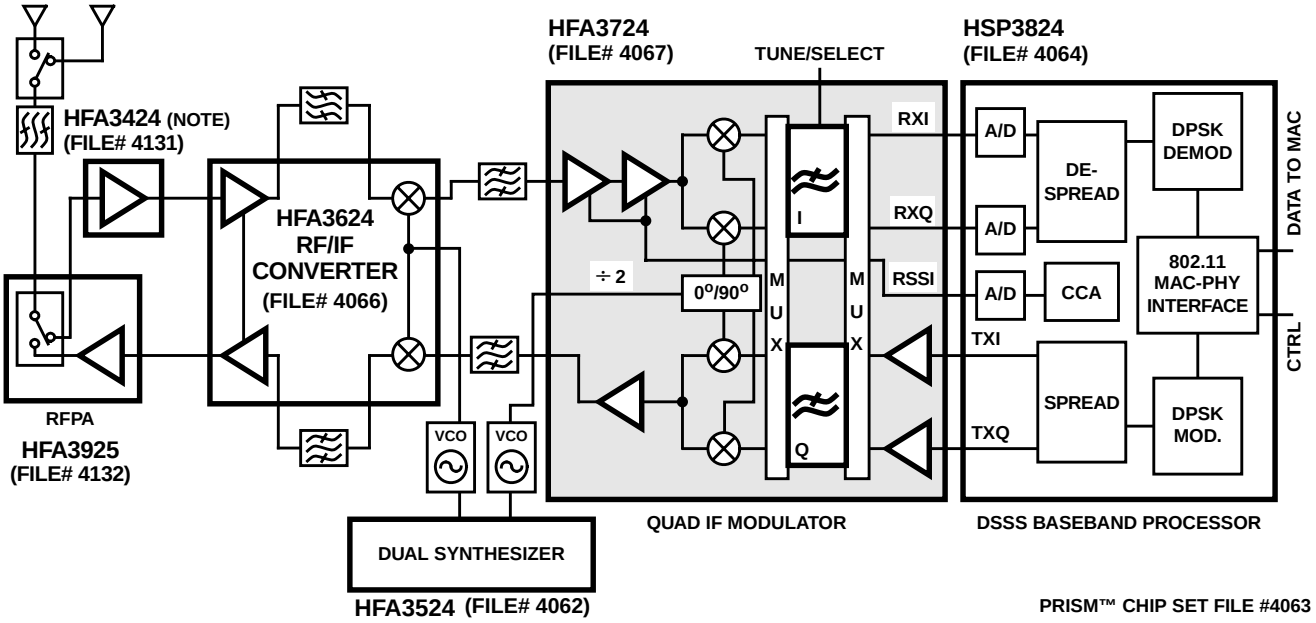


Block Diagram



NOTE: V_{CC}, GND and Bypass capacitors not shown.

Typical Application Diagram



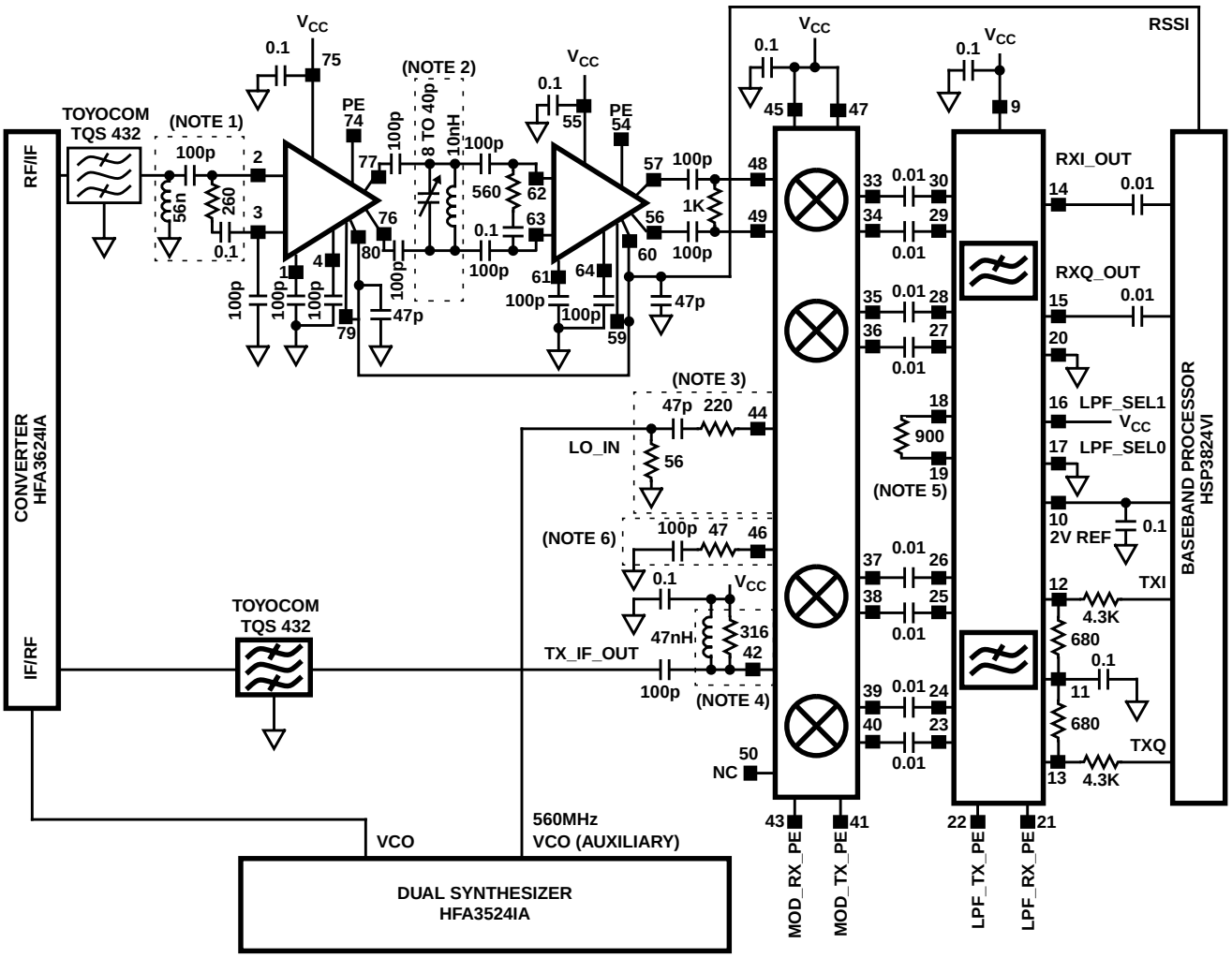
TYPICAL TRANSCEIVER APPLICATION USING THE HFA3724

NOTE: Required for systems targeting 802.11 specifications.

For additional information on the PRISM™ chip set, call (407) 724-7800 to access Harris' AnswerFAX system. When prompted, key in the four-digit document number (File #) of the datasheets you wish to receive.

The four-digit file numbers are shown in Typical Application Diagram, and correspond to the appropriate circuit.

Typical Application Diagram (Targeting IEEE 802.11 Standard)



TYPICAL APPLICATION DIAGRAM (TARGETING IEEE 802.11 STANDARD)

NOTES:

1. Input termination used to match a SAW filter.
2. Typical bandpass filter for 280MHz, BW = 47MHz, Q = 6. Can also be used if desired after the second stage.
3. Network shown for a typical -10dBm input at 50Ω.
4. Output termination used to match a SAW filter.
5. R_{TUNE} value for a 7.7MHz cutoff frequency setting.
6. LO buffer output termination is needed only when the buffer is enabled by pin 50 connected to GND, otherwise tie pin 46 to pin 47.

Pin Description

PIN	SYMBOL	DESCRIPTION
1	LIM1_BYP+	DC feedback pin for Limiter amplifier 1. Requires good decoupling and minimum wire length to a solid signal ground.
2	LIM1_In+	Non inverting analog input of Limiter amplifier 1.
3	LIM1_In-	Inverting input of Limiter amplifier 1.
4	LIM1_BYP-	DC feedback pin for Limiter amplifier 1. Requires good decoupling and minimum wire length to a solid signal ground.
5, 6, 7, 8	GND	Ground. Connect to a solid ground plane.
9	LPF_V_{CC}	Supply pin for the Low pass filter. Use high quality decoupling capacitors right at the pin.
10	2V REF	Stable 2V reference voltage output for external applications. Loading must be higher than 10kΩ. A bypass capacitor of at least 0.1µF is required.
11	LPF_BYP	Internal reference bypass pin. This is the common voltage (V_{CM}) used for the LPF digital thresholds. Requires 0.1µF decoupling capacitor.
12	LPF_TXI_In	Low pass filter in phase (I) channel transmit input. Conventional or attenuated direct coupling is required for digital inputs. (Note 7)
13	LPF_TXQ_In	Low pass filter quadrature (Q) channel transmit input. Conventional or attenuated direct coupling is required for digital inputs. (Note 7)
14	LPF_RXI_Out	Low pass filter in phase (I) channel receive output. Requires AC coupling. (Note 8)
15	LPF_RXQ_Out	Low pass filter quadrature (Q) channel receive output. Requires AC coupling. (Note 8)
16	LPF_Sel1	Digital control input pins. Selects four programed cut off frequencies for both receive and transmit channels. Tuning speed from one cutoff to another is less than 1µs. SEL1 SEL0 Cutoff Frequency — SEL1 SEL0 Cutoff Frequency LO LO 2.2MHz — HI LO 8.8MHz LO HI 4.4MHz — HI HI 17.6MHz
17	LPF_Sel0	
18	LPF_Tune1	These two pins are used to fine tune the Low pass filter cutoff frequency. A resistor connected between the two pins (R_{TUNE}) will fine tune both transmit and receive filters. Refer to the tuning equation in the LPF AC specifications.
19	LPF_Tune0	
20	GND	Ground. Connect to a solid ground plane.
21	LPF_RX_PE	Digital input control pin to enable the LPF receive mode of operation. Enable logic level is High.
22	LPF_TX_PE	Digital input control pin to enable the LPF transmit mode of operation. Enable logic level is High.
23	LPF_TXQ-	Negative output of the transmit Low pass filter, quadrature channel. AC coupling is required. Normally connects to the inverting input of the quadrature Modulator (Mod_TXQ-), pin 40.
24	LPF_TXQ+	Positive output of the transmit Low pass filter, quadrature channel. AC coupling is required. Normally connects to the non inverting input of the quadrature Modulator (Mod_TXQ+), pin 39.
25	LPF_TXI-	Negative output of the transmit Low pass filter, in phase channel. AC coupling is required. Normally connects to the inverting input of the in phase Modulator (Mod_TXI-), pin 38.
26	LPF_TXI+	Positive output of the transmit Low pass filter, in phase channel. AC coupling is required. Normally connects to the non inverting input of the in phase Modulator (Mod_TXI+), pin 37.
27	LPF_RXQ-	Low pass filter inverting input of the receive quadrature channel. AC coupling is required. This input is normally coupled to the negative output of the quadrature demodulator (Mod_RXQ-), pin 36.
28	LPF_RXQ+	Low pass filter non inverting input of the receive quadrature channel. AC coupling is required. This input is normally coupled to the positive output of the quadrature demodulator (Mod_RXQ+), pin 35.
29	LPF_RXI-	Low pass filter inverting input of the receive in phase channel. AC coupling is required. This input is normally coupled to the negative output of the in phase demodulator (Mod_RXI-), pin 34.

Pin Description (Continued)

PIN	SYMBOL	DESCRIPTION
30	LPF_RXI+	Low pass filter non inverting input of the receive in phase channel. AC coupling is required. This input is normally coupled to the positive output of the in phase demodulator (Mod_RXI-), pin 33.
31, 32	GND	Ground. Connect to a solid ground plane.
33	Mod_RXI+	In phase demodulator positive output. AC coupling is required. Normally connects to the non inverting input of the Low pass filter (LPF_RXI+), pin 30.
34	Mod_RXI-	In phase demodulator negative output. AC coupling is required. Normally connects to the inverting input of the Low pass filter (LPF_RXI-), pin 29.
35	Mod_RXQ+	Quadrature demodulator positive output. AC coupling is required. Normally connects to the non inverting input of the Low pass filter (LPF_RXQ+), pin 28.
36	Mod_RXQ-	Quadrature demodulator negative output. AC coupling is required. Normally connects to the inverting input of the Low pass filter (LPF_RXQ+), pin 27.
37	Mod_TXI+	In phase modulator non inverting input. AC coupling is required. This input is normally coupled to the Low pass filter positive output (LPF_TXI+), pin 26.
38	Mod_TXI-	In phase modulator inverting input. AC coupling is required. This input is normally coupled to the Low pass filter negative output (LPF_TXI-), pin 25.
39	Mod_TXQ+	Quadrature modulator non inverting input. AC coupling is required. This input is normally coupled to the Low pass filter positive output (LPF_TXQ+), pin 24.
40	Mod_TXQ-	Quadrature modulator inverting input. AC coupling is required. This input is normally coupled to the Low pass filter negative output (LPF_TXQ-), pin 23.
41	Mod_TX_PE	Digital input control to enable the Modulator section. Enable logic level is High for transmit.
42	Mod_TX_IF_Out	Modulator open collector output, single ended. Termination resistor to V_{CC} with a typical value of 316Ω.
43	Mod_RX_PE	Digital input control to enable the demodulator section. Enable logic level is High for receive.
44	Mod_LO_In (2XLO)	Single ended local oscillator current input. Frequency of input signal must be twice the required modulator carrier and demodulator LO frequency. Input current is optimum at $200\mu A_{RMS}$. Input matching networks and filters can be designed for a wide range of power and impedances at this port. Typical input impedance is 130Ω.This pin requires AC coupling. (Note 9) NOTE: High second harmonic content input waveforms may degrade I/Q phase accuracy.
45	Mod_V_{CC}	Modulator/Demodulator supply pin. Use high quality decoupling capacitors right at the pin.
46	Mod_LO_Out	Divide by 2 buffered output reference from “Mod_LO_in” input. Used for external applications where the modulating and demodulating carrier reference frequency is required. 50Ω single end driving capability.This output can be disabled by use of pin 50. AC coupling is required, otherwise tie to pin 47 (V_{CC}).
47	Mod_V_{CC}	Modulator/Demodulator supply pin. Use high quality decoupling capacitors right at the pin.
48	Mod_IF_In+	Demodulator non inverting input. Requires AC coupling.
49	Mod_IF In-	Demodulator inverting input. Requires AC coupling.
50	LO_GND	When grounded, this pin enables the LO buffer (Mod_LO_Out). When open (NC) it disables the LO buffer.
51, 52, 53	GND	Ground. Connect to a solid ground plane.
54	LIM2_PE	Digital input control to enable the limiter amplifier 2. Enable logic level is High.
55	LIM2_V_{CC}	Limiter amplifier 2 supply pin. Use high quality decoupling capacitors right at the pin.
56	LIM2_Out-	Positive output of limiter amplifier 2. Requires AC coupling.
57	LIM2_Out+	Negative output of limiter amplifier 2. Requires AC coupling.
58	GND	Ground. Connect to a solid ground plane.

Pin Description (Continued)

PIN	SYMBOL	DESCRIPTION
59	RSSI_RL2	Load resistor to ground. Nominal value is 6kΩ. This load is used to terminate the LIM RSSI current output and maintain temperature and process variation to a minimum.
60	LIM2_RSSI	Current output of RSSI for the limiter amplifier 2. Connect in parallel with the RSSI output of the amplifier limiter 1 for cascaded response.
61	LIM2_BYP+	DC feedback pin for Limiter amplifier 2. Requires good decoupling and minimum wire length to a solid signal ground.
62	LIM2_In+	Non inverting analog input of Limiter amplifier 2.
63	LIM2_In-	Inverting input of Limiter amplifier 2.
64	LIM2_BYP-	DC feedback pin for Limiter amplifier 2. Requires good decoupling and minimum wire length to a solid signal ground.
65, 66, 67, 68, 69, 70, 71, 72, 73	GND	Ground. Connect to a solid ground plane.
74	LIM1_PE	Digital input control to enable the limiter amplifier 1. Enable logic level is High.
75	LIM1_V_{CC}	Limiter amplifier 1 supply pin. Use high quality decoupling capacitors right at the pin.
76	LIM1_Out-	Negative output of limiter amplifier 1. Requires AC coupling.
77	LIM1_Out+	Positive output of limiter amplifier 1. Requires AC coupling.
78	GND	Ground. Connect to a solid ground plane.
79	RSSI_RL1	Load resistor to ground. Nominal value is 6kΩ. This load is used to terminate the LIM RSSI current output and maintain temperature and process variation to a minimum.
80	LIM1_RSSI	Current output of RSSI for the limiter amplifier 1. Connect in parallel with the RSSI output of the amplifier limiter 2 for cascaded response.

NOTES:

7. The HFA3724 generates a lower sideband signal when the “I” input leads the “Q” input by 90 degrees.
8. For a reference LO frequency higher than a CW IF signal input, the “I” channel leads the “Q” channel by 90 degrees.
9. The in-phase reference LO transitions occur at the rising edges of the 2XLO clock signal. Quadrature LO transitions occur at the falling edges. 180 degrees phase ambiguity is expected for carrier locked systems without differential encoding.

TABLE 1. POWER MANAGEMENT

	TRANSMIT	RECEIVE	POWER DOWN
LIM1_PE	0	1	0
LIM2_PE	0	1	0
LPF_RX_PE	0	1	0
MOD_RX_PE	0	1	0
MOD_TX_PE	1	0	0
LPF_TX_PE	1	0	0

Absolute Maximum Ratings

Supply Voltage . . . . . -0.3V to +6.0V
Voltage on Any Other Pin . . . . . -0.3V to V_{CC} +0.3V

Operating Conditions

Supply Voltage Range . . . . . +2.7V to +5.5V
Temperature Range . . . . . $-40^oC \le T_A \le 85^oC$

Thermal Information

Thermal Resistance (Typical, Note 10) θ_{JA} ($^oC/W$)
TQFP Package 75
Package Power Dissipation at 70^{o}C
TQFP Package 1.1W
Maximum Junction Temperature (Plastic Package . . . . . 150^{o}C
Maximum Storage Temperature Range . . . . . $-65^oC \le T_A \le 150^oC$
Maximum Lead Temperature (Soldering 10s) . . . . . 300^{o}C
(TQFP - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

10. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

DC Electrical Specifications

V_{CC} = 2.7V to 5.5V, Unless Otherwise Specified

PARAMETER	SYMBOL	(NOTE 11) TEST LEVEL	TEMP (^{o}C)	MIN	TYP	MAX	UNITS
Total Supply Current, RX Mode at 5.5V	RXI_{CC}	A	Full	-	70	105	mA
Total Supply Current, TX Mode at 5.5V	TXI_{CC}	A	Full	-	60	80	mA
Shutdown Current at 5.5V	I_{CCOFF}	A	Full	-	0.8	2.0	mA
All Digital Inputs V_{IH} (TTL Threshold for All V_{CC})	V_{IH}	A	Full	2.0		V_{CC}	V
All Digital Inputs V_{IL} (TTL Threshold for All V_{CC})	V_{IL}	A	Full	-0.2		0.8	V
High Level Input Current at 2.7V V_{CC}, V_{IN} = 2.4V	I_{IHI}	A	25	-	-	80	µA
High Level Input Current at 5.5V V_{CC}, V_{IN} = 4.0V	I_{IHh}	A	25	-	-	400	µA
Low Level Input Current, V_{IN} = 0.8V	I_{IL}	A	25	-20	-	+20	µA
RX to TX/TX to RX Switching Speed (Figure 23)	PEt	B	25	-	2	-	µs
Power Down/Up Switching Speed (Figure 23)	PEtpd	B	25	-	10	-	µs
Reference Voltage	V_{REF}	A	Full	1.87	2.0	2.13	V
Reference Voltage Variation Over Temperature	V_{REFT}	B	25	-	800	-	µV/^{o}C
Reference Voltage Variation Over Supply Voltage	V_{REFV}	B	25	-	1.6	-	mV/V
Reference Voltage Minimum Load Resistance	V_{REFRL}	C	25	10	-	–	kΩ

NOTE:

11. A = Production Tested, B = Based on Characterization, C = By Design

AC Electrical Specifications, Demodulator Performance

Application Targeting IEEE 802.11, V_{CC} = 3V, Figure 23 Unless Otherwise Specified

PARAMETER	SYMBOL	(NOTE 12) TEST LEVEL	TEMP (^{o}C)	MIN	TYP	MAX	UNITS
IF Demodulator 3dB Limiting Sensitivity (Note 13)	D3db	B	25	-	-84	-	dBm
IF Demodulator I and Q Outputs Voltage Swing	DIQsw	A	Full	300	460	650	mV_{P-P}
IF Demodulator I and Q Channels Output Drive Capability (Z_{OUT} = 50Ω) C_{MAX} = 10pF	Doutz	C	25	1.2	2	-	kΩ
IF Demodulator I/Q Amplitude Balance, IFin = -70dbm at 50Ω	Dabal	A	Full	-1.0	0	+1.0	dB
IF Demodulator I/Q Phase Balance, IFin = -70dbm at 50Ω	Dphbal	A	Full	-4.0	0	+4.0	Degrees
IF Demodulator Output Variation at -70dbm to 0dbm input	Dovar	A	Full	-0.5	0	+0.5	dB
IF Demodulator RSSI Noise Induced Offset Voltage (Note 14)	Drssio	B	25	-	580	-	mV_{DC}
IF Demodulator RSSI Voltage Output Slope (Note 15)	Drssis	B	25	-	15	-	mV/dB

AC Electrical Specifications, Demodulator Performance

Application Targeting IEEE 802.11, V_{CC} = 3V, Figure 23 Unless Otherwise Specified **(Continued)**

PARAMETER	SYMBOL	(NOTE 12) TEST LEVEL	TEMP (^oC)	MIN	TYP	MAX	UNITS
IF Demodulator RSSI DC Level, Pin = -30dBm (Note 15)	Drssi_30	A	Full	0.90	1.46	1.71	V_{DC}
IF Demodulator RSSI DC Level, Pin = -70dBm (Note 15)	Drssi_70	A	Full	0.456	0.86	0.99	V_{DC}
IF Demodulator RSSI Linear Dynamic Range (Note 16)	Drssidr	B	25	-	60	-	dB
IF Demodulator RSSI Rise and Fall Time from -30dBm to -50dBm Input at 100pF Load	Drssitr	B	25	-	0.3	-	µs

NOTES:

12. A = Production Tested, B = Based on Characterization, C = By Design
13. 2XLO input = 572MHz, measure IF input level required to drop the I and Q output at 6MHz by 3dB from a reference output generated at IF input = -30dBm (hard limiting). LPF selected for 8.8MHz. This is a noise limited case with a BW of 47MHz. Please refer to the Overall Device Description, IF limiter.
14. The residual DC voltage generated by the RSSI circuit due to a noise limited stage at the end of the chain with no IF input. IF port terminated into 50Ω. Please referred to the Overall Device Description, IF limiter.
15. Both limiter RSSI current outputs are summed by on chip 6KΩ resistors in parallel.
16. Range is defined where the indicated received input strength by the RSSI is ±3dBm accurate.

AC Electrical Specifications, Modulator Performance

Application Targeting IEEE 802.11, V_{CC} = 3V, Figure 23 Unless Otherwise Specified

PARAMETER	SYMBOL	(NOTE 17) TEST LEVEL	TEMP (^oC)	MIN	TYP	MAX	UNITS
IF Modulator I/Q Amplitude Balance (Note 18)	Mabal	B	25	-1.0	0	+1.0	dB
IF Modulator I/Q Phase Balance (Note 18)	Mphbal	B	25	-4.0	0	+4.0	Degrees
IF modulator SSB Output Power (Note 19)	Mssbpw	A	Full	-12	-7	-4	dBm
IF Modulator Side Band Suppression (Note 19)	Mssbss	A	Full	26	33	-	dBc
IF Mod Carrier Suppression (LO Buffer Enabled) (Note 19)	Mssbcs	A	Full	28	30	-	dBc
IF Mod Carrier Suppression (LO Buffer Disabled) (Note 19)	Mssbcs1	B	25	28	36	-	dBc
IF Modulator Output Noise Floor (Out of Band)	Moutn0	B	25	-	-132	-	dBm/Hz
IF Modulator I/Q 3dB Cutoff SEL0/1 = 2.2MHz (Note 20)	Msel1f	A	Full	1.8	2.2	2.5	MHz
IF Modulator I/Q 3dB Cutoff SEL0/1 = 4.4MHz (Note 20)	Msel2f	A	Full	3.6	4.4	5.0	MHz
IF Modulator I/Q 3dB Cutoff SEL0/1 = 8.8MHz (Note 20)	Msel3f	A	Full	7.3	8.8	9.8	MHz
IF Modulator I/Q 3dB Cutoff SEL0/1 = 17.6MHz (Note 20)	Msel4f	A	Full	14.6	17.6	19.6	MHz
IF Modulator Spread Spectrum Output Power (Note 21)	Mdsspw	B	25	-12	-7	-4	dBm
IF Modulator Side Lobe to Main Lobe Ratio, LPF = 8.8MHz (Note 21)	Mdsssl	A	Full	32	35	-	dB

NOTES:

17. A = Production Tested, B = Based on Characterization, C = By Design
18. Data is characterized by DC levels applied to MOD TXI and Q pins for 4 quadrants with LO output as reference or indirectly by the SSB characteristics.
19. Power at the fundamental SSB frequency of two 6MHz, 90 degrees apart square waves applied at TXI and TXQ inputs. V_{IH} = 3.0V, V_{IL} = 0.5V. LPF selected to 8.8MHz cutoff.
20. Cutoff frequencies are specified for both modulator and demodulator as the filter bank is shared and multiplexed for Transmit and Receive. Data is characterized by observing the attenuation of the fundamental of a square wave digital input swept at each channel separately. The IF output is down converted by an external wideband mixer with a coherent LO input for each of quadrature signals separately.
21. Typical ratio characterization with R_{TUNE} set to 7.7MHz, LPF selected for 8.8MHz. TXI and TXQ Digital Inputs at two independent and aligned 11M chip/s, 2^{23}-1 sequence code signals.

Typical Performance Curves, Demodulator (See Figure 23 Test Diagram)

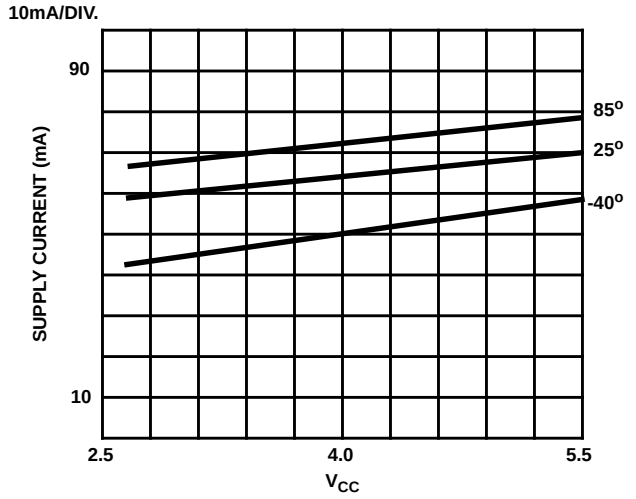


FIGURE 1. DEMODULATOR SUPPLY CURRENT vs V_{CC} AND TEMPERATURE

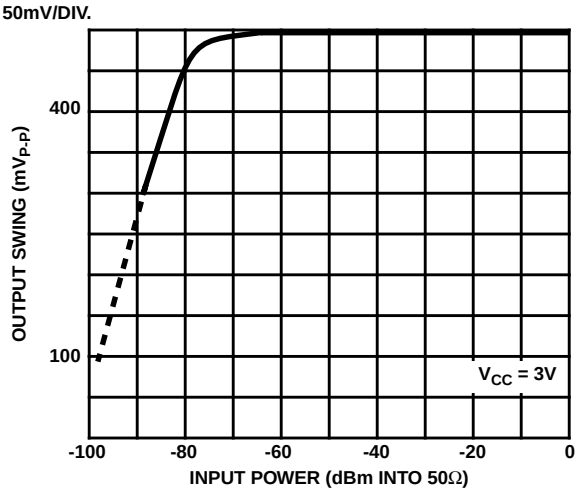


FIGURE 2. DEMODULATOR I/Q OUTPUT SWING vs INPUT POWER

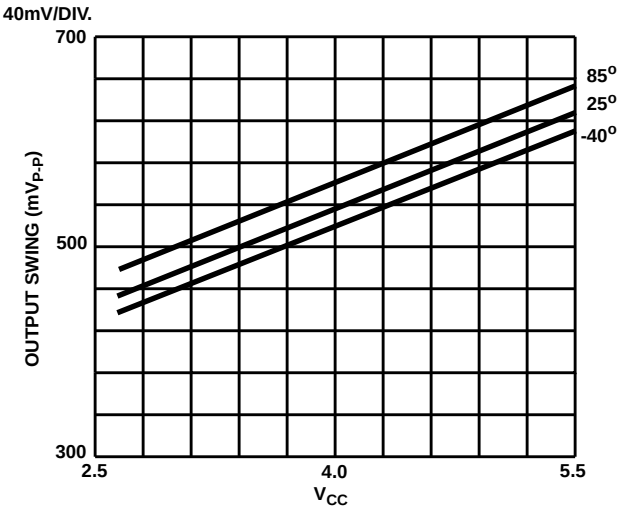


FIGURE 3. DEMOD I/Q OUTPUT SWING vs V_{CC} AND TEMPERATURE

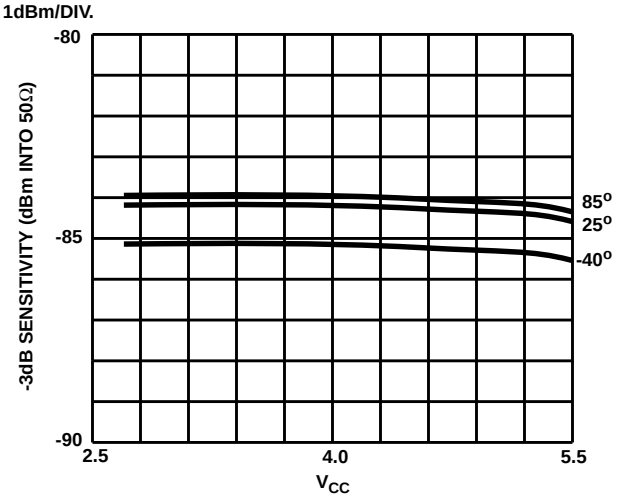


FIGURE 4. CASCADED LIMITER -3dB INPUT SENSITIVITY RESPONSE vs V_{CC} AND TEMPERATURE

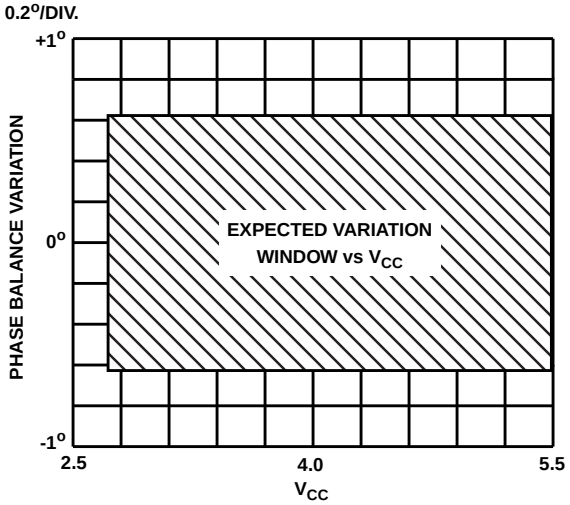


FIGURE 5. DEMOD I/Q PHASE BALANCE VARIATION vs V_{CC}

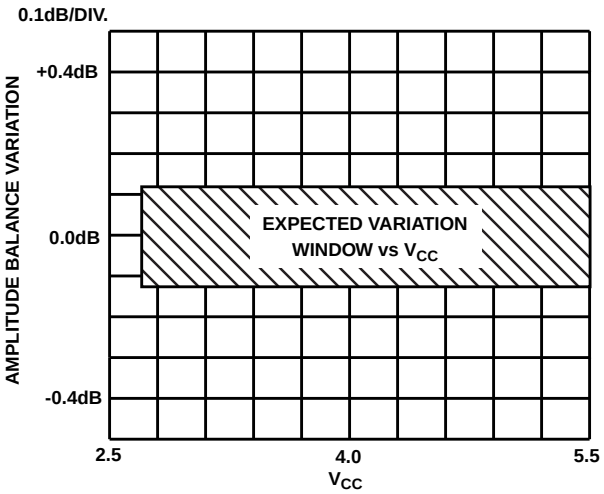


FIGURE 6. DEMOD I/Q AMPLITUDE BALANCE VARIATION vs V_{CC}

Typical Performance Curves, Demodulator (See Figure 23 Test Diagram) (Continued)

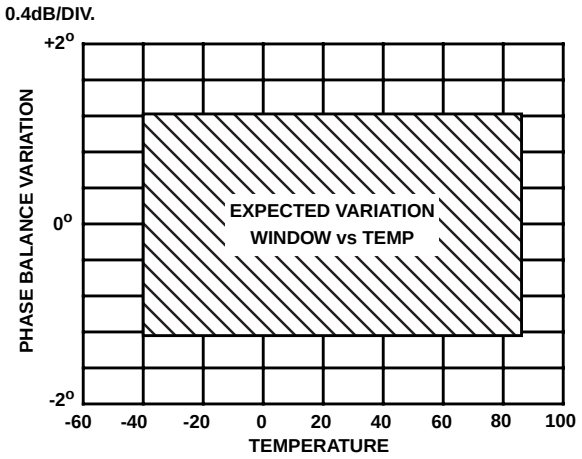


FIGURE 7. DEMOD I/Q PHASE BALANCE VARIATION vs TEMPERATURE

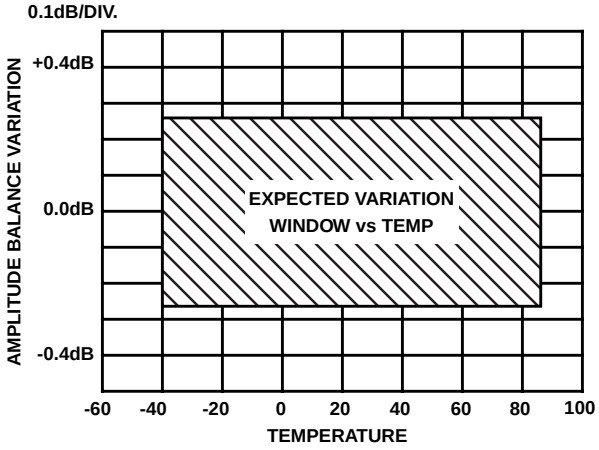


FIGURE 8. DEMOD I/Q AMPLITUDE BALANCE VARIATION vs TEMPERATURE

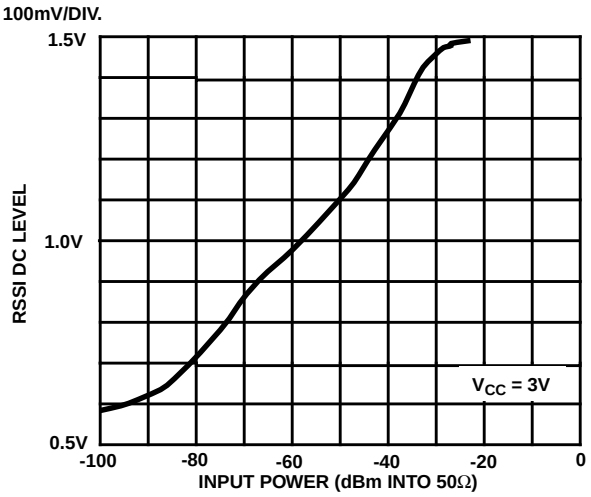


FIGURE 9. DEMOD RSSI DC LEVEL vs INPUT POWER

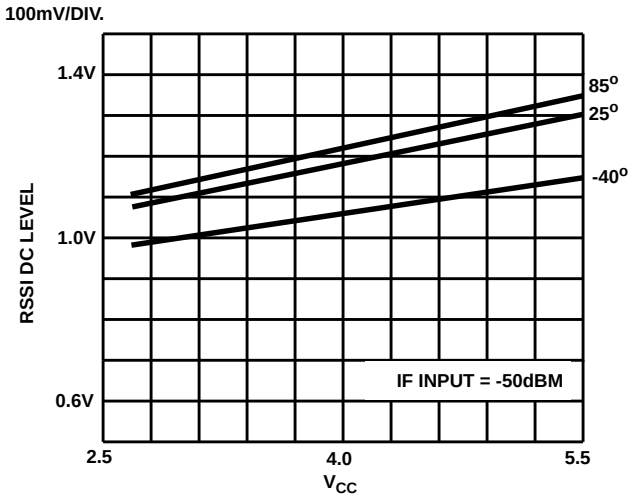


FIGURE 10. DEMOD RSSI DC LEVEL vs V_{CC} AND TEMPERATURE

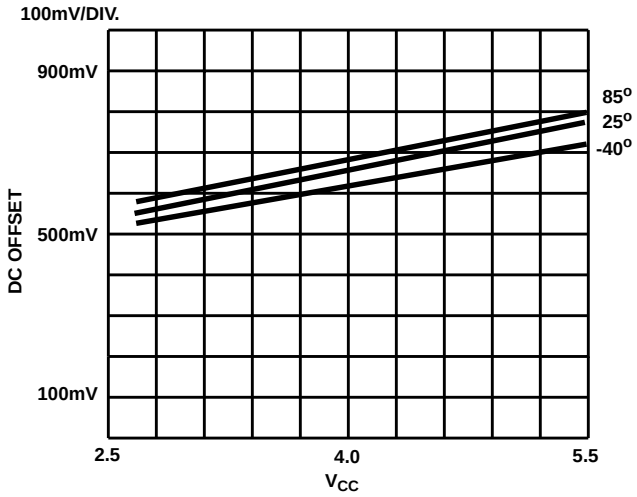


FIGURE 11. DEMODULATOR RSSI DC OFFSET vs V_{CC} AND TEMPERATURE

Typical Performance Curves, Modulator (See Figure 23 Test Diagram)

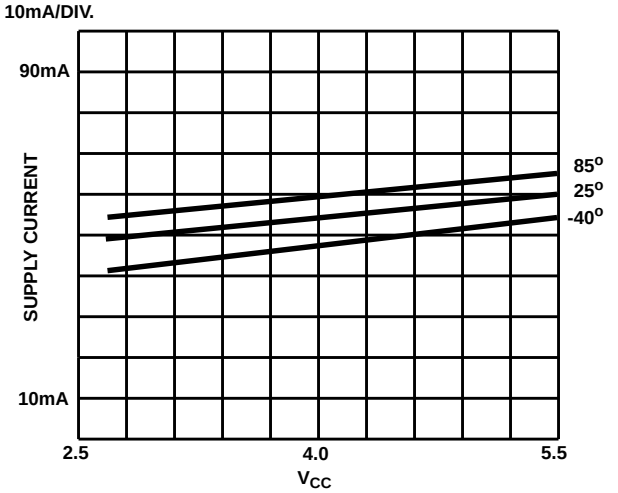


FIGURE 12. MODULATOR SUPPLY CURRENT vs V_{CC} AND TEMPERATURE

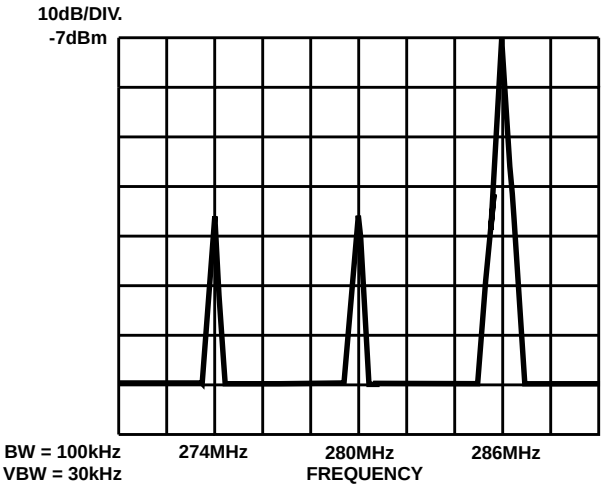


FIGURE 13. TYPICAL SSB MODULATOR RESPONSE (NOTE 3 ON AC ELECTRICAL SPECIFICATIONS, MODULATOR PERFORMANCE TABLE, LO BUFFER ENABLED)

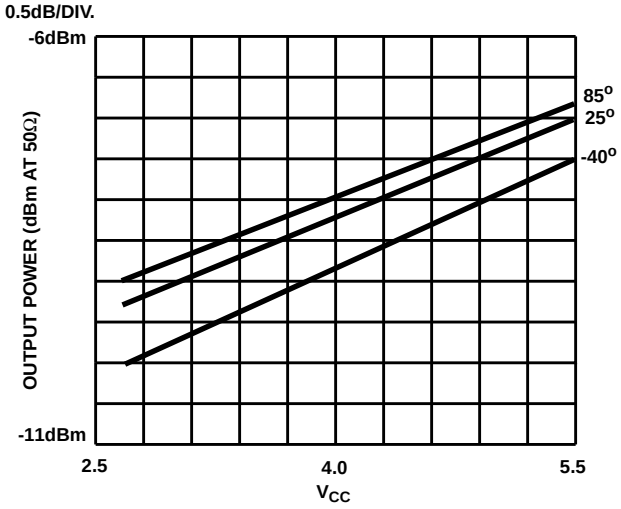


FIGURE 14. MODULATOR SSB OUTPUT POWER vs V_{CC} AND TEMPERATURE

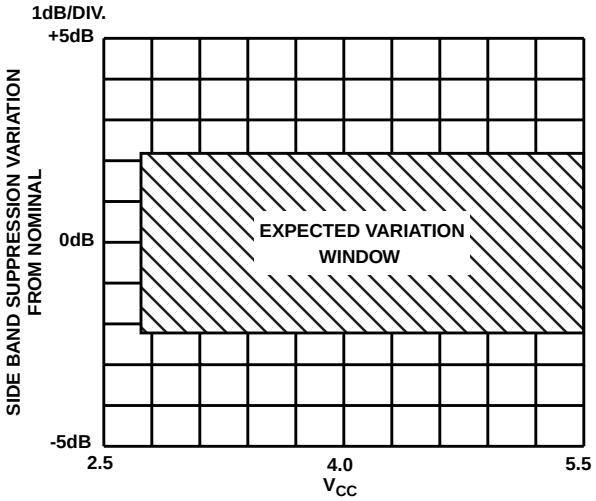


FIGURE 15. MODULATOR SSB SIDE BAND SUPPRESSION VARIATION vs V_{CC} AND TEMPERATURE

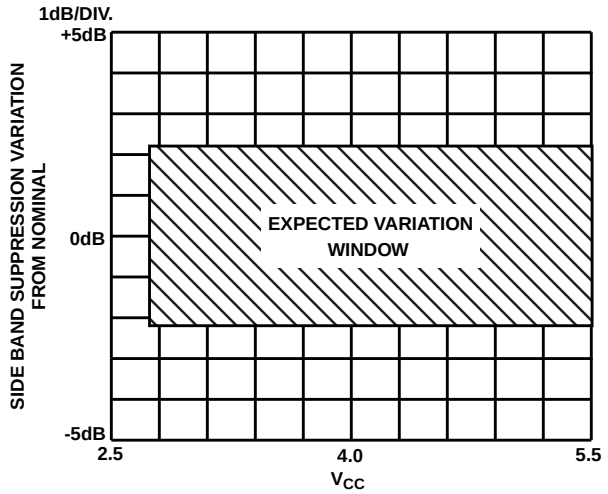


FIGURE 16. MODULATOR LO LEAKAGE VARIATION vs V_{CC} AND TEMPERATURE

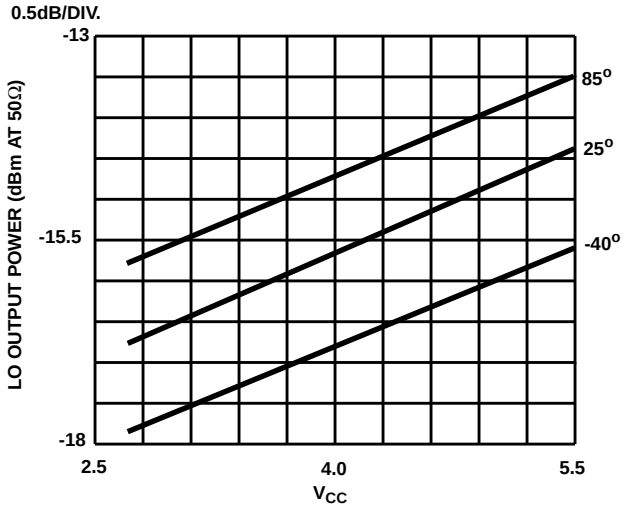


FIGURE 17. MODULATOR LO OUTPUT POWER (FUNDAMENTAL) vs V_{CC} AND TEMPERATURE

Typical Performance Curves, Modulator (See Figure 23 Test Diagram) **(Continued)**

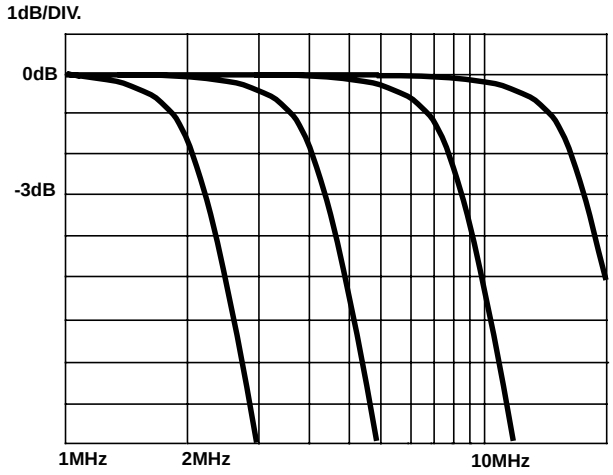


FIGURE 18. TYPICAL MODULATOR I/Q 3dB CUTOFF FREQUENCY CURVES

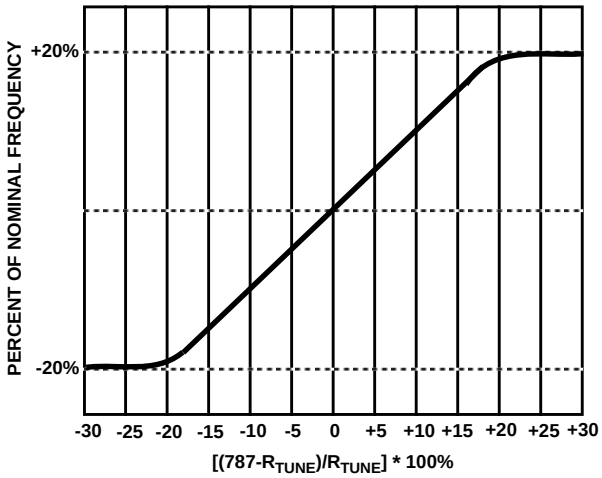


FIGURE 19. LPF CUTOFF FREQUENCY vs R_{TUNE}, V_{CC} = 3V, T_A = 25°C

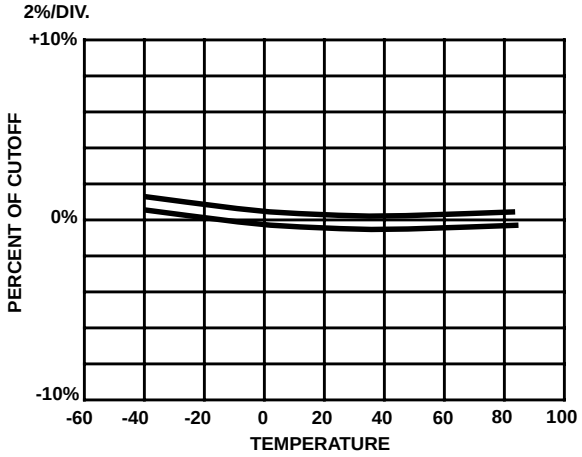


FIGURE 20. LPF CUTOFF FREQUENCY vs TEMPERATURE AND V_{CC} (NOTE 4 ON AC ELECTRICAL SPECIFICATIONS, MODULATOR PERFORMANCE TABLE)

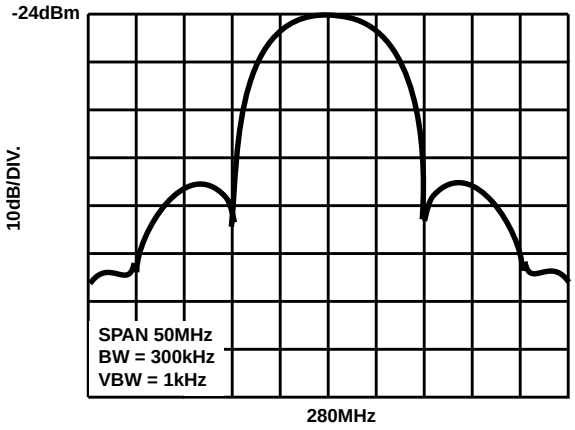


FIGURE 21. TYPICAL MODULATOR SPREAD SPECTRUM OUTPUT 11M CHIPS/s, QPSK. R_{TUNE} TO 7.7MHz, 8.8MHz SETTING

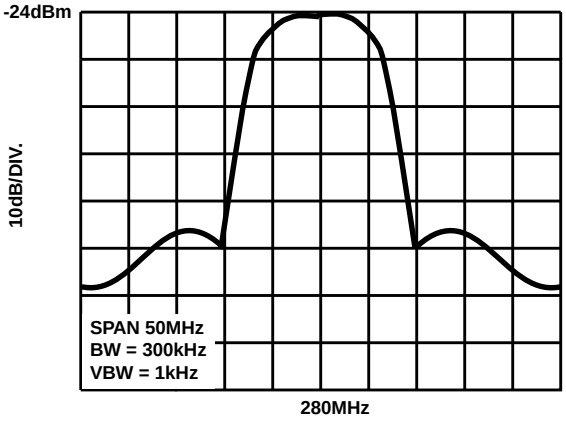


FIGURE 22. TYPICAL MODULATOR SPREAD SPECTRUM OUTPUT WITH R_{TUNE} TO +20% OF 4.4MHz SETTING FOR ILLUSTRATION PURPOSES ONLY

Test Diagram (280MHz IF)

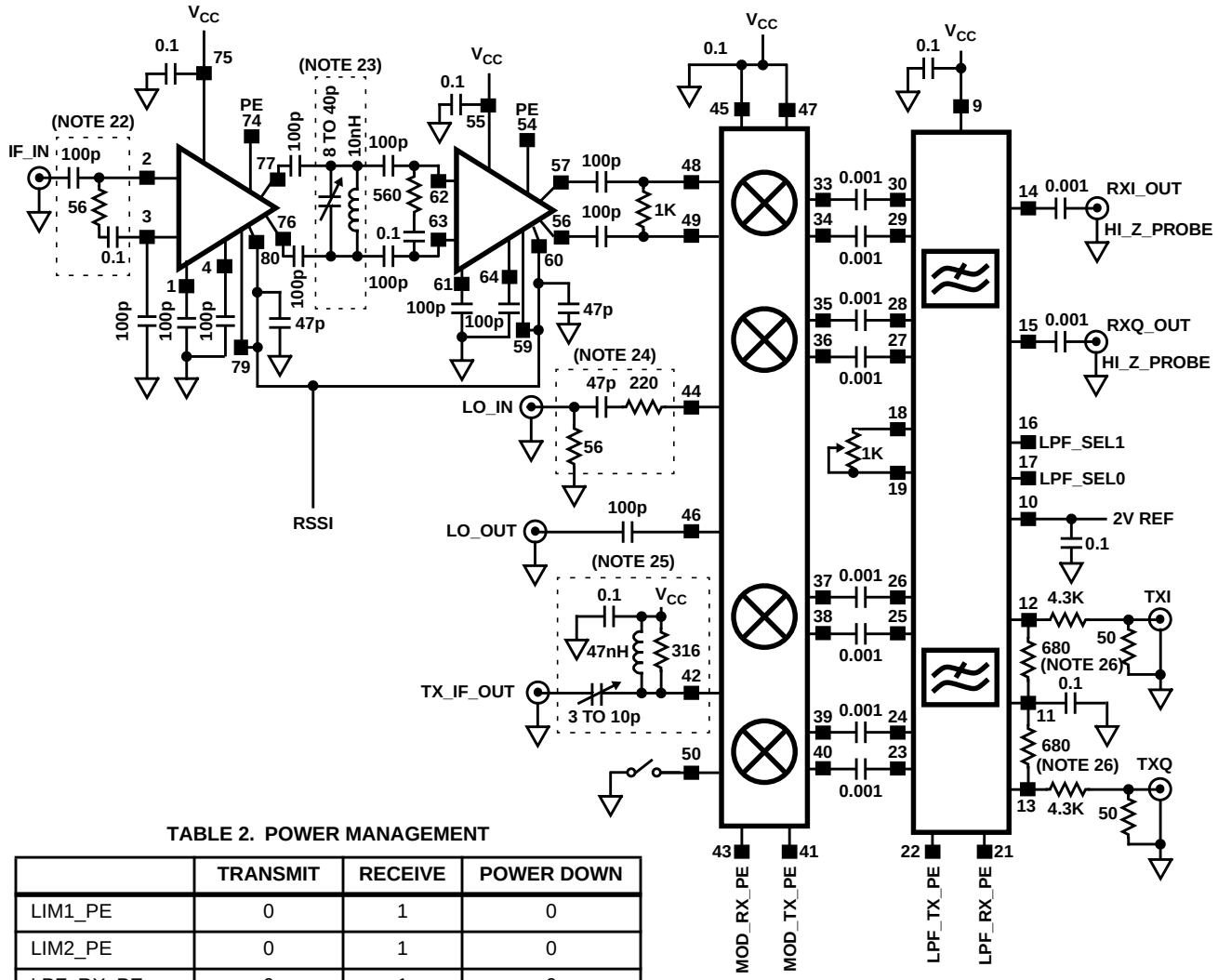


TABLE 2. POWER MANAGEMENT

	TRANSMIT	RECEIVE	POWER DOWN
LIM1_PE	0	1	0
LIM2_PE	0	1	0
LPF_RX_PE	0	1	0
MOD_RX_PE	0	1	0
MOD_TX_PE	1	0	0
LPF_TX_PE	1	0	0

FIGURE 23. TEST DIAGRAM (280MHz IF)

NOTES:

22. Input termination used to provide a 50Ω impedance. Limiter Noise Figure ≅ 9dB for this configuration.
23. Bandpass filter for 280MHz, BW = 47MHz, Q = 6.
24. Network shown for a typical -10dBm input at 50Ω.
25. Matching network from 250Ω to 50Ω at 280MHz.
26. Attenuator is optional if TTL driver can drive 50Ω.

Overall Device Description

The HFA3724 is a highly integrated baseband converter for half duplex wireless data applications. It features all the necessary blocks for baseband modulation and demodulation of “I” and “Q” quadrature multiplexing signals. It targets applications using all phase shift types of modulation (PSK) due to its hard limiting receiving front end. Four fully independent blocks adds flexibility for numerous applications covering a wide range of IF frequencies. A differential design architecture, device pin out and layout have been chosen to improve system RF properties like common mode signal immunity (noise, crosstalk), reduce relevant parasitics and settling times and optimize dynamic range for low power requirements. Single power supply requirements from $2.7V_{DC}$ to $5.5V_{DC}$ makes the HFA3724 a good choice for portable transceiver designs.

The HFA3724 has a two stage integrated limiting IF amplifier with frequency response to 400MHz. These amplifiers exhibit a -84dbm, -3db cascaded limiting sensitivity with a built in Receive Signal Strength Indicator (RSSI) covering 60db of dynamic range with excellent linearity. An up conversion and down conversion pair of quadrature doubly balanced mixers are available for “I” and “Q” baseband IF processing. These converters are driven by an internal quadrature LO generator which exhibits a broadband response with excellent quadrature properties. To achieve broadband operation, the Local Oscillator frequency input is required to be twice the desired frequency for modulation/demodulation. Duty cycle and signal purity requirements for the 2X LO input using this type of quadrature architecture are less restrictive for the HFA3724. Ground reference input signals as low as -15dBm and frequencies up to 900MHz (2XLO) can be used and tailored by the user. A buffered, divide by 2, LO single ended 50Ω selectable output is provided for convenience of PLL designs. The receive channel mixers “I” and “Q” quadrature outputs have a frequency response up to 30MHz for baseband signals and the transmit mixers are summed and amplified to a single ended open collector output with frequency response up to 400MHz.

Multiplexed or half duplex baseband 5th order Butterworth low pass filters are also included in the design. The “I” and “Q” filters address applications requiring low pass and antialiasing filtering for external baseband threshold comparison or simple analog to digital conversion in the receive channel. During transmission, the filter is used for pulse shaping or control of spectral mask.

Four filter bandwidths are programmable, (2.2MHz, 4.4MHz, 8.8MHz and 17.6MHz) via a two bit digital or hardwired control interface. These cut off frequencies are selected for optimization of spectrum output responses for 2.25M, 5.5M, 11M and 22M chips/sec respectively for spread spectrum applications (These rates can also be interpreted as symbol rates for conventional data transmission). External processing correlators in the receive channel as in the Harris HSP3824 baseband converter, will bring the demodulation to lower effective data rates. As an example, the use of 11M chips/sec, 11 chip Barker code using the 8.8MHz low pass filter in a QPSK type of modulation scheme will bring a post processed effective data rate to 1M symbol/sec or 2M bits/sec. Likewise, the use of a 2.4M chips/sec, 16 chip spreading code and the use of 2.2MHz filter can process an effective data rate of 150K symbols/sec or 300K bits/sec. In addition, these filters are continuously tunable over a ±20% frequency range via one external resistor. This feature gives the user the ability to reshape the spectrum of a transmitted signal at the antenna port which takes into account any spectral regrowth along the transmitter chain. The modulator “I” and “Q” filter inputs accept digital signal levels data for modulation and their phase and gain characteristics, including I / Q matching and group delay are well suitable for reliable data transmission. In the Receive mode and over the full input limiting dynamic range, both low pass filters outputs swing a $500mV_{P-P}$ baseband signal.

Each block has its own independent power enable control for power management and half duplex transmit/receive operation. A stable 2V DC output and a buffered band gap reference voltage are also provided for an external analog to digital conversion reference.

Detailed Description

(Refer to Block Diagram)

IF Limiter

Two independent limiting amplifiers are available in the HFA3724. Each one exhibits a broadband response to 400MHz with 45dB of gain. The low frequency response is limited by external components because the device has no internal coupling capacitors. The differential limiting output swing with a 500Ω load is typically $200mV_{P-P}$ at the fundamental frequency and is temperature stable.

Both amplifiers are very stable within their passband and the cascaded performance also exhibits very good stability for any input source impedance. Wide bandwidth SAW filters for spread spectrum applications or any desired source impedance filter implementation can be used for IF filtering before the cascaded amplifiers. The stability is remarkable for such an integrated solution. In fact, in many applications it is possible to remove the bypass pin capacitors with no degradation in stability. The cascaded -1dB and -3dB input limiting sensitivity have been characterized as -79dbm and 84dbm respectively, for a 50Ω single ended input at 280MHz and with a 47MHz bandwidth interstage bandpass LC filter (refer to Figure 23, Test Diagram). The input sensitivity is determined to a large extent by the bandwidth of the interstage filter and input source impedance.

The noise figure for each stage has been characterized at 6dB for a 250Ω single end input impedance and 9dB for a 50Ω input impedance. These low noise figures combined with their high gain, eliminate the need for additional IF gain components. The use of interstage bandpass filtering is suggested to decrease the noise bandwidth of the signal driving the second stage. Excessive broadband noise energy amplified by the first stage will force the last limiting stage to lose some of its effective gain or “limit on the noise”. The use of interstage filters with narrower bandwidths will further improve the sensitivity of the cascaded limiter chain.

The amplifier differential output impedance is 140Ω (70Ω single ended) which gives the user, the ability to design simple wide or narrow LC bandwidth interstage filters, or tailor a desired cascaded gain by using differential attenuators. The filter can be designed with a desired “Q” by using the followIng relationship: Q = Rp/X; where Rp is the parallel combination of 140Ω source resistance and the load (approximately 500Ω when using 560Ω termination as in Figure 23, Test Diagram), and X is the reactance of either L or C at the desired center frequency.

Another independent feature of the limiting amplifier is its Receive Signal Strength Indicator (RSSI). A Log-Amp design was developed which resulted in a current output proportional to the input power. The RSSI output voltage is set by summing the two stages output currents, which are full wave rectified signals, to a common resistor to ground. This full wave rectified voltage can then be converted to DC by the use of a filter capacitor in parallel with the resistor (The larger the capacitor value, the less the AC ripple with the expense of longer RSSI settling times). This arrangement gives the user the flexibility to set the dynamic voltage swing to any desired level by an appropriate resistance choice. Each stage has an available on chip 6KΩ low temperature coefficient resistor to ground for current output termination that can be used for convenience. The RSSI gives a ±3dBm accurate indication of the receive input power. This accuracy is across a 60dB input dynamic range. The cascaded HFA3724 RSSI slope is of 5.0μA/dB.

Quadrature Down Converter

The quadrature down converter mixers are based in a Gilbert cell design. The input signal is routed to both mixers in parallel. With full balanced differential architecture, these mixers are driven by an accurate internal Local Oscillator (LO) chain as described later. Phase and gain accuracy of the output baseband signals are excellent and are a function of the combination of LO accuracy, balanced device design and layout characteristics. Mainly used for down conversion, its input frequency response exceeds 400MHz with a differential voltage gain of 2.5. With a differential input impedance of 1KΩ, the input compression point exceeds $2V_{P-P}$, which makes it suitable for use with the hard limiting output from the limiter amplifier chain or any low power external AGC application. The output frequency response is limited to 30MHz for “I” and “Q” baseband signals driving a 4KΩ differential load.

The HFA3724 down conversion mixers can generate two 10MHz, 90^o apart signals, with the use of proper low pass filtering, and exhibits $\pm4^o$ and ±0.5dB of phase and amplitude match for a input CW IF signal of 400MHz and a 2XLO input of 780MHz.

LO Quadrature Generator

The In Phase and Quadrature reference signals are generated by a divide by two chain internal to the device which drives both the up and down conversion mixers. With a fully balanced approach, the phase relationship between the two quadrature signals is within $90^o \pm4^o$ for a wide 10 to 400MHz frequency range. The reference signal input frequency needs to be twice the desired internal reference frequency. The ground referenced 2XLO input is current driven, which makes the input power requirement a function of external components that can be calculated assuming the input impedance of 130Ω. A typical input current value of $200\mu A_{RMS}$ is the only requirement for reliable LO generation. Figure 25 shows a typical 2XLO input network.

Divide by two flip flop architectures for LO generation often require tight control of signal purity or duty cycles. The HFA3724 has an internal duty cycle compensation scheme which eases the requirements of tight controlled duty cycles.

In addition, a 50Ω LO buffer is available to the user for PLL’s design reference. It substitutes a divide by two prescaler needed to bring the 2X LO frequency reference down. It is capable to drive $100mV_{P-P}$ into 50Ω and its frequency response is from 10MHz to 400MHz corresponding to a 2XLO input frequency response of 20MHz to 800MHz. The LO buffer can be disabled by removing the ground connection to the pin LO GND. The quadrature generator is always enabled for either transmit or receive modes.

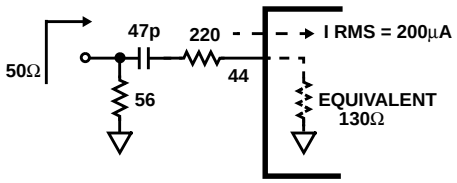


FIGURE 25. MOD LO IN (2XLO) EQUIVALENT CIRCUIT

Quadrature Up Converter

The Quadrature up converter mixers are also based on a doubly balanced Gilbert Cell design. “I” and “Q” Up converter signals are summed and buffered together through a single end open collector stage. As with the demodulators, both modulator mixers are driven from the same quadrature LO generator. It features a $\pm4^o$ and 0.5dB of phase and amplitude balance up to 400MHz which are reflected into its SSB characteristics. For “I” and “Q” differential inputs of $500mV_{P-P}$, 90^o apart, the carrier feedthrough or LO leakage is typical -30dBc into 250Ω with a sideband suppression of minimum 26dBc at 400MHz. Carrier feedthrough can be further improved by disabling the LO output port (please refer to pin#50 description) or using a DC bias network as in Figure 26. Featuring an output compression level of $1V_{P-P}$, the modulator output can generate a CW signal of typical -10dbm into 250Ω ($158mV_{RMS}$) when differential DC inputs of $500mV_{P-P}$ (equivalent to applying ±125mV ground referenced levels from the DC bias quiescent point of the device input) are applied to both “I” and “Q” inputs. Four quadrant phase shifts of the carrier output, like in Vector Modulator applications, can be set by proper choice of “I” and “Q” DC differential inputs, such that the square root of the sum of the squares of I and Q is constant.

Although specified to drive a 250Ω load, the HFA3724 modulator open collector output enables user designed output matching networks to suit any application interface.

The nominal AC current capability of this port is of $1.3mA_{RMS}$, which is shared between the termination resistor and the load for I and Q differential DC inputs of $500mV_{P-P}$ as explained above. (Use 70.7% of this AC capability for I and Q quadrature signals in case of SSB generation).

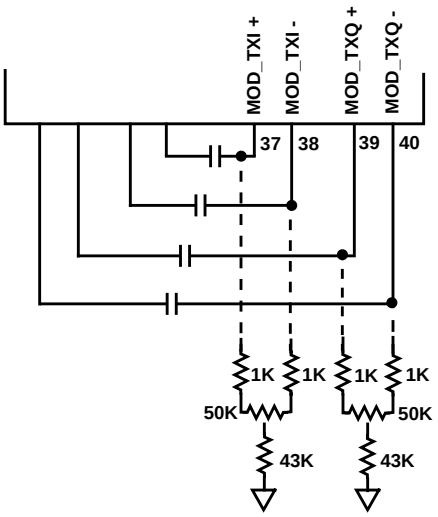


FIGURE 26. CARRIER NULL BIASING

Programmable Low Pass Filters

These filters are implemented using a 5th order Butterworth architecture. They are multiplexed, i.e., the same filter bank is used for both transmit and receive modes.

The filter block, in the transmit mode is set to accept digital (TTL threshold) input data for “I” and “Q” signals and is programmable with 4 frequency cutoffs: (2.2MHz, 4.4MHz, 8.8MHz and 17.8MHz). Digital control pins are used to switch all programmed cutoff modes. The user can design a multi data rate transceiver or simply hardwire these inputs. An external resistor is used to fine tune the cut off frequencies for each setting within ±20% of the nominal value. This feature is often needed to fulfill requirements of spectral mask compliance at the antenna output.

The “I” and “Q” filter matching is within 2^o for phase and 0.25dB for amplitude at the passband. Group delay characteristics follow closely a theoretical 5th order Butterworth design.

When in the receive mode, the filters exhibit a 0dB of gain with differential inputs and single ended outputs.

In the transmit mode, the digital ground referenced “I” and “Q” input signals are level shifted, shaped and buffered with constant driving differential outputs of $550mV_{P-P}$.

Baseband Digital Interfacing

Special precautions must be taken when interfacing the HFA3724 to a digital baseband processor: Large TTL signal swings, overshoots and current spikes, must be carefully considered when dealing with the generation of analog spread spectrum signals which are relatively much smaller in energy per bandwidth.

In order to avoid distortion or spurious tones on the analog transmit path, it may be necessary to decrease and/or limit digital excursions as much as possible without compromising the specifications. Figure 27 shows a simplified block diagram of the Transmit digital inputs.

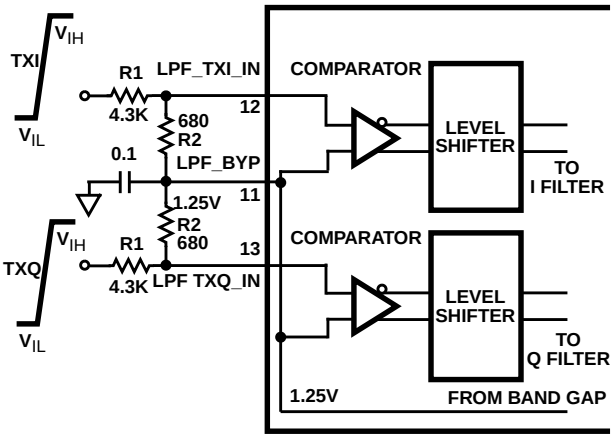


FIGURE 27. SIMPLIFIED BLOCK DIAGRAM OF THE TRANSMIT DIGITAL INPUTS

Because of the input comparators high gain, a small overdrive of about ±150mV from the reference level of 1.25V is all what is needed to reliably switch and level shift the “I” and “Q” digital signals. An external attenuator comprising of R1 and R2 with termination in the available 1.25V reference voltage pin (LPF BYP) can be calculated based on expected V_{IH} and V_{IL} inputs from a digital interface. Capacitive coupling must be avoided which could affect rise and fall times needed for proper overdrive speed of the comparators. Limiting the digital excursion on those pins greatly reduce the possibility of signal corruption at the transmit chain.

Coupling Capacitors

Capacitor coupling is used to tie all HFA3724 blocks together. Special bias is used to maintain the DC levels on both ends of coupling pins (capacitors) when the device is changes from Transmitter to a Receiver and vice versa. The capacitance values must be chosen as a compromise to maintain proper frequency response and settling times (when the device is brought up from sleep mode or power down).

AC Electrical Specifications, IF Limiter, Single Stage Individual Performance Full Supply Range, $T_A = 25^oC$

PARAMETER	SYMBOL	(NOTE 27) TEST LEVEL	MIN	TYP	MAX	UNITS
IF Frequency Range (Min Limited by Bypass Capacitors)	IFf	A	-	-	400	MHz
IF Voltage Gain	IFvG	A	39	45	-	dB
IF Amp. Noise Figure at 250Ω Source Input	IFNF	B	-	-	7	dB
Maximum IF Input, Single Ended	IFinmax	B	-	-	500	mV_{P-P}
IF Differential Limiting Output (1st Harmonic at 500Ω Load)	IFVpp	A	160	200	260	mV_{P-P}
IF Voltage Output Variation at -40dBm to -10dBm Input Range, 500Ω Load	IFVppl	A	-0.5	-	+0.5	dB
RSSI Slope, Current Output	IFRSSIsi	B		5.7	-	µA/dB
RSSI Slope, Voltage Output at 6K Load	IFRSSIv	A	25	34	45	mV/dB
RSSI Output Voltage Compliance	IFRSSIvc	B	-	-	V_{CC}- 0.7	V
RSSI DC Offset and Noise Induced Voltage at 6K Load	IFRSSIof	A	200	400	600	mV
RSSI Absolute Accuracy, V_{IN} = -40dBm	IFRSSIa	A	-10	-	+10	%
RSSI Rise and Fall Time at 50pF Load (-20dBm to -40dBm Input)	IFRSSIt	B	-	-	1	µs

NOTE:

27. A = Production Tested, B = Based on Characterization, C = By Design

TABLE 3. IF LIMITER S11, S22 PARAMETER

FREQUENCY	S11 (SINGLE ENDED)		S22 (DIFFERENTIAL)	
50MHz	0.96	-4.0^o	0.45	0.0^o
100MHz	0.95	-8.0^o	0.45	3.0^o
200MHz	0.91	-17.0^o	0.47	7.0^o
300MHz	0.84	-26.0^o	0.50	9.0^o
400MHz	0.80	-33.0^o	0.53	10.0^o

AC Electrical Specifications, I/Q Down Converter Individual Performance Full Supply Range, $T_A = 25^oC$

PARAMETER	SYMBOL	(NOTE 28) TEST LEVEL	MIN	TYP	MAX	UNITS
Quadrature Demodulator Input Frequency Range	QDf	B	10	-	400	MHz
Demodulator Baseband I/Q Frequency Range	QDIQf	C	-	-	30	MHz
Demodulator Voltage Gain at Frequency Range	QDg	A	6	8	9	dB
Demodulator Differential Input Resistance	Drin	C	-	1	-	kΩ
Demodulator Differential Input Capacitance	Dcin	C	-	0.5	-	pF

AC Electrical Specifications, I/Q Down Converter Individual Performance Full Supply Range, $T_A = 25^oC$ **(Continued)**

PARAMETER	SYMBOL	(NOTE 28) TEST LEVEL	MIN	TYP	MAX	UNITS
Demodulator Differential Output Level at 4K Load, Input = 200mV_{P-P}	QDdo	A	400	500	560	mV_{P-P}
Demodulator Amplitude Balance	QDab	A	-0.5	-	0.5	dB
Demodulator Phase Balance at 200MHz	QDpb	A	-1.85	-	1.85	Degrees
Demodulator Phase Balance at 400MHz	QDPb1	B	-4	-	4	Degrees
Demodulator Output Compression Voltage at 4K Load	QDoc	B	-	1.25	-	V_{P-P}

NOTE:

28. A = Production Tested, B = Based on Characterization, C = By Design

AC Electrical Specifications, I/Q Up Converter and LO Individual Performance Full Supply Range, $T_A = 25^oC$

PARAMETER	SYMBOL	(NOTE 29) TEST LEVEL	MIN	TYP	MAX	UNITS
2XLO Input Frequency Range (2 X Input Range)	LOinf	B	20	-	800	MHz
2XLO Input Current Range	LOinz	C	50	200	300	μA_{RMS}
2XLO Input Impedance	LOz	C	-	130	-	Ω
Buffered LO Output Voltage, Single Ended	BLOout	A	80	100	-	mV_{P-P}
Buffered LO Output Impedance	BLOoutZ	C	-	50	-	Ω
Quadrature IF Modulator Output Frequency Range	QMLOf	B	10	-	400	MHz
IF Modulator I/Q Input Frequency Range	QMIQf	C	-	-	30	MHz
IF Modulator Differential I/Q Max Input Voltage	QMdi	C	-	2.25	-	V_{P-P}
IF Modulator Differential I/Q Input Impedance	QMIQdz	C	-	4	-	kΩ
IF Modulator Differential Input Capacitance	Mcin	C	-	0.5	-	pF
IF Modulator I/Q Amplitude Balance	QMIQac	A	-0.5	-	0.5	dB
IF Modulator I/Q Phase Balance at 200MHz	QMIQpac	A	-2	-	2	Degrees
IF Modulator I/Q Phase Balance at 400MHz	QMIQp1	B	-4	-	4	Degrees
IF Modulator Output at SSB Into 50Ω, I and Q, 500mV_{P-P}	QMIFo	A	-22	-	-10.0	dBm
IF Modulator Carrier Suppression (LO Buffer Enabled)	QMCs	A	28	30	-	dBc
IF Modulator Carrier Suppression (LO Buffer Disabled)	QMCs1	A	28	36	-	dBc
IF Modulator SSB Sideband Suppression at 200MHz	QMSSBs	A	28	-	-	dBc
IF Modulator SSB Sideband Suppression at 400MHz	QMSSBs	B	26	-	-	dBc
IF Output Level Compression Point	QMIFP1	C	-	1.0	-	V_{P-P}
IF Modulator Intermodulation Suppression	QMIMsup	B	26	-	-	dBc

NOTE:

29. A = Production Tested, B = Based on Characterization, C = By Design

TABLE 4. QUADRATURE MODULATOR S22 PARAMETER

FREQUENCY	S22	
50MHz	0.99	-2.8^{o}
100MHz	0.98	-6.5^{o}
200MHz	0.96	-12.3^{o}
300MHz	0.87	-25.1^{o}
400MHz	0.82	-30.8^{o}

AC Electrical Specifications, TX Buffer Individual Performance Full Supply Range, $T_A = 25^{o}C$

PARAMETER	SYMBOL	(NOTE 30) TEST LEVEL	MIN	TYP	MAX	UNITS
TX LPF Buffer Serial Data Rate	TXBrat	A	-	11	22	MBPS
TX LPF Buffer Digital Input Impedance	LPFDz	C	10	12.5	-	kΩ

NOTE:

30. A = Production Tested, B = Based on Characterization, C = By Design

AC Electrical Specifications, RX/TX 5TH Order LPF Individual Performance Full Supply Range, $T_A = 25^{o}C$

PARAMETER	SYMBOL	(NOTE 31) TEST LEVEL	MIN	TYP	MAX	UNITS
TX/RX LPF 3dB Bandwidth, Sel0 = 0, Sel1 = 0	LPF3db0	A	1.8	2.20	2.4	MHz
TX/RX LPF 3dB Bandwidth, Sel0 = 1, Sel1 = 0	LPF3db1	A	3.6	4.40	4.8	MHz
TX/RX LPF 3dB Bandwidth, Sel0 = 0, Sel1 = 1	LPF3db2	A	7.4	8.80	9.6	MHz
TX/RX LPF 3dB Bandwidth, Sel0 = 1, Sel1 = 1	LPF3db3	A	14.8	17.60	19.2	MHz
TX/RX LPF Sel0, Sel1 Tuning Speed	LPFsp	B	-	-	1	µs
TX/RX LPF 3dB Bandwidth Tuning	LPFtu	A	-20	-	+20	%
LPF Tune Nominal Resistance	LPFTr	B	-	787	-	Ω
RX LPF Voltage Gain	LPFg	A	-1.0	0	1.0	dB
RX LPF Single Ended Output Voltage Swing at 2kΩ Load	LPFRXar	B	-	500	-	mV_{P-P}
RX LPF Differential Input Impedance	LPFRXzi	A	4	5	-	kΩ
TX LPF Differential Digital Output Voltage Swing at 4kΩ Load	LPFTXo	A	450	550	670	mV_{P-P}
TX/RX I/Q Channel Amplitude Match	LPFIQm	A	-0.5	-	0.5	dB
TX/RX I/Q Channel Phase Match	LPFIQpm	A	-3	-	3	Degrees
TX/RX LPF Total Harmonic Distortion	LPFTHD	B	-	3	-	%

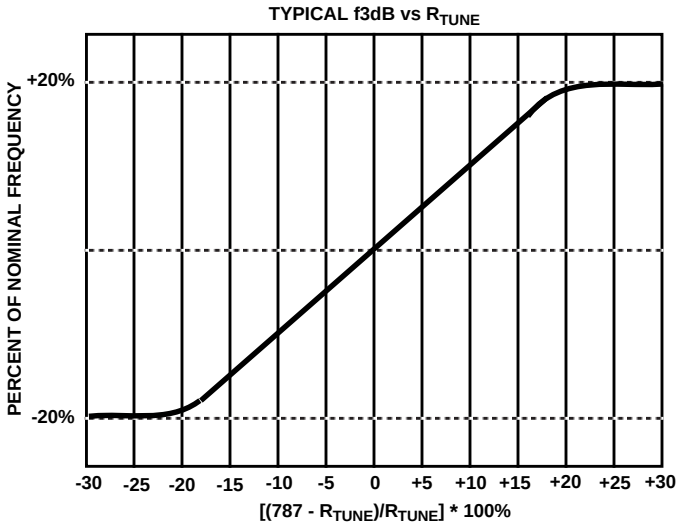
NOTE:

31. A = Production Tested, B = Based on Characterization, C = By Design

TABLE 5. LOW PASS FILTER PROGRAMMING AND TUNING INFORMATION

MODE	LPF SEL1	LPF SEL0	f_{3dB} (NOMINAL R_{TUNE})
BW0	0	0	2.2MHz
BW1	0	1	4.4MHz
BW2	1	0	8.8MHz
BW3	1	1	17.6MHz

$$f_{TUNED}3dB = \frac{f_{3dBNOMINAL} * 787}{R_{TUNE}}$$



FREQUENCY	R_{TUNE}
20% Low	984Ω
Nominal	787Ω
20% High	656Ω

FIGURE 28.

Typical Performance Curves, Individual Blocks

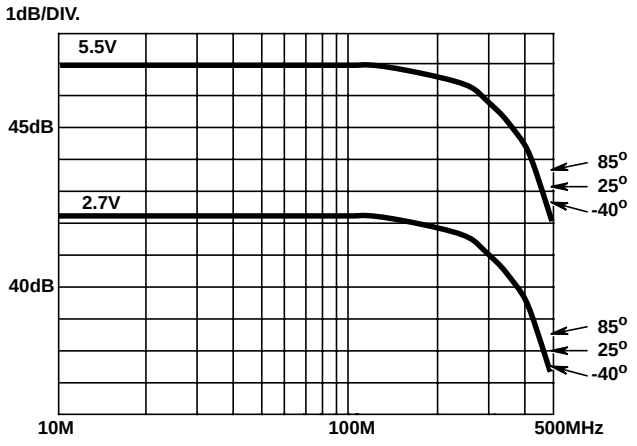


FIGURE 29. SINGLE STAGE LIMITER GAIN vs FREQUENCY AND TEMPERATURE, V_{CC} = 2.7V, 5.5V

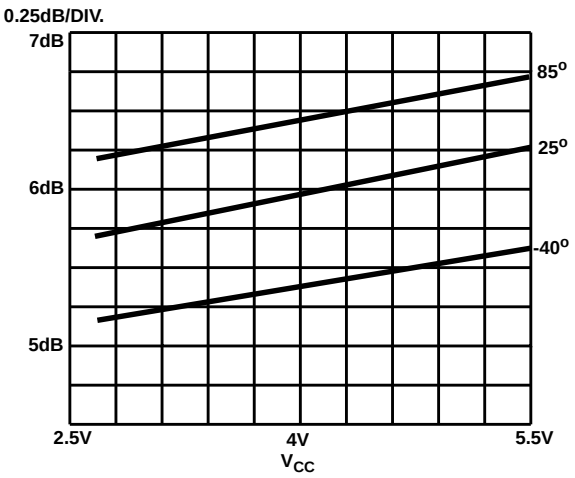
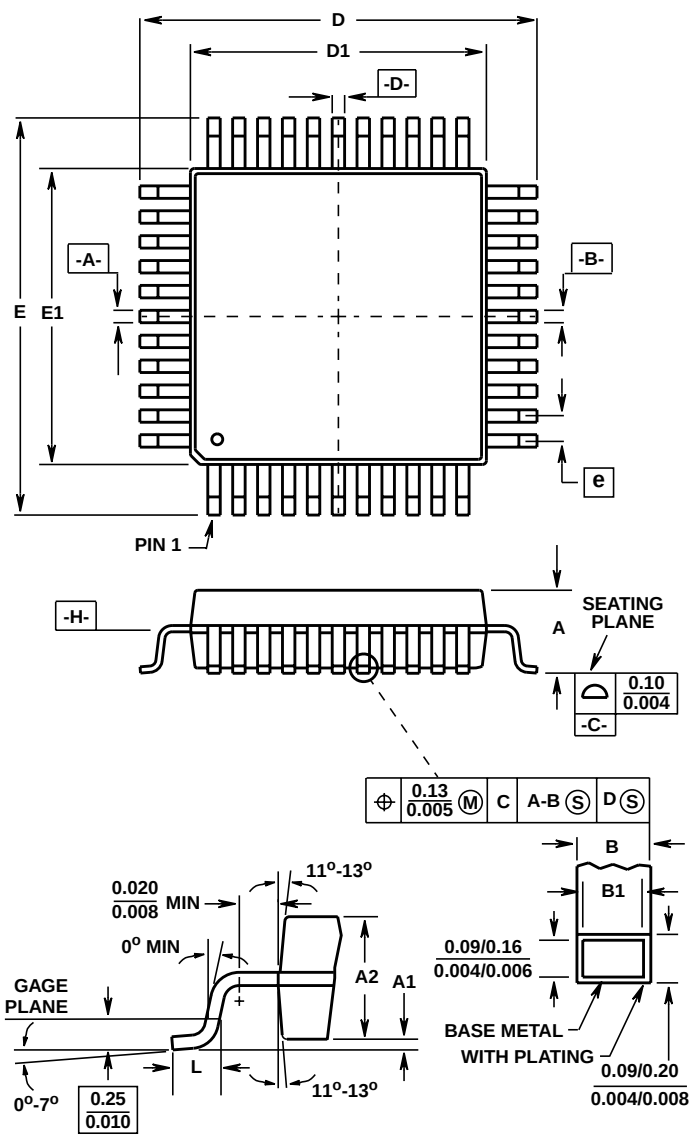


FIGURE 30. SINGLE STAGE LIMITER NOISE FIGURE vs V_{CC} AND TEMPERATURE, RS = 250Ω, FREQUENCY = 300MHz

Thin Plastic Quad Flatpack Packages (TQFP)



Q80.14x14 (JEDEC MO-136BQ ISSUE C)
80 LEAD THIN PLASTIC QUAD FLATPACK PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.062	-	1.60	-
A1	0.002	0.005	0.05	0.15	-
A2	0.054	0.057	1.35	1.45	-
B	0.009	0.014	0.22	0.38	6
B1	0.009	0.012	0.22	0.33	-
D	0.623	0.637	15.80	16.20	3
D1	0.544	0.559	13.80	14.20	4, 5
E	0.623	0.637	15.80	16.20	3
E1	0.544	0.559	13.80	14.20	4, 5
L	0.018	0.029	0.45	0.75	-
N	80		80		7
e	0.026 BSC		0.65 BSC		-

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NOTES:

1. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.
2. All dimensions and tolerances per ANSI Y14.5M-1982.
3. Dimensions D and E to be determined at seating plane -C-.
4. Dimensions D1 and E1 to be determined at datum plane -H-.
5. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25mm (0.010 inch) per side.
6. Dimension B does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum B dimension by more than 0.08mm (0.003 inch).
7. “N” is the number of terminal positions.

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