

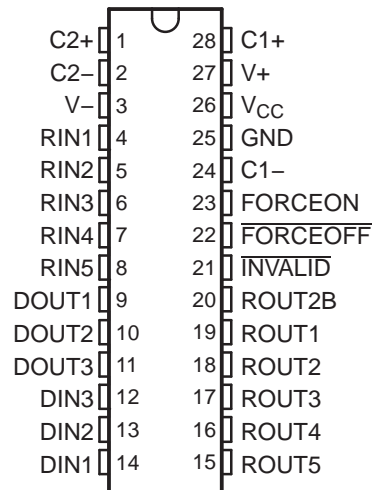
FEATURES

- Single-Chip and Single-Supply Interface for IBM™ PC/AT™ Serial Port
- RS-232 Bus-Pin ESD Protection Exceeds ± 15 kV Using Human-Body Model (HBM)
- Meets or Exceeds the Requirements of TIA/EIA-232-F and ITU v.28 Standards
- Operates With 3-V to 5.5-V V_{CC} Supply
- Three Drivers and Five Receivers
- Low Standby Current . . . 1 mA Typical
- External Capacitors . . . 4×0.1 mF
- Accepts 5-V Logic Input With 3.3-V Supply
- Always-Active Noninverting Receiver Output (ROUT2B)
- Operating Speed
 - TRS3243C, TRS3243I . . . 250 Kbit/s
 - TRS3243FC, TRS3243FI . . . 1000 Kbit/s
- Operating Temperature
 - TRS3243C, TRS3243FC . . . 0°C to 70°C
 - TRS3243I, TRS3243FI . . . –40°C to 85°C
- Serial-Mouse Driveability
- Auto-Powerdown Feature to Disable Driver Outputs When No Valid RS-232 Signal Is Sensed

APPLICATIONS

- Battery-Powered
- Systems
- PDAs
- Notebooks
- Laptops
- Palmtop
- PCs
- Hand-Held Equipment

DB, DW, OR PW PACKAGE
(TOP VIEW)



DESCRIPTION/ORDERING INFORMATION

The TRS3243 consists of three line drivers, five line receivers, and a dual charge-pump circuit with ± 15 -kV ESD (HBM) protection pin to pin (serial-port connection pins, including GND). The device meets the requirements of TIA/EIA-232-F and provides the electrical interface between an asynchronous communication controller and the serial-port connector. This combination of drivers and receivers matches that needed for the typical serial port used in an IBM PC/AT or compatible. The charge pump and four small external capacitors allow operation from a single 3-V to 5.5-V supply. In addition, the device includes an always-active noninverting output (ROUT2B), which allows applications using the ring indicator to transmit data while the device is powered down.

Flexible control options for power management are available when the serial port is inactive. The auto-powerdown feature functions when FORCEON is low and $\overline{\text{FORCEOFF}}$ is high. During this mode of operation, if the device does not sense a valid RS-232 signal, the driver outputs are disabled. If $\overline{\text{FORCEOFF}}$ is set low, both drivers and receivers (except ROUT2B) are shut off, and the supply current is reduced to 1 μA . Disconnecting the serial port or turning off the peripheral drivers causes the auto-powerdown condition to occur.

Auto-powerdown can be disabled when FORCEON and $\overline{\text{FORCEOFF}}$ are high and should be done when driving a serial mouse. With auto-powerdown enabled, the device is activated automatically when a valid signal is applied to any receiver input. The $\overline{\text{INVALID}}$ output is used to notify the user if an RS-232 signal is present at any receiver input. $\overline{\text{INVALID}}$ is high (valid data) if any receiver input voltage is greater than 2.7 V or less than –2.7 V or has been between –0.3 V and 0.3 V for less than 30 μs . $\overline{\text{INVALID}}$ is low (invalid data) if all receiver input voltages are between –0.3 V and 0.3 V for more than 30 μs . Refer to Figure 5 for receiver input levels.



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TRS3243
3-V TO 5.5-V MULTICHANNEL RS-232 LINE DRIVER/RECEIVER
WITH ± 15 -kV ESD (HBM) PROTECTION

SLLS806–JUNE 2007

ORDERING INFORMATION

T _A	PACKAGE ⁽¹⁾⁽²⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	SOIC – DW	Tube of 20	TRS3243CDW	TRS3243C
		Reel of 1000	TRS3243CDWR	
	SSOP – DB	Tube of 50	TRS3243CDB	TRS3243C
		Reel of 2000	TRS3243CDBR	
	TSSOP – PW	Tube of 50	TRS3243CPW	TRS3243
		Reel of 2000	TRS3243CPWR	
–40°C to 85°C	SOIC – DW	Tube of 50	TRS3243IDW	TRS3243I
		Reel of 2000	TRS3243IDWR	
	SSOP – DB	Tube of 50	TRS3243IDB	TRS3243I
		Reel of 2000	TRS3243IDBR	
	TSSOP – PW	Tube of 50	TRS3243IPW	TRS3243I
		Reel of 2000	TRS3243IPWR	

- (1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.
(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

FUNCTION TABLES

Each Driver⁽¹⁾

INPUTS				OUTPUT DOUT	DRIVER STATUS
DIN	FORCEON	FORCEOFF	VALID RIN RS-232 LEVEL		
X	X	L	X	Z	Powered off
L	H	H	X	H	Normal operation with auto-powerdown disabled
H	H	H	X	L	
L	L	H	Yes	H	Normal operation with auto-powerdown enabled
H	L	H	Yes	L	
L	L	H	No	Z	Power off by auto-powerdown feature
H	L	H	No	Z	

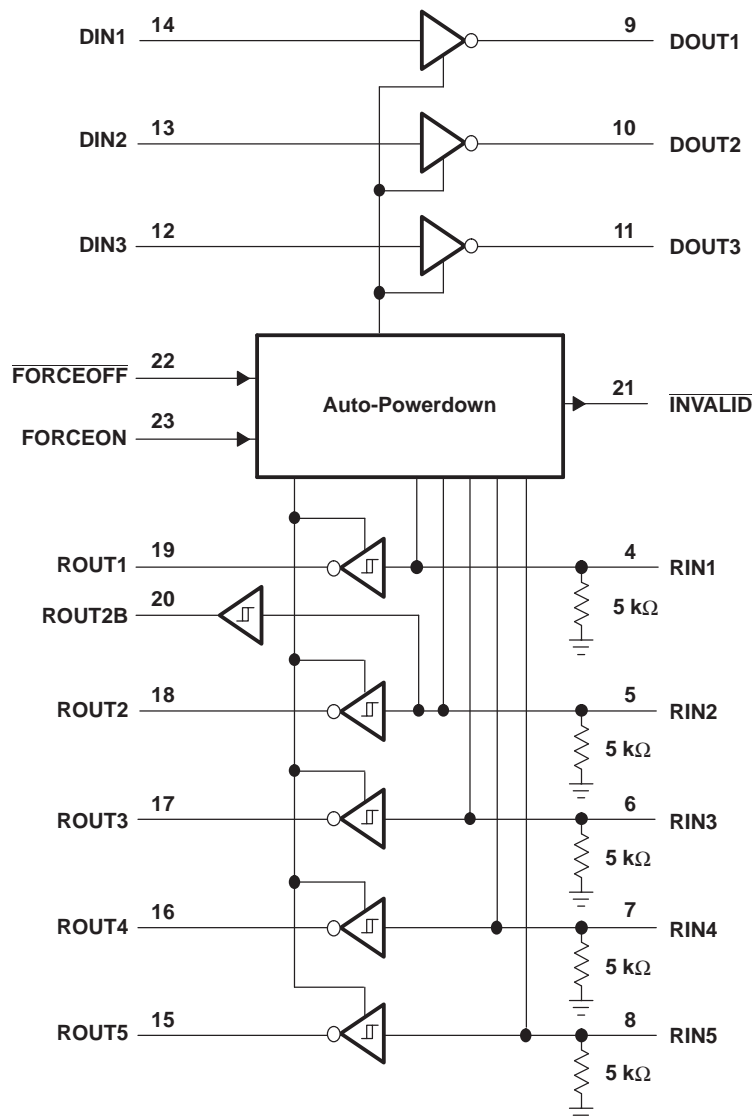
- (1) H = high level, L = low level, X = irrelevant, Z = high impedance

Each Receiver⁽¹⁾

INPUTS				OUTPUTS		RECEIVER STATUS
RIN2	RIN1, RIN3–RIN5	FORCEOFF	VALID RIN RS-232 LEVEL	ROUT2B	ROUT	
L	X	L	X	L	Z	Powered off while ROUT2B is active
H	X	L	X	H	Z	
L	L	H	Yes	L	H	Normal operation with auto-powerdown disabled/enabled
L	H	H	Yes	L	L	
H	L	H	Yes	H	H	
H	H	H	Yes	H	L	
Open	Open	H	Yes	L	H	

- (1) H = high level, L = low level, X = irrelevant, Z = high impedance (off), Open = input disconnected or connected driver off

LOGIC DIAGRAM (POSITIVE LOGIC)



TRS3243

3-V TO 5.5-V MULTICHANNEL RS-232 LINE DRIVER/RECEIVER

WITH ± 15 -kV ESD (HBM) PROTECTION

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Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V _{CC}	Supply voltage range ⁽²⁾		−0.3	6	V
V+	Positive output supply voltage range ⁽²⁾		−0.3	7	V
V−	Negative output supply voltage range ⁽²⁾		0.3	−7	V
V+ − V−	Supply voltage difference ⁽²⁾			13	V
V _I	Input voltage range	Driver (FORCEOFF, FORCEON)	−0.3	6	V
		Receiver	−25	25	
V _O	Output voltage range	Driver	−13.2	13.2	V
		Receiver (INVALID)	−0.3	V _{CC} + 0.3	
θ _{JA}	Package thermal impedance ⁽³⁾⁽⁴⁾	DB package		62	°C/W
		DW package		46	
		PW package		62	
T _J	Operating virtual junction temperature			150	°C
T _{stg}	Storage temperature range		−65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to network GND.
- (3) Maximum power dissipation is a function of T_J(max), θ_{JA} , and T_A. The maximum allowable power dissipation at any allowable ambient temperature is P_D = (T_J(max) − T_A)/ θ_{JA} . Operating at the absolute maximum T_J of 150°C can affect reliability.
- (4) The package thermal impedance is calculated in accordance with JEDEC 51-7.

Recommended Operating Conditions⁽¹⁾

See [Figure 6](#)

		MIN	NOM	MAX	UNIT
Supply voltage	V _{CC} = 3.3 V	3	3.3	3.6	V
	V _{CC} = 5 V	4.5	5	5.5	
V _{IH} Driver and control high-level input voltage	DIN, FORCEOFF, FORCEON	V _{CC} = 3.3 V	2		V
		V _{CC} = 5 V	2.4		
V _{IL} Driver and control low-level input voltage	DIN, FORCEOFF, FORCEON			0.8	V
V _I Driver and control input voltage	DIN, FORCEOFF, FORCEON	0		5.5	V
V _I Receiver input voltage		−25		25	V
T _A Operating free-air temperature	TRS3243C, TRS3243FC	0		70	°C
	TRS3243I, TRS3243FI	−40		85	

- (1) Test conditions are C1–C4 = 0.1 μ F at V_{CC} = 3.3 V \pm 0.3 V; C1 = 0.047 μ F, C2–C4 = 0.33 μ F at V_{CC} = 5 V \pm 0.5 V.

Electrical Characteristics⁽¹⁾

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [Figure 6](#))

PARAMETER	TEST CONDITIONS	MIN	TYP ⁽²⁾	MAX	UNIT
I _I Input leakage current	FORCEOFF, FORCEON		± 0.01	± 1	μ A
I _{CC} Supply current (T _A = 25°C)	Auto-powerdown disabled	No load, FORCEOFF and FORCEON at V _{CC}	0.3	1	μ A
	Powered off	No load, FORCEOFF at GND	1	10	
	Auto-powerdown enabled	No load, FORCEOFF at V _{CC} , FORCEON at GND, All RIN are open or grounded, All DIN are grounded	1	10	

- (1) Test conditions are C1–C4 = 0.1 μ F at V_{CC} = 3.3 V \pm 0.3 V; C1 = 0.047 μ F, C2–C4 = 0.33 μ F at V_{CC} = 5 V \pm 0.5 V.
- (2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

DRIVER SECTION

Electrical Characteristics⁽¹⁾

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [Figure 6](#))

PARAMETER	TEST CONDITIONS	MIN	TYP ⁽²⁾	MAX	UNIT
V _{OH} High-level output voltage	All DOUT at R _L = 3 k Ω to GND	5	5.4		V
V _{OL} Low-level output voltage	All DOUT at R _L = 3 k Ω to GND	–5	–5.4		V
V _O Output voltage (mouse driveability)	DIN1 = DIN2 = GND, DIN3 = V _{CC} , 3-k Ω to GND at DOUT3, DOUT1 = DOUT2 = 2.5 mA	± 5			V
I _{IH} High-level input current	V _I = V _{CC}		± 0.01	± 1	μ A
I _{IL} Low-level input current	V _I at GND		± 0.01	± 1	μ A
V _{hys} Input hysteresis				± 1	V
I _{OS} Short-circuit output current ⁽³⁾	V _{CC} = 3.6 V, V _O = 0 V		± 35	± 60	mA
	V _{CC} = 5.5 V, V _O = 0 V		± 35	± 60	
r _o Output resistance	V _{CC} , V+, and V– = 0 V, V _O = ± 2 V	300	10M		Ω
I _{off} Output leakage current	FORCEOFF = GND, V _O = ± 12 V, V _{CC} = 3 V to 3.6 V			± 25	μ A
				± 25	

(1) Test conditions are C1–C4 = 0.1 μ F at V_{CC} = 3.3 V \pm 0.3 V; C1 = 0.047 μ F, C2–C4 = 0.33 μ F at V_{CC} = 5 V \pm 0.5 V.

(2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

(3) Short-circuit durations should be controlled to prevent exceeding the device absolute power dissipation ratings, and not more than one output should be shorted at a time.

Switching Characteristics⁽¹⁾

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [Figure 6](#))

PARAMETER	TEST CONDITIONS	TRS3243C, TRS3243I			UNIT
		MIN	TYP ⁽²⁾	MAX	
Maximum data rate	C _L = 1000 pF, R _L = 3 k Ω , One DOUT switching, See Figure 1	150	250		kbit/s
t _{sk(p)} Pulse skew ⁽³⁾	C _L = 150 pF to 2500 pF, R _L = 3 k Ω to 7 k Ω , See Figure 2		100		ns
SR(tr) Slew rate, transition region (see Figure 1)	V _{CC} = 3.3 V, R _L = 3 k Ω to 7 k Ω	C _L = 150 pF to 1000 pF	6	30	V/ μ s
		C _L = 150 pF to 2500 pF	4	30	

(1) Test conditions are C1–C4 = 0.1 μ F at V_{CC} = 3.3 V \pm 0.3 V; C1 = 0.047 μ F, C2–C4 = 0.33 μ F at V_{CC} = 5 V \pm 0.5 V.

(2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

(3) Pulse skew is defined as |t_{PLH} – t_{PHL}| of each channel of the same device.

Switching Characteristics⁽¹⁾

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [Figure 6](#))

PARAMETER	TEST CONDITIONS	TRS3243FC, TRS3243FI			UNIT
		MIN	TYP ⁽²⁾	MAX	
Maximum data rate (see Figure 1)	R _L = 3 k Ω , One DOUT switching,	C _L = 1000 pF	250		kbit/s
		C _L = 250 pF, V _{CC} = 3 V to 4.5 V	1000		
		C _L = 1000 pF, V _{CC} = 4.5 V to 4.5 V	1000		
t _{sk(p)} Pulse skew ⁽³⁾	C _L = 150 pF to 2500 pF, R _L = 3 k Ω to 7 k Ω , See Figure 2		25		ns
SR(tr) Slew rate, transition region (see Figure 1)	C _L = 150 pF to 1000 pF, R _L = 3 k Ω to 7 k Ω , V _{CC} = 3.3 V	18		150	V/ μ s

(1) Test conditions are C1–C4 = 0.1 μ F at V_{CC} = 3.3 V \pm 0.3 V; C1 = 0.047 μ F, C2–C4 = 0.33 μ F at V_{CC} = 5 V \pm 0.5 V.

(2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

(3) Pulse skew is defined as |t_{PLH} – t_{PHL}| of each channel of the same device.

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WITH ± 15 -kV ESD (HBM) PROTECTION

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RECEIVER SECTION

Electrical Characteristics⁽¹⁾

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [Figure 6](#))

PARAMETER	TEST CONDITIONS	MIN	TYP ⁽²⁾	MAX	UNIT
V _{OH} High-level output voltage	I _{OH} = –1 mA	V _{CC} – 0.6	V _{CC} – 0.1		V
V _{OL} Low-level output voltage	I _{OH} = 1.6 mA			0.4	V
V _{IT+} Positive-going input threshold voltage	V _{CC} = 3.3 V		1.6	2.4	V
	V _{CC} = 5 V		1.9	2.4	
V _{IT–} Negative-going input threshold voltage	V _{CC} = 3.3 V	0.6	1.1		V
	V _{CC} = 5 V	0.8	1.4		
V _{hys} Input hysteresis (V _{IT+} – V _{IT–})			0.5		V
I _{off} Output leakage current (except ROUT2B)	FORCEOFF = 0 V		±0.05	±10	µA
r _i Input resistance	V _i = ±3 V or ±25 V	3	5	7	kΩ

(1) Test conditions are C1–C4 = 0.1 µF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 µF, C2–C4 = 0.33 µF at V_{CC} = 5 V ± 0.5 V.

(2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

Switching Characteristics⁽¹⁾

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	TYP ⁽²⁾	UNIT
t _{PLH} Propagation delay time, low- to high-level output	C _L = 150 pF, See Figure 3	150	ns
t _{PHL} Propagation delay time, high- to low-level output		150	ns
t _{en} Output enable time	C _L = 150 pF, R _L = 3 kΩ, See Figure 4	200	ns
t _{dis} Output disable time		200	ns
t _{sk(p)} Pulse skew ⁽³⁾	See Figure 3	50	ns

(1) Test conditions are C1–C4 = 0.1 µF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 µF, C2–C4 = 0.33 µF at V_{CC} = 5 V ± 0.5 V.

(2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

(3) Pulse skew is defined as |t_{PLH} – t_{PHL}| of each channel of the same device.

AUTO-POWERDOWN SECTION

Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [Figure 5](#))

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$V_{IT+(valid)}$	Receiver input threshold for INVALID high-level output voltage	FORCEON = GND, $\overline{FORCEOFF} = V_{CC}$		2.7	V
$V_{IT-(valid)}$	Receiver input threshold for INVALID high-level output voltage	FORCEON = GND, $\overline{FORCEOFF} = V_{CC}$	–2.7		V
$V_{T(invalid)}$	Receiver input threshold for INVALID low-level output voltage	FORCEON = GND, $\overline{FORCEOFF} = V_{CC}$	–0.3	0.3	V
V_{OH}	INVALID high-level output voltage	$I_{OH} = -1$ mA, FORCEON = GND, $\overline{FORCEOFF} = V_{CC}$	$V_{CC} - 0.6$		V
V_{OL}	INVALID low-level output voltage	$I_{OL} = 1.6$ mA, FORCEON = GND, $\overline{FORCEOFF} = V_{CC}$		0.4	V

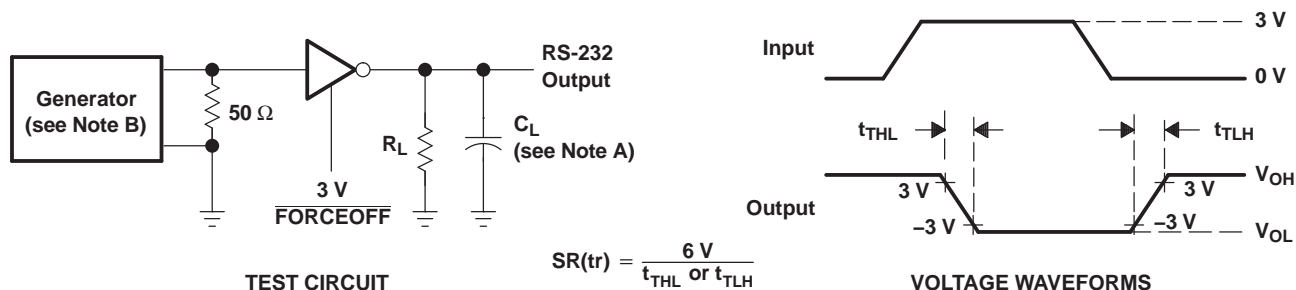
Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [Figure 5](#))

PARAMETER		TEST CONDITIONS	TYP ⁽¹⁾	UNIT
t_{valid}	Propagation delay time, low- to high-level output	$V_{CC} = 5$ V	1	μ s
$t_{invalid}$	Propagation delay time, high- to low-level output	$V_{CC} = 5$ V	30	μ s
t_{en}	Supply enable time	$V_{CC} = 5$ V	100	μ s

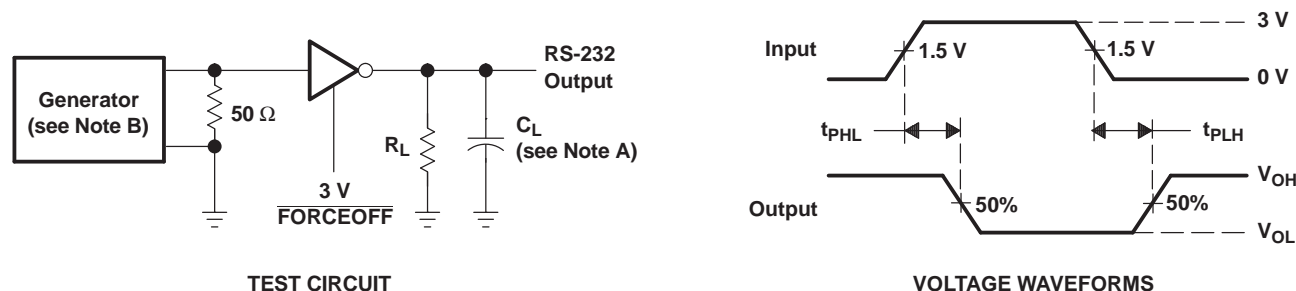
(1) All typical values are at $V_{CC} = 3.3$ V or $V_{CC} = 5$ V, and $T_A = 25^\circ\text{C}$.

PARAMETER MEASUREMENT INFORMATION



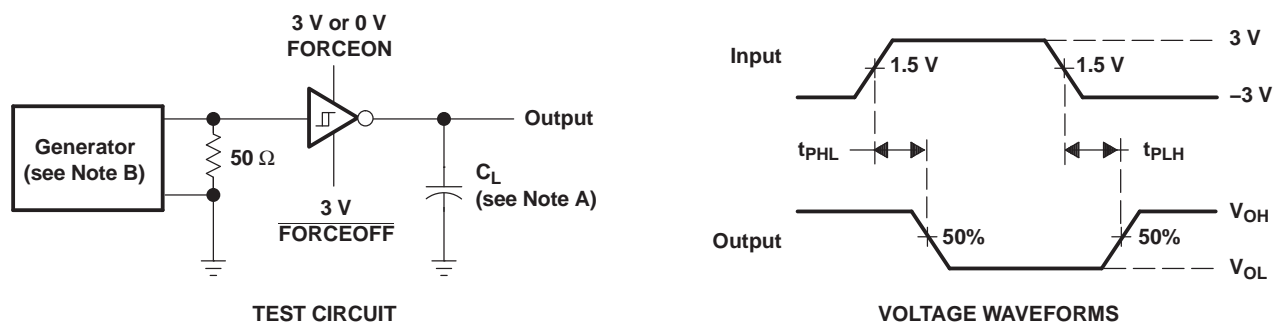
- NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: PRR = 250 kbit/s (MAX3243C/I) and 1 Mbit/s (MAX3243FC/I), $Z_O = 50\ \Omega$, 50% duty cycle, $t_r \leq 10\text{ ns}$, $t_f \leq 10\text{ ns}$.

Figure 1. Driver Slew Rate



- NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: PRR = 250 kbit/s (MAX3243C/I) and 1 Mbit/s (MAX3243FC/I), $Z_O = 50\ \Omega$, 50% duty cycle, $t_r \leq 10\text{ ns}$, $t_f \leq 10\text{ ns}$.

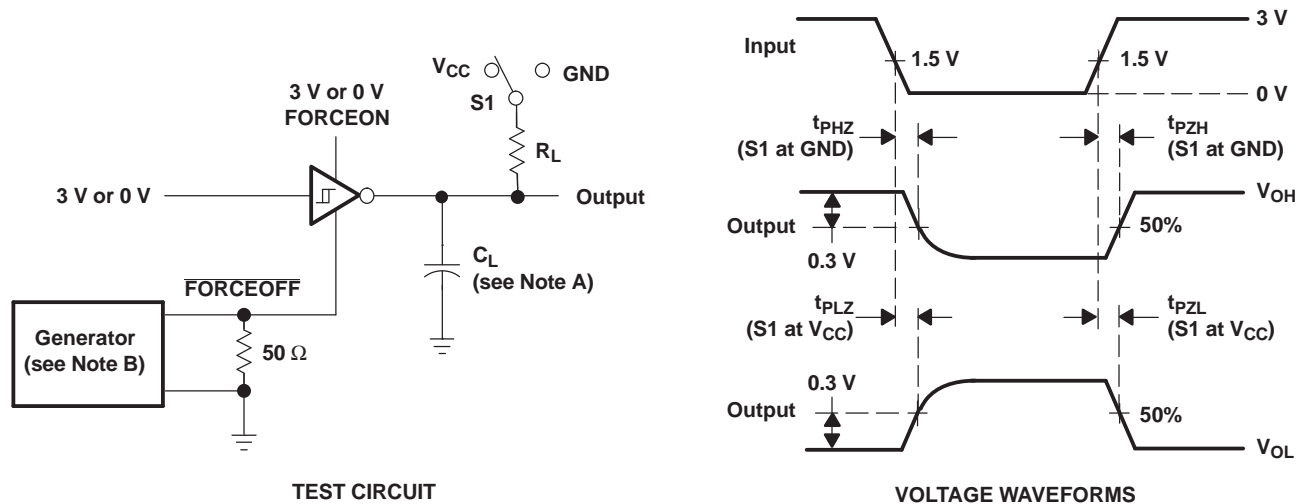
Figure 2. Driver Pulse Skew



- NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: $Z_O = 50\ \Omega$, 50% duty cycle, $t_r \leq 10\text{ ns}$, $t_f \leq 10\text{ ns}$.

Figure 3. Receiver Propagation Delay Times

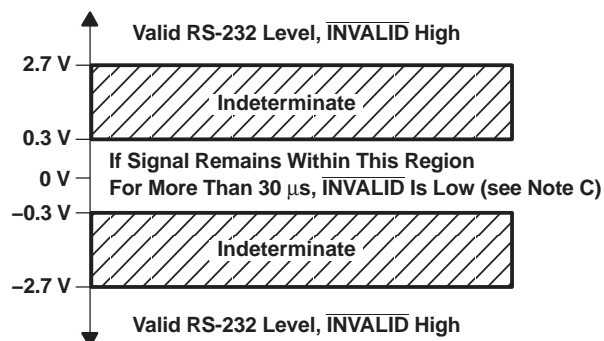
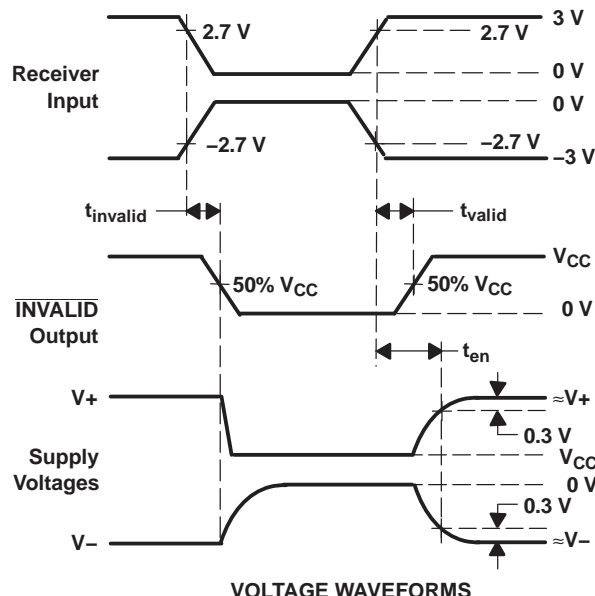
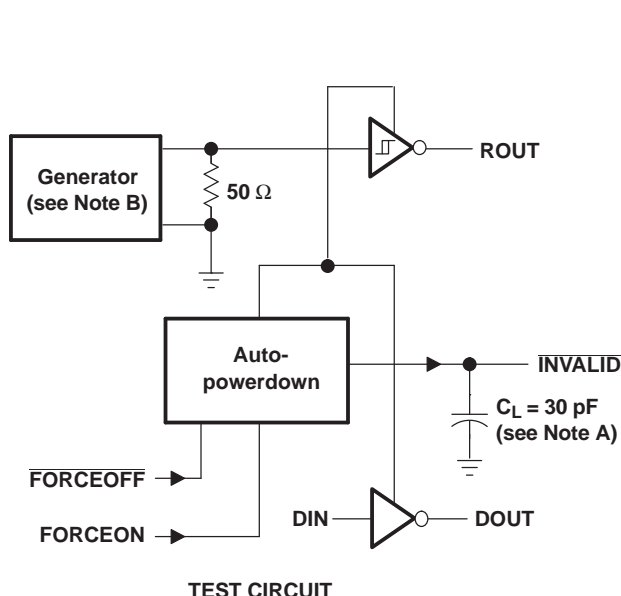
PARAMETER MEASUREMENT INFORMATION (continued)



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. The pulse generator has the following characteristics: $Z_O = 50\ \Omega$, 50% duty cycle, $t_r \leq 10\text{ ns}$, $t_f \leq 10\text{ ns}$.
 - C. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - D. t_{PZL} and t_{PZH} are the same as t_{en} .

Figure 4. Receiver Enable and Disable Times

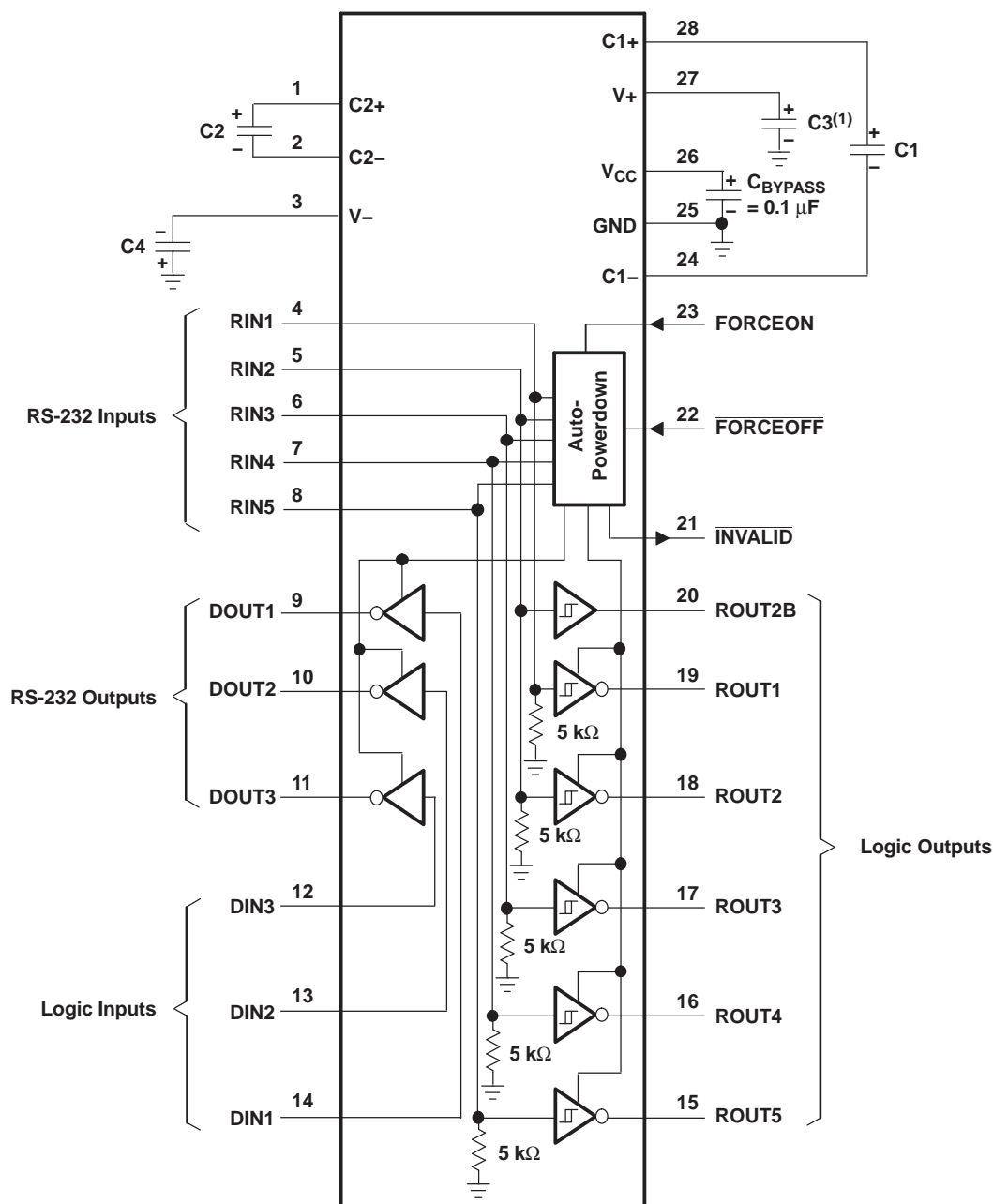
PARAMETER MEASUREMENT INFORMATION (continued)



- NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: PRR = 5 kbit/s, $Z_O = 50 \Omega$, 50% duty cycle, $t_r \leq 10$ ns, $t_f \leq 10$ ns.
C. Auto-powerdown disables drivers and reduces supply current to 1 μ A.

Figure 5. $\overline{\text{INVALID}}$ Propagation Delay Times and Supply Enabling Time

APPLICATION INFORMATION



(1) C3 can be connected to V_{CC} or GND.

NOTES: A. Resistor values shown are nominal.

B. Nonpolarized ceramic capacitors are acceptable. If polarized tantalum or electrolytic capacitors are used, they should be connected as shown.

V_{CC} vs CAPACITOR VALUES

V_{CC}	C1	C2, C3, and C4
3.3 V \pm 0.3 V	0.1 μ F	0.1 μ F
5 V \pm 0.5 V	0.047 μ F	0.33 μ F
3 V to 5.5 V	0.1 μ F	0.47 μ F

Figure 6. Typical Operating Circuit and Capacitor Values

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TRS3243CDB	ACTIVE	SSOP	DB	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TRS3243C	Samples
TRS3243CDBG4	ACTIVE	SSOP	DB	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TRS3243C	Samples
TRS3243CDBR	ACTIVE	SSOP	DB	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TRS3243C	Samples
TRS3243CDBRG4	ACTIVE	SSOP	DB	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TRS3243C	Samples
TRS3243CDW	ACTIVE	SOIC	DW	28	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TRS3243C	Samples
TRS3243CDWG4	ACTIVE	SOIC	DW	28	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TRS3243C	Samples
TRS3243CDWR	ACTIVE	SOIC	DW	28	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TRS3243C	Samples
TRS3243CDWRG4	ACTIVE	SOIC	DW	28	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TRS3243C	Samples
TRS3243CPW	ACTIVE	TSSOP	PW	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	RS43C	Samples
TRS3243CPWG4	ACTIVE	TSSOP	PW	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	RS43C	Samples
TRS3243CPWR	ACTIVE	TSSOP	PW	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	RS43C	Samples
TRS3243CPWRG4	ACTIVE	TSSOP	PW	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	RS43C	Samples
TRS3243IDB	ACTIVE	SSOP	DB	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TRS3243I	Samples
TRS3243IDBG4	ACTIVE	SSOP	DB	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TRS3243I	Samples
TRS3243IDBR	ACTIVE	SSOP	DB	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TRS3243I	Samples
TRS3243IDBRG4	ACTIVE	SSOP	DB	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TRS3243I	Samples
TRS3243IDW	ACTIVE	SOIC	DW	28	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TRS3243I	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TRS3243IDWG4	ACTIVE	SOIC	DW	28	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TRS3243I	Samples
TRS3243IDWR	ACTIVE	SOIC	DW	28	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TRS3243I	Samples
TRS3243IDWRG4	ACTIVE	SOIC	DW	28	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TRS3243I	Samples
TRS3243IPW	ACTIVE	TSSOP	PW	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	RS43I	Samples
TRS3243IPWG4	ACTIVE	TSSOP	PW	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	RS43I	Samples
TRS3243IPWR	ACTIVE	TSSOP	PW	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	RS43I	Samples
TRS3243IPWRG4	ACTIVE	TSSOP	PW	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	RS43I	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Only one of markings shown within the brackets will appear on the physical device.

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TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TRS3243CDBR	SSOP	DB	28	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
TRS3243CDWR	SOIC	DW	28	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1
TRS3243CPWR	TSSOP	PW	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1
TRS3243IDBR	SSOP	DB	28	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
TRS3243IDWR	SOIC	DW	28	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1
TRS3243IPWR	TSSOP	PW	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS

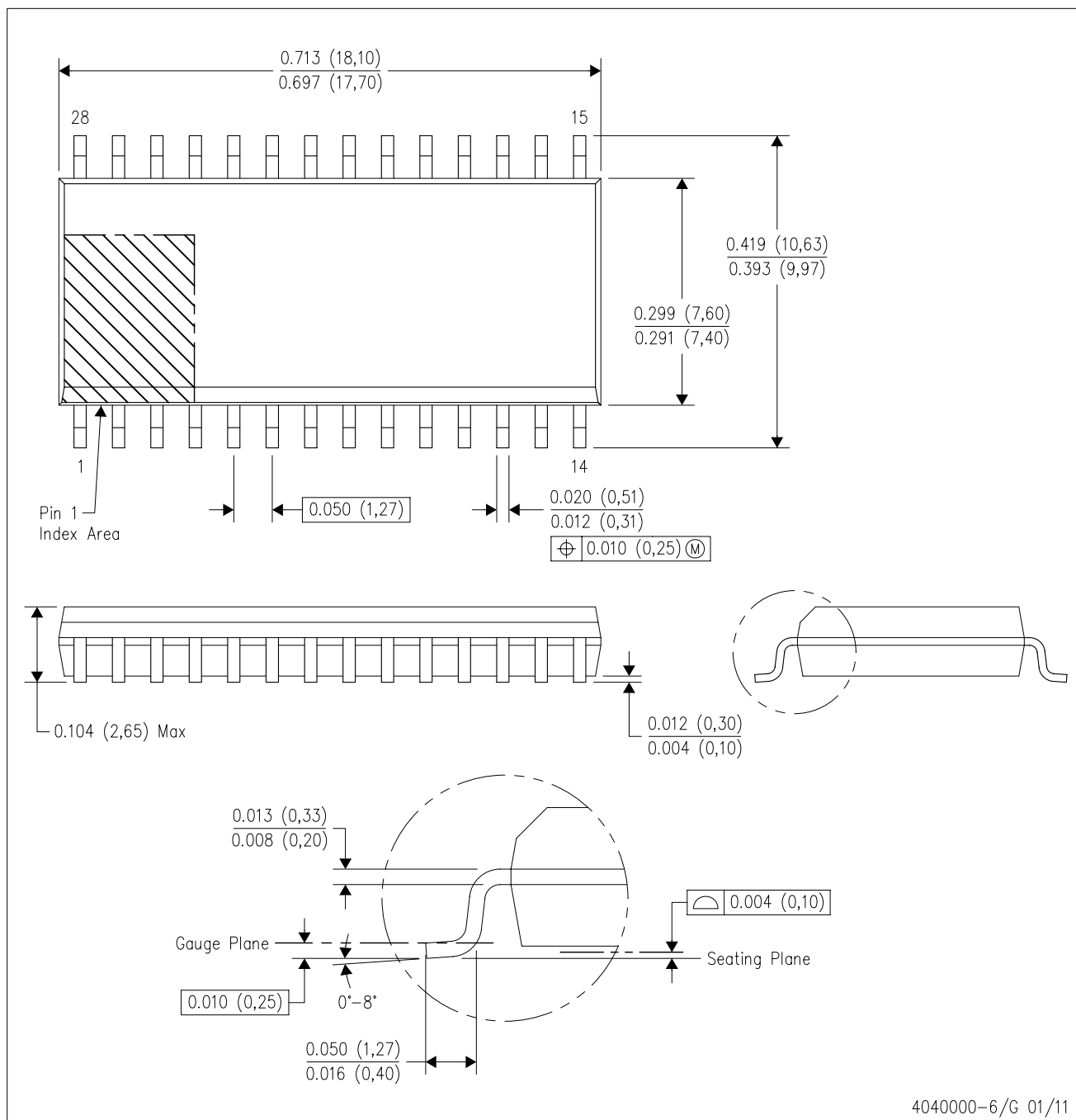


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TRS3243CDBR	SSOP	DB	28	2000	367.0	367.0	38.0
TRS3243CDWR	SOIC	DW	28	1000	367.0	367.0	55.0
TRS3243CPWR	TSSOP	PW	28	2000	367.0	367.0	38.0
TRS3243IDBR	SSOP	DB	28	2000	367.0	367.0	38.0
TRS3243IDWR	SOIC	DW	28	1000	367.0	367.0	55.0
TRS3243IPWR	TSSOP	PW	28	2000	367.0	367.0	38.0

DW (R-PDSO-G28)

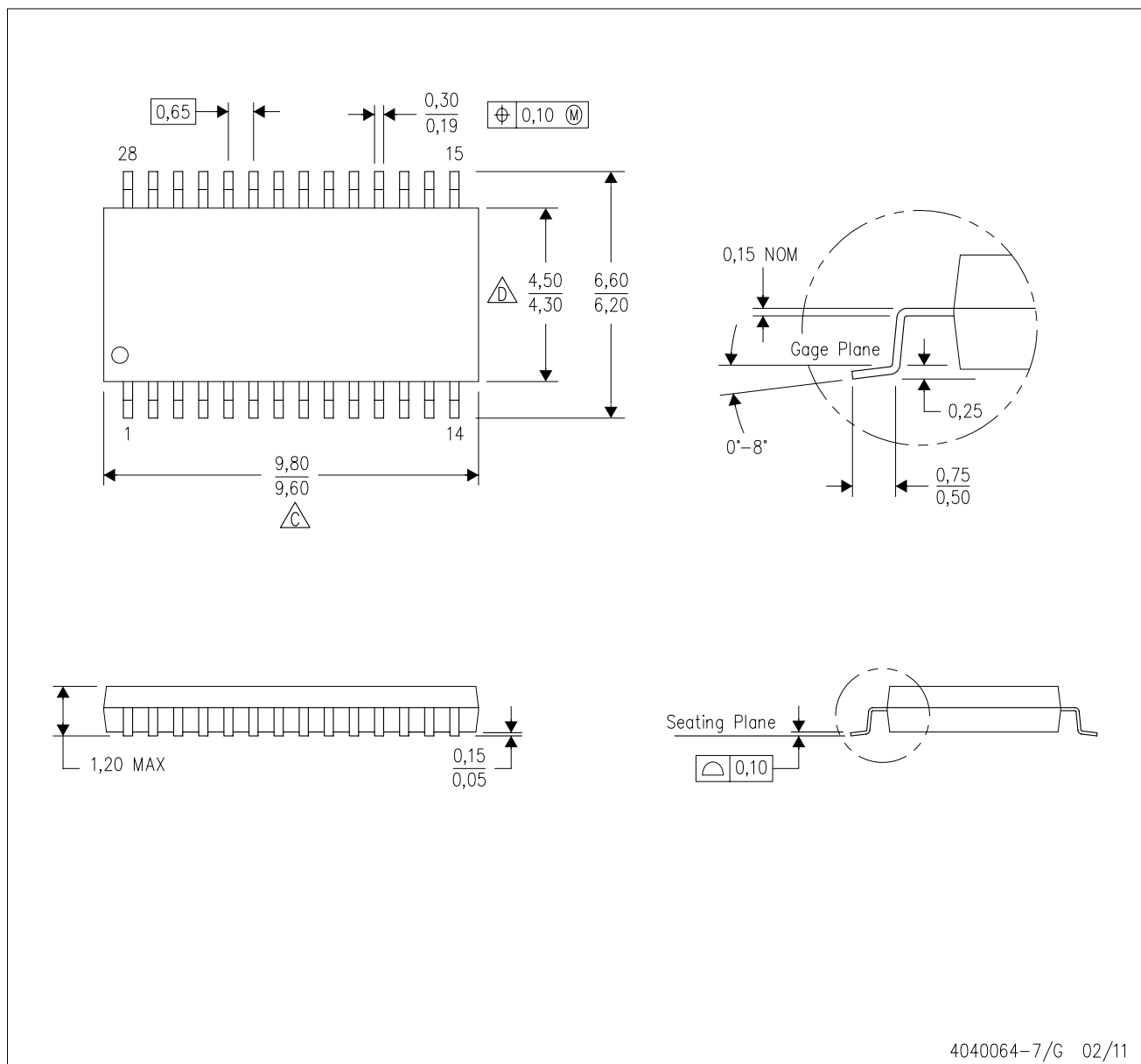
PLASTIC SMALL OUTLINE



4040000-6/G 01/11

PW (R-PDSO-G28)

PLASTIC SMALL OUTLINE

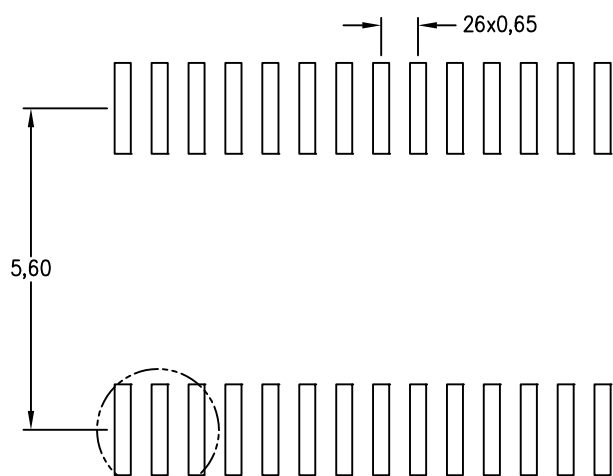


- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

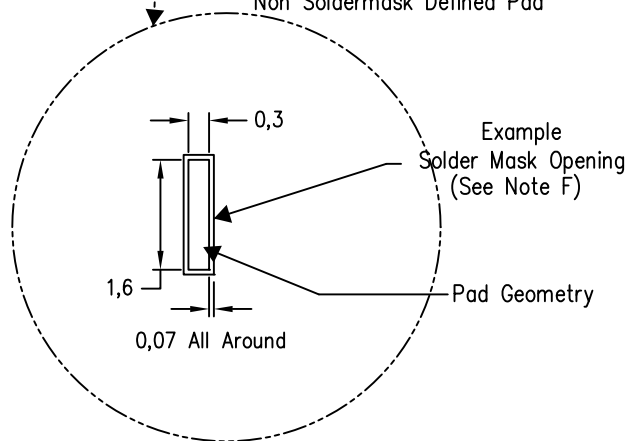
PW (R-PDSO-G28)

PLASTIC SMALL OUTLINE

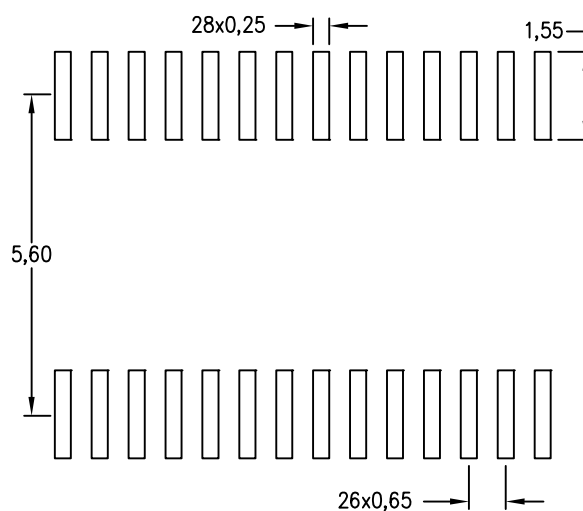
Example Board Layout



Example
Non Soldermask Defined Pad



Stencil Openings
Based on a stencil thickness
of .127mm (.005inch).



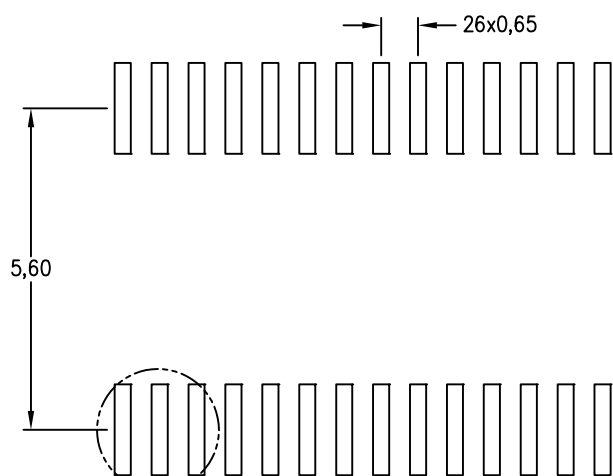
4211284-6/F 12/12

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate design.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

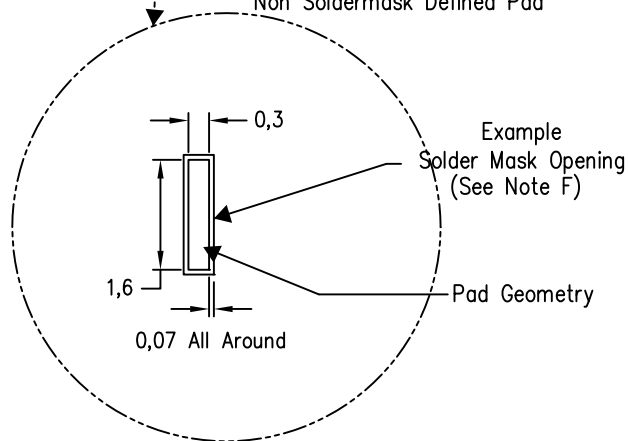
PW (R-PDSO-G28)

PLASTIC SMALL OUTLINE

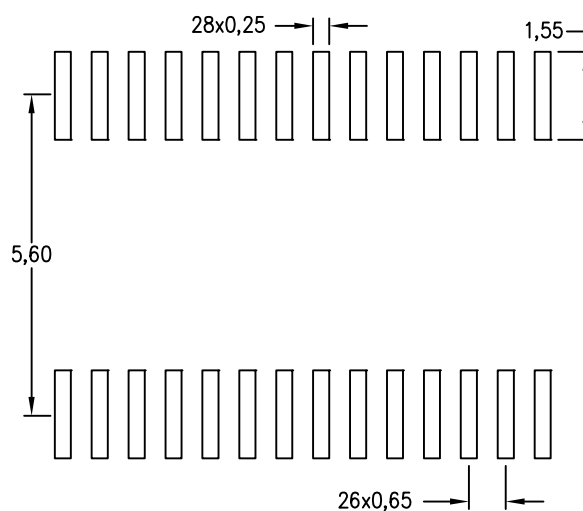
Example Board Layout



Example
Non Soldermask Defined Pad



Stencil Openings
Based on a stencil thickness
of .127mm (.005inch).



4211284-6/F 12/12

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate design.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

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