

# FDPF8N50NZU

## N-Channel UniFET™ II Ultra FRFET™ MOSFET

500 V, 6.5 A, 1.2  $\Omega$

### Features

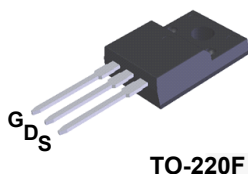
- $R_{DS(on)} = 1.0 \Omega$  (Typ.) @  $V_{GS} = 10 \text{ V}$ ,  $I_D = 3.25 \text{ A}$
- Low Gate Charge (Typ. 14 nC)
- Low  $C_{rss}$  (Typ. 5 pF)
- 100% Avalanche Tested
- Improved dv/dt Capability
- ESD Improved Capability
- RoHS Compliant

### Applications

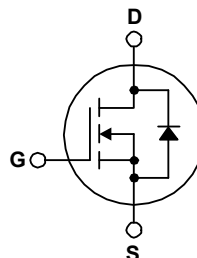
- LCD/LED TV
- Lighting
- Uninterruptible Power Supply
- AC-DC Power Supply

### Description

UniFET™ II MOSFET is Fairchild Semiconductor's high voltage MOSFET family based on advanced planar stripe and DMOS technology. This advanced MOSFET family has the smallest on-state resistance among the planar MOSFET, and also provides superior switching performance and higher avalanche energy strength. In addition, internal gate-source ESD diode allows UniFET II MOSFET to withstand over 2kV HBM surge stress. UniFET II Ultra FRFET™ MOSFET has much superior body diode reverse recovery performance. Its  $t_{rr}$  is less than 50nsec and the reverse dv/dt immunity is 20V/nsec while normal planar MOSFETs have over 200nsec and 4.5V/nsec respectively. Therefore UniFET II Ultra FRFET MOSFET can remove additional component and improve system reliability in certain applications that require performance improvement of the MOSFET's body diode. This device family is suitable for switching power converter applications such as power factor correction (PFC), flat panel display (FPD) TV power, ATX and electronic lamp ballasts.



TO-220F



### Absolute Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	FDPF8N50NZU	Unit
$V_{DSS}$	Drain to Source Voltage	500	V
$V_{GSS}$	Gate to Source Voltage	$\pm 25$	V
$I_D$	Drain Current	- Continuous ( $T_C = 25^\circ\text{C}$ )	A
		- Continuous ( $T_C = 100^\circ\text{C}$ )	
$I_{DM}$	Drain Current	- Pulsed (Note 1)	A
$E_{AS}$	Single Pulsed Avalanche Energy	(Note 2)	mJ
$I_{AR}$	Avalanche Current	(Note 1)	A
$E_{AR}$	Repetitive Avalanche Energy	(Note 1)	mJ
dv/dt	Peak Diode Recovery dv/dt	(Note 3)	V/ns
$P_D$	Power Dissipation	( $T_C = 25^\circ\text{C}$ )	W
		- Derate Above $25^\circ\text{C}$	W/ $^\circ\text{C}$
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$
$T_L$	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds	300	$^\circ\text{C}$

\*Drain current limited by maximum junction temperature

### Thermal Characteristics

Symbol	Parameter	FDPF8N50NZU	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	3.1	$^\circ\text{C/W}$
$R_{\theta CS}$	Thermal Resistance, Case to Sink, Typ.	0.5	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	62.5	

## Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FDPF8N50NZU	FDPF8N50NZU	TO-220F	Tube	N/A	N/A	50 units

## Electrical Characteristics T<sub>C</sub> = 25°C unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
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### Off Characteristics

BV <sub>DSS</sub>	Drain to Source Breakdown Voltage	I <sub>D</sub> = 250μA, V <sub>GS</sub> = 0V, T <sub>C</sub> = 25°C	500	-	-	V
ΔBV <sub>DSS</sub> / ΔT <sub>J</sub>	Breakdown Voltage Temperature Coefficient	I <sub>D</sub> = 250μA, Referenced to 25°C	-	0.5	-	V/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 500V, V <sub>GS</sub> = 0V	-	-	25	μA
		V <sub>DS</sub> = 400V, T <sub>C</sub> = 125°C	-	-	250	
I <sub>GSS</sub>	Gate to Body Leakage Current	V <sub>GS</sub> = ±25V, V <sub>DS</sub> = 0V	-	-	±10	μA

### On Characteristics

V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = 250μA	3.0	-	5.0	V
R <sub>DS(on)</sub>	Static Drain to Source On Resistance	V <sub>GS</sub> = 10V, I <sub>D</sub> = 4A	-	1.0	1.2	Ω
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> = 20V, I <sub>D</sub> = 4A	-	6.3	-	S

### Dynamic Characteristics

C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = 25V, V <sub>GS</sub> = 0V f = 1MHz	-	565	735	pF
C <sub>oss</sub>	Output Capacitance		-	80	105	pF
C <sub>rss</sub>	Reverse Transfer Capacitance		-	5	8	pF
Q <sub>g(tot)</sub>	Total Gate Charge at 10V	V <sub>DS</sub> = 400V, I <sub>D</sub> = 6.5A V <sub>GS</sub> = 10V	-	14	18	nC
Q <sub>gs</sub>	Gate to Source Gate Charge		-	4	-	nC
Q <sub>gd</sub>	Gate to Drain "Miller" Charge		-	6	-	nC

(Note 4)

### Switching Characteristics

t <sub>d(on)</sub>	Turn-On Delay Time	V <sub>DD</sub> = 250V, I <sub>D</sub> = 6.5A, V <sub>GS</sub> = 10V, R <sub>G</sub> = 25Ω	-	17	45	ns
t <sub>r</sub>	Turn-On Rise Time		-	34	80	ns
t <sub>d(off)</sub>	Turn-Off Delay Time		-	43	95	ns
t <sub>f</sub>	Turn-Off Fall Time		-	27	60	ns

(Note 4)

### Drain-Source Diode Characteristics

I <sub>S</sub>	Maximum Continuous Drain to Source Diode Forward Current		-	-	6.5	A
I <sub>SM</sub>	Maximum Pulsed Drain to Source Diode Forward Current		-	-	26	A
V <sub>SD</sub>	Drain to Source Diode Forward Voltage	V <sub>GS</sub> = 0V, I <sub>SD</sub> = 6.5A	-	-	1.6	V
t <sub>rr</sub>	Reverse Recovery Time	V <sub>GS</sub> = 0V, I <sub>SD</sub> = 6.5A	-	50	-	ns
Q <sub>rr</sub>	Reverse Recovery Charge	dI <sub>F</sub> /dt = 100A/μs	-	0.05	-	μC

#### Notes:

1. Repetitive rating: pulse-width limited by maximum junction temperature.
2. L = 3.8 mH, I<sub>AS</sub> = 6.5 A, V<sub>DD</sub> = 50 V, R<sub>G</sub> = 25 Ω, starting T<sub>J</sub> = 25°C.
3. I<sub>SD</sub> ≤ 6.5 A, di/dt ≤ 200 A/μs, V<sub>DD</sub> ≤ BV<sub>DSS</sub>, starting T<sub>J</sub> = 25°C.
4. Essentially independent of operating temperature typical characteristics.

# Typical Performance Characteristics

Figure 1. On-Region Characteristics

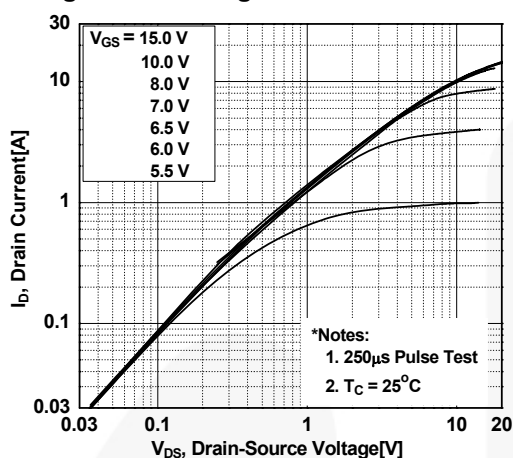


Figure 2. Transfer Characteristics

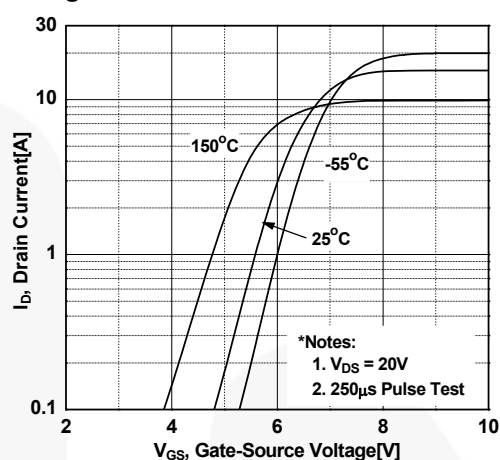


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

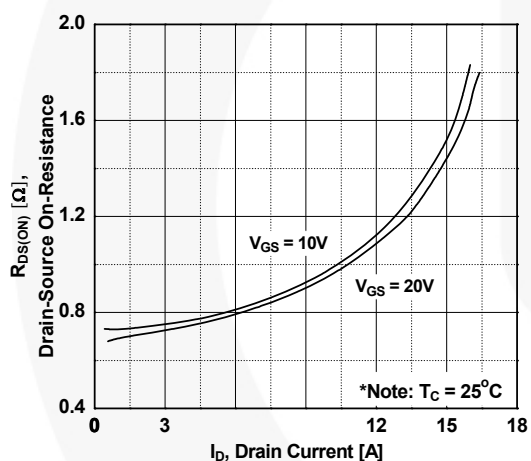


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

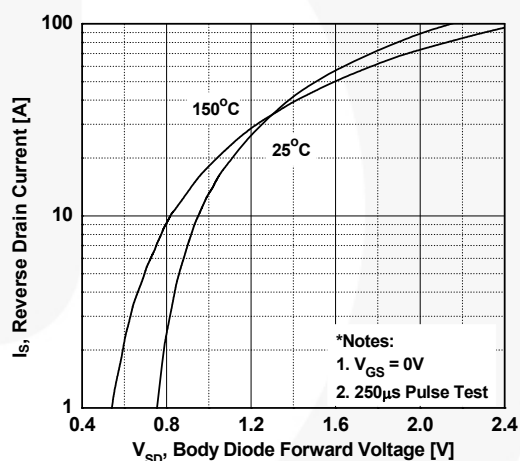


Figure 5. Capacitance Characteristics

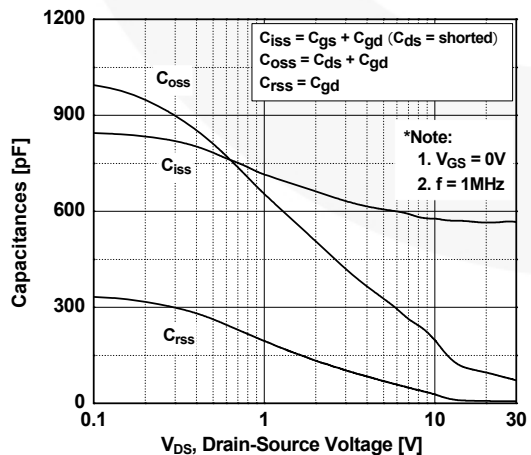
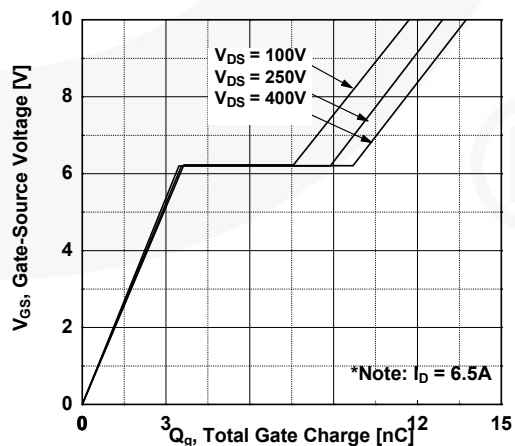
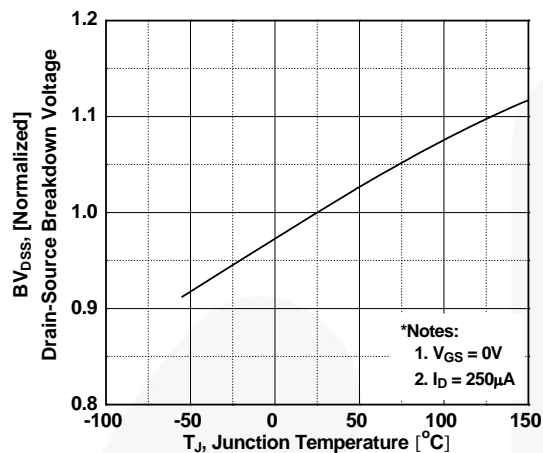


Figure 6. Gate Charge Characteristics

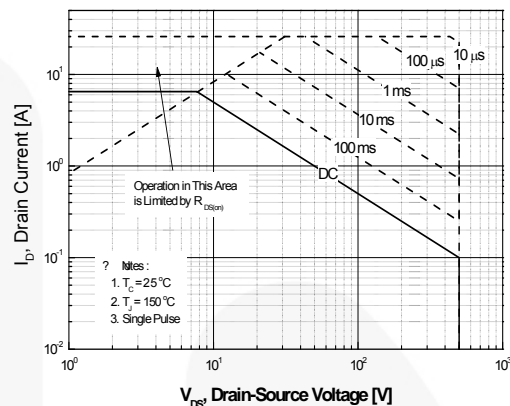


# Typical Performance Characteristics (Continued)

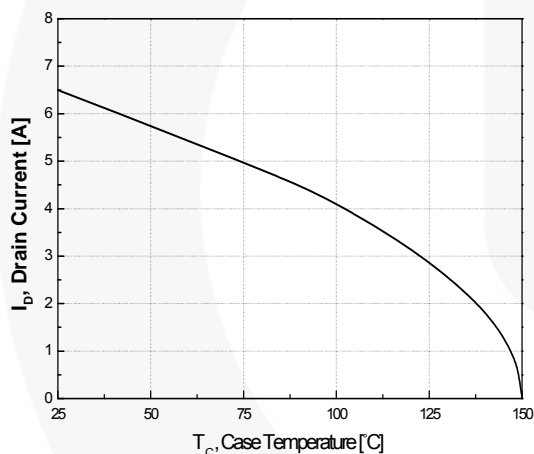
**Figure 7. Breakdown Voltage Variation vs. Temperature**



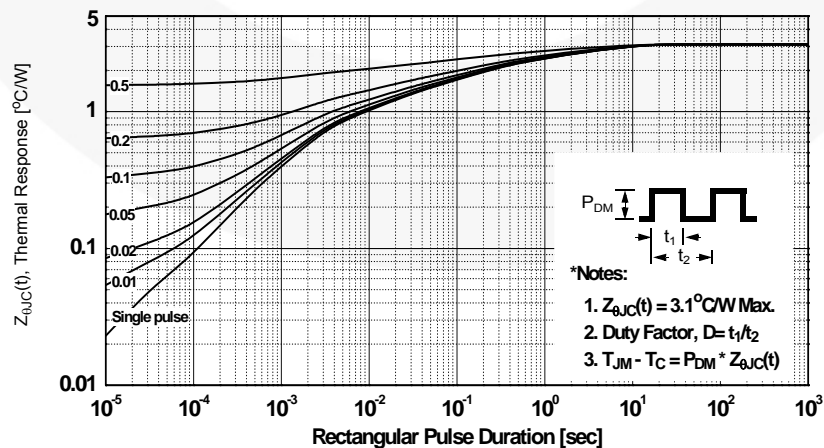
**Figure 8. Maximum Safe Operating Area**

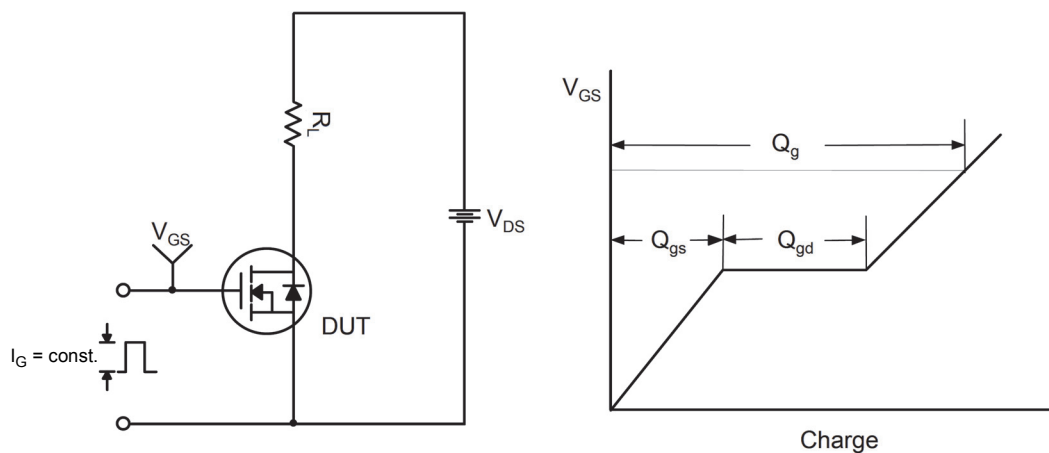


**Figure 9. Maximum Drain Current vs. Case Temperature**

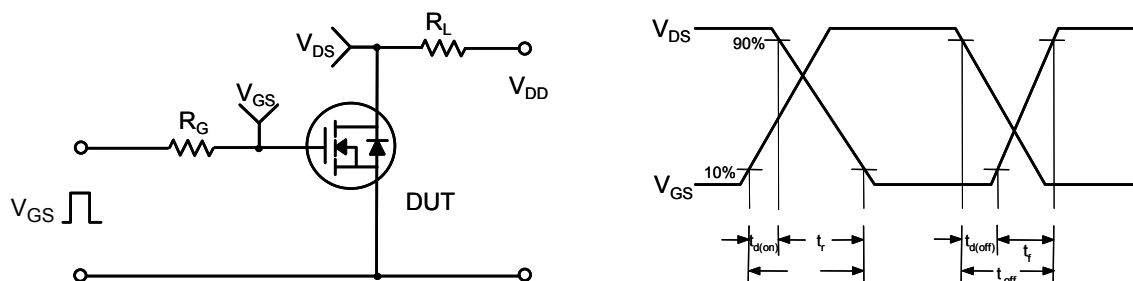


**Figure 10. Transient Thermal Response Curve**

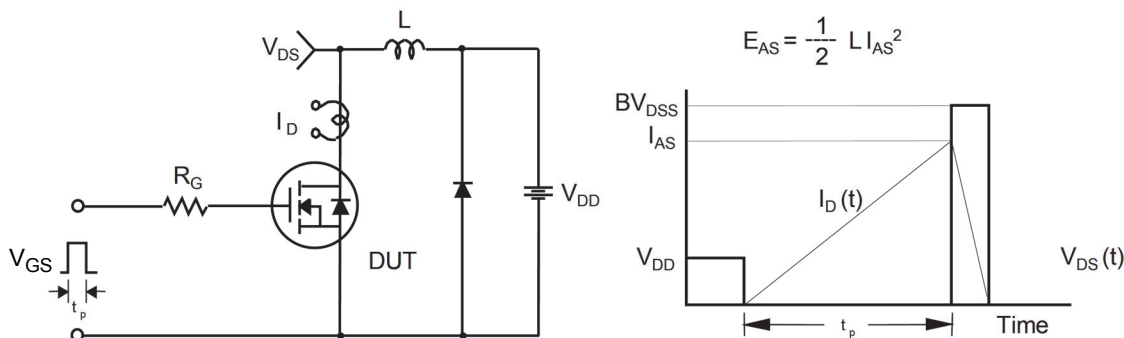




**Figure 11. Gate Charge Test Circuit & Waveform**



**Figure 12. Resistive Switching Test Circuit & Waveforms**



**Figure 13. Unclamped Inductive Switching Test Circuit & Waveforms**

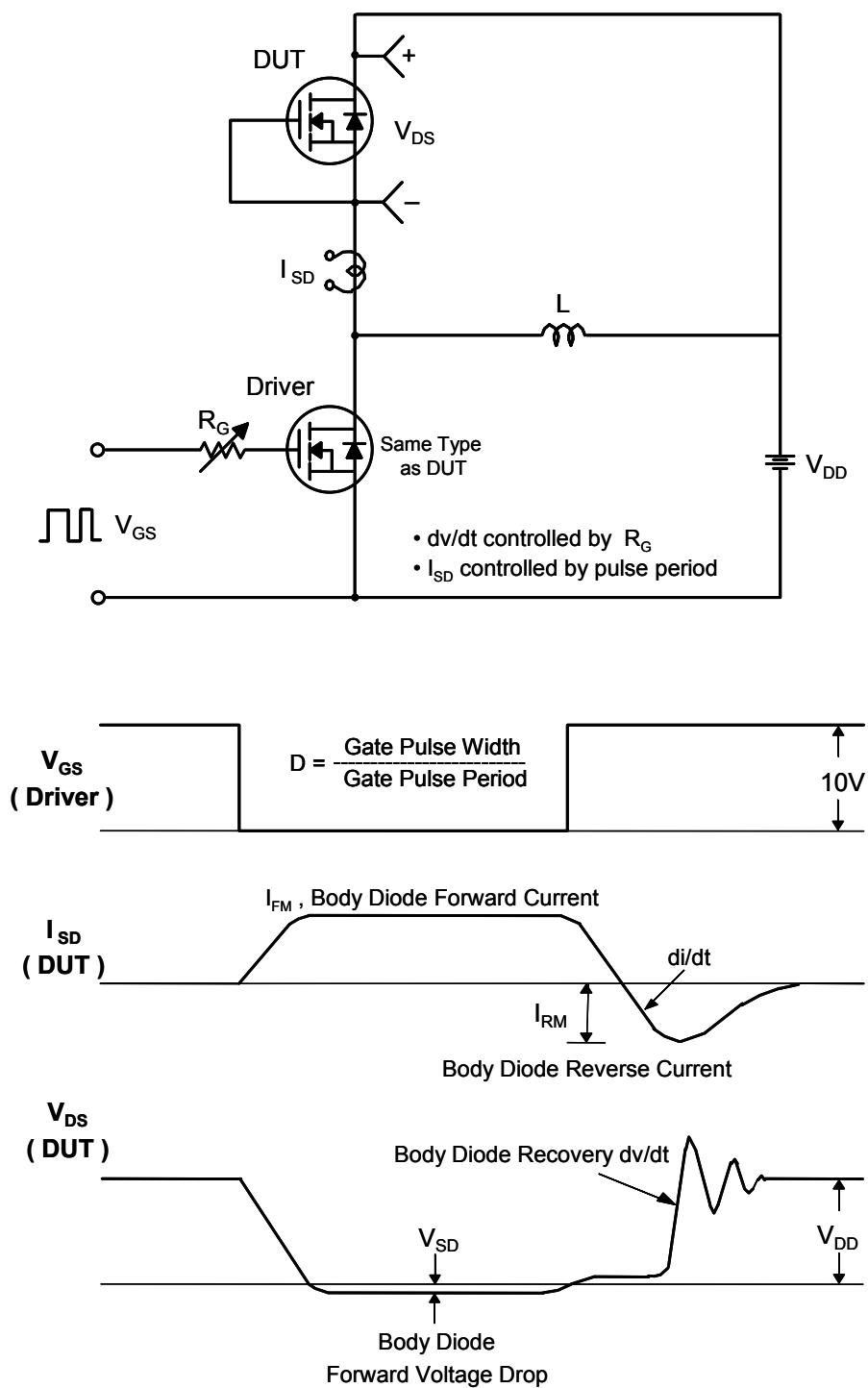




Figure 14. Peak Diode Recovery  $dv/dt$  Test Circuit & Waveforms





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