Introduction

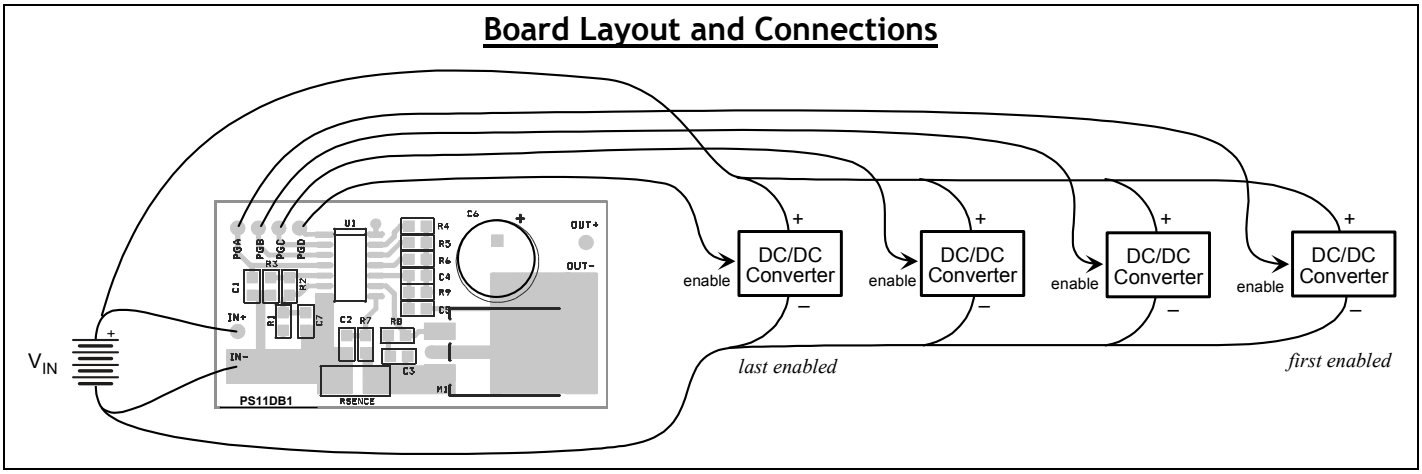
The Supertex PS11DB1 demo board contains all circuitry necessary to demonstrate the features of the PS11 power sequencing controller. Four sequenced power-good signals are provided, with timing controlled via three external resistors.

The board may be modified to meet custom requirements. Instructions are provided on the next page for modifications.

Specifications

Input Voltage	10V to 90V
Undervoltage Trip	35.0V on, 32.2V off
Overvoltage Trip	64.5V on, 70.0V off
Power Good Signals	Active Low
PWRGD A	~12ms after tripping UVon
PWRGD B	~200ms after 'A'
PWRGD C	~100ms after 'B'
PWRGD D	~5ms after 'C'

Board Layout and Connections



V_{IN}

Connect the supply voltage to these terminals. Supply voltage may range from 10 volts to 90 volts.

A high source impedance may cause oscillations when the input voltage is near the undervoltage trip point. A high source impedance results in a large voltage drop when loaded, causing undervoltage lockout to kick in, deactivating the PWRGD outputs. With the load removed, input voltage rises, causing undervoltage to release and activating the PWRGD outputs. The cycle repeats, resulting in oscillations. Source impedance must be less than the following to avoid oscillations:

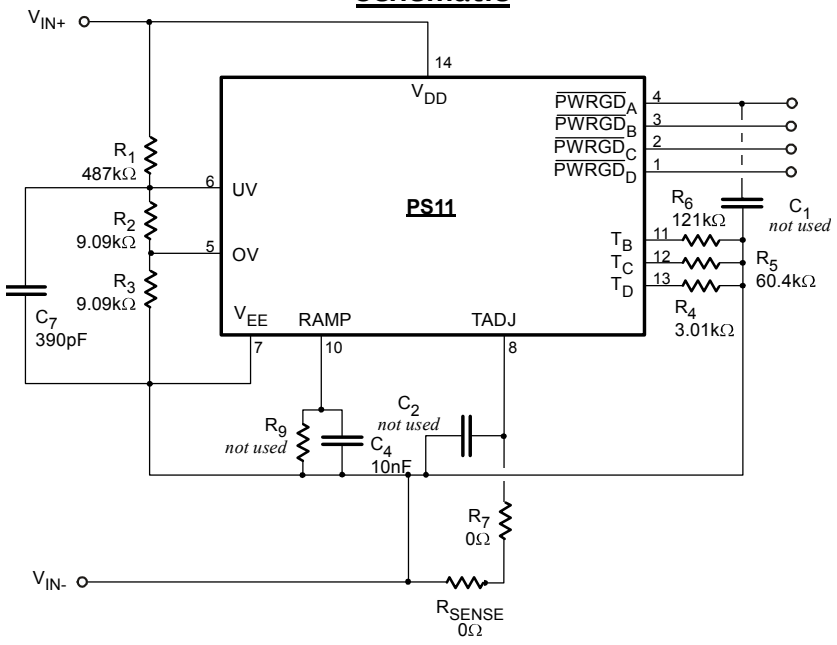
$$R_{SOURCE} < \frac{3V}{I_{LOAD}}$$

PWRGD

Connect to the power supply's ENABLE inputs. Depending on the power supply, it may be necessary to level-translate this signal via opto-isolator or discrete circuit. Refer to the PS10/PS11 datasheet for a description of PWRGD and related application circuits.

PWRGD is an open-drain output. During start-up and whenever V_{IN} is lower than the undervoltage trip point or greater than the overvoltage trip point, PWRGD is in a high impedance state. Once V_{IN} is within the proper range, PWRGD is pulled down to V_{IN-}.

Schematic



Timing

Timing capacitor C_4 determines start-up delay. Changing this capacitor will alter the timing. Refer to the PS10/PS11 datasheet for the equations that relate this timing to the values.

Resistors R_4, R_5, and R_6 set the delays for PWRGDs B, C, and D according to the following equation:

$$t_D = 1.67\mu\text{F} \cdot R_X$$

Undervoltage/Overvoltage Lockout

Resistors R_1, R_2, and R_3 set the undervoltage and overvoltage trip points. New trip points may be programmed by changing the values of these resistors. Refer to the PS10/PS11 datasheet for more information.

Additional Components

If the PWRGD A signal is used and experiences large voltage swings, a 10nF capacitor should be installed at C_1. This limits dV/dt which may otherwise cause undesirable coupling to internal circuits.

PS11DB1 - BOM

Item	Reference	Part	Part Number	Manufacturer
1	C1	Not used		
2	C2	Not used		
3	C3	Not used		
4	C4	10 nF, 50V, 10%		Kemet or equivalent
5	C5	Not used		
6	C6	Not used		
7	C7	390 pF		Kemet or equivalent
8	Q1	Not used		
9	R1	487k-ohm, 1%, 1/8W		Panasonic or equivalent
10	R2	9.09k-ohm, 1%, 1/8W		Panasonic or equivalent
11	R3	9.09k-ohm, 1%, 1/8W		Panasonic or equivalent
12	R4	3.01k-ohm,1%,1/8W		Panasonic or equivalent
13	R5	60.4k-ohm,1%,1/8W		Panasonic or equivalent
14	R6	121k-ohm,1%,1/8W		Panasonic or equivalent
15	R7	Zero Ohm Jumper		Panasonic or equivalent
16	R8	Not used		
17	R9	Not used		
18	R_{SENCE}	Zero Ohm		
19	U1	PS11NG		Supertex, Inc.

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PS11DB1