

74HC14-Q100; 74HCT14-Q100

Hex inverting Schmitt trigger

Rev. 4 — 19 April 2013

Product data sheet

1. General description

The 74HC14-Q100; 74HCT14-Q100 is a high-speed Si-gate CMOS device and is pin compatible with Low-power Schottky TTL (LSTTL). It is specified in compliance with JEDEC standard No. 7A.

The 74HC14-Q100; 74HCT14-Q100 provides six inverting buffers with Schmitt-trigger action. They are capable of transforming slowly changing input signals into sharply defined, jitter-free output signals.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
 - ◆ Specified from $-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$ and from $-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$
- Low-power dissipation
- ESD protection:
 - ◆ MIL-STD-883, method 3015 exceeds 2000 V
 - ◆ HBM JESD22-A114F exceeds 2000 V
 - ◆ MM JESD22-A115-A exceeds 200 V ($C = 200\text{ pF}$, $R = 0\text{ }\Omega$)
- Multiple package options

3. Applications

- Wave and pulse shapers
- Astable multivibrators
- Monostable multivibrators

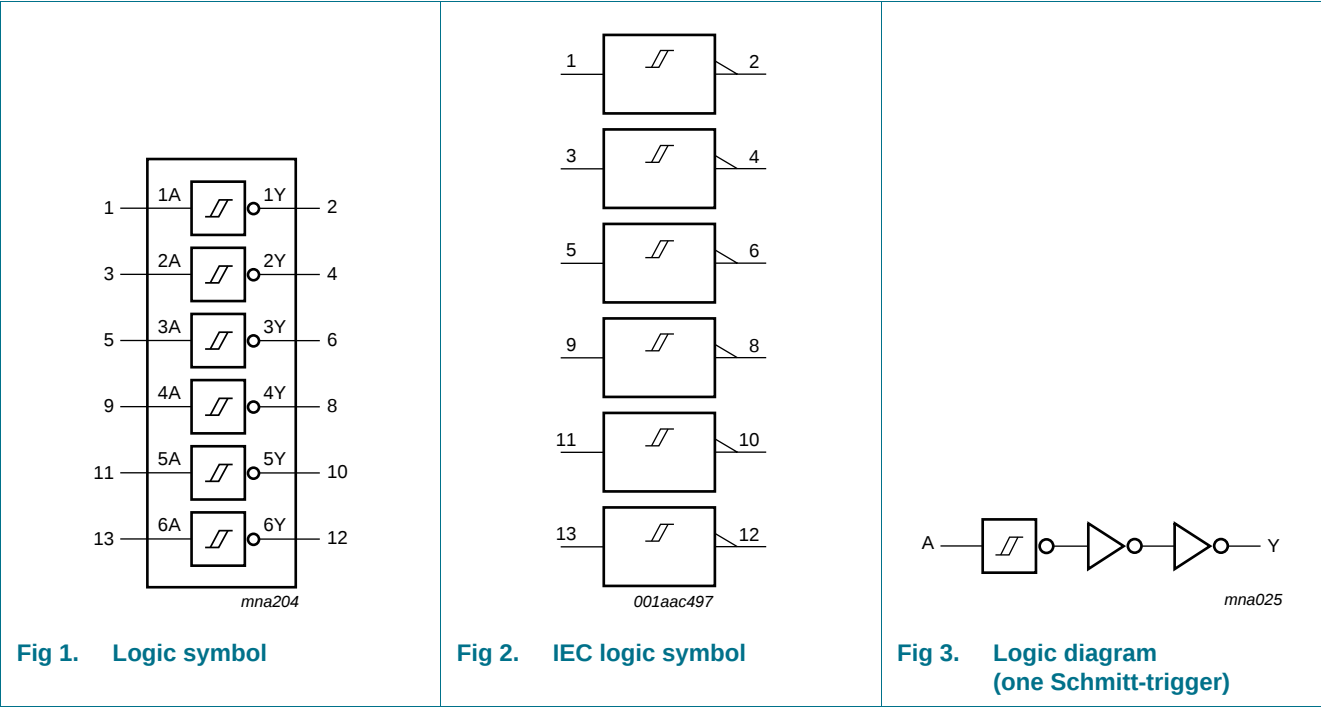


4. Ordering information

Table 1. Ordering information

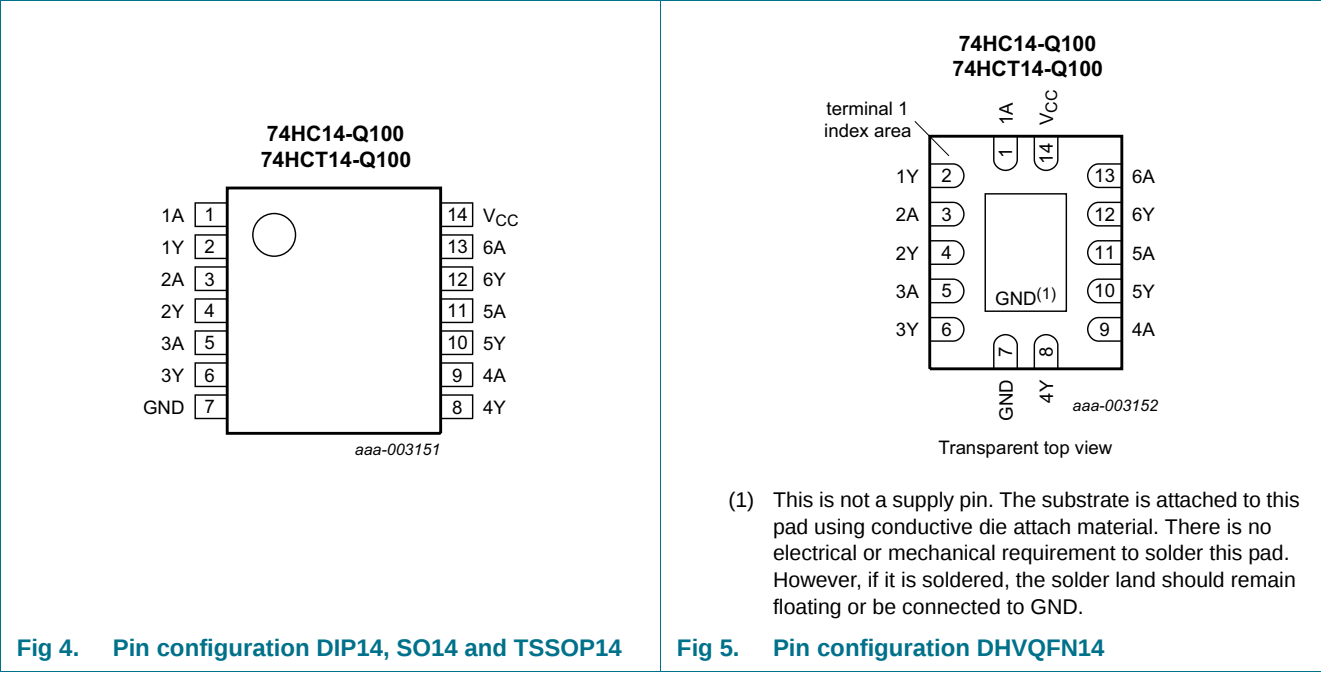
Type number	Package			
	Temperature range	Name	Description	Version
74HC14N-Q100	−40 °C to +125 °C	DIP14	plastic dual in-line package; 14 leads (300 mil)	SOT27-1
74HC14D-Q100	−40 °C to +125 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
74HCT14D-Q100				
74HC14PW-Q100	−40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1
74HCT14PW-Q100				
74HC14BQ-Q100	−40 °C to +125 °C	DHVQFN14	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 × 3 × 0.85 mm	SOT762-1
74HCT14BQ-Q100				

5. Functional diagram



6. Pinning information

6.1 Pinning



6.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
1A to 6A	1, 3, 5, 9, 11, 13	data input 1
1Y to 6Y	2, 4, 6, 8, 10, 12	data output 1
GND	7	ground (0 V)
V _{CC}	14	supply voltage

7. Functional description

Table 3. Function table^[1]

Input	Output
nA	nY
L	H
H	L

[1] H = HIGH voltage level;
L = LOW voltage level.

8. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+7	V
I_{IK}	input clamping current	$V_I < -0.5\text{ V}$ or $V_I > V_{CC} + 0.5\text{ V}$	[1] -	±20	mA
I_{OK}	output clamping current	$V_O < -0.5\text{ V}$ or $V_O > V_{CC} + 0.5\text{ V}$	[1] -	±20	mA
I_O	output current	$-0.5\text{ V} < V_O < V_{CC} + 0.5\text{ V}$	-	±25	mA
I_{CC}	supply current		-	50	mA
I_{GND}	ground current		-50	-	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation		[2]		
	DIP14 package		-	750	mW
	SO14, TSSOP14 and DHVQFN14 packages		-	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For DIP14 package: P_{tot} derates linearly with 12 mW/K above 70 °C.
 For SO14 package: P_{tot} derates linearly with 8 mW/K above 70 °C.
 For TSSOP14 packages: P_{tot} derates linearly with 5.5 mW/K above 60 °C.
 For DHVQFN14 packages: P_{tot} derates linearly with 4.5 mW/K above 60 °C.

9. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	74HC14-Q100			74HCT14-Q100			Unit
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
V_I	input voltage		0	-	V_{CC}	0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	0	-	V_{CC}	V
T_{amb}	ambient temperature		-40	+25	+125	-40	+25	+125	°C

10. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	T _{amb} = 25 °C			T _{amb} = –40 °C to +85 °C		T _{amb} = –40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC14-Q100										
V _{OH}	HIGH-level output voltage	V _I = V _{T+} or V _{T–}								
		I _O = –20 μA; V _{CC} = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I _O = –20 μA; V _{CC} = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I _O = –20 μA; V _{CC} = 6.0 V	5.9	6.0	-	5.9	-	5.9	-	V
		I _O = –4.0 mA; V _{CC} = 4.5 V	3.98	4.32	-	3.84	-	3.7	-	V
		I _O = –5.2 mA; V _{CC} = 6.0 V	5.48	5.81	-	5.34	-	5.2	-	V
V _{OL}	LOW-level output voltage	V _I = V _{T+} or V _{T–}								
		I _O = 20 μA; V _{CC} = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 20 μA; V _{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 20 μA; V _{CC} = 6.0 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 4.0 mA; V _{CC} = 4.5 V	-	0.15	0.26	-	0.33	-	0.4	V
		I _O = 5.2 mA; V _{CC} = 6.0 V	-	0.16	0.26	-	0.33	-	0.4	V
I _I	input leakage current	V _I = V _{CC} or GND; V _{CC} = 6.0 V	-	-	±0.1	-	±1.0	-	±1.0	μA
I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 6.0 V	-	-	2.0	-	20	-	40	μA
C _I	input capacitance		-	3.5	-	-	-	-	-	pF
74HCT14-Q100										
V _{OH}	HIGH-level output voltage	V _I = V _{T+} or V _{T–} ; V _{CC} = 4.5 V								
		I _O = –20 μA	4.4	4.5	-	4.4	-	4.4	-	V
		I _O = –4.0 mA	3.98	4.32	-	3.84	-	3.7	-	V
V _{OL}	LOW-level output voltage	V _I = V _{T+} or V _{T–} ; V _{CC} = 4.5 V								
		I _O = 20 μA;	-	0	0.1	-	0.1	-	0.1	V
		I _O = 4.0 mA;	-	0.15	0.26	-	0.33	-	0.4	V
I _I	input leakage current	V _I = V _{CC} or GND; V _{CC} = 5.5 V	-	-	±0.1	-	±1.0	-	±1.0	μA
I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 5.5 V	-	-	2.0	-	20	-	40	μA
ΔI _{CC}	additional supply current	per input pin; V _I = V _{CC} – 2.1 V; other pins at V _{CC} or GND; I _O = 0 A; V _{CC} = 4.5 V to 5.5 V	-	30	108	-	135	-	147	μA
C _I	input capacitance		-	3.5	-	-	-	-	-	pF

11. Dynamic characteristics

Table 7. Dynamic characteristics

$GND = 0\text{ V}$; $C_L = 50\text{ pF}$; for load circuit see [Figure 7](#).

Symbol	Parameter	Conditions	$T_{\text{amb}} = 25\text{ °C}$			$T_{\text{amb}} = -40\text{ °C to }+125\text{ °C}$		Unit
			Min	Typ	Max	Max (85 °C)	Max (125 °C)	

74HC14-Q100

t_{pd}	propagation delay	nA to nY; see Figure 6	[1]					
		$V_{\text{CC}} = 2.0\text{ V}$	-	41	125	155	190	ns
		$V_{\text{CC}} = 4.5\text{ V}$	-	15	25	31	38	ns
		$V_{\text{CC}} = 5.0\text{ V}$; $C_L = 15\text{ pF}$	-	12	-	-	-	ns
		$V_{\text{CC}} = 6.0\text{ V}$	-	12	21	26	32	ns
t_t	transition time	see Figure 6	[2]					
		$V_{\text{CC}} = 2.0\text{ V}$	-	19	75	95	110	ns
		$V_{\text{CC}} = 4.5\text{ V}$	-	7	15	19	22	ns
		$V_{\text{CC}} = 6.0\text{ V}$	-	6	13	15	19	ns
C_{PD}	power dissipation capacitance	per package; $V_I = GND$ to V_{CC}	[3]	-	7	-	-	pF

74HCT14-Q100

t_{pd}	propagation delay	nA to nY; see Figure 6	[1]					
		$V_{\text{CC}} = 4.5\text{ V}$	-	20	34	43	51	ns
		$V_{\text{CC}} = 5.0\text{ V}$; $C_L = 15\text{ pF}$	-	17	-	-	-	ns
t_t	transition time	$V_{\text{CC}} = 4.5\text{ V}$; see Figure 6	[2]	-	7	15	19	ns
C_{PD}	power dissipation capacitance	per package; $V_I = GND$ to $V_{\text{CC}} - 1.5\text{ V}$	[3]	-	8	-	-	pF

[1] t_{pd} is the same as t_{PHL} and t_{PLH} .

[2] t_t is the same as t_{THL} and t_{TLH} .

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

$$P_D = C_{\text{PD}} \times V_{\text{CC}}^2 \times f_i \times N + \sum (C_L \times V_{\text{CC}}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz;

f_o = output frequency in MHz;

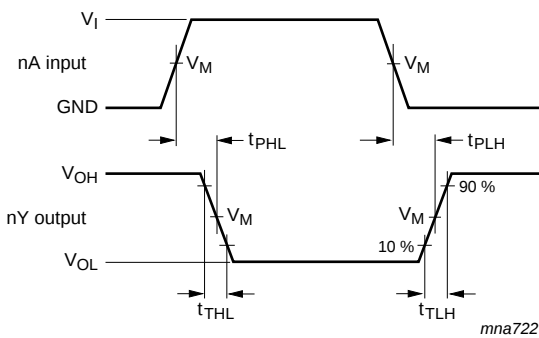
C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

$\sum (C_L \times V_{\text{CC}}^2 \times f_o)$ = sum of outputs.

12. Waveforms

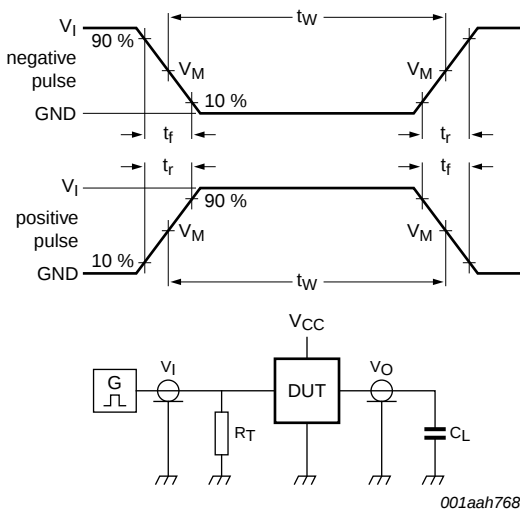


Measurement points are given in [Table 8](#).
 V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 6. Input to output propagation delays

Table 8. Measurement points

Type	Input	Output		
	V_M	V_M	V_X	V_Y
74HC14-Q100	$0.5V_{CC}$	$0.5V_{CC}$	$0.1V_{CC}$	$0.9V_{CC}$
74HCT14-Q100	1.3 V	1.3 V	$0.1V_{CC}$	$0.9V_{CC}$



Test data is given in [Table 9](#).
Definitions test circuit:
 R_T = termination resistance should be equal to output impedance Z_o of the pulse generator.
 C_L = load capacitance including jig and probe capacitance.

Fig 7. Test circuit for measuring switching times

Table 9. Test data

Type	Input		Load	Test
	V_I	t_r, t_f	C_L	
74HC14-Q100	V_{CC}	6.0 ns	15 pF, 50 pF	t_{PLH}, t_{PHL}
74HCT14-Q100	3.0 V	6.0 ns	15 pF, 50 pF	t_{PLH}, t_{PHL}

13. Transfer characteristics

Table 10. Transfer characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); see [Figure 8](#) and [Figure 9](#).

Symbol	Parameter	Conditions	T _{amb} = 25 °C			T _{amb} = −40 °C to +85 °C		T _{amb} = −40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC14-Q100										
V _{T+}	positive-going threshold voltage	V _{CC} = 2.0 V	0.7	1.18	1.5	0.7	1.5	0.7	1.5	V
		V _{CC} = 4.5 V	1.7	2.38	3.15	1.7	3.15	1.7	3.15	V
		V _{CC} = 6.0 V	2.1	3.14	4.2	2.1	4.2	2.1	4.2	V
V _{T−}	negative-going threshold voltage	V _{CC} = 2.0 V	0.3	0.52	0.9	0.3	0.9	0.3	0.9	V
		V _{CC} = 4.5 V	0.9	1.4	2.0	0.9	2.0	0.9	2.0	V
		V _{CC} = 6.0 V	1.2	1.89	2.6	1.2	2.6	1.2	2.6	V
V _H	hysteresis voltage	V _{CC} = 2.0 V	0.2	0.66	1.0	0.2	1.0	0.2	1.0	V
		V _{CC} = 4.5 V	0.4	0.98	1.4	0.4	1.4	0.4	1.4	V
		V _{CC} = 6.0 V	0.6	1.25	1.6	0.6	1.6	0.6	1.6	V
74HCT14-Q100										
V _{T+}	positive-going threshold voltage	V _{CC} = 4.5 V	1.2	1.41	1.9	1.2	1.9	1.2	1.9	V
		V _{CC} = 5.5 V	1.4	1.59	2.1	1.4	2.1	1.4	2.1	V
V _{T−}	negative-going threshold voltage	V _{CC} = 4.5 V	0.5	0.85	1.2	0.5	1.2	0.5	1.2	V
		V _{CC} = 5.5 V	0.6	0.99	1.4	0.6	1.4	0.6	1.4	V
V _H	hysteresis voltage	V _{CC} = 4.5 V	0.4	0.56	-	0.4	-	0.4	-	V
		V _{CC} = 5.5 V	0.4	0.6	-	0.4	-	0.4	-	V

14. Transfer characteristics waveforms

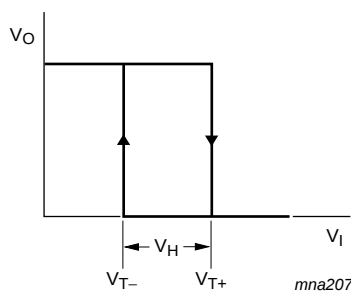


Fig 8. Transfer characteristics

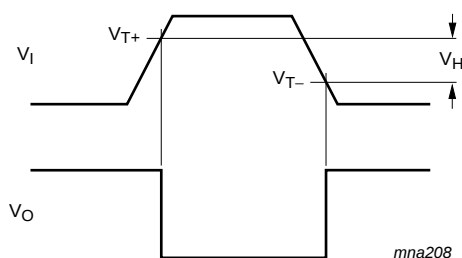


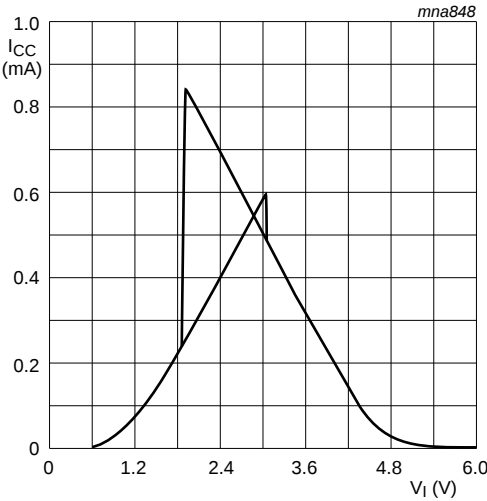
Fig 9. Transfer characteristics definitions



a. $V_{CC} = 2.0\text{ V}$



b. $V_{CC} = 4.5\text{ V}$



c. $V_{CC} = 6.0\text{ V}$

Fig 10. Typical 74HC transfer characteristics

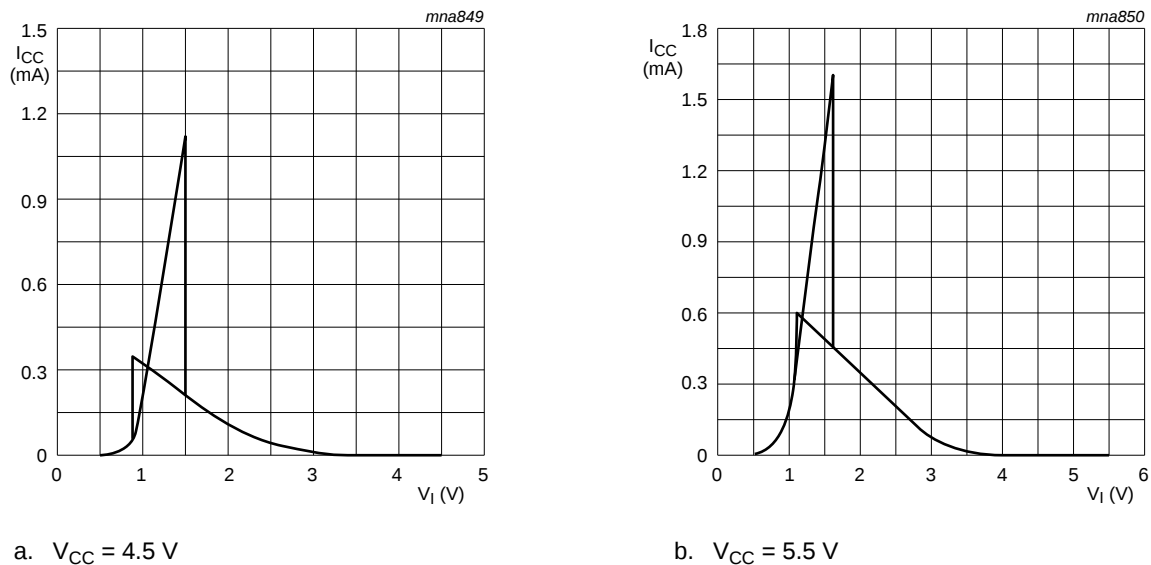


Fig 11. Typical 74HCT transfer characteristics

15. Application information

The slow input rise and fall times cause additional power dissipation, this can be calculated using the following formula:

$$P_{\text{add}} = f_i \times (t_r \times \Delta I_{CC(\text{AV})} + t_f \times \Delta I_{CC(\text{AV})}) \times V_{CC} \text{ where:}$$

P_{add} = additional power dissipation (μW);

f_i = input frequency (MHz);

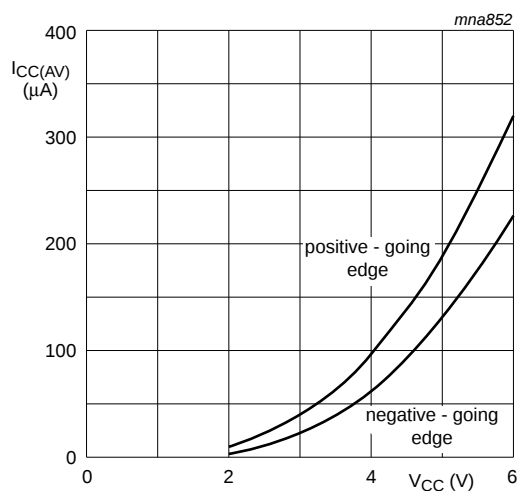
t_r = rise time (ns); 10 % to 90 %;

t_f = fall time (ns); 90 % to 10 %;

$\Delta I_{CC(\text{AV})}$ = average additional supply current (μA).

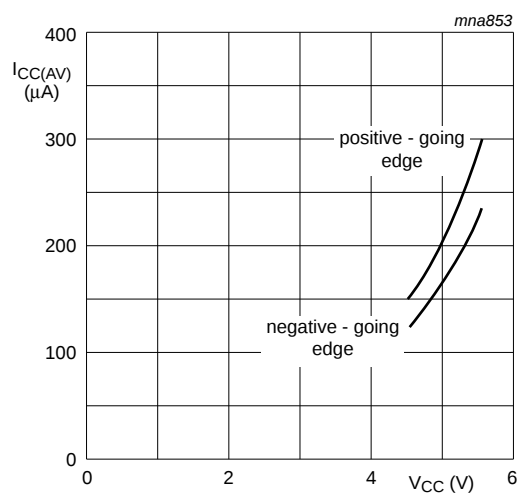
Average $\Delta I_{CC(\text{AV})}$ differs with positive or negative input transitions, as shown in [Figure 12](#) and [Figure 13](#).

An example of a relaxation circuit using the 74HC14-Q100; 74HCT14-Q100 is shown in [Figure 14](#).



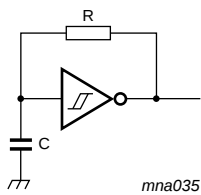
- (1) Positive-going edge.
- (2) Negative-going edge.

Fig 12. Average additional supply current as a function of V_{CC} for 74HC14-Q100; linear change of V_I between $0.1V_{CC}$ to $0.9V_{CC}$.



- (1) Positive-going edge.
- (2) Negative-going edge.

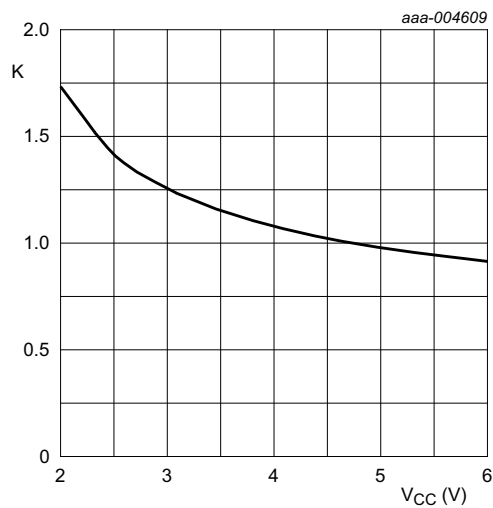
Fig 13. Average additional supply current as a function of V_{CC} for 74HCT14-Q100; linear change of V_I between $0.1V_{CC}$ to $0.9V_{CC}$.



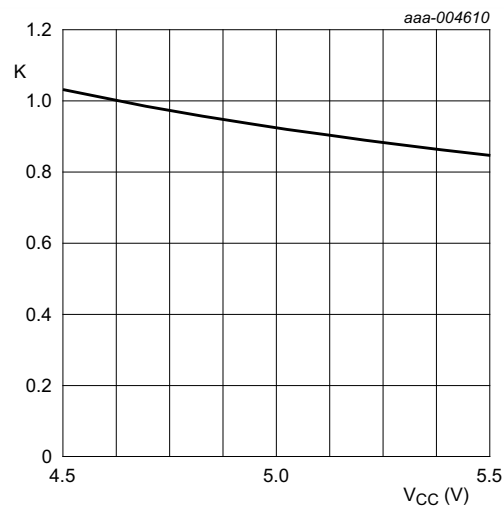
For 74HC14-Q100 and 74HCT14-Q100: $f = \frac{1}{T} \approx \frac{1}{K \times RC}$

For K-factor see [Figure 15](#)

Fig 14. Relaxation oscillator



K-factor for 74HC14-Q100



K-factor for 74HCT14-Q100

Fig 15. Typical K-factor for relaxation oscillator

16. Package outline

DIP14: plastic dual in-line package; 14 leads (300 mil)

SOT27-1

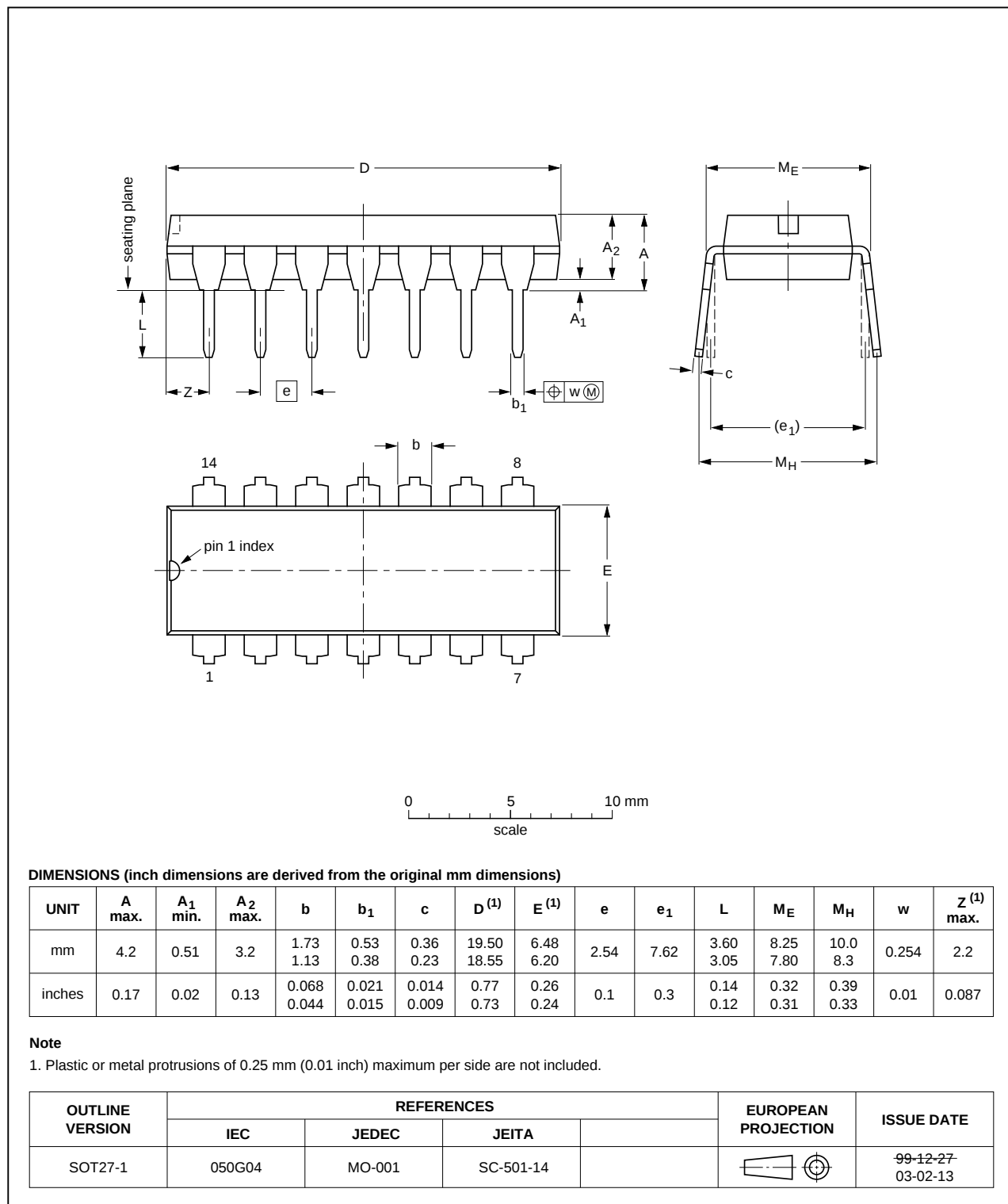


Fig 16. Package outline SOT27-1 (DIP14)

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1



Fig 17. Package outline SOT108-1 (SO14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1

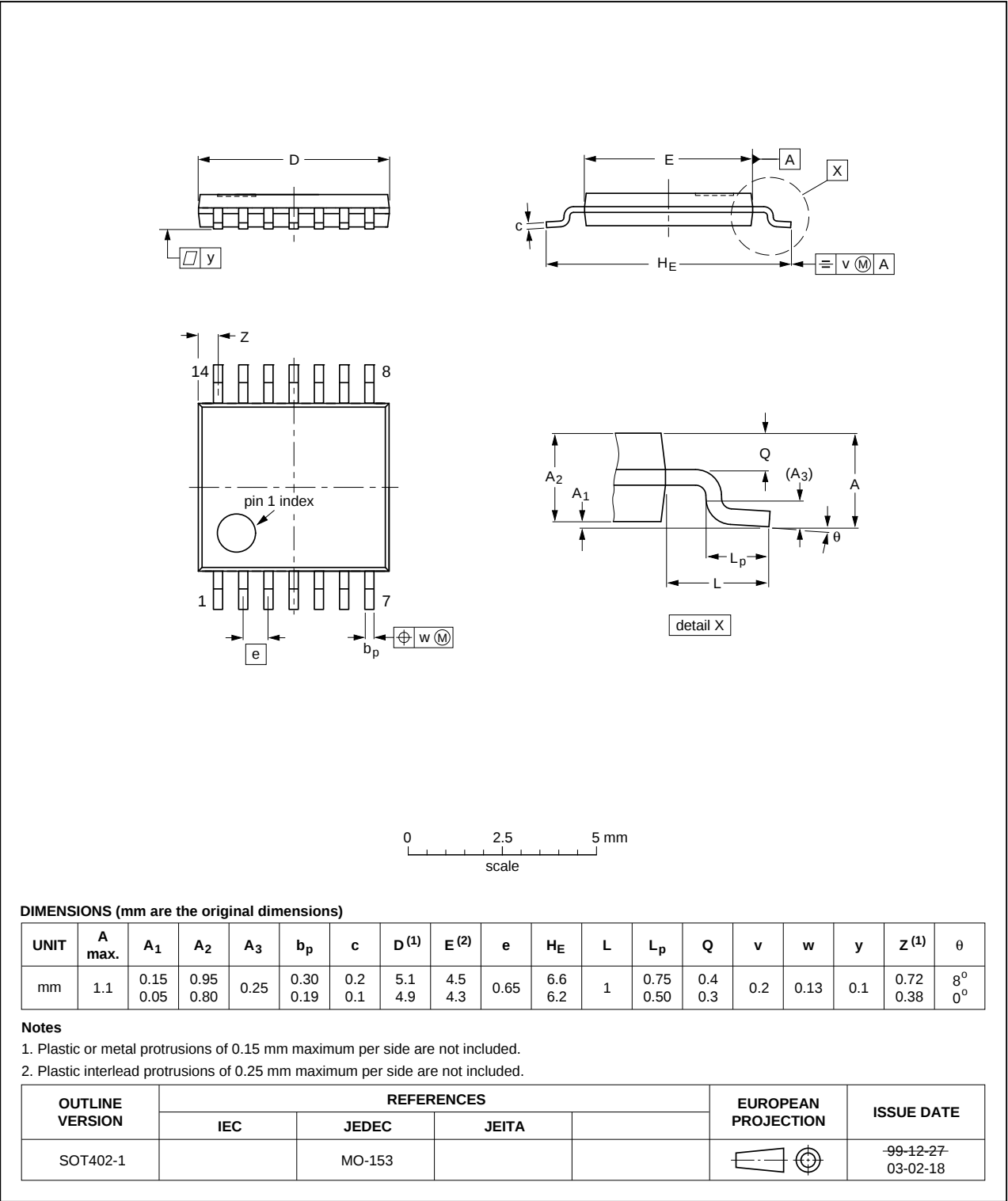


Fig 18. Package outline SOT402-1 (TSSOP14)

DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 x 3 x 0.85 mm

SOT762-1

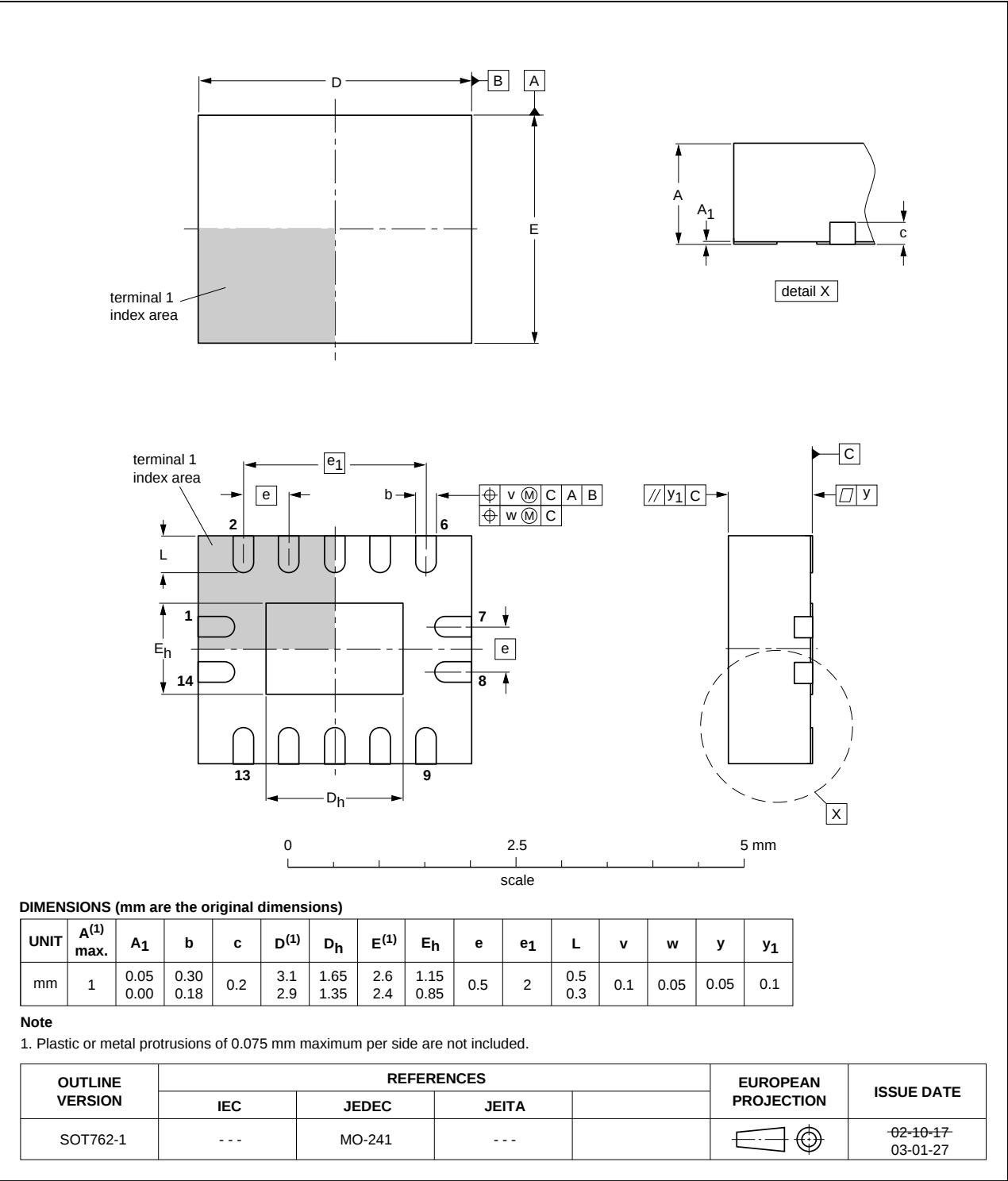


Fig 19. Package outline SOT762-1 (DHVQFN14)

17. Abbreviations

Table 11. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
LSTTL	Low-power Schottky Transistor-Transistor Logic
MM	Machine Model
MIL	Military

18. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT14_Q100 v.4	20130419	Product data sheet	-	74HC_HCT14_Q100 v.3
Modifications:	• 74HCT14N-Q100 removed.			
74HC_HCT14_Q100 v.3	20130410	Product data sheet	-	74HC_HCT14_Q100 v.2
Modifications:	• 74HC14N-Q100 and 74HCT14N-Q100 added.			
74HC_HCT14_Q100 v.2	20120810	Product data sheet	-	74HC_HCT14_Q100 v.1
Modifications:	• Figure 15 added (typical K-factor for relaxation oscillator).			
74HC_HCT14_Q100 v.1	20120709	Product data sheet	-	-

19. Legal information

19.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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21. Contents

1	General description	1
2	Features and benefits	1
3	Applications	1
4	Ordering information	2
5	Functional diagram	2
6	Pinning information	3
6.1	Pinning	3
6.2	Pin description	3
7	Functional description	3
8	Limiting values	4
9	Recommended operating conditions	4
10	Static characteristics	5
11	Dynamic characteristics	6
12	Waveforms	7
13	Transfer characteristics	8
14	Transfer characteristics waveforms	8
15	Application information	10
16	Package outline	13
17	Abbreviations	17
18	Revision history	17
19	Legal information	18
19.1	Data sheet status	18
19.2	Definitions	18
19.3	Disclaimers	18
19.4	Trademarks	19
20	Contact information	19
21	Contents	20

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Date of release: 19 April 2013

Document identifier: 74HC_HCT14_Q100