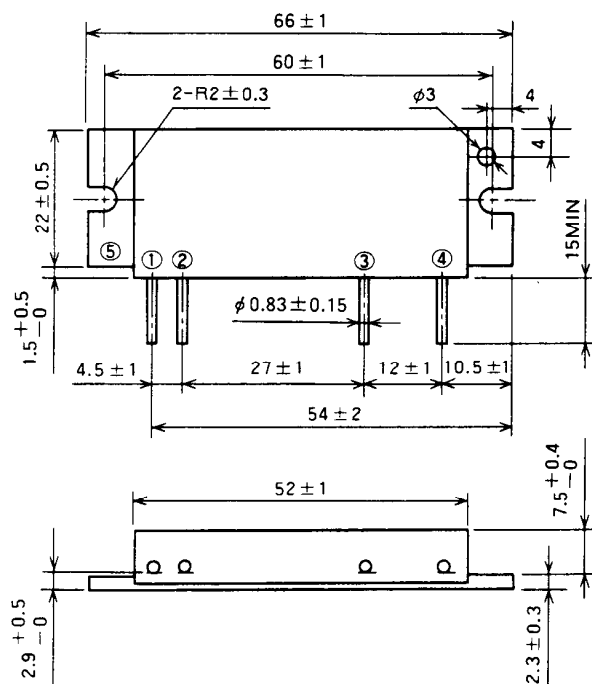


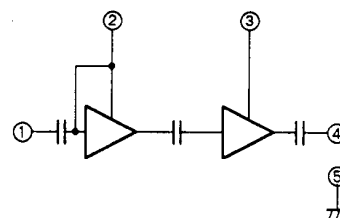
## OUTLINE DRAWING

Dimensions in mm



## H2

### BLOCK DIAGRAM



PIN :

- ①Pin : RF INPUT  
②Vcc1 : 1st. DC SUPPLY  
③Vcc2 : 2nd. DC SUPPLY  
④Po : RF OUTPUT  
⑤GND : FIN

**ABSOLUTE MAXIMUM RATINGS** (T<sub>C</sub> = 25 °C unless otherwise noted)

| Symbol               | Parameter                  | Conditions                             | Ratings     | Unit |
|----------------------|----------------------------|----------------------------------------|-------------|------|
| V <sub>CC</sub>      | Supply voltage             |                                        | 17          | V    |
| I <sub>CC</sub>      | Total current              |                                        | 14          | A    |
| P <sub>in(max)</sub> | Input power                | Z <sub>G</sub> = Z <sub>L</sub> = 50 Ω | 0.6         | W    |
| P <sub>O(max)</sub>  | Output power               | Z <sub>G</sub> = Z <sub>L</sub> = 50 Ω | 55          | W    |
| T <sub>C(OP)</sub>   | Operation case temperature |                                        | − 30 to 110 | °C   |
| T <sub>stg</sub>     | Storage temperature        |                                        | − 40 to 110 | °C   |

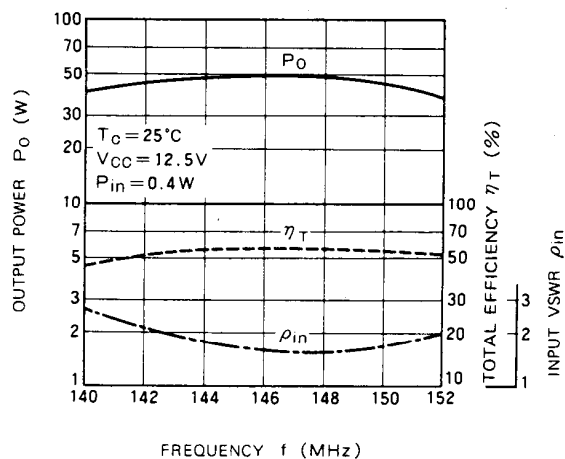
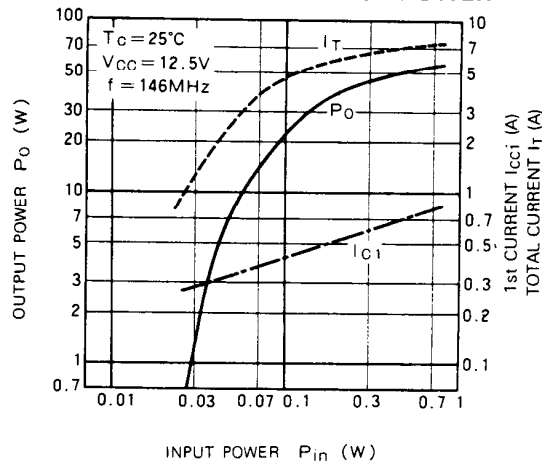
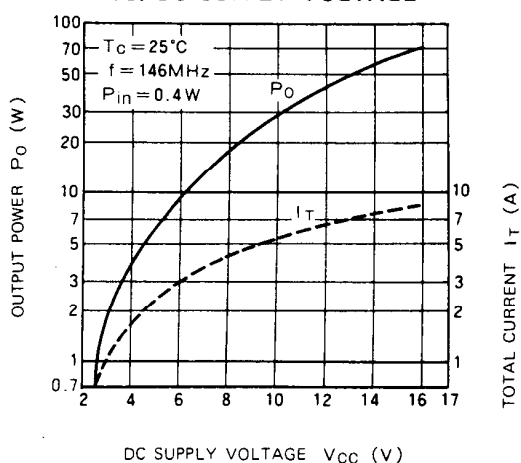
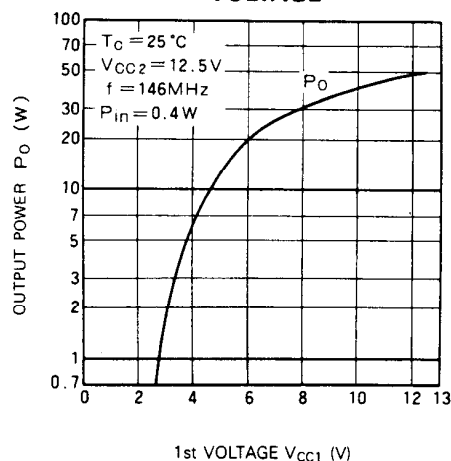
Note. Above parameters are guaranteed independently.

### ELECTRICAL CHARACTERISTICS (T<sub>c</sub> = 25 °C unless otherwise noted)

| Symbol      | Parameter           | Test conditions                                                                                                     | Limits                    |      | Unit |
|-------------|---------------------|---------------------------------------------------------------------------------------------------------------------|---------------------------|------|------|
|             |                     |                                                                                                                     | Min                       | Max  |      |
| f           | Frequency range     | $P_{in} = 0.3W$<br>$V_{CC} = 12.5V$<br>$Z_G = Z_L = 50 \Omega$                                                      | 144                       | 148  | MHz  |
| $P_o$       | Output power        |                                                                                                                     | 43                        |      | W    |
| $\eta_T$    | Total efficiency    |                                                                                                                     | 50                        |      | %    |
| 2fo         | 2nd. harmonic       |                                                                                                                     |                           | - 35 | dBc  |
| 3fo         | 3rd. harmonic       |                                                                                                                     |                           | - 45 | dBc  |
| $\rho_{in}$ | Input VSWR          |                                                                                                                     |                           | 2.8  | -    |
| -           | Load VSWR tolerance | $V_{CC} = 15.2V$ ,<br>$P_o = 45W$ ( $P_{in}$ : controlled)<br>Load VSWR=20:1 (All phase), 5sec.<br>$Z_G = 50\Omega$ | No degradation or destroy |      | -    |

Note. Above parameters, ratings, limits and conditions are subject to change.

## TYPICAL PERFORMANCE DATA

OUTPUT POWER, TOTAL EFFICIENCY,  
INPUT VSWR VS. FREQUENCYOUTPUT POWER, 1st CURRENT  
TOTAL CURRENT VS. INPUT POWEROUTPUT POWER, TOTAL CURRENT  
VS. DC SUPPLY VOLTAGEOUTPUT POWER VS. 1st  
VOLTAGE

## DESIGN CONSIDERATION OF HEAT RADIATION.

Please refer to following consideration when designing heat sink.

### 1. Junction temperature of incorporated transistors at standard operation.

- (1) Thermal resistance between junction and package of incorporated transistors.

a) First stage transistor

$$R_{th(j-c)1} = 4.3^{\circ}\text{C/W (Typ.)}$$

b) Final stage transistor

$$R_{th(j-c)2} = 1.5^{\circ}\text{C/W (Typ.)}$$

- (2) Junction temperature of incorporated transistors at standard operation.

- Conditions for standard operation.

$P_O = 43\text{W}$ ,  $V_{CC} = 12.5\text{V}$ ,  $P_{in} = 0.4\text{W}$ ,  $\eta_T = 50\%$  (minimum rating),  $P_{O1}$  (Note 1) =  $9.4\text{W}$ ,  $I_T = 6.88\text{A}$  ( $I_{T1}$  (2) =  $1.25\text{A}$ ,  $I_{T2}$  (3) =  $5.63\text{A}$ )

Note 1: Output power of the first stage transistor

Note 2: Circuit current of the first stage transistor

Note 3: Circuit current of the final stage transistor

- Junction temperature of the first stage transistor

$$\begin{aligned} T_{j1} &= (V_{CC} \times I_{T1} - P_{O1} + P_{in}) \times R_{th(j-c)1} + T_c^{(4)} \\ &= (12.5 \times 1.25 - 9.4 + 0.4) \times 4.3 + T_c \\ &= 28.5 + T_c (^{\circ}\text{C}) \end{aligned}$$

Note 4: Package temperature of device

- Junction temperature of the final stage transistor

$$\begin{aligned} T_{j2} &= (V_{CC} \times I_{T2} - P_O + P_{O1}) \times R_{th(j-c)2} + T_c \\ &= (12.5 \times 5.63 - 43 + 9.4) \times 1.5 + T_c \\ &= 55.2 + T_c (^{\circ}\text{C}) \end{aligned}$$

### 2. Heat sink design

In thermal design of heat sink, try to keep the package temperature at the upper limit of the operating ambient temperature (normally  $T_a = 60^{\circ}\text{C}$ ) and at the output power of 43W below  $90^{\circ}\text{C}$ .

The thermal resistance  $R_{th(c-a)}$  (5) of the heat sink to realize this:

$$\begin{aligned} R_{th(c-a)} &= \frac{T_c - T_a}{(P_O/\eta_T) - P_O + P_{in}} = \frac{90 - 60}{(43/0.5) - 43 + 0.4} \\ &= 0.69 (^{\circ}\text{C/W}) \end{aligned}$$

Note 5: Inclusive of the contact thermal resistance between device and heat sink

Mounting the heat sink of the above thermal resistance on the device,

$$T_{j1} = 118.5^{\circ}\text{C}, T_{j2} = 145.2^{\circ}\text{C} \text{ at } T_a = 60^{\circ}\text{C}, T_c = 90^{\circ}\text{C}.$$

In the annual average of ambient temperature is  $30^{\circ}\text{C}$ ,

$$T_{j1} = 88.5^{\circ}\text{C}, T_{j2} = 115.2^{\circ}\text{C}$$

As the maximum junction temperature of these incorporated transistors  $T_{jmax}$  are  $175^{\circ}\text{C}$ , application under fully derated condition is ensured.