

CURRENT MODE PWM CONTROLLER

FEATURES

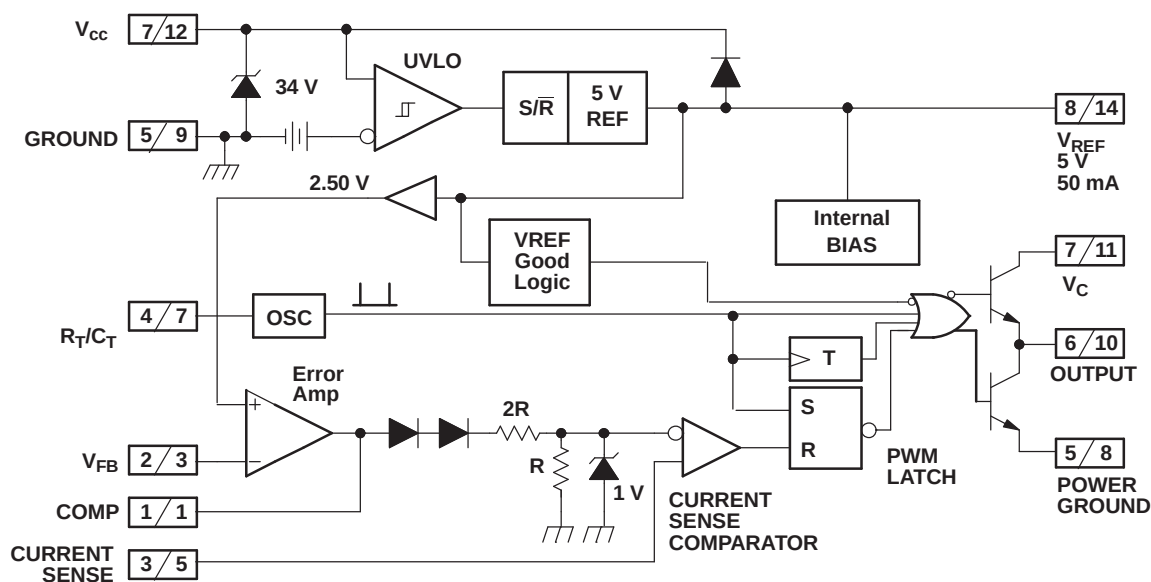
- Optimized For Off-line and DC-to-DC Converters
- Low Start-Up Current (<1 mA)
- Automatic Feed Forward Compensation
- Pulse-by-Pulse Current Limiting
- Enhanced Load Response Characteristics
- Under-Voltage Lockout With Hysteresis
- Double Pulse Suppression
- High Current Totem Pole Output
- Internally Trimmed Bandgap Reference
- 500-kHz Operation
- Low R_O Error Amp

DESCRIPTION

The UC1842/3/4/5 family of control devices provides the necessary features to implement off-line or dc-to-dc fixed frequency current mode control schemes with a minimal external parts count. Internally implemented circuits include under-voltage lockout featuring start up current less than 1 mA, a precision reference trimmed for accuracy at the error amp input, logic to insure latched operation, a PWM comparator which also provides current limit control, and a totem pole output stage designed to source or sink high peak current. The output stage, suitable for driving N-Channel MOSFETs, is low in the off state.

Differences between members of this family are the under-voltage lockout thresholds and maximum duty cycle ranges. The UC1842 and UC1844 have UVLO thresholds of 16 V_{ON} and 10 V_{OFF} , ideally suited to off-line applications. The corresponding thresholds for the UC1843 and UC1845 are 8.4 V and 7.6 V. The UC1842 and UC1843 can operate to duty cycles approaching 100%. A range of zero to 50% is obtained by the UC1844 and UC1845 by the addition of an internal toggle flip flop which blanks the output off every other clock cycle.

BLOCK DIAGRAM



Note 1: **A/B** A = DIL-8 Pin Number. B = SO-14 and CFP-14 Pin Number.

Note 2: Toggle flip flop used only in 1844 and 1845.



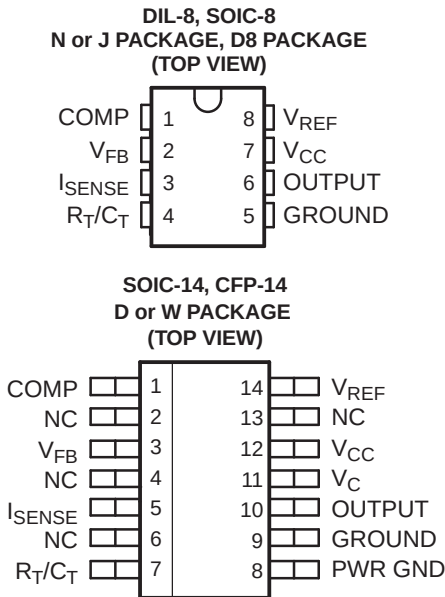
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

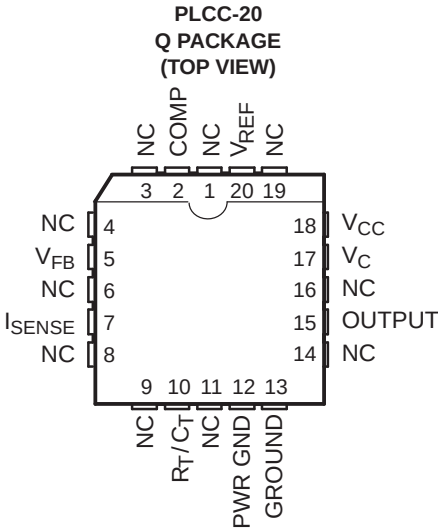
		UNIT
Supply voltage	Low impedance source	30 V
	$I_{CC} < 30\text{ mA}$	Self Limiting
Output current		$\pm 1\text{ A}$
Output energy (capacitive load)		5 μJ
Analog inputs (Pins 2, 3)		–0.3 V to 6.3 V
Error amp output sink current		10 mA
Power dissipation	$T_A \leq 25^\circ\text{C}$ (DIL-8)	1 W
	$T_A \leq 25^\circ\text{C}$ (SOIC-14)	725 mW
	$T_A \leq 25^\circ\text{C}$ (SOIC-8)	650 mW
Storage temperature range		–65°C to 150°C
Junction temperature range		–55°C to 150°C
Lead temperature (soldering, 10 seconds)		300°C

(1) All voltages are with respect to Pin 5. All currents are positive into the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

CONNECTION DIAGRAMS



NC – No internal connection



THERMAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PACKAGE		θ_{JC}	θ_{JA}
DIL-8	J	28 ⁽¹⁾	125-160
	N	25	110 ⁽²⁾
SOIC-8	D8	42	84-160 ⁽²⁾
SOIC-14	D14	35	50-120 ⁽²⁾
CFP-14	W	5.49°C/W	175.4C/W
PLCC-20	Q	34	43-75 ⁽²⁾

(1) θ_{JC} data values stated were derived from MIL-STD-1835B.

(2) Specified θ_{JA} (junction to ambient) is for devices mounted to 5 in² FR4 PC board with one ounce copper where noted. When resistance range is given, lower values are for 5 in². Test PWB was 0.062 in thick and typically used 0.635-mm trace widths for power packages and 1.3-mm trace widths for non-power packages with 100 x 100-mil probe land area at the end of each trace.

DISSIPATION RATINGS

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A \leq 25^\circ\text{C}$	$T_A \leq 70^\circ\text{C}$ POWER RATING	$T_A \leq 85^\circ\text{C}$ CPO WER RATING	$T_A \leq 125^\circ\text{C}$ POWER RATING
W	700 mW	5.5 mW/°C	452 mW	370 mW	150 mW

ELECTRICAL CHARACTERISTICS

Unless otherwise stated, these specifications apply for $-55^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$ for the UC184X; $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$ for the UC284X; $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$ for the 384X; $V_{CC} = 15\text{ V}^{(1)}$; $R_T = 10\text{ k}\Omega$; $C_T = 3.3\text{ nF}$, $T_A = T_J$.

PARAMETER	TEST CONDITIONS	UC1842/3/4/5 UC2842/3/4/5			UC3842/3/4/5			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
REFERENCE SECTION								
Output Voltage	T _J = 25°C, I _O = 1 mA	4.95	5.00	5.05	4.90	5.00	5.10	V
Line Regulation	12 ≤ V _{IN} ≤ 25 V		6	20		6	20	mV
Load Regulation	1 ≤ I _O ≤ 20 mA		6	25		6	25	
Temp. Stability	See ⁽²⁾⁽³⁾		0.2	0.4		0.2	0.4	mV/°C
Total Output Variation	Line, load, tempature ⁽²⁾	4.9		5.1	4.82		5.18	V
Output Noise Voltage	10 Hz ≤ f ≤ 10 kHz, T _J = 25°C ⁽²⁾		50			50		μV
Long Term Stability	T _A = 125°C, 1000 Hrs ⁽²⁾		5	25		5	25	mV
Output Short Circuit		−30	−100	−180	−30	−100	−180	mA
OSCILLATOR SECTION								
Initial Accuracy	T _J = 25°C ⁽⁴⁾	47	52	57	47	52	57	kHz
Voltage Stability	12 ≤ V _{CC} ≤ 25 V		0.2%	1%		0.2%	1%	
Temp. Stability	T _{MIN} ≤ T _A ≤ T _{MAX} ⁽²⁾		5%			5%		
Amplitude	V _{PIN} 4 peak-to-peak ⁽²⁾		1.7			1.7		V

(1) Adjust V_{CC} above the start threshold before setting at 15 V.

(2) These parameters, although specified, are not 100% tested in production.

(3) Temperature stability, sometimes referred to as average temperature coefficient, is described by the equation:

$$\text{Temp Stability} = \frac{V_{REF(max)} - V_{REF(min)}}{T_J(max) - T_J(min)}$$

$V_{REF(max)}$ and $V_{REF(min)}$ are the maximum and minimum reference voltages measured over the appropriate temperature range. Note that the extremes in voltage do not necessarily occur at the extremes in temperature.

(4) Output frequency equals oscillator frequency for the UC1842 and UC1843.

Output frequency is one half oscillator frequency for the UC1844 and UC1845.

ELECTRICAL CHARACTERISTICS (continued)

Unless otherwise stated, these specifications apply for $-55^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$ for the UC184X; $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ for the UC284X; $0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$ for the 384X; $V_{CC} = 15\text{ V}$; $R_T = 10\text{ k}\Omega$; $C_T = 3.3\text{ nF}$; $T_A = T_J$.

PARAMETER	TEST CONDITIONS	UC1842/3/4/5 UC2842/3/4/5			UC3842/3/4/5			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
ERROR AMP SECTION								
Input Voltage	V _{PIN 1} = 2.5 V	2.45	2.50	2.55	2.42	2.50	2.58	V
Input Bias Current			−0.3	−1		−0.3	−2	μA
A _{VOL}	2 ≤ V _O ≤ 4 V	65	90		65	90		dB
Unity Gain Bandwidth	T _J = 25°C ⁽⁵⁾	0.7	1		0.7	1		MHz
PSRR	12 ≤ V _{CC} ≤ 25 V	60	70		60	70		dB
Output Sink Current	V _{PIN 2} = 2.7 V, V _{PIN 1} = 1.1 V	2	6		2	6		mA
Output Source Current	V _{PIN 2} = 2.3 V, V _{PIN 1} = 5 V	−0.5	−0.8		−0.5	−0.8		
V _{OUT} High	V _{PIN 2} = 2.3 V, R _L = 15 kΩ to ground	5	6		5	6		V
V _{OUT} Low	V _{PIN 2} = 2.7 V, R _L = 15 kΩ to Pin 8		0.7	1.1		0.7	1.1	
CURRENT SENSE SECTION								
Gain	See ⁽⁶⁾⁽⁷⁾	2.85	3	3.15	2.85	3	3.15	V/V
Maximum Input Signal	V _{PIN 1} = 5 V ⁽⁶⁾	0.9	1	1.1	0.9	1	1.1	V
PSRR	12 ≤ V _{CC} ≤ 25 V ⁽⁵⁾⁽⁶⁾		70			70		dB
Input Bias Current			−2	−10		−2	−10	μA
Delay to Output	V _{PIN 3} = 0 V to 2 V ⁽⁵⁾		150	300		150	300	ns
OUTPUT SECTION								
Output Low Level	I _{SINK} = 20 mA		0.1	0.4		0.1	0.4	V
	I _{SINK} = 200 mA		1.5	2.2		1.5	2.2	
Output High Level	I _{SOURCE} = 20 mA	13	13.5		13	13.5		
	I _{SOURCE} = 200 mA	12	13.5		12	13.5		
Rise Time	T _J = 25°C, C _L = 1 nF ⁽⁵⁾		50	150		50	150	ns
Fall Time	T _J = 25°C, C _L = 1nF ⁽⁵⁾		50	150		50	150	
UNDER-VOLTAGE LOCKOUT SECTION								
Start Threshold	X842/4	15	16	17	14.5	16	17.5	V
	X843/5	7.8	8.4	9.0	7.8	8.4	9.0	
Min. Operating Voltage After Turn On	X842/4	9	10	11	8.5	10	11.5	
	X843/5	7.0	7.6	8.2	7.0	7.6	8.2	
PWM SECTION								
Maximum Duty Cycle	X842/3	95%	97%	100%	95%	97%	100%	
	X844/5	46%	48%	50%	47%	48%	50%	
Minimum Duty Cycle				0%			0%	
TOTAL STANDBY CURRENT								
Start-Up Current			0.5	1		0.5	1	mA
Operating Supply Current	V _{PIN 2} = V _{PIN 3} = 0 V		11	17		11	17	
V _{CC} Zener Voltager	I _{CC} = 25 mA	30	34		30	34		V

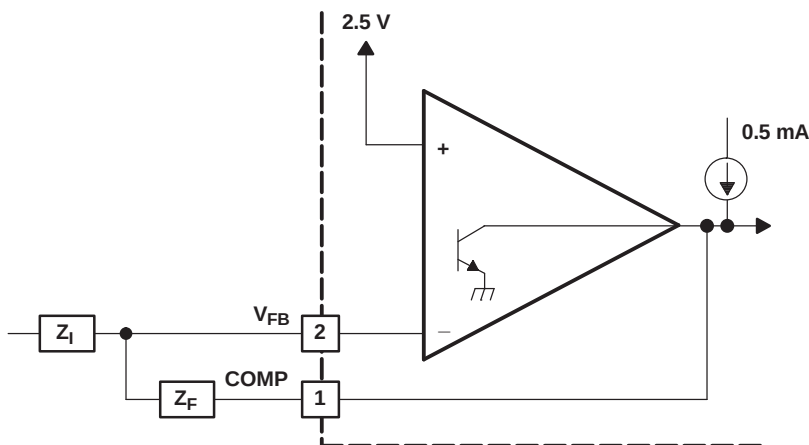
(5) These parameters, although specified, are not 100% tested in production.

(6) Parameter measured at trip point of latch with $V_{PIN\ 2} = 0$.

(7) Gain defined as: $A = \frac{\Delta V_{PIN\ 1}}{\Delta V_{PIN\ 3}}$, $0 \leq V_{PIN\ 3} \leq 0.8\text{ V}$

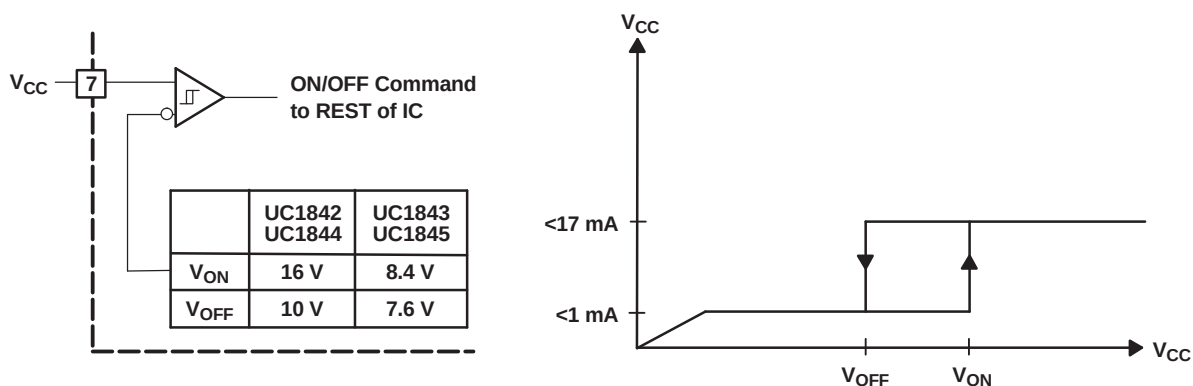
ERROR AMP CONFIGURATION

Error amp can source or sink up to 0.5 mA.



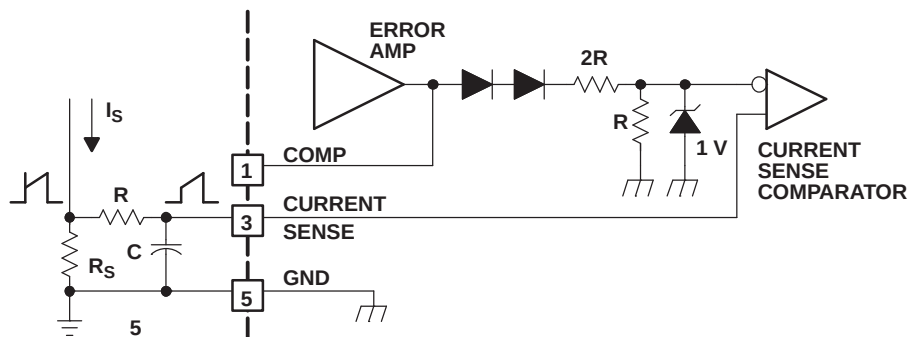
UNDER-VOLTAGE LOCKOUT

During under-voltage lock-out, the output drive is biased to sink minor amounts of current. Pin 6 should be shunted to ground with a bleeder resistor to prevent activating the power switch with extraneous leakage currents.



CURRENT SENSE CIRCUIT

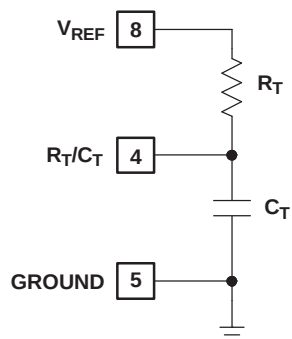
A small RC filter may be required to suppress switch transients.



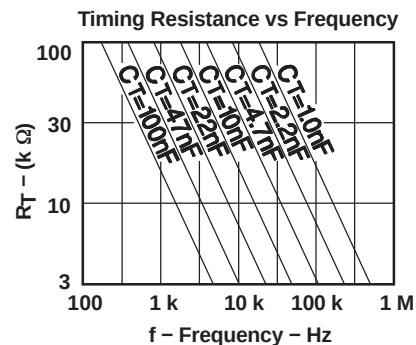
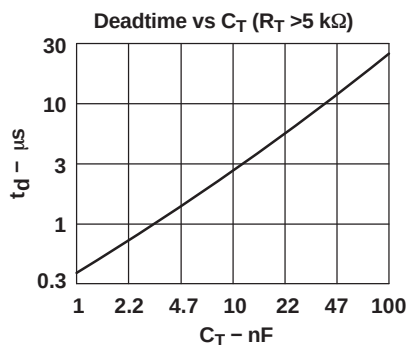
Peak Current (I_S) is Determined By The Formula

$$I_{S\text{MAX}} = \frac{1.0 \text{ V}}{R_S}$$

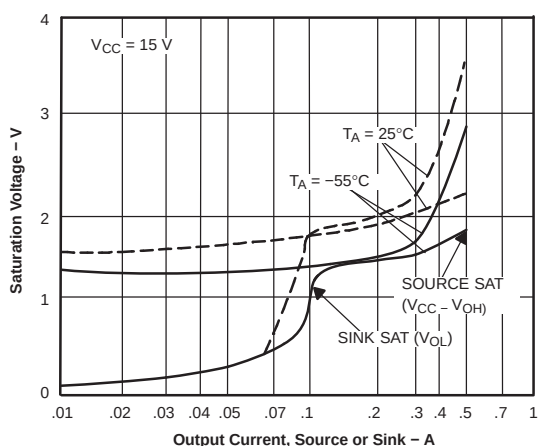
OSCILLATOR SECTION



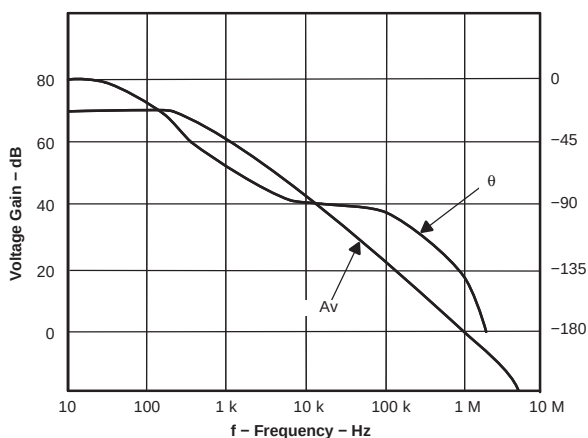
$$\text{For } R_T > 5 \text{ K } f \sim \frac{1.72}{R_T C_T}$$



OUTPUT SATURATION CHARACTERISTICS

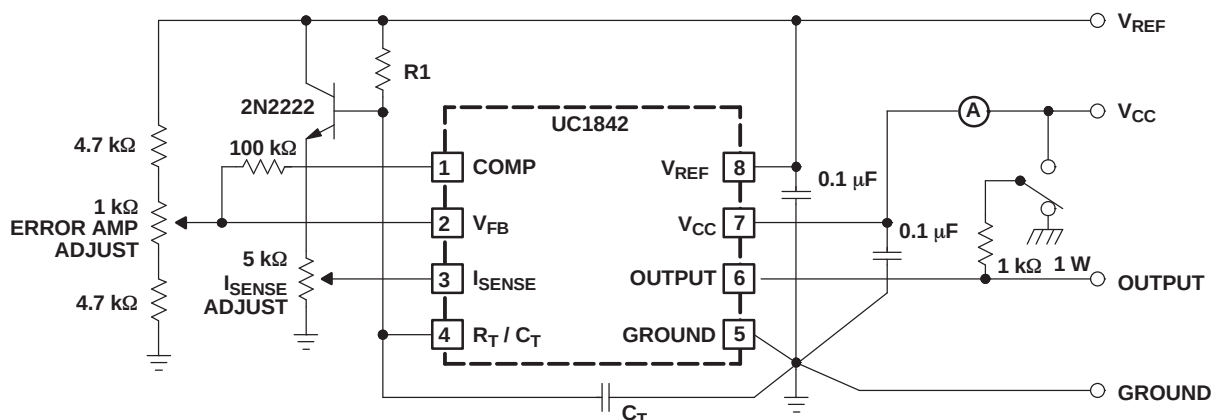


ERROR AMPLIFIER OPEN-LOOP FREQUENCY RESPONSE



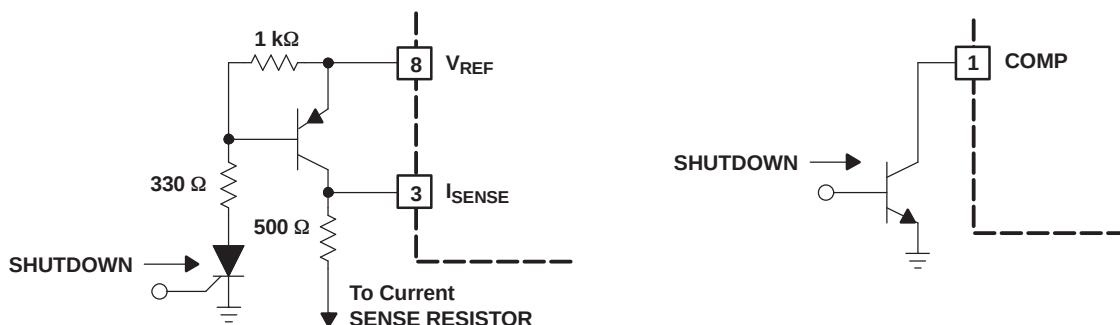
OPEN-LOOP LABORATORY FIXTURE

High peak currents associated with capacitive loads necessitate careful grounding techniques. Timing and bypass capacitors should be connected close to pin 5 in a single point ground. The transistor and 5k potentiometer are used to sample the oscillator waveform and apply an adjustable ramp to pin 3.

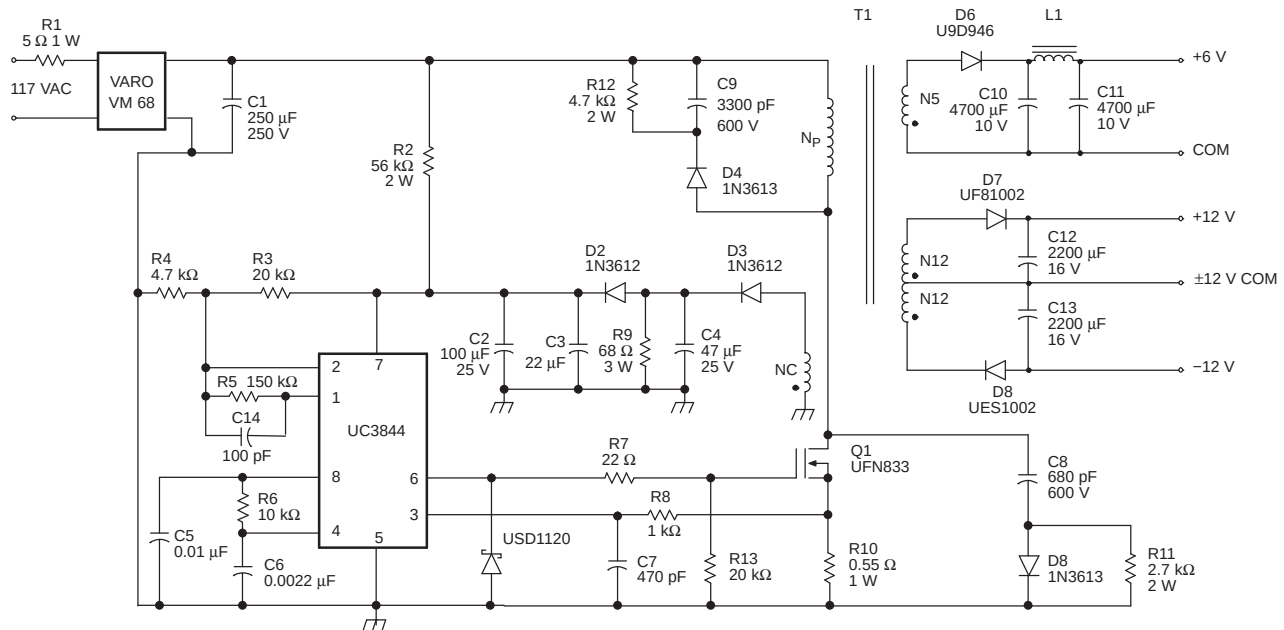


SHUTDOWN TECHNIQUES

Shutdown of the UC1842 can be accomplished by two methods; either raise pin 3 above 1 V or pull pin 1 below a voltage two diode drops above ground. Either method causes the output of the PWM comparator to be high (refer to block diagram). The PWM latch is reset dominant so that the output will remain low until the next clock cycle after the shutdown condition at pin 1 and/or 3 is removed. In one example, an externally latched shutdown may be accomplished by adding an SCR which will be reset by cycling V_{CC} below the lower UVLO threshold. At this point the reference turns off, allowing the SCR to reset.



OFFLINE FLYBACK REGULATOR

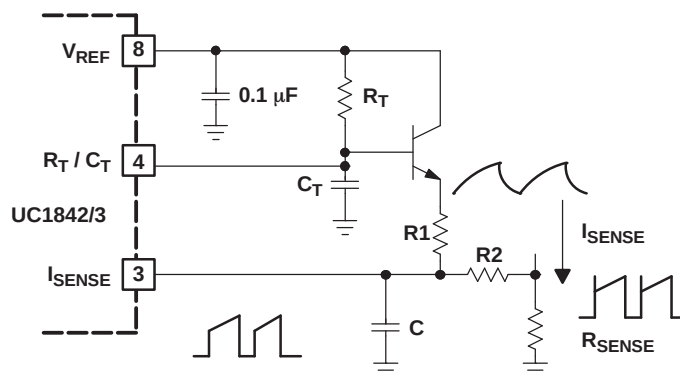


Power Supply Specifications

1. Input Voltages
 - a. 5VAC to 130VA (50 Hz/60 Hz)
2. Line Isolation: 3750 V
3. Switching Frequency: 40 kHz
4. Efficiency at Full Load 70%
5. Output Voltage:
 - a. +5 V, $\pm 5\%$; 1A to 4A load
Ripple voltage: 50 mV P-P Max
 - b. +12 V, $\pm 3\%$; 0.1A to 0.3A load
Ripple voltage: 100 mV P-P Max
 - c. -12 V, $\pm 3\%$; 0.1A to 0.3A load
Ripple voltage: 100 mV P-P Max

SLOPE COMPENSATION

A fraction of the oscillator ramp can be resistively summed with the current sense signal to provide slope compensation for converters requiring duty cycles over 50%.



PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
5962-8670401PA	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type
5962-8670401XA	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
5962-8670402PA	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type
5962-8670402XA	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
5962-8670403PA	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type
5962-8670403XA	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
5962-8670404DA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type
5962-8670404PA	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type
5962-8670404XA	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
UC1842J	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type
UC1842J883B	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type
UC1842L883B	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
UC1842W	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type
UC1843J	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type
UC1843J883B	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type
UC1843L	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
UC1843L883B	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
UC1843W	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type
UC1844J	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type
UC1844J883B	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type
UC1844L883B	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
UC1845J	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type
UC1845J883B	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type
UC1845L	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
UC1845L883B	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
UC1845W	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type
UC1845W883B	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type
UC2842D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UC2842D8	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UC2842D8G4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UC2842D8TR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UC2842D8TRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UC2842DG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UC2842DTR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UC2842DTRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UC2842J	OBSOLETE	CDIP	JG	8		TBD	Call TI	Call TI

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
UC2842N	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
UC2842NG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
UC2842P	OBSOLETE	PDIP	P	8		TBD	Call TI	Call TI
UC2843D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UC2843D8	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UC2843D8G4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UC2843D8TR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UC2843D8TRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UC2843DG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UC2843DTR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UC2843DTRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UC2843J	OBSOLETE	CDIP	JG	8		TBD	Call TI	Call TI
UC2843N	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
UC2843NG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
UC2844D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UC2844D8	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UC2844D8G4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UC2844D8TR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UC2844D8TRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UC2844DG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UC2844DTR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UC2844DTRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UC2844N	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
UC2844NG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
UC2845D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UC2845D8	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UC2845D8G4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
no Sb/Br)								
UC2845D8TR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UC2845D8TRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UC2845DG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UC2845DTR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UC2845DTRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UC2845J	OBSOLETE	CDIP	JG	8		TBD	Call TI	Call TI
UC2845N	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
UC2845NG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
UC3842D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UC3842D8	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UC3842D8G4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UC3842D8TR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UC3842D8TRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UC3842DG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UC3842DTR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UC3842DTRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UC3842N	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
UC3842NG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
UC3842P	OBSOLETE	PDIP	P	8		TBD	Call TI	Call TI
UC3843D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UC3843D8	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UC3843D8G4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UC3843D8TR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UC3843D8TRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UC3843DG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UC3843DTR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
UC3843DTRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UC3843N	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
UC3843NG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
UC3843P	OBSOLETE	PDIP	P	8		TBD	Call TI	Call TI
UC3843QTR	OBSOLETE	PLCC	FN	20		TBD	Call TI	Call TI
UC3844D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UC3844D8	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UC3844D8G4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UC3844D8TR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UC3844D8TRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UC3844DG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UC3844DTR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UC3844DTRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UC3844N	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
UC3844NG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
UC3844P	OBSOLETE	PDIP	P	8		TBD	Call TI	Call TI
UC3845AJ	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type
UC3845D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UC3845D8	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UC3845D8G4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UC3845D8TR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UC3845D8TRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UC3845DG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UC3845DTR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UC3845DTRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UC3845N	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
UC3845NG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
UC3845P	OBSOLETE	PDIP	P	8		TBD	Call TI	Call TI

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

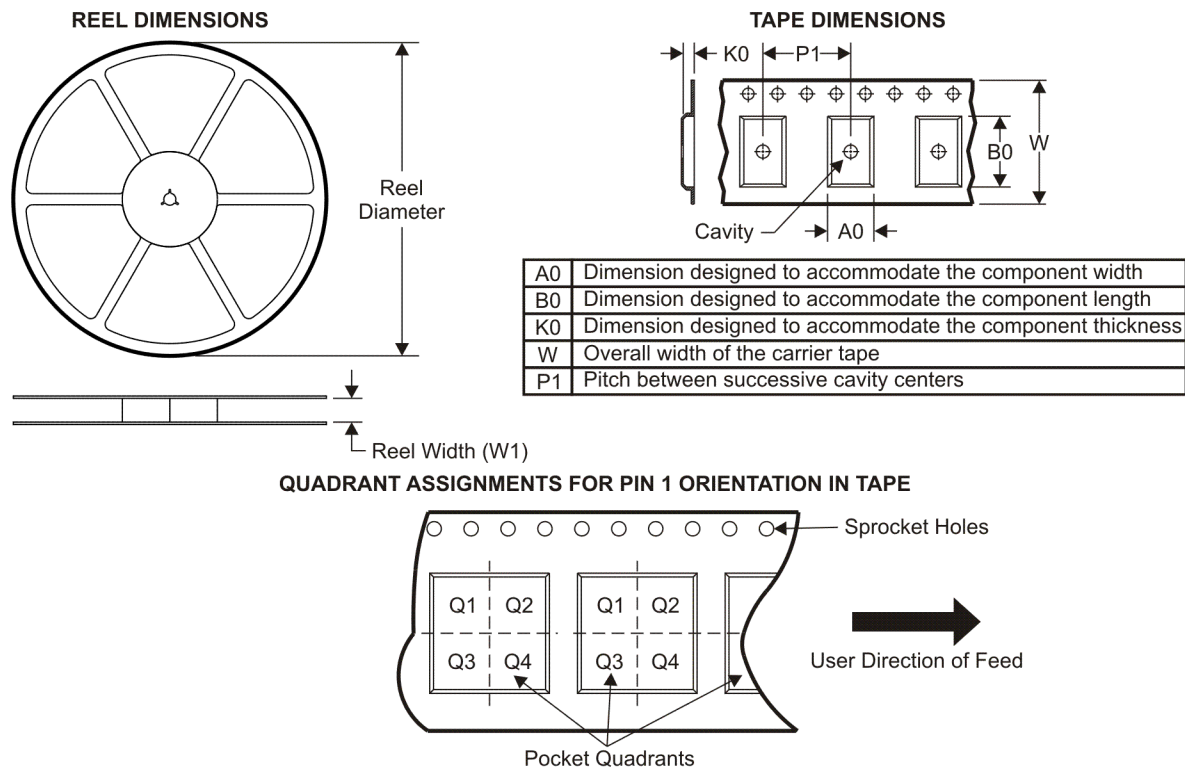
OTHER QUALIFIED VERSIONS OF UC1842, UC1843, UC1844, UC1845, UC3842, UC3843, UC3844, UC3845, UC3845AM :

- Catalog: [UC3842M](#), [UC3845A](#)
- Space: [UC1842-SP](#), [UC1843-SP](#), [UC1844-SP](#), [UC1845-SP](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

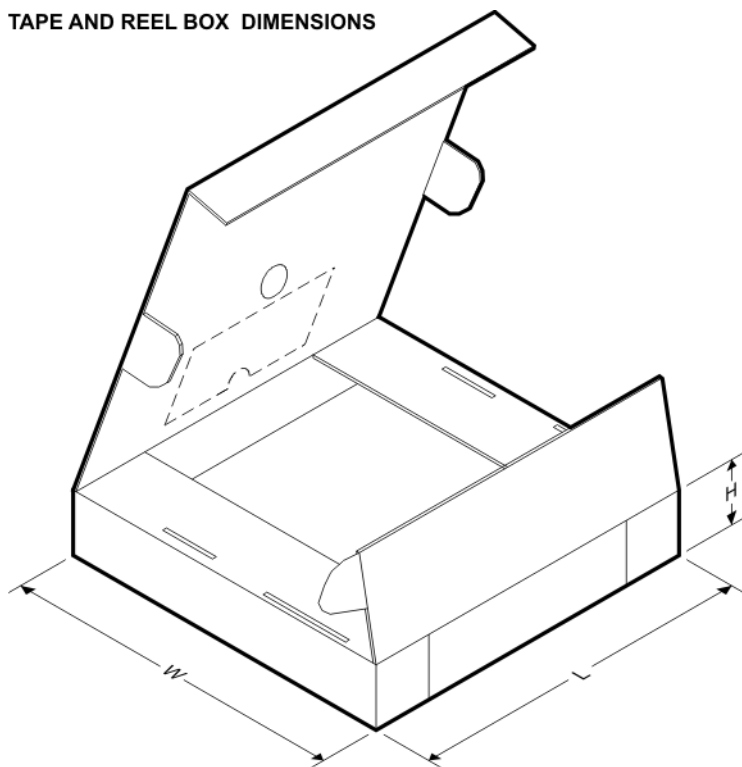
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UC2842D8TR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UC2842DTR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
UC2843D8TR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UC2843DTR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
UC2844D8TR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UC2844DTR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
UC2845D8TR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UC2845DTR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
UC3842D8TR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UC3842DTR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
UC3843D8TR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UC3843DTR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
UC3844D8TR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UC3844DTR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
UC3845D8TR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UC3845DTR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



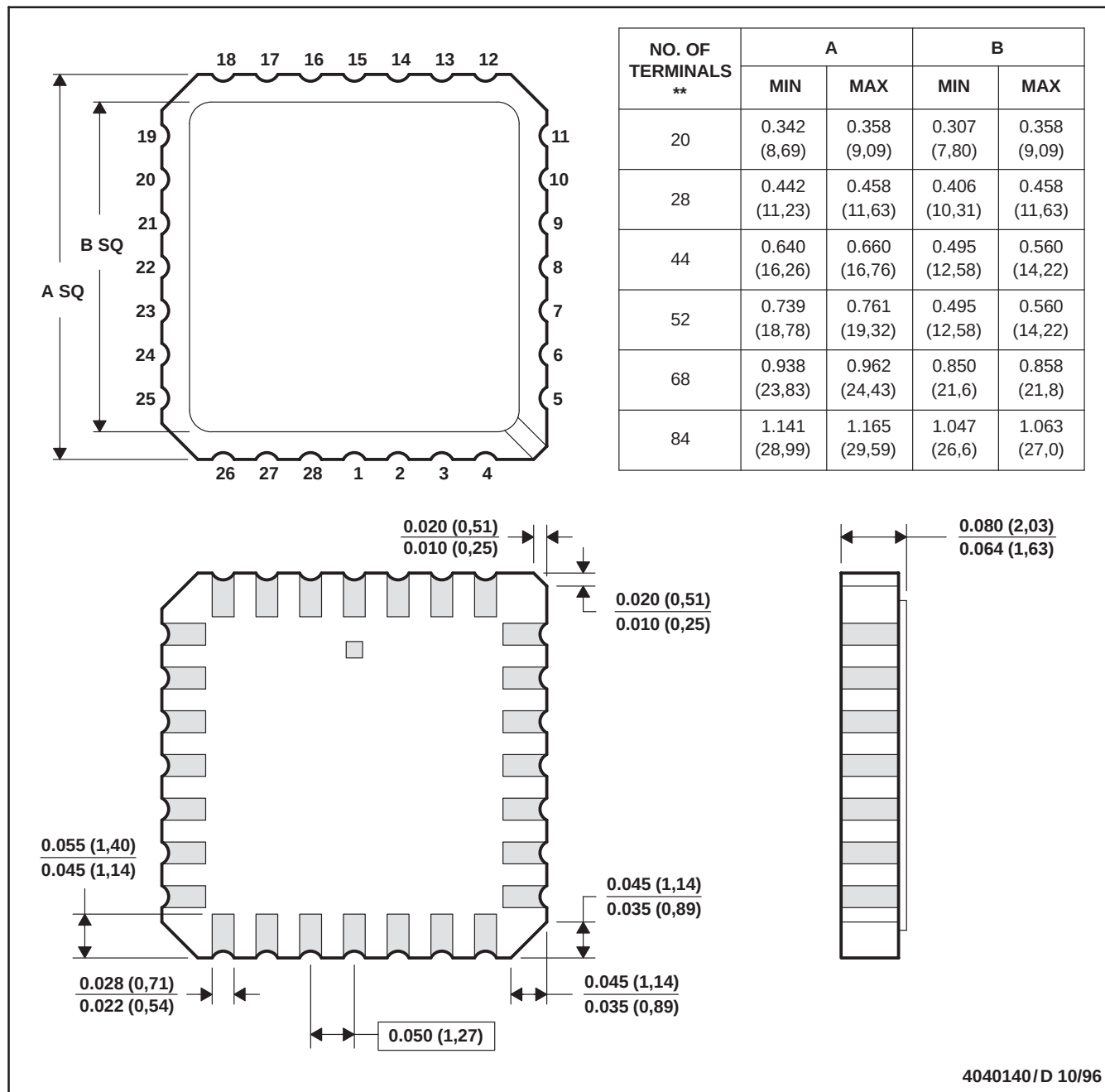
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UC2842D8TR	SOIC	D	8	2500	340.5	338.1	20.6
UC2842DTR	SOIC	D	14	2500	333.2	345.9	28.6
UC2843D8TR	SOIC	D	8	2500	340.5	338.1	20.6
UC2843DTR	SOIC	D	14	2500	333.2	345.9	28.6
UC2844D8TR	SOIC	D	8	2500	340.5	338.1	20.6
UC2844DTR	SOIC	D	14	2500	333.2	345.9	28.6
UC2845D8TR	SOIC	D	8	2500	340.5	338.1	20.6
UC2845DTR	SOIC	D	14	2500	333.2	345.9	28.6
UC3842D8TR	SOIC	D	8	2500	340.5	338.1	20.6
UC3842DTR	SOIC	D	14	2500	333.2	345.9	28.6
UC3843D8TR	SOIC	D	8	2500	340.5	338.1	20.6
UC3843DTR	SOIC	D	14	2500	333.2	345.9	28.6
UC3844D8TR	SOIC	D	8	2500	340.5	338.1	20.6
UC3844DTR	SOIC	D	14	2500	333.2	345.9	28.6
UC3845D8TR	SOIC	D	8	2500	340.5	338.1	20.6
UC3845DTR	SOIC	D	14	2500	333.2	345.9	28.6

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

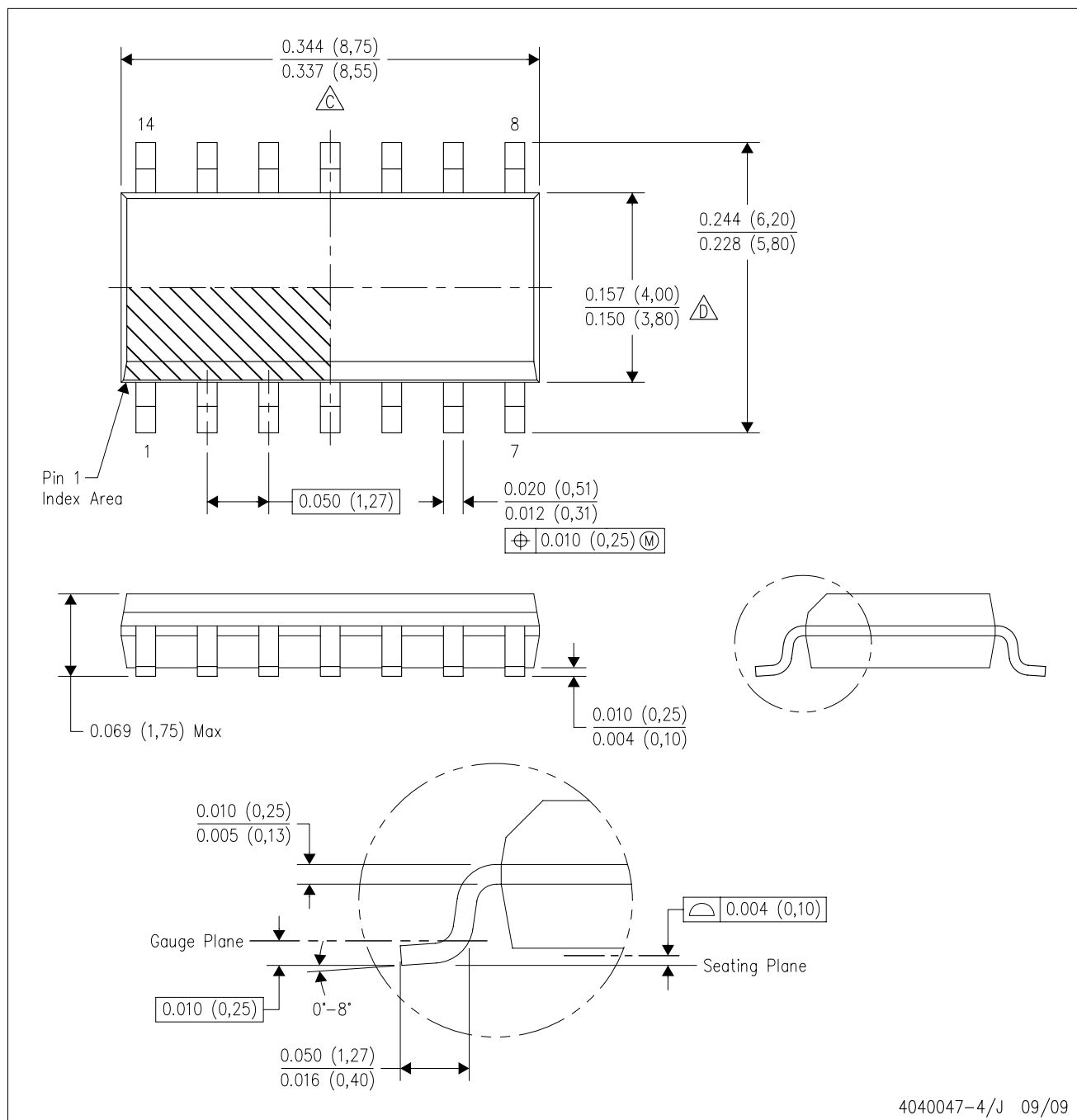
28 TERMINAL SHOWN



- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a metal lid.
 - The terminals are gold plated.
 - Falls within JEDEC MS-004

D (R-PDSO-G14)

PLASTIC SMALL-OUTLINE PACKAGE

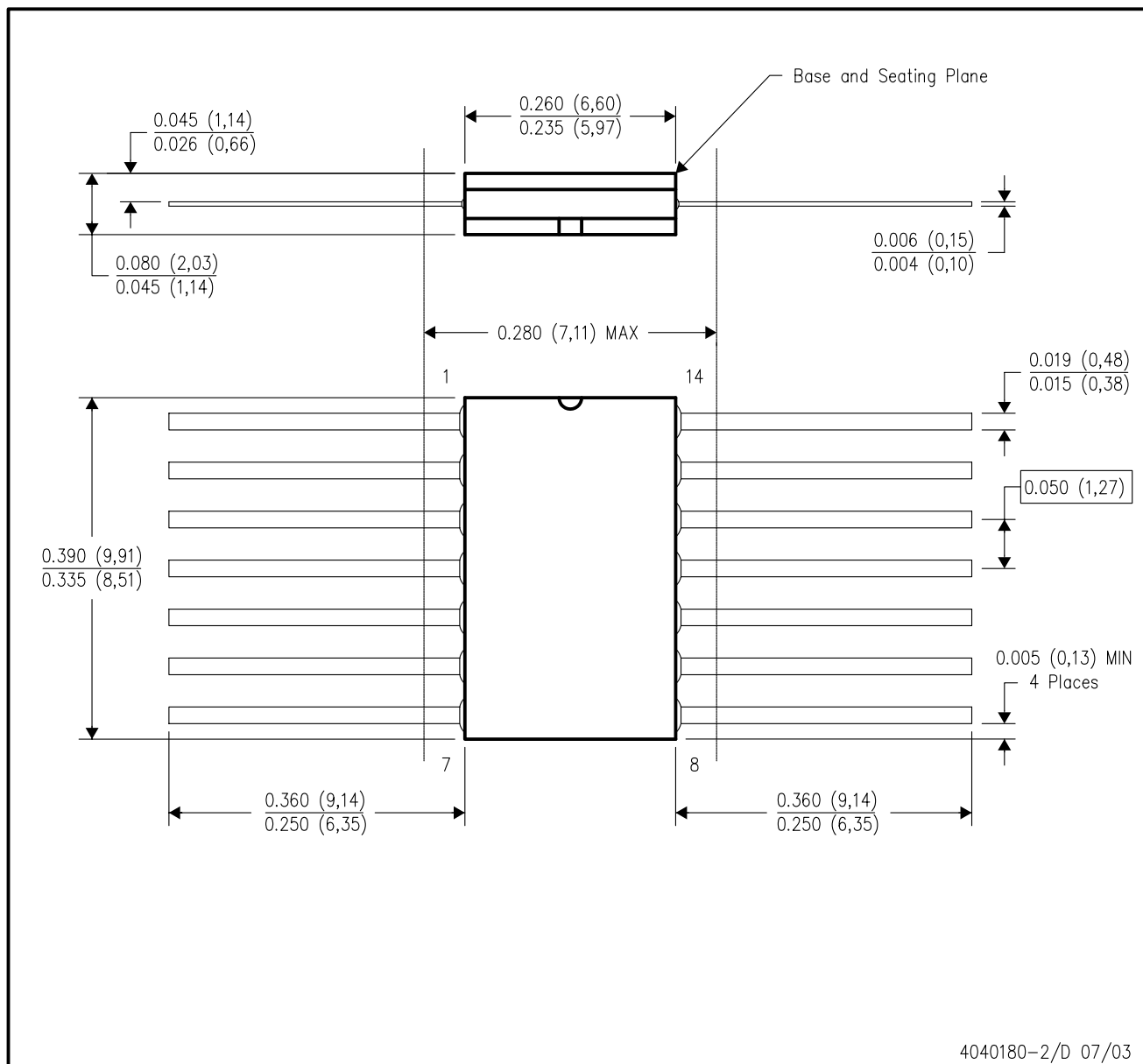


NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
- D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
- E. Reference JEDEC MS-012 variation AB.

W (R-GDFP-F14)

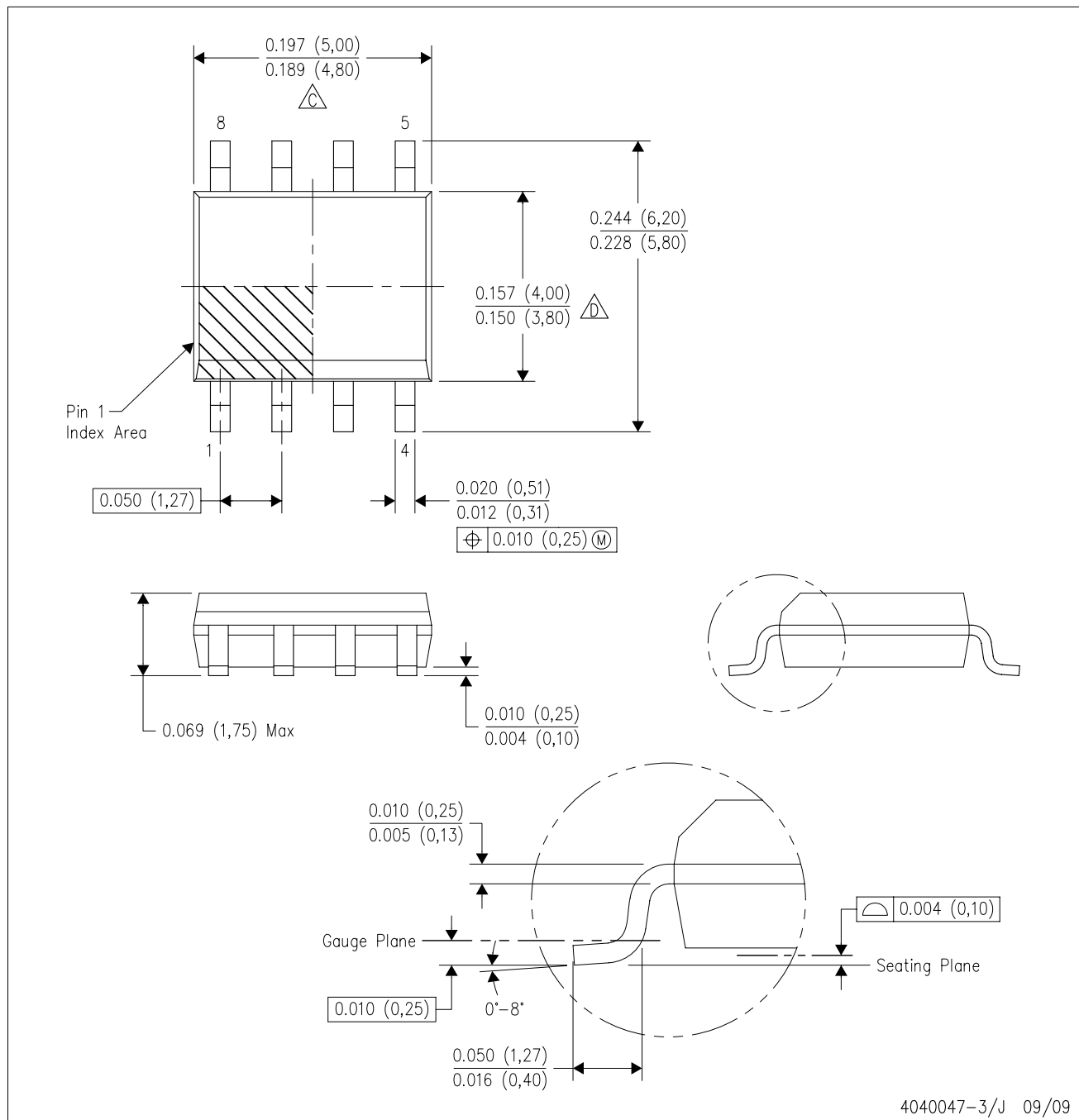
CERAMIC DUAL FLATPACK



- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only.
 - Falls within MIL STD 1835 GDFP1-F14 and JEDEC MO-092AB

D (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE

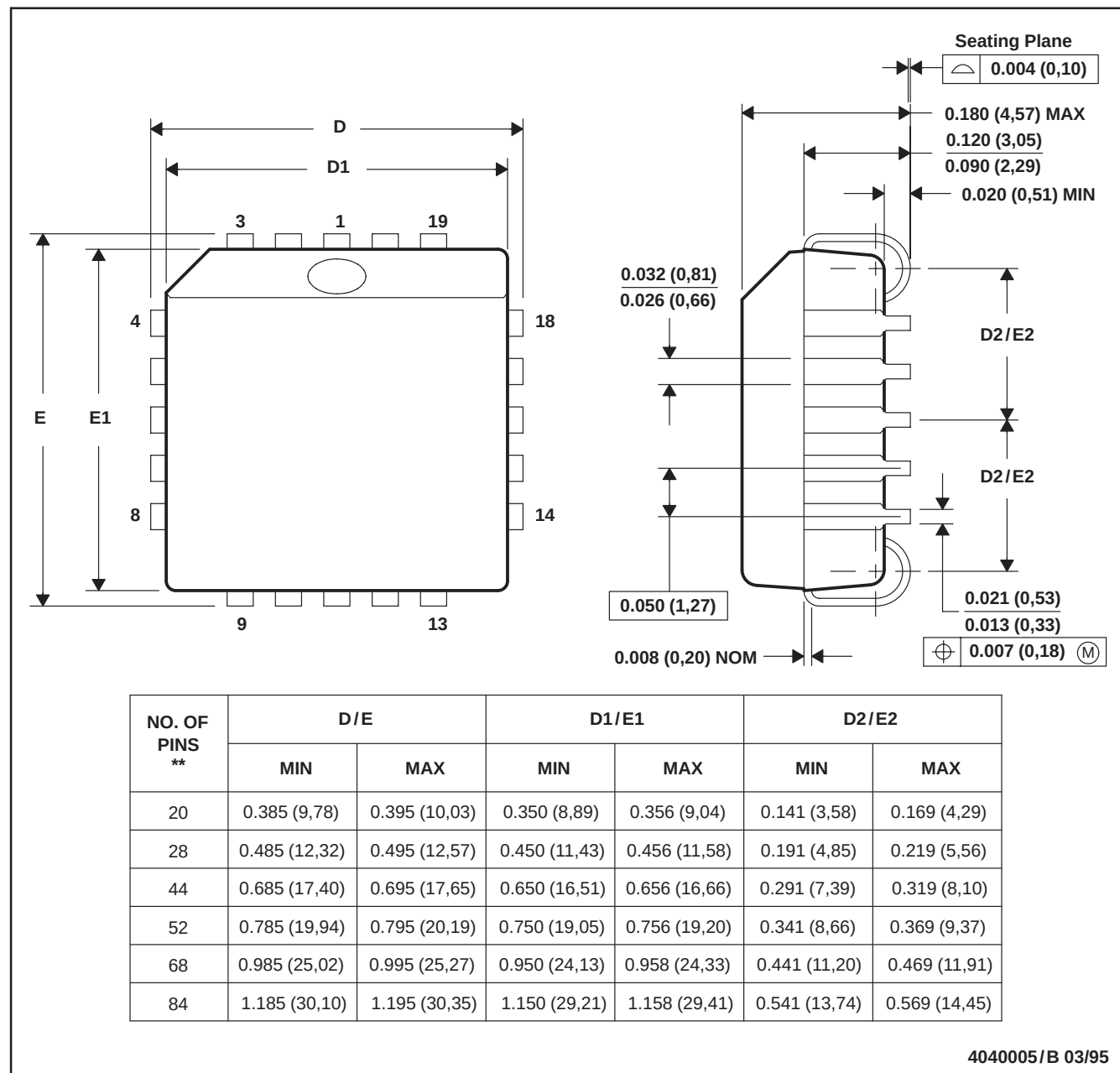


- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - $\triangle C$ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
 - $\triangle D$ Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
 - E. Reference JEDEC MS-012 variation AA.

FN (S-PQCC-J**)

PLASTIC J-LEADED CHIP CARRIER

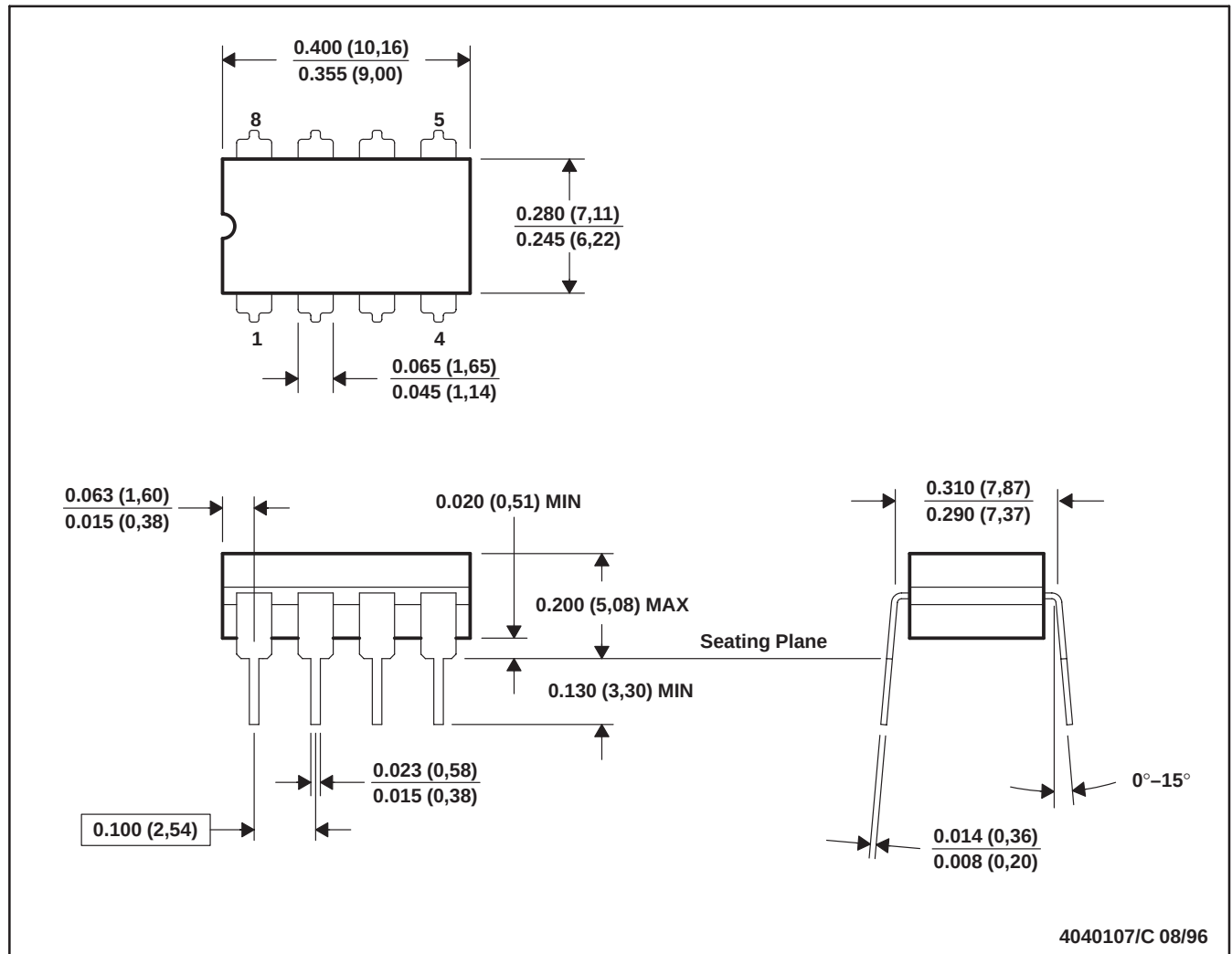
20 PIN SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Falls within JEDEC MS-018

JG (R-GDIP-T8)

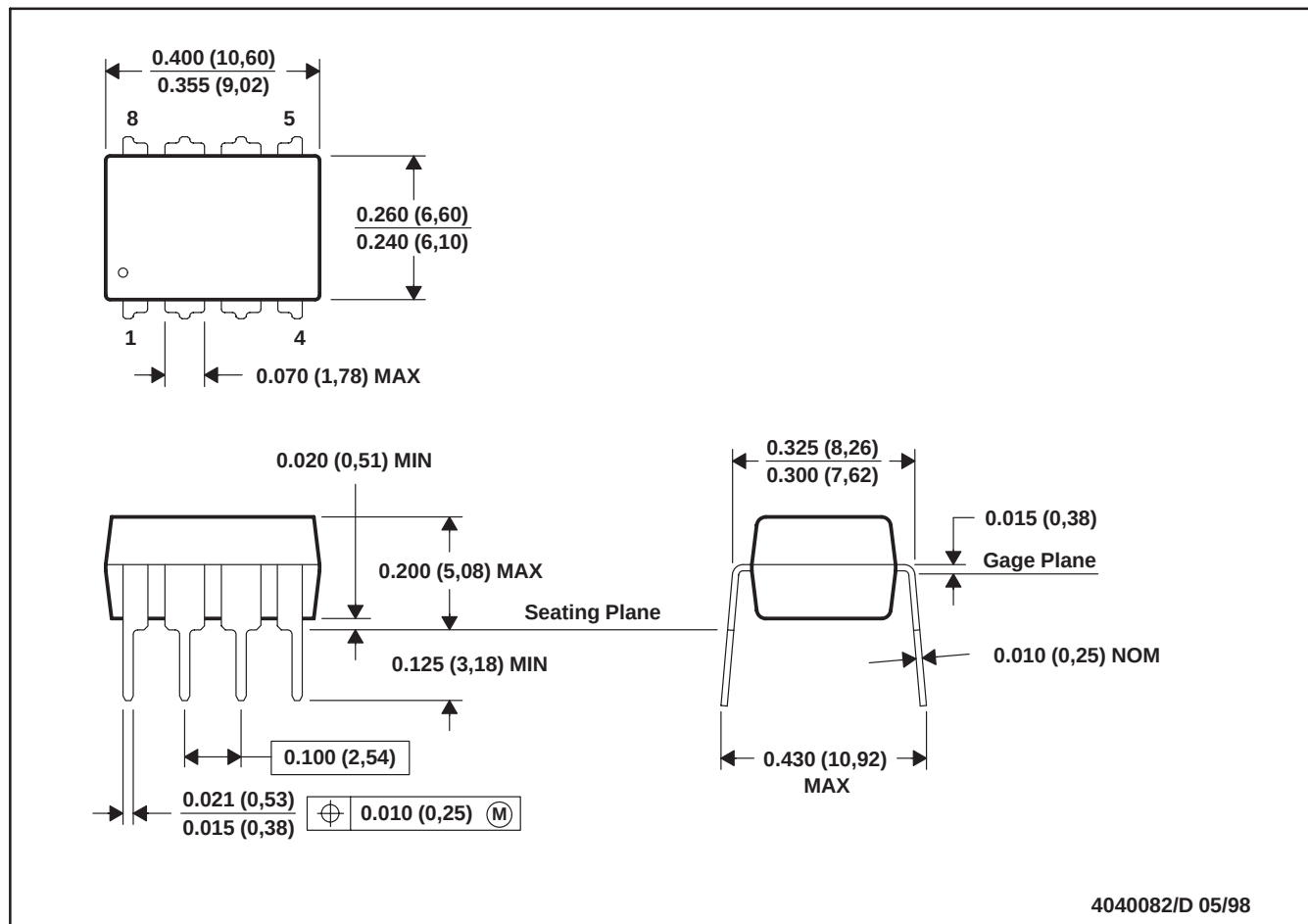
CERAMIC DUAL-IN-LINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification.
 - E. Falls within MIL STD 1835 GDIP1-T8

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Falls within JEDEC MS-001

For the latest package information, go to http://www.ti.com/sc/docs/package/pkg_info.htm

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products

Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DLP® Products	www.dlp.com
DSP	dsp.ti.com
Clocks and Timers	www.ti.com/clocks
Interface	interface.ti.com
Logic	logic.ti.com
Power Mgmt	power.ti.com
Microcontrollers	microcontroller.ti.com
RFID	www.ti-rfid.com
RF/IF and ZigBee® Solutions	www.ti.com/lprf

Applications

Audio	www.ti.com/audio
Automotive	www.ti.com/automotive
Broadband	www.ti.com/broadband
Digital Control	www.ti.com/digitalcontrol
Medical	www.ti.com/medical
Military	www.ti.com/military
Optical Networking	www.ti.com/opticalnetwork
Security	www.ti.com/security
Telephony	www.ti.com/telephony
Video & Imaging	www.ti.com/video
Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2009, Texas Instruments Incorporated