TOSHIBA Field Effect Transistor Silicon N Channel MOS Type

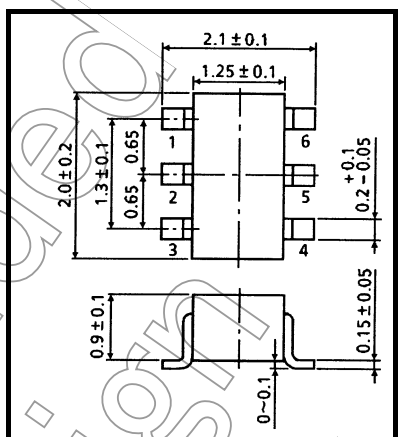
SSM6K07FU

DC-DC Converters

High-Speed Switching Applications

- Small package
- Low ON-resistance: $R_{DS(ON)}$ = 130 mΩ max (@V_{GS} = 10 V)
  : $R_{DS(ON)}$ = 220 mΩ max (@V_{GS} = 4 V)
- Low input capacitance : C_{iss} = 102 pF typ.
  : C_{rss} = 22 pF typ.

Unit: mm



US6	
JEDEC	—
JEITA	—
TOSHIBA	2-2J1D

Weight: 6.8 mg (typ.)

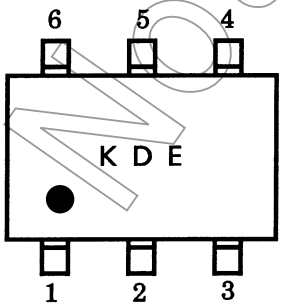
Absolute Maximum Ratings (Ta = 25°C)

Characteristics		Symbol	Rating	Unit
Drain-source voltage		V_{DS}	30	V
Gate-source voltage		V_{GSS}	±20	V
Drain current	DC	I_D	1.5	A
	Pulse	I_{DP}	3.0	
Drain power dissipation		P_D (Note 1)	300	mW
Channel temperature		T_{ch}	150	°C
Storage temperature range		T_{stg}	−55 to 150	°C

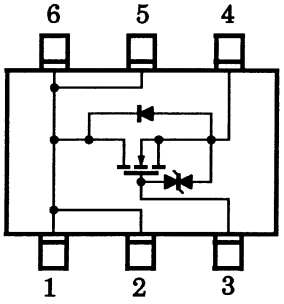
Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: Mounted on FR4 board.
(25.4 mm × 25.4 mm × 1.6 mm (t), Cu pad: 0.32 mm2 × 6)

Marking



Equivalent Circuit (top view)



Handling Precaution

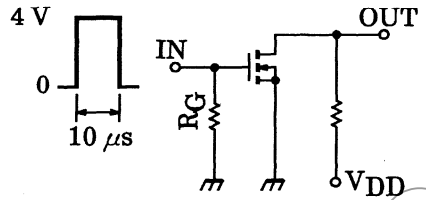
When handling individual devices (which are not yet mounting on a circuit board), be sure that the environment is protected against electrostatic electricity. Operators should wear anti-static clothing, and containers and other objects that come into direct contact with devices should be made of anti-static materials.

Electrical Characteristics (Ta = 25°C)

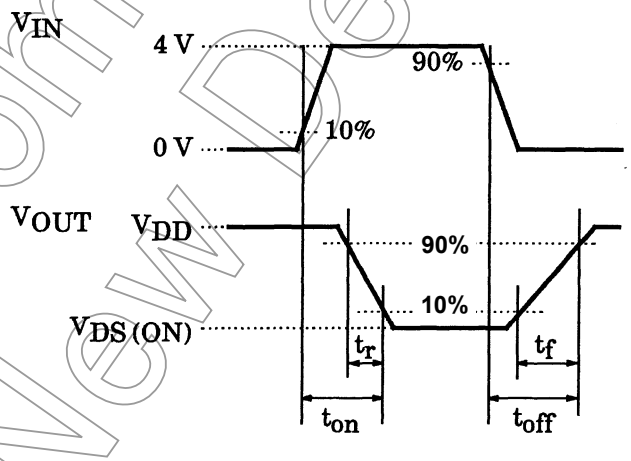
Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current		I_{GSS}	V_{GS} = ±16 V, V_{DS} = 0	—	—	±1	μA
Drain-source breakdown voltage		$V_{(BR)\ DSS}$	I_D = 1 mA, V_{GS} = 0	30	—	—	V
Drain cut-off current		I_{DSS}	V_{DS} = 30 V, V_{GS} = 0	—	—	1	μA
Gate threshold voltage		V_{th}	V_{DS} = 5 V, I_D = 0.1 mA	1.1	—	1.8	V
Forward transfer admittance		$\|Y_{fs}\|$	V_{DS} = 5 V, I_D = 0.75 A (Note 2)	1.0	—	—	S
Drain-source ON resistance		$R_{DS\ (ON)}$	I_D = 0.75 A, V_{GS} = 10 V (Note 2)	—	105	130	mΩ
		$R_{DS\ (ON)}$	I_D = 0.75 A, V_{GS} = 4 V (Note 2)	—	170	220	
		$R_{DS\ (ON)}$	I_D = 0.75 A, V_{GS} = 3.3 V (Note 2)	—	230	500	
Input capacitance		C_{iss}	V_{DS} = 15 V, V_{GS} = 0, f = 1 MHz	—	102	—	pF
Reverse transfer capacitance		C_{rss}	V_{DS} = 15 V, V_{GS} = 0, f = 1 MHz	—	22	—	pF
Output capacitance		C_{oss}	V_{DS} = 15 V, V_{GS} = 0, f = 1 MHz	—	57	—	pF
Switching time	Turn-on time	t_{on}	V_{DD} = 15 V, I_D = 0.75 A, V_{GS} = 0 to 4 V, R_G = 10 Ω	—	46	—	ns
	Turn-off time	t_{off}		—	65	—	

Note 2: Pulse test

Switching Time Test Circuit



V_{DD} = 15 V
R_G = 10 Ω
Duty ≤ 1%
V_{IN} : t_r, t_f < 5 ns
COMMON SOURCE
Ta = 25°C



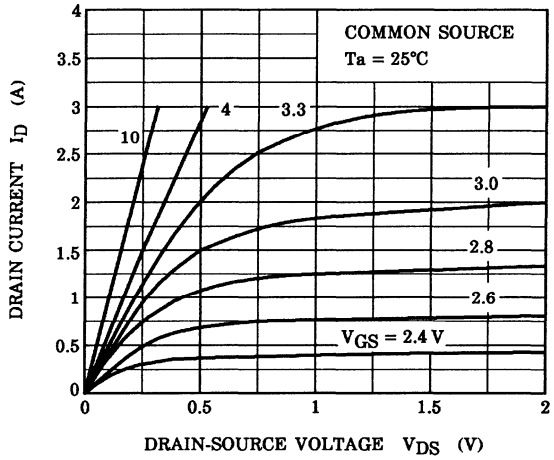
Precaution

V_{th} can be expressed as voltage between gate and source when low operating current value is I_D = 100 μA for this product. For normal switching operation, $V_{GS\ (on)}$ requires higher voltage than V_{th} and $V_{GS\ (off)}$ requires lower voltage than V_{th}.

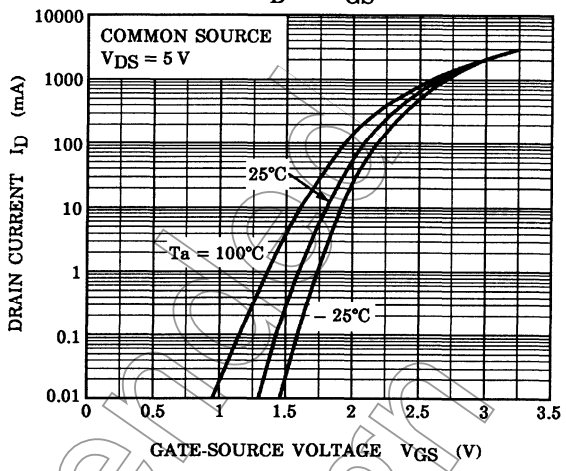
(Relationship can be established as follows: $V_{GS\ (off)} < V_{th} < V_{GS\ (on)}$)

Please take this into consideration for using the device.

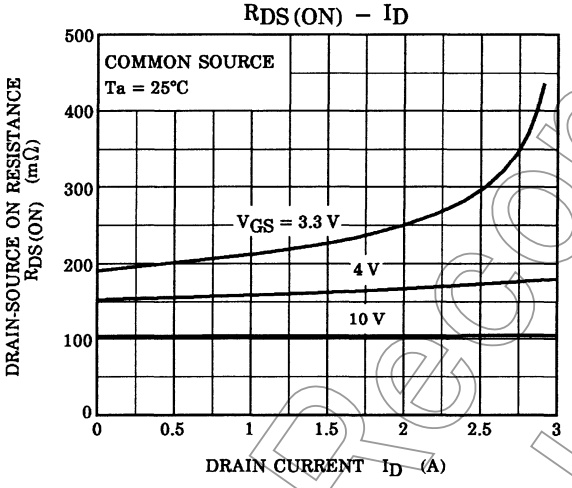
$I_D - V_{DS}$



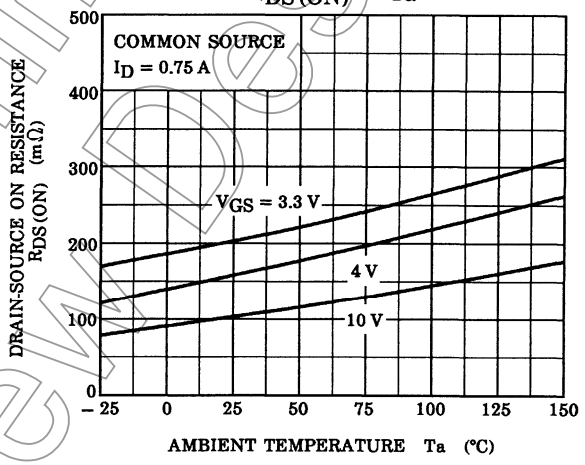
$I_D - V_{GS}$



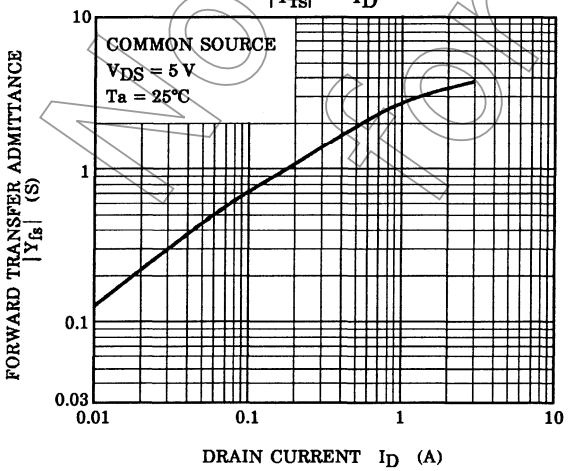
$R_{DS\,(ON)} - I_D$



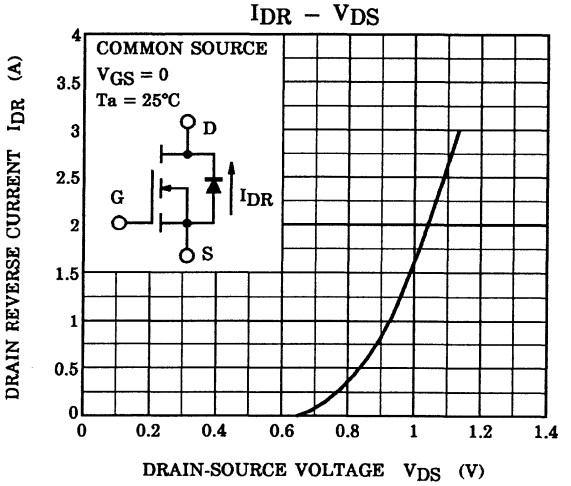
$R_{DS\,(ON)} - Ta$



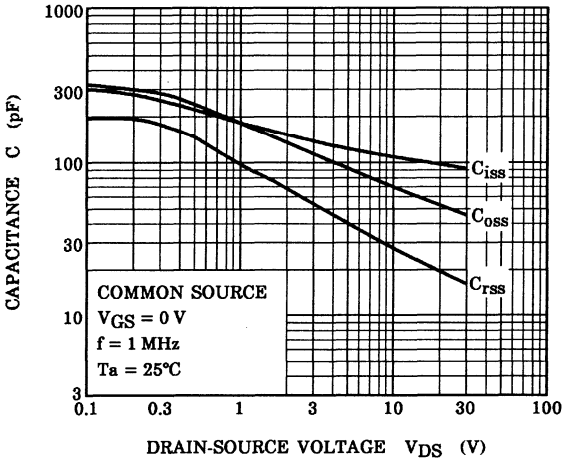
$|Y_{fs}| - I_D$



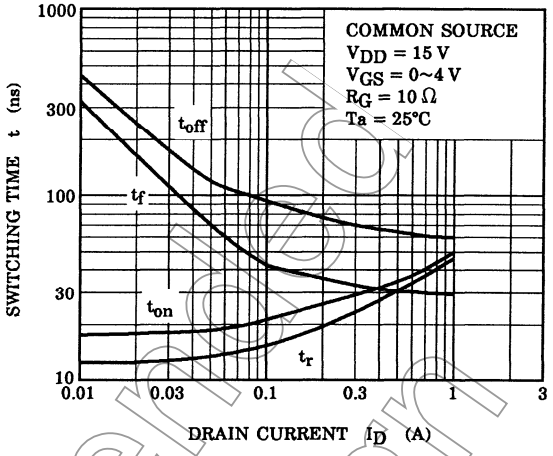
$I_{DR} - V_{DS}$



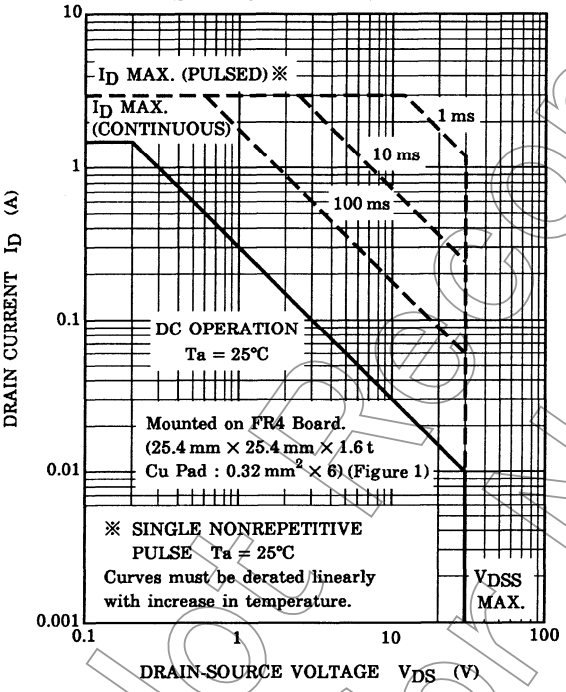
C – V_{DS}



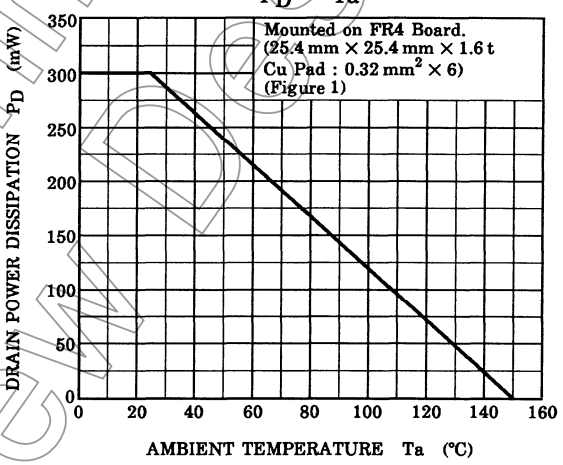
t – I_D



SAFE OPERATING AREA



P_D – Ta



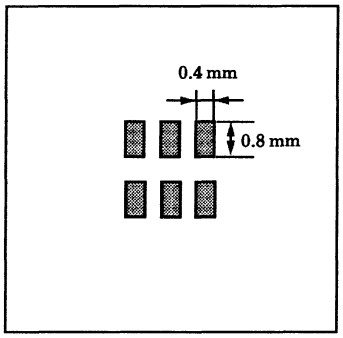


Figure 1 25.4 mm × 25.4 mm × 1.6 mm (t), Cu Pad: 0.32 mm^2 × 6

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