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NTE1690
Integrated Circuit
Telephone DTMF Dialer

Description:

The NTE1690 is a low threshold voltage, field–implanted, metal gate CMOS integrated circuit in a 16–Lead DIP type package. This device interfaces directly to a standard telephone keypad and generates all dual tone multi–frequency pairs required in tone dialing systems. The tone synthesizers are locked to an on–chip reference oscillator using an inexpensive 3.579545MHz crystal for high tone accuracy. The crystal and an output load resistor are the only external components required for tone generation. A $\overline{\text{MUTE}}$ OUT logic signal, which changes state when any key is depressed is also provided.

Features:

- 3V to 10V Operation When Generating Tones
- 2V Operation of Keyscan and $\overline{\text{MUTE}}$ Logic
- Static Sensing of Key Closures or Logic Inputs
- On–Chip 3.579545MHz Crystal–Controlled Oscillator
- Output Amplitudes Proportional to Supply Voltage
- High Group Pre–Emphasis
- Low Harmonic Distortion
- Open Emitter–Follower Low–Impedance Output
- $\overline{\text{SINGLE TONE INHIBIT}}$ Pin

Absolute Maximum Ratings:

Supply Voltage ($V_{DD} - V_{SS}$) 15V
Maximum Voltage at Any Pin . . . . . V_{DD}+0.3V to V_{SS}–0.3V
Power Dissipation, P_D 500mW
Operating Temperature Range, T_{opr} . . . . . –30° to +60°C
Storage Temperature Range, T_{stg} . . . . . –55° to +150°C

Electrical Characteristics: (–30°C < T_A < +60°C, 3V < V_{DD} < 10V unless otherwise specified)

Parameter	Test Conditions	Min	Typ	Max	Unit
Minimum Supply Voltage for Keysense and $\overline{\text{MUTE}}$ Logic Functions		–	–	2	V
Operating Current, Idle	R_L = 10kΩ	–	20	–	μA
Operating Current, Generating Tones	V_O = 5V	–	2	–	mA

Electrical Characteristics (Cont'd): (–30°C < T_A < +60°C, 3V < V_{DD} < 10V unless othewise specified)

Parameter	Test Conditions	Min	Typ	Max	Unit
Input Resistors					
COLUMN and ROW (Pull–Up)		–	40	–	kΩ
$\overline{\text{SINGLE TONE INHIBIT}}$ (Pull–Down)		–	50	–	kΩ
$\overline{\text{TONE DISABLE}}$ (Pull–Up)		–	50	–	kΩ
$\overline{\text{MUTE}}$ OUT Sink Current (COLUMN and ROW Active)	V_{DD} = 3V, V_O = 0.5V	0.5	–	–	mA
Output Amplitudes, Low Group	R_L = 240Ω, V_{DD} = 3V	–	250	–	mV_{rms}
	R_L = 240Ω, V_{DD} = 10V	–	850	–	mV_{rms}
Output Amplitudes, High Group	R_L = 240Ω, V_{DD} = 3V	–	315	–	mV_{rms}
	R_L = 240Ω, V_{DD} = 10V	–	1000	–	mV_{rms}
Mean Output DC Offset	V_{DD} = 3V	–	1.2	–	V
	V_{DD} = 10V	–	4.2	–	V
High Group Pre–Emphasis		2.4	2.7	3.0	dB
Dual Tone/Harmonic Distortion Ratio	1MHz Bandwidth	22	–	–	dB
Start–Up Time (90% Amplitude)		–	3	5	ms

Note 1. Crystal Specification: Parallel Resonant 3.579545MHz, $R_S \leq 150\Omega$, L = 100mH, C_0 = 5pF, C_1 = 0.02pf.

Pin Descriptions:

V_{DD} (Pin1): This is the positive voltage supply to the device, referenced to V_{SS}. The collector of the TONE OUT transistor is connected to this pin.

V_{SS} (Pin6): This is the negative voltage supply.

OSCILLATOR (Pin7 and Pin8): All tone generation timing is derived from the on–chip oscillator circuit. A low–cost 3.579545MHz A–cut crystal (NTSC TV color–burst) is needed between Pin7 and Pin8. Load capacitors and feedback resistor are included on–chip for good start–up and stability. The oscillator stops when column inputs are sensed with no valid input having been detected. The oscillator is also stopped when the $\overline{\text{TONE DISABLE}}$ input is pulled to logic low.

Row and Column Inputs (Pins 3, 4, 5, 9, 11, 12, 13, 14): When no key is pushed, pull–up resistors are active on row and column inputs. A key closure is recognized when a single row and a single column are connected to V_{SS}, which starts the oscillator and initiates tone generation. Negative–true logic signals simulating key closures can also be used.

$\overline{\text{TONE DISABLE}}$ Input (Pin2): The $\overline{\text{TONE DISABLE}}$ input has an internal pull–up resistor. When this input is open or at logic high, the normal tone output mode will occur. When $\overline{\text{TONE DISABLE}}$ input is at logic low, the device will be in the inactive mode, TONE OUTPUT will be at an open circuit state.

$\overline{\text{MUTE}}$ Output (Pin10): The $\overline{\text{MUTE}}$ output is an open–drain N–channel device that sinks current to V_{SS} with any key input and is open when no key input is sensed. The $\overline{\text{MUTE}}$ output will switch regardless o the state of he $\overline{\text{SINGLE TONE INHIBIT}}$ input.

$\overline{\text{SINGLE TONE INHIBIT}}$ Input (Pin15): The $\overline{\text{SINGLE TONE INHIBIT}}$ input is used to inhibit the generation of other than valid tone pairs due to multiple row–column closures. It has a pull–down resistor to V_{SS}, and when left open or tied to V_{SS} any input condition that would normally result in a single tone will now result in no tone, with all other functions operating normally. When tied to V_{DD}, single or dual tones may be generated (See Table II).

TONE OUT (Pin16): This output is the open emitter of an NPN transistor, the collector of which is connected to V_{DD}. When an external load resistor is connected from TONE OUT to V_{SS}, the output voltage on this pin is the sum of the high and low group sine–waves superimposed on a DC offset. When not generating tones, this output transistor is turned OFF to minimize the device idle current.

Pin Descriptions (Cont'd):

Adjustment of the emitter load resistor results in variation of the mean DC current during tone generation, the sine–wave signal current through the output transistor, and the output distortion. Increasing values of load resistances decreases both the signal current and distortion.

Functional Description:

With no key inputs to the device the oscillator is inhibited, the output transistor is pulled OFF and device current consumption is reduced to a minimum. Key closures are sensed statically to ensure no modification of the line when tones are not being generated. Any key closure activates the $\overline{\text{MUTE}}$ output, starts the oscillator and sets the high group and low group programmable counters to the appropriate divide ratio. These counters sequence two ratioed–capacitor D/A converters through a series of 28 equal duration steps per sine–wave cycle. The two tones are summed by a mixer amplifier, with pre–emphasis applied to the high group tone. The output is an NPN emitter–follower requiring the addition of an external load resistor to V_{SS}. This resistor facilitates adjustment of the signal current flowing from V_{DD} through the output transistors.

The amplitude of the output tones is directly proportional to the device supply voltage.

Table I. Output Frequency Accuracy

Tone Group	Valid Input	Standard DTMF (Hz)	Tone Output Frequency	% Deviation from Standard
Low Group f_L	R1	697	694.8	–0.32
	R2	770	770.1	+0.02
	R3	852	852.4	+0.03
	R4	941	940.0	–0.11
High Group f_H	C1	1209	1206.0	–0.24
	C2	1336	1331.7	–0.32
	C3	1477	1486.5	+0.64
	C4	16334	1639.0	+0.37

Table II. Functional Truth Table

$\overline{\text{SINGLE TONE}}$ $\overline{\text{INHIBIT}}$	$\overline{\text{TONE}}$ $\overline{\text{DISABLE}}$	ROW	COLUMN	Tones		MUTE
				Low	High	
X	O	X	X	0V	0V	0
X	X	O/C	O/C	0V	0V	0
X	1	One	One	f_L	f_H	1
1	1	2 or More	One	–	f_H	1
1	1	One	2 or More	f_L	–	1
1	1	2 or More	2 or More	V_{OS}	V_{OS}	1
0	1	2 or More	One	V_{OS}	V_{OS}	1
0	1	One	2 or More	V_{OS}	V_{OS}	1
0	1	2 or More	2 or More	V_{OS}	V_{OS}	1

Note 2. X is don't care state.

Note 3. V_{OS} is the output offset voltage.

Pin Connection Diagram