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EVALUATION KIT AVAILABLE

PMIC with Integrated Charger and Smart Power Selector for Handheld Devices

General Description

The MAX8671X integrated power-management IC (PMIC) is ideal for use in portable media players and other handheld devices. In addition to five regulated output voltages, the MAX8671X integrates a 1-cell lithium ion (Li+) or lithium polymer (Li-Poly) charger and Smart Power Selector™ with dual (AC-to-DC adapter and USB) power inputs*. The dual-input Smart Power Selector supports end products with dual or single power connectors. All power switches for charging and switching the system load between battery and external power are included on-chip. No external MOSFETs are required.

Maxim's Smart Power Selector makes the best use of limited USB or AC-to-DC adapter power. Battery charge current and input current limit are independently set. Input power not used by the system charges the battery. Charge current and DC current limit are programmable up to 1A while USB input current can be set to 100mA or 500mA. Automatic input selection switches the system load from battery to external power. Other features include overvoltage protection, charge status and fault outputs, power-OK monitors, charge timer, and battery thermistor monitor. In addition, on-chip thermal limiting reduces battery charge rate to prevent charger overheating.

The MAX8671X offers adjustable voltages for all outputs. Similar parts with factory-preset output voltages are also available (contact factory for availability).

Applications

Portable Audio Players

GPS Portable Navigators

*Protected by US Patent #6,507,172.

Features

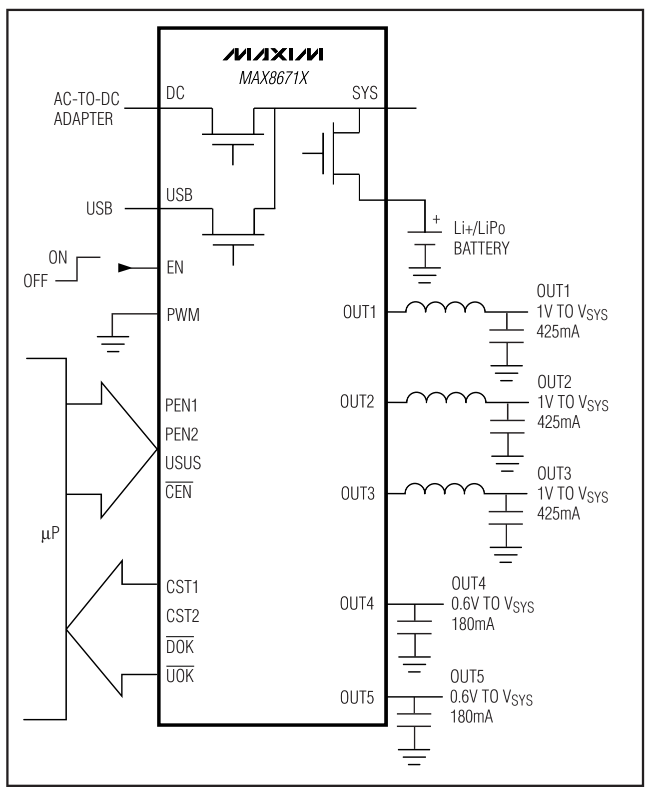
- ♦ 16V-Tolerant USB and DC Inputs
- ♦ Automatically Powers from External Power or Battery
- ♦ Operates with No Battery Present
- ♦ Single-Cell Li+/Li-Poly Charger
- ♦ Three 2MHz Step-Down Regulators
  Up to 96% Efficiency
- ♦ Two Low I_Q Linear Regulators
- ♦ Output Power-Up Sequencing
- ♦ Thermal-Overload Protection

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	PKG CODE
MAX8671XETL+	-40°C to +85°C	40 Thin QFN-EP* 5mm x 5mm	T4055-1

+Denotes a lead-free package.
**EP = Exposed paddle.*

Simplified Applications Circuit



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ABSOLUTE MAXIMUM RATINGS

USB, DC, PEN1 to AGND ....-0.3V to +16V
SYS, BAT, PV1, PV2, PV3 to AGND..........................-0.3V to +6V
PG1, PG2, PG3, AGND ....-0.3V to +0.3V
PV1, PV2, PV3 to SYS...-0.3V to +0.3V
VL to AGND ....-0.3V to +4.0V
CISET, DISET, BVSET, CT, THM to AGND ..-0.3V to (V_{VL} + 0.3V)
PV4, PV5, BP, FB1, FB2, FB3 to AGND ....-0.3V to (V_{SYS} + 0.3V)
PEN2, USUS, $\overline{\text{CEN}}$, EN, PWM to AGND ....-0.3V to +6V
CST1, CST2, $\overline{\text{DOK}}$, $\overline{\text{UOK}}$ to AGND ....-0.3V to +6V
OUT4, FB4 to AGND ....-0.3V to (V_{PV4} + 0.3V)
OUT5, FB5 to AGND ....-0.3V to (V_{PV5} + 0.3V)
LX1, LX2, LX3 Continuous RMS Current (Note 1).................1.5A
BAT Continuous Current 1.5A
SYS Continuous Current 1.5A
Continuous Power Dissipation (T_A = +70°C)
40-Pin, 5mm x 5mm, Thin QFN (derate 35.7mW/°C above +70°C)..2857mW
Operating Junction Temperature.....................................+150°C
Storage Junction Temperature Range ....-65°C to +150°C
Lead Temperature (soldering, 10s) ....+300°C

Note 1: LX_ has internal clamp diodes to PG_ and PV_. Applications that forward bias these diodes must take care not to exceed the package power dissipation limits.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(DC, USB, BVSET, $\overline{\text{UOK}}$, $\overline{\text{DOK}}$, LX_ unconnected; V_{THM} = V_L/2, $V_{PG\_}$ = V_{AGND} = 0V, V_{BAT} = 4V, $\overline{\text{CEN}}$ = low, USUS = low, EN = high, V_{PEN1} = V_{PEN2} = 3.3V, V_{PWM} = 0V, C_{OUT4} = 1µF, C_{OUT5} = 1µF, C_{SYS} = 10µF, PV1 = PV2 = PV3 = PV4 = PV5 = SYS, R_{DISET} = 3kΩ, R_{CISET} = 3kΩ, C_{VL} = 0.1µF, C_{CT} = 0.15µF, C_{BP} = 0.01µF, V_{FB1} = 1.1V, V_{FB2} = 1.1V, V_{FB3} = 1.1V, T_A = -40°C to +85°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC POWER INPUT (V_{DC} = 5.0V, EN = low)						
DC Voltage Range	V_{DC}	Operating voltage	4.1		6.6	V
		Withstand voltage	0		14	
SYS Regulation Voltage	V_{SYS_REG}	V_{DC} = 6V, USUS = low, $\overline{\text{CEN}}$ = high, system current is less than the input current limit	5.2	5.3	5.4	V
DC Undervoltage Threshold	V_{DCL}	V_{DC} rising, 500mV typical hysteresis	3.95	4.00	4.05	V
DC Overvoltage Threshold	V_{DCH}	V_{DC} rising, 400mV typical hysteresis	6.8	6.9	7.0	V
DC Current Limit	I_{DCLIM}	V_{DC} = 6V, V_{SYS} = 5V USB unconnected, $\overline{\text{CEN}}$ = low, T_A = +25°C, VL = no load (Note 3); PEN1 = low, PEN2 = low, USUS = low	90	95	100	mA
		PEN1 = low, PEN2 = high, USUS = low	450	475	500	
		PEN1 = high, R_{DISET} = 3kΩ	950	1000	1050	
R_{DISET} Resistance Range			3		6	kΩ
DC Quiescent Current	I_{DCIQ}	PEN1 = low, USUS = high		0.11		mA
		USUS = low, $\overline{\text{CEN}}$ = low; I_{SYS} = 0mA, I_{BAT} = 0mA, EN = low; VL no load		1.1		
		USUS = low, $\overline{\text{CEN}}$ = high; I_{SYS} = 0mA, V_{EN} = 0V, VL no load		0.7		
Minimum DC-to-BAT Voltage Headroom		V_{DC} falling, 200mV hysteresis	0	15	30	mV
Minimum DC-to-SYS Voltage Headroom		V_{DC} falling, 200mV hysteresis	0	15	30	mV
DC-to-SYS Dropout Resistance	R_{DS}	V_{DC} = 5V, I_{SYS} = 400mA, USUS = low		0.325	0.600	Ω

ELECTRICAL CHARACTERISTICS (continued)

(DC, USB, BVSET, $\overline{UOK}$, $\overline{DOK}$, LX_ unconnected; $V_{THM} = V_L/2$, $V_{PG\_} = V_{AGND}$ = 0V, V_{BAT} = 4V, $\overline{CEN}$ = low, USUS = low, EN = high, $V_{PEN1} = V_{PEN2}$ = 3.3V, V_{PWM} = 0V, C_{OUT4} = 1µF, C_{OUT5} = 1µF, C_{SYS} = 10µF, PV1 = PV2 = PV3 = PV4 = PV5 = SYS, R_{DISET} = 3kΩ, R_{CISET} = 3kΩ, C_{VL} = 0.1µF, C_{CT} = 0.15µF, C_{BP} = 0.01µF, V_{FB1} = 1.1V, V_{FB2} = 1.1V, V_{FB3} = 1.1V, T_A = -40°C to +85°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC-to-SYS Soft-Start Time	t_{SS-D-S}	Starting DC when no USB present		1.0		ms
		Starting DC with USB present		35		µs
DC Thermal-Limit Temperature		Die temperature at which current limit is reduced		+100		°C
DC Thermal-Limit Gain		Amount of input current reduction above thermal-limit temperature		5		%/°C
USB POWER INPUT (V_{USB} = 5.0V, EN = low)						
USB Voltage Range	V_{USB}	Operating voltage	4.1		6.6	V
		Withstand voltage	0		14	
SYS Regulation Voltage	V_{SYS_REG}	V_{USB} = 6V, USUS = low, $\overline{CEN}$ = high, system current is less than the input current limit	5.2	5.3	5.4	V
USB Undervoltage Threshold	V_{USBL}	V_{USB} rising, 500mV hysteresis	3.95	4.0	4.05	V
USB Overvoltage Threshold	V_{USBH}	V_{USB} rising, 400mV hysteresis	6.8	6.9	7.0	V
USB Current Limit	I_{USBLIM}	V_{USB} = 6V, V_{SYS} = 5V, DC unconnected, $\overline{CEN}$ = low, T_A = +25°C, I_{VL} = 0A (Note 3); PEN2 = low, USUS = low	90	95	100	mA
		V_{USB} = 6V, V_{SYS} = 5V, DC unconnected, $\overline{CEN}$ = low, T_A = +25°C, I_{VL} = 0A (Note 3); PEN2 = high, USUS = low	450	475	500	
USB Quiescent Current	I_{USBIQ}	USUS = high		0.11		mA
		USUS = low, $\overline{CEN}$ = low; I_{SYS} = 0mA, I_{BAT} = 0mA, VL no load		1.1	2.0	
		USUS = low, $\overline{CEN}$ = high; I_{SYS} = 0mA, VL no load		0.7	1.3	
Minimum USB-to-BAT Voltage Headroom		V_{USB} falling, 200mV hysteresis	0	15	30	mV
Minimum USB-to-SYS Voltage Headroom		V_{USB} falling, 200mV hysteresis	0	15	30	mV
USB-to-SYS Dropout Resistance	R_{US}	V_{USB} = 5V, I_{SYS} = 400mA, USUS = low		0.325	0.600	Ω
USB-to-SYS Soft-Start Time	t_{SS-U-S}			1.0		ms
USB Thermal-Limit Temperature		Die temperature at which current limit is reduced		100		°C
USB Thermal-Limit Gain		Amount of input current reduction above thermal-limit temperature		5		%/°C
SYSTEM (V_{DC} = 5.0V, EN = low)						
System Operating Voltage Range	V_{SYS}		2.6		5.5	V
System Undervoltage Threshold	V_{UVLO_SYS}	SYS falling, 100mV hysteresis	2.45	2.50	2.55	V

ELECTRICAL CHARACTERISTICS (continued)

(DC, USB, BVSET, $\overline{UOK}$, $\overline{DOK}$, LX_ unconnected; $V_{THM} = V_L/2$, $V_{PG\_} = V_{AGND} = 0V$, $V_{BAT} = 4V$, $\overline{CEN}$ = low, USUS = low, EN = high, $V_{PEN1} = V_{PEN2} = 3.3V$, $V_{PWM} = 0V$, $C_{OUT4} = 1\mu F$, $C_{OUT5} = 1\mu F$, $C_{SYS} = 10\mu F$, PV1 = PV2 = PV3 = PV4 = PV5 = SYS, $R_{DISET} = 3k\Omega$, $R_{CISET} = 3k\Omega$, $C_{VL} = 0.1\mu F$, $C_{CT} = 0.15\mu F$, $C_{BP} = 0.01\mu F$, $V_{FB1} = 1.1V$, $V_{FB2} = 1.1V$, $V_{FB3} = 1.1V$, T_A = -40°C to +85°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
BAT-to-SYS Reverse Regulation Voltage	V_{BSREG}	DC or USB and BAT are sourcing current	BAT is sourcing 105mA	65	82	115	mV
			BAT is sourcing 905mA		130		
Quiescent Current	I_{PV1} + I_{PV2} + I_{PV3} + I_{PV4} + I_{PV5} + I_{SYS}	DC and USB unconnected, EN = low, V_{BAT} = 4V			0	10	µA
		$V_{DC} = V_{USB}$ = 5V, USUS = high, PEN1 = low, EN = low, V_{BAT} = 4V			0	10	
		DC and USB unconnected, EN = high, V_{BAT} = 4V (step-down converters are not in dropout), PWM = low (Note 4)			155	285	
		DC and USB unconnected, EN = high, V_{BAT} = 2.8V (at least one step-down converter is in dropout), PWM = low (Note 4)			425	550	
		$V_{DC} = V_{USB}$ = 5V, USUS = high, EN = high, V_{BAT} = 4V, PWM = low (Note 4)			180	320	
		DC and USB unconnected, EN = high, V_{BAT} = 4.0V, PWM = high			9		mA
BATTERY CHARGER (V_{DC} = 5.0V, EN = low)							
BAT-to-SYS On-Resistance	R_{BS}	V_{USB} = 0V, V_{BAT} = 4.2V, I_{SYS} = 1A			0.08	0.16	Ω
BAT Regulation Voltage (Figure 6)	V_{BATREG}	BVSET = VL or BVSET unconnected	T_A = +25°C	4.174	4.200	4.221	V
			T_A = -40°C to +85°C	4.145	4.200	4.242	
		BVSET = AGND	T_A = +25°C	4.073	4.100	4.121	
			T_A = -40°C to +85°C	4.047	4.100	4.141	
		R_{BVSET} = 49.9kΩ to AGND	T_A = +25°C	4.325	4.350	4.376	
			T_A = -40°C to +85°C	4.297	4.350	4.398	
BAT Recharge Threshold	$V_{BATRCHG}$	(Note 5)		-170	-120	-70	mV
BAT Prequalification Threshold	V_{BATPRQ}	V_{BAT} rising, 180mV hysteresis, Figure 6		2.9	3.0	3.1	V
R_{CISET} Resistance Range		Guaranteed by BAT fast-charge current limit		3		15	kΩ
CISET Voltage	V_{CISET}	R_{CISET} = 7.5kΩ, I_{BAT} = 267mA, Figure 9		0.9	1.0	1.1	V

ELECTRICAL CHARACTERISTICS (continued)

(DC, USB, BVSET, $\overline{UOK}$, $\overline{DOK}$, LX_ unconnected; V_{THM} = V_L/2, $V_{PG\_}$ = V_{AGND} = 0V, V_{BAT} = 4V, $\overline{CEN}$ = low, USUS = low, EN = high, V_{PEN1} = V_{PEN2} = 3.3V, V_{PWM} = 0V, C_{OUT4} = 1µF, C_{OUT5} = 1µF, C_{SYS} = 10µF, PV1 = PV2 = PV3 = PV4 = PV5 = SYS, R_{DISET} = 3kΩ, R_{CISET} = 3kΩ, C_{VL} = 0.1µF, C_{CT} = 0.15µF, C_{BP} = 0.01µF, V_{FB1} = 1.1V, V_{FB2} = 1.1V, V_{FB3} = 1.1V, T_A = -40°C to +85°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
BAT Fast-Charge Current Limit		Low-power USB charging from the USB input, DC unconnected, R_{CISET} = 3kΩ, PEN2 = low, USUS = low	87	92	100	mA
		Low-power USB charging from the DC input, R_{CISET} = 3kΩ, PEN1 = low, PEN2 = low, USUS = low	87	92	100	
		High-power USB charging from the USB input, DC unconnected, R_{CISET} = 3kΩ, PEN2 = high, USUS = low	450	472	500	
		High-power USB charging from the DC input, R_{CISET} = 3kΩ, PEN2 = high, USUS = low	450	472	500	
		AC-to-DC adapter charging from the DC input, R_{DISET} = 3kΩ, R_{CISET} = 15kΩ, PEN1 = high	170	200	230	
		AC-to-DC adapter charging from the DC input, R_{DISET} = 3kΩ, R_{CISET} = 7.5kΩ, PEN1 = high	375	400	425	
		AC-to-DC adapter charging from the DC input, R_{DISET} = 3kΩ, R_{CISET} = 3.74kΩ, PEN1 = high	750	802	850	
BAT Prequalification Current		V_{BAT} = 2.5V, R_{CISET} = 3.74kΩ	65	82	100	mA
Top-Off Threshold		T_A = +25°C, R_{CISET} = 3.74kΩ (Note 6)	20	30	40	mA
BAT Leakage Current		EN = low, T_A = +25°C; No DC or USB power connected		0	+5	µA
		EN = low, T_A = +25°C; DC and/or USB power connected, $\overline{CEN}$ = high	-5	1	+5	
Charger Soft-Start Time	t_{SS_CHG}	Slew rate		450		mA/ms
		Time from 0mA to 500mA		1.10		ms
		Time from 0mA to 100mA		0.22		
		Time from 100mA to 500mA		0.88		
Timer Accuracy		C_{CT} = 0.15µF	-20		+20	%
Timer Suspend Threshold		CISET voltage when the fast-charge timer suspends; 300mV translates to 20% of the maximum fast-charge current limit	250	300	350	mV
Timer Extend Threshold		CISET voltage when the fast-charge timer suspends; 750mV translates to 50% of the maximum fast-charge current limit	700	750	800	mV

ELECTRICAL CHARACTERISTICS (continued)

(DC, USB, BVSET, $\overline{UOK}$, $\overline{DOK}$, LX_ unconnected; $V_{THM} = V_L/2$, $V_{PG\_} = V_{AGND}$ = 0V, V_{BAT} = 4V, $\overline{CEN}$ = low, USUS = low, EN = high, $V_{PEN1} = V_{PEN2}$ = 3.3V, V_{PWM} = 0V, C_{OUT4} = 1µF, C_{OUT5} = 1µF, C_{SYS} = 10µF, PV1 = PV2 = PV3 = PV4 = PV5 = SYS, R_{DISET} = 3kΩ, R_{CISET} = 3kΩ, C_{VL} = 0.1µF, C_{CT} = 0.15µF, C_{BP} = 0.01µF, V_{FB1} = 1.1V, V_{FB2} = 1.1V, V_{FB3} = 1.1V, T_A = -40°C to +85°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Prequalification Time	t_{PQ}	C_{CT} = 0.15µF			33		min
Fast-Charge Time	t_{FC}	C_{CT} = 0.15µF			660		min
Top-Off Time	t_{TO}				15		s
THERMISTOR INPUT (THM) (V_{DC} = 5.0V, EN = low)							
THM Threshold, Cold	V_{THMC}	V_{THM} rising, 65mV hysteresis		73.0	74.0	75.5	% of V_{VL}
THM Threshold, Hot	V_{THMH}	V_{THM} falling, 65mV hysteresis		27.0	28.4	30.0	% of V_{VL}
THM Input Leakage Current	I_{THM}	THM = AGND or VL, T_A = +25°C		-0.100	0.001	+0.200	µA
		THM = AGND or VL, T_A = +85°C			0.01		
POWER SEQUENCING (Figures 11 and 12)							
EN to REG3 Enable Delay	t_{D1}				120		µs
REG1 Soft-Start Time	t_{SS1}				2.6		ms
REG3 to REG1/2 Delay	t_{D2}				0.4		ms
REG2 Soft-Start Time	t_{SS2}				2.6		ms
REG3 Soft-Start Time	t_{SS3}				2.6		ms
REG1/2 to REG4 Delay	t_{D3}				0.3		ms
REG4 Soft-Start Time	t_{SS4}				3.0		ms
REG5 Soft-Start Time	t_{SS5}				3.0		ms
REGULATOR THERMAL SHUTDOWN							
Thermal Shutdown Temperature		T_J rising			+165		°C
Thermal Shutdown Hysteresis					15		°C
REG1—SYNCHRONOUS STEP-DOWN CONVERTER							
Input Voltage		PV1 supplied from SYS			V_{SYS}		V
Maximum Output Current		L = 4.7µH, R_L = 0.13Ω (Note 7)		425			mA
FB1 Voltage		(Note 8)		0.997	1.012	1.028	V
Adjustable Output Voltage Range				1		V_{SYS}	V
FB1 Leakage Current		V_{FB1} = 1.012V	T_A = +25°C	-50	-5	+50	nA
			T_A = +85°C		-5		
Load Regulation		PWM mode			4.4		%/A
Line Regulation		PWM mode (Note 9)			1		%/D
p-Channel On-Resistance		V_{PV1} = 4V, I_{LX1} = 180mA			165	330	mΩ
n-Channel On-Resistance		V_{PV1} = 4V, I_{LX1} = 180mA			200	400	mΩ
p-Channel Current-Limit Threshold				0.555	0.615	0.675	A

PMIC with Integrated Charger and Smart Power Selector for Handheld Devices

ELECTRICAL CHARACTERISTICS (continued)

(DC, USB, BVSET, $\overline{UOK}$, $\overline{DOK}$, LX_ unconnected; $V_{THM} = V_L/2$, $V_{PG\_} = V_{AGND} = 0V$, $V_{BAT} = 4V$, $\overline{CEN}$ = low, USUS = low, EN = high, $V_{PEN1} = V_{PEN2} = 3.3V$, $V_{PWM} = 0V$, $C_{OUT4} = 1µF$, $C_{OUT5} = 1µF$, $C_{SYS} = 10µF$, PV1 = PV2 = PV3 = PV4 = PV5 = SYS, $R_{DISET} = 3kΩ$, $R_{CISET} = 3kΩ$, $C_{VL} = 0.1µF$, $C_{CT} = 0.15µF$, $C_{BP} = 0.01µF$, $V_{FB1} = 1.1V$, $V_{FB2} = 1.1V$, $V_{FB3} = 1.1V$, $T_A = -40°C$ to $+85°C$, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Skip Mode Transition Current		(Note 10)			60		mA
n-Channel Zero-Crossing Threshold					10		mA
Maximum Duty Cycle					100		%
Minimum Duty Cycle		PWM mode			12.5		%
Internal Oscillator Frequency				1.8	2.0	2.2	MHz
Internal Discharge Resistance in Shutdown		EN = low, resistance from LX1 to PG1		0.5	1.0	2.0	kΩ
REG2—SYNCHRONOUS STEP-DOWN CONVERTER							
Input Voltage		PV2 supplied from SYS			V_{SYS}		V
Maximum Output Current		L = 4.7µH, R_L = 0.13Ω (Note 7)		425			mA
FB2 Voltage		(Note 8)		0.997	1.012	1.028	V
Adjustable Output Voltage Range				1		V_{SYS}	V
FB2 Leakage Current		V_{FB2} = 1.012V	T_A = +25°C	-50	-5	+50	nA
			T_A = +85°C		-50		
Load Regulation		PWM mode			4.4		%/A
Line Regulation		PWM mode (Note 9)			1		%/D
p-Channel On-Resistance		V_{PV2} = 4V, I_{LX2} = 180mA			200	400	mΩ
n-Channel On-Resistance		V_{PV2} = 4V, I_{LX2} = 180mA			150	265	mΩ
p-Channel Current-Limit Threshold				0.555	0.615	0.675	A
Skip Mode Transition Current		(Note 10)			60		mA
n-Channel Zero-Crossing Threshold					10		mA
Maximum Duty Cycle					100		%
Minimum Duty Cycle		PWM mode			12.5		%
Internal Oscillator Frequency				1.8	2.0	2.2	MHz
Internal Discharge Resistance in Shutdown		EN = low, resistance from LX2 to PG2		0.5	1.0	2.0	kΩ
REG3—SYNCHRONOUS STEP-DOWN CONVERTER							
Input Voltage		PV3 supplied from SYS			V_{SYS}		V
Maximum Output Current		L = 4.7µH, R_L = 0.13Ω (Note 7)		425			mA
FB3 Voltage		(Note 8)		0.997	1.012	1.028	V
Adjustable Output Voltage Range				1		V_{SYS}	V
FB3 Leakage Current		V_{FB2} = 1.012V	T_A = +25°C	-50	-5	+50	nA
			T_A = +85°C		-50		
Load Regulation		PWM mode			4.4		%/A

ELECTRICAL CHARACTERISTICS (continued)

(DC, USB, BVSET, $\overline{UOK}$, $\overline{DOK}$, LX_ unconnected; $V_{THM} = V_L/2$, $V_{PG\_} = V_{AGND} = 0V$, $V_{BAT} = 4V$, $\overline{CEN}$ = low, USUS = low, EN = high, $V_{PEN1} = V_{PEN2} = 3.3V$, $V_{PWM} = 0V$, $C_{OUT4} = 1\mu F$, $C_{OUT5} = 1\mu F$, $C_{SYS} = 10\mu F$, PV1 = PV2 = PV3 = PV4 = PV5 = SYS, $R_{DISET} = 3k\Omega$, $R_{CISET} = 3k\Omega$, $C_{VL} = 0.1\mu F$, $C_{CT} = 0.15\mu F$, $C_{BP} = 0.01\mu F$, $V_{FB1} = 1.1V$, $V_{FB2} = 1.1V$, $V_{FB3} = 1.1V$, T_A = -40°C to +85°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Line Regulation		PWM mode (Note 9)		1		%/D
p-Channel Current-Limit Threshold			0.555	0.615	0.675	A
Skip Mode Transition Current		(Note 10)		60		mA
n-Channel Zero-Crossing Threshold				10		mA
p-Channel On-Resistance		$V_{PV3} = 4V$, $I_{LX3} = 180mA$		230	460	mΩ
n-Channel On-Resistance		$V_{PV3} = 4V$, $I_{LX3} = 180mA$		120	210	mΩ
Maximum Duty Cycle				100		%
Minimum Duty Cycle		PWM mode		12.5		%
Internal Oscillator Frequency			1.8	2.0	2.2	MHz
Internal Discharge Resistance in Shutdown		EN = low, resistance from LX3 to PG3	0.5	1.0	2.0	kΩ
REG4—LINEAR REGULATOR						
PV4 Operating Range	V_{PV4}		1.7		V_{SYS}	V
PV4 Undervoltage Lockout Threshold		V_{PV4} rising, 100mV hysteresis	1.55	1.60	1.65	V
FB4 Voltage		No load	0.582	0.600	0.618	V
FB4 Leakage Current		$V_{FB4} = 0.6V$, $T_A = +25°C$	-50	-5	+50	nA
		$V_{FB4} = 0.6V$, $T_A = +85°C$		-5		
Drop-Out Resistance		PV4 to OUT4, $V_{PV4} = 3.3V$		0.45		Ω
		PV4 to OUT4, $V_{PV4} = 2.0V$		0.75	1.8	
Current Limit		$V_{FB4} = 0.54V$	200	230	265	mA
		$V_{FB4} = 0V$		235		
Output Noise		10Hz to 100kHz; $C_{OUT4} = 3.3\mu F$, $I_{OUT4} = 10mA$, $V_{PV4} = 2V$, V_{OUT4} set for 1.8V		120		μV_{RMS}
PSRR		f = 1kHz, $I_{OUT4} = 10mA$, $V_{PV4} = 2V$, V_{OUT4} set for 1.8V		67		dB
		f = 10kHz, $I_{OUT4} = 10mA$, $V_{PV4} = 2V$, V_{OUT4} set for 1.8V		50		
Internal Discharge Resistance in Shutdown		EN = low, resistance from OUT4 to AGND	0.5	1.0	2.0	kΩ

PMIC with Integrated Charger and Smart Power Selector for Handheld Devices

ELECTRICAL CHARACTERISTICS (continued)

(DC, USB, BVSET, $\overline{UOK}$, $\overline{DOK}$, LX_ unconnected; V_{THM} = V_L/2, $V_{PG\_}$ = V_{AGND} = 0V, V_{BAT} = 4V, $\overline{CEN}$ = low, USUS = low, EN = high, V_{PEN1} = V_{PEN2} = 3.3V, V_{PWM} = 0V, C_{OUT4} = 1µF, C_{OUT5} = 1µF, C_{SYS} = 10µF, PV1 = PV2 = PV3 = PV4 = PV5 = SYS, R_{DISET} = 3kΩ, R_{CISET} = 3kΩ, C_{VL} = 0.1µF, C_{CT} = 0.15µF, C_{BP} = 0.01µF, V_{FB1} = 1.1V, V_{FB2} = 1.1V, V_{FB3} = 1.1V, T_A = -40°C to +85°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
REG5—LINEAR REGULATOR							
PV5 Operating Range	V_{PV5}			1.7		V_{SYS}	V
PV5 Undervoltage Lockout Threshold		V_{PV5} rising, 100mV hysteresis		1.55	1.60	1.65	V
FB5 Voltage		No load		0.582	0.600	0.618	V
FB5 Leakage Current		V_{FB5} = 0.6V	T_A = +25°C	-50	-5	+50	nA
			T_A = +85°C		-5		
Drop-Out Resistance		V_{PV5} to OUT5, V_{PV5} = 3.3V			0.45		Ω
		V_{PV5} to OUT5, V_{PV5} = 2.0V			0.75	1.8	
Current Limit		V_{FB5} = 0.54V		200	230	265	mA
		V_{FB5} = 0V			235		
Output Noise		10Hz to 100kHz, C_{OUT5} = 2.2µF, I_{OUT5} = 10mA, V_{PV5} = 3.5V, V_{OUT5} set for 3.3V			180		$µV_{RMS}$
PSRR		f = 1kHz, I_{OUT5} = 10mA, V_{PV5} = 3.5V, V_{OUT5} set for 3.3V			62		dB
		f = 10kHz, I_{OUT5} = 10mA, V_{PV5} = 3.5V, V_{OUT5} set for 3.3V			44		
Internal Discharge Resistance in Shutdown		EN = low, resistance from OUT5 to AGND		0.5	1.0	2.0	kΩ
VL—LINEAR REGULATOR							
VL Voltage	V_{VL}	I_{VL} = 0mA to 3mA		3.0	3.3	3.6	V
LOGIC ($\overline{UOK}$, $\overline{DOK}$, PEN1, PEN2, USUS, $\overline{CEN}$, CST1, CST2, EN, PWM)							
Logic Input-Voltage Low		V_{USB} or V_{DC} = 4.1V to 6.6V, V_{SYS} = 2.6V to 5.5V				0.6	V
Logic Input-Voltage High		V_{USB} or V_{DC} = 4.1V to 6.6V, V_{SYS} = 2.6V to 5.5V		1.3			V
Logic Input Leakage Current		V_{LOGIC} = 0V to 5.5V	T_A = +25°C		0.001	1	µA
			T_A = +85°C		0.01		
Logic Output-Voltage Low		I_{SINK} = 1mA			10	30	mV
Logic Output-High Leakage Current		V_{LOGIC} = 5.5V	T_A = +25°C		0.001	1	µA
			T_A = +85°C		0.01		
TRI-STATE INPUT (BVSET)							
BVSET Input-Voltage Low		V_{USB} or V_{DC} = 4.1V to 6.6V				0.3	V
BVSET Input-Voltage Mid		V_{USB} or V_{DC} = 4.1V to 6.6V		1.2		V_{VL} - 1.2	V

PMIC with Integrated Charger and Smart Power Selector for Handheld Devices

ELECTRICAL CHARACTERISTICS (continued)

(DC, USB, BVSET, $\overline{UOK}$, $\overline{DOK}$, LX_ unconnected; $V_{THM} = V_L/2$, $V_{PG\_} = V_{AGND} = 0V$, $V_{BAT} = 4V$, $\overline{CEN}$ = low, USUS = low, EN = high, $V_{PEN1} = V_{PEN2} = 3.3V$, $V_{PWM} = 0V$, $C_{OUT4} = 1µF$, $C_{OUT5} = 1µF$, $C_{SYS} = 10µF$, PV1 = PV2 = PV3 = PV4 = PV5 = SYS, $R_{DISET} = 3kΩ$, $R_{CISET} = 3kΩ$, $C_{VL} = 0.1µF$, $C_{CT} = 0.15µF$, $C_{BP} = 0.01µF$, $V_{FB1} = 1.1V$, $V_{FB2} = 1.1V$, $V_{FB3} = 1.1V$, T_A = -40°C to +85°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
BVSET Input-Voltage High		V_{USB} or V_{DC} = 4.1V to 6.6V	V_{VL} - 0.3		V_{VL} + 0.3	V
Internal BVSET Pullup Resistance				52.5		kΩ
External BVSET Pulldown Resistance for Midrange Voltage	R_{BVSET}		45	50	55	kΩ

Note 2: Limits are 100% production tested at T_A = +25°C. Limits over the operating temperature range are guaranteed through correlation using statistical quality control (SQC) methods.

Note 3: The USB/DC current limit does not include the VL output current. See the *VL Linear Regulator* section for more information.

Note 4: Quiescent current excludes the energy needed for the REG1–REG5 external resistor-dividers. All typical operating characteristics include the energy for the REG1–REG5 external resistor-dividers. For the circuit of Figure 1, the typical quiescent current with DC and USB unconnected, EN = high, V_{BAT} = 4V, and PWM = low is 175µA.

Note 5: The charger transitions from done to fast-charge mode at this BAT recharge threshold (Figure 7).

Note 6: The charger transitions from fast-charge to top-off mode at this top-off threshold (Figure 7).

Note 7: The maximum output current is guaranteed by correlation to the p-channel current-limit threshold, p-channel on-resistance, n-channel on-resistance, oscillator frequency, input voltage range, and output voltage range. The parameter is stated for a 4.7µH inductor with 0.13Ω series resistance. See the *Step-Down Converter Output Current* section for more information.

Note 8: The step-down output voltages are 1% high with no load due to the load-line architecture. When calculating the external resistor-dividers, use an FB_ voltage of 1.000V.

Note 9: Line regulation for the step-down converters is measured as $\Delta V_{OUT}/\Delta D$, where D is the duty cycle (approximately V_{OUT}/V_{IN}).

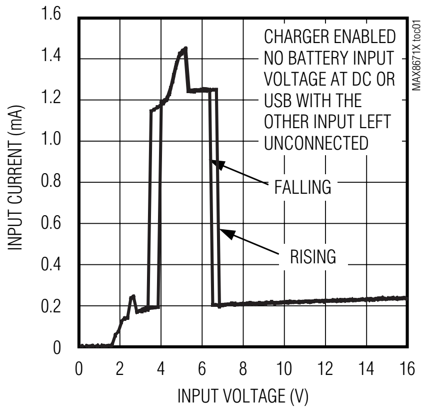
Note 10: The skip mode current threshold is the transition point between fixed-frequency PWM operation and skip mode operation. The specification is given in terms of output load current for inductor values shown in the typical application circuits.

PMIC with Integrated Charger and Smart Power Selector for Handheld Devices

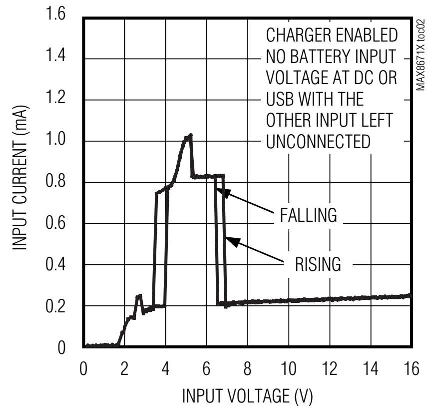
Typical Operating Characteristics

(Circuit of Figure 1, I_{VL} = 0mA, T_A = +25°C, unless otherwise noted.)

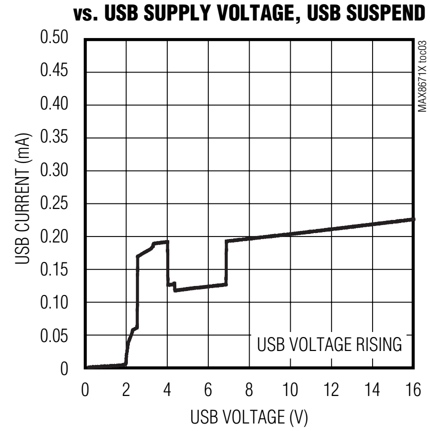
QUIESCENT CURRENT vs. DC OR USB SUPPLY VOLTAGE



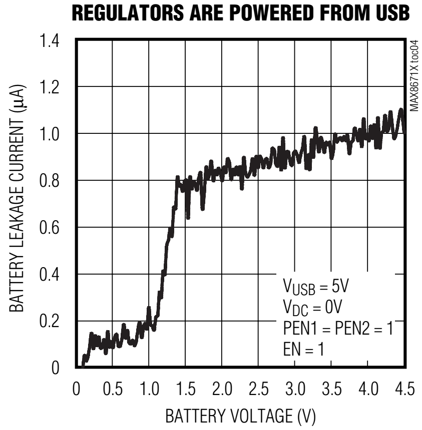
QUIESCENT CURRENT vs. DC OR USB SUPPLY VOLTAGE



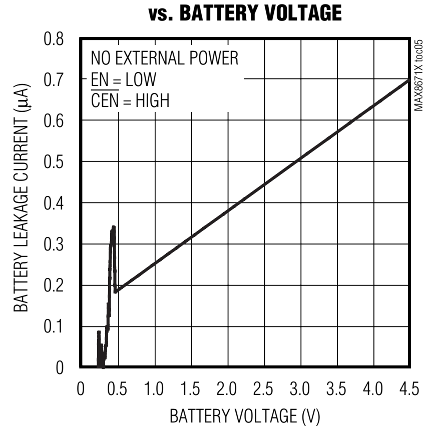
USB QUIESCENT CURRENT vs. USB SUPPLY VOLTAGE, USB SUSPEND



BATTERY LEAKAGE CURRENT vs. BATTERY VOLTAGE WHEN REGULATORS ARE POWERED FROM USB



BATTERY LEAKAGE CURRENT vs. BATTERY VOLTAGE

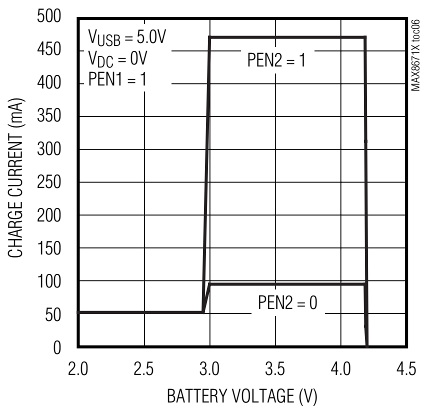


PMIC with Integrated Charger and Smart Power Selector for Handheld Devices

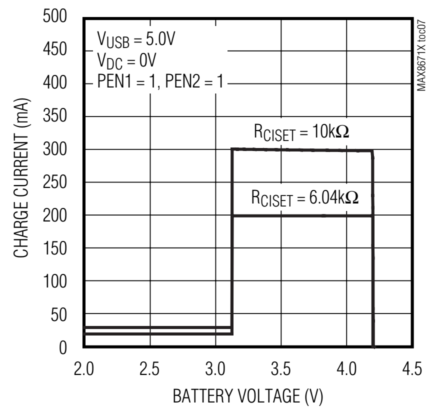
Typical Operating Characteristics (continued)

(Circuit of Figure 1, I_{VL} = 0mA, T_A = +25°C, unless otherwise noted.)

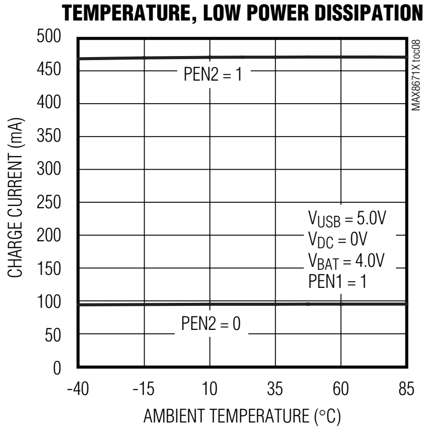
CHARGE CURRENT vs. BATTERY VOLTAGE WITH USB INPUT



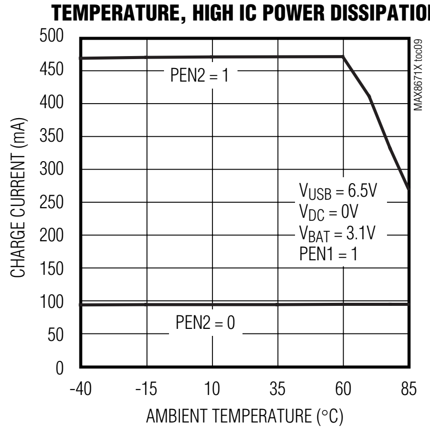
CHARGE CURRENT vs. BATTERY VOLTAGE



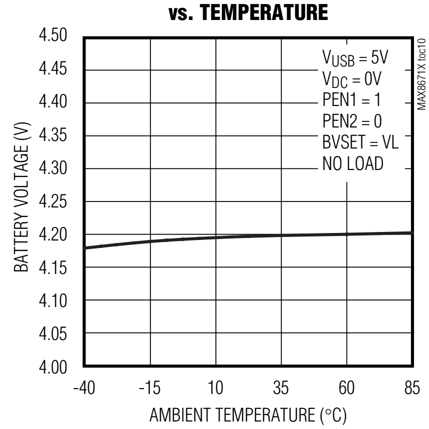
CHARGE CURRENT vs. AMBIENT TEMPERATURE, LOW POWER DISSIPATION



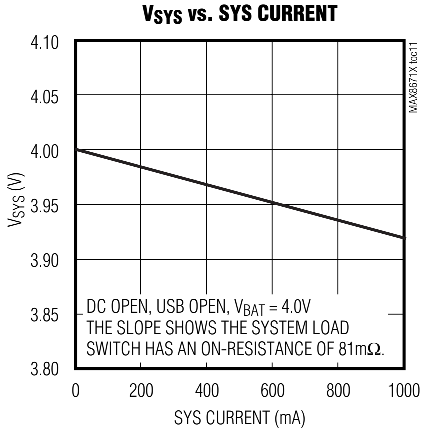
CHARGE CURRENT vs. AMBIENT TEMPERATURE, HIGH IC POWER DISSIPATION



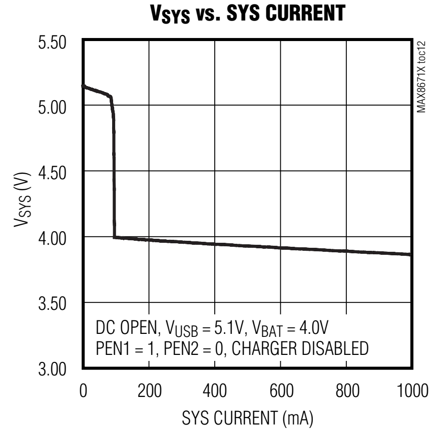
BATTERY REGULATION VOLTAGE vs. TEMPERATURE



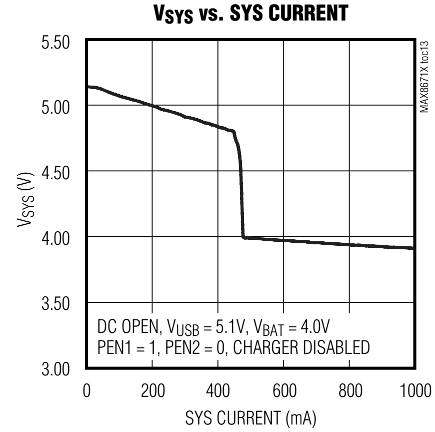
V_{SYS} vs. SYS CURRENT



V_{SYS} vs. SYS CURRENT

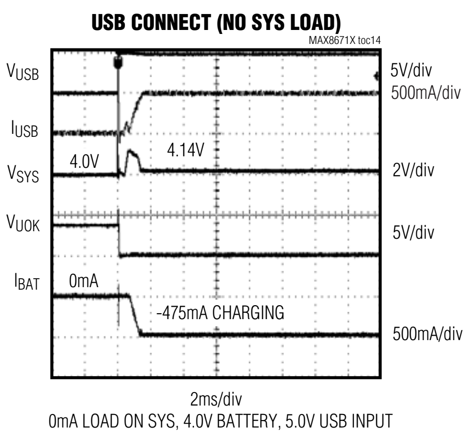


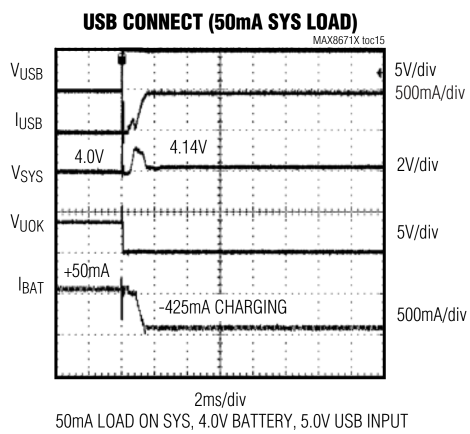
V_{SYS} vs. SYS CURRENT

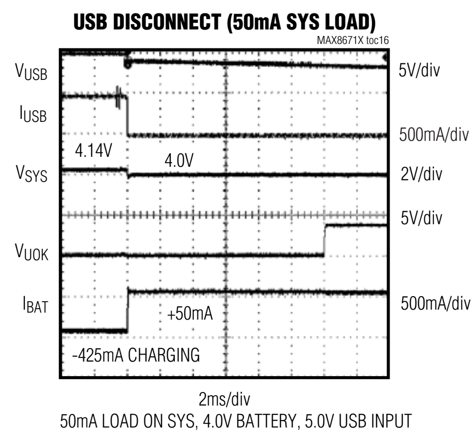


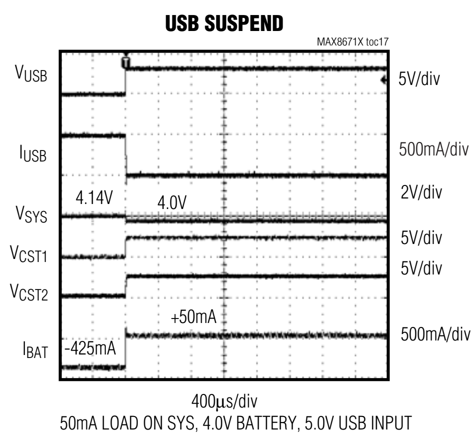
Typical Operating Characteristics (continued)

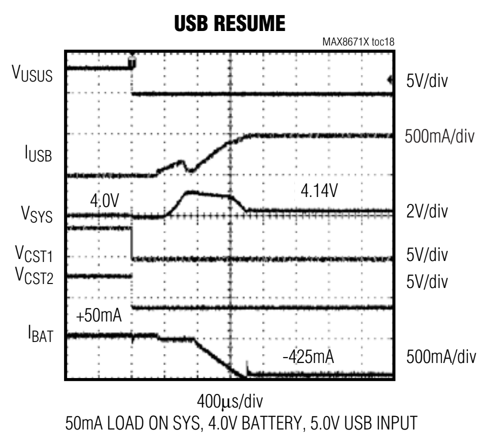
(Circuit of Figure 1, I_{VL} = 0mA, T_A = +25°C, unless otherwise noted.)









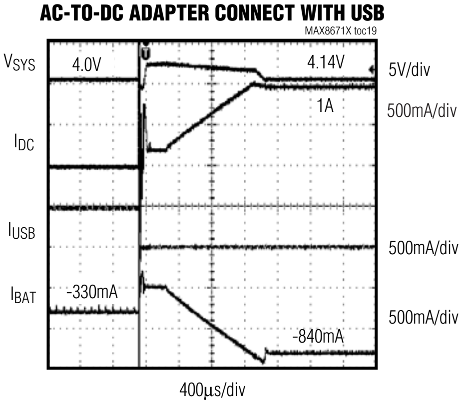


PMIC with Integrated Charger and Smart Power Selector for Handheld Devices

Typical Operating Characteristics (continued)

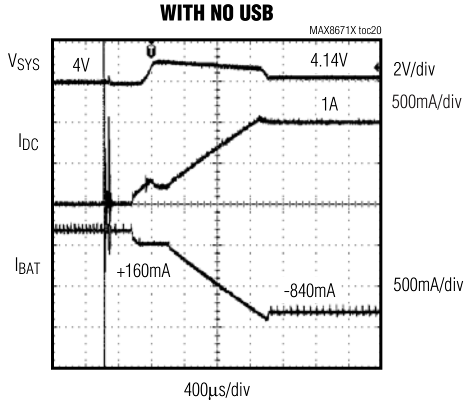
(Circuit of Figure 1, I_{VL} = 0mA, T_A = +25°C, unless otherwise noted.)

AC-TO-DC ADAPTER CONNECT WITH USB



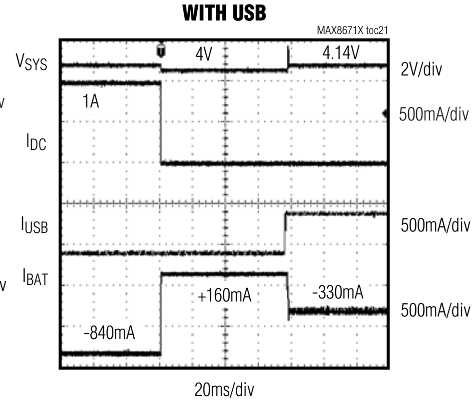
25Ω LOAD ON SYS, PEN1 = PEN2 = HIGH 1A DC LIMIT, R_{DISET} = 3.01kΩ

AC-TO-DC ADAPTER CONNECT WITH NO USB



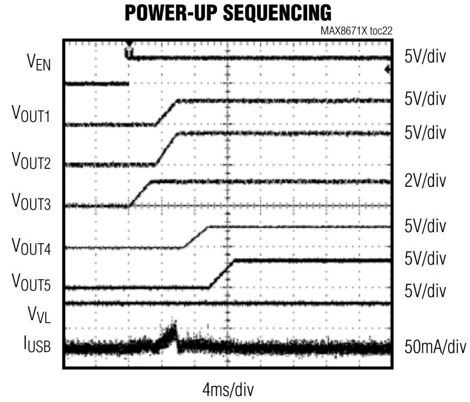
25Ω LOAD ON SYS, PEN1 = PEN2 = HIGH 1A DC LIMIT

AC-TO-DC ADAPTER DISCONNECT WITH USB



25Ω LOAD ON SYS, PEN1 = PEN2 = HIGH 1A DC LIMIT

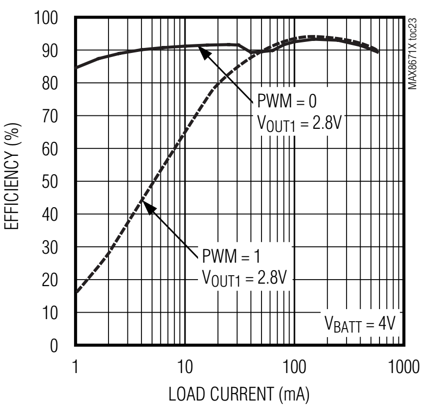
POWER-UP SEQUENCING



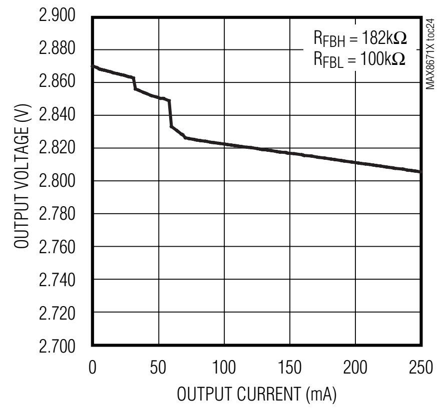
Typical Operating Characteristics (continued)

(Circuit of Figure 1, I_{VL} = 0mA, T_A = +25°C, unless otherwise noted.)

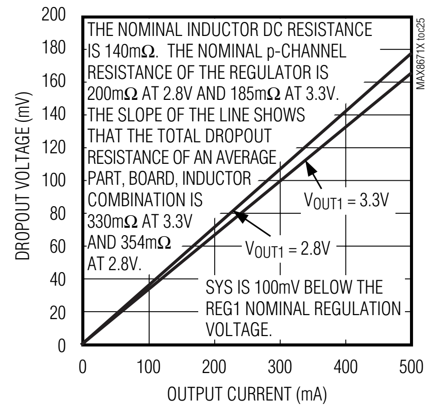
REG1 EFFICIENCY vs. LOAD CURRENT



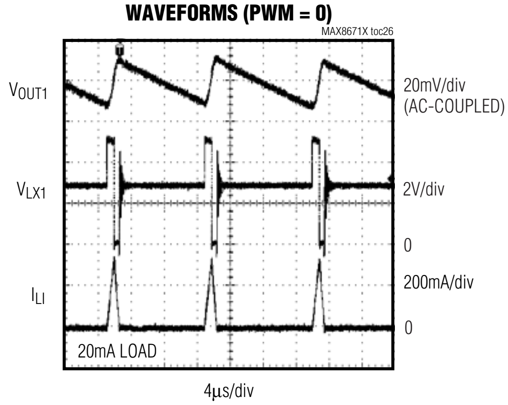
REG1 LOAD REGULATION



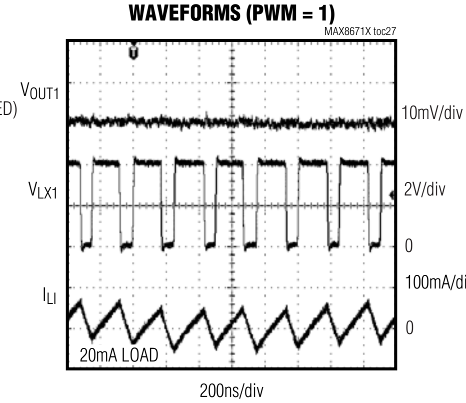
REG1 DROPOUT VOLTAGE vs. LOAD CURRENT



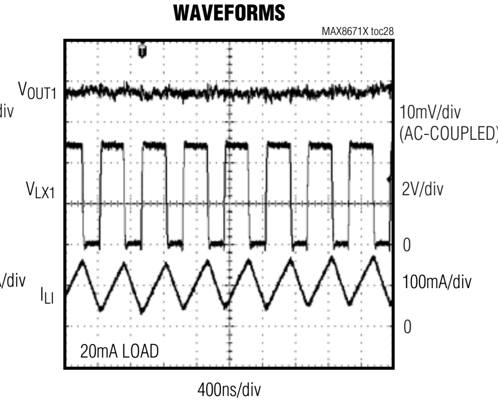
REG1 LIGHT-LOAD SWITCHING WAVEFORMS (PWM = 0)



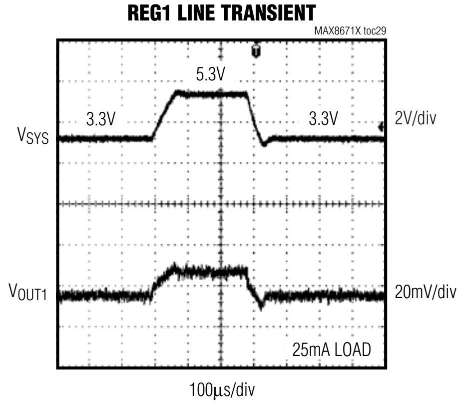
REG1 LIGHT-LOAD SWITCHING WAVEFORMS (PWM = 1)



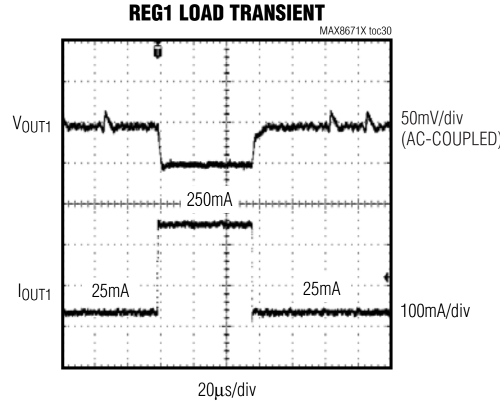
REG1 HEAVY-LOAD SWITCHING WAVEFORMS



REG1 LINE TRANSIENT



REG1 LOAD TRANSIENT

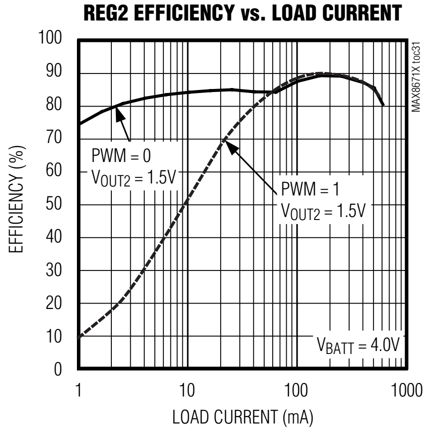


PMIC with Integrated Charger and Smart Power Selector for Handheld Devices

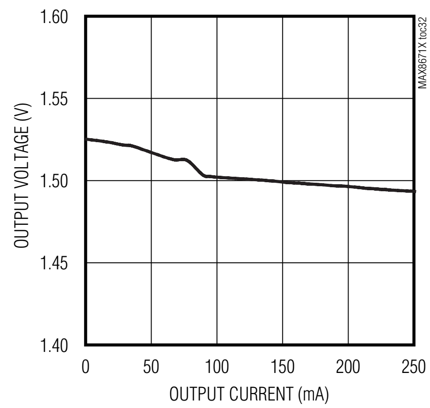
Typical Operating Characteristics (continued)

(Circuit of Figure 1, I_{VL} = 0mA, T_A = +25°C, unless otherwise noted.)

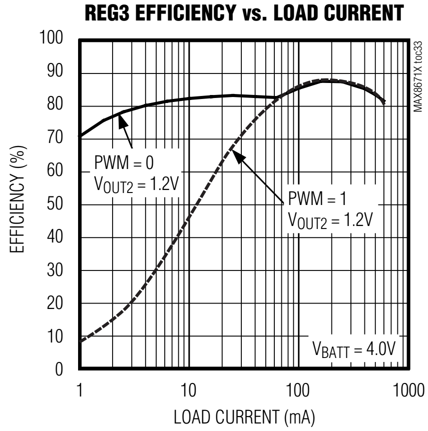
REG2 EFFICIENCY vs. LOAD CURRENT



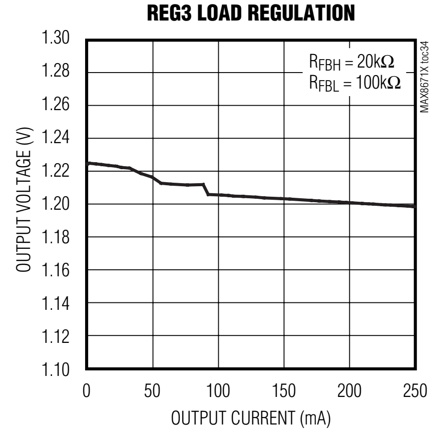
REG2 LOAD REGULATION



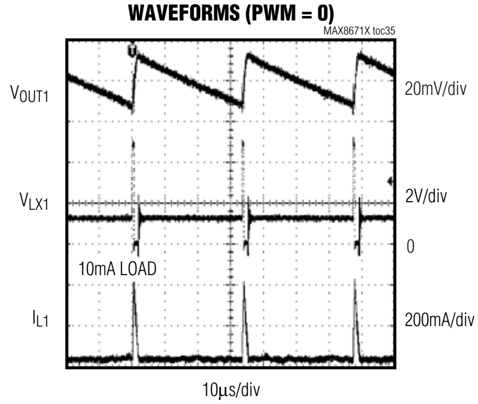
REG3 EFFICIENCY vs. LOAD CURRENT



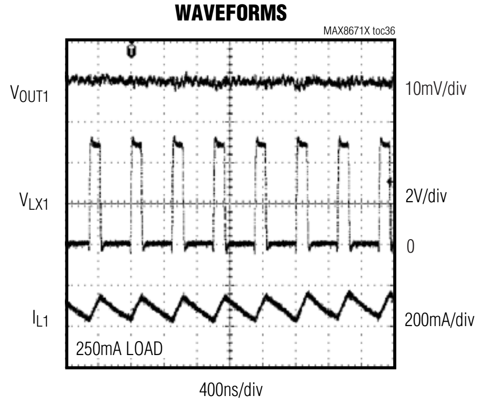
REG3 LOAD REGULATION



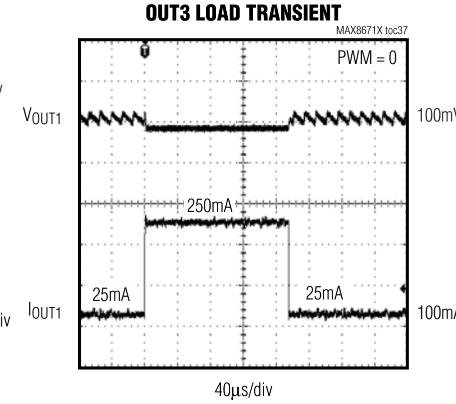
OUT3 LIGHT-LOAD SWITCHING WAVEFORMS (PWM = 0)



OUT3 HEAVY-LOAD SWITCHING WAVEFORMS



OUT3 LOAD TRANSIENT



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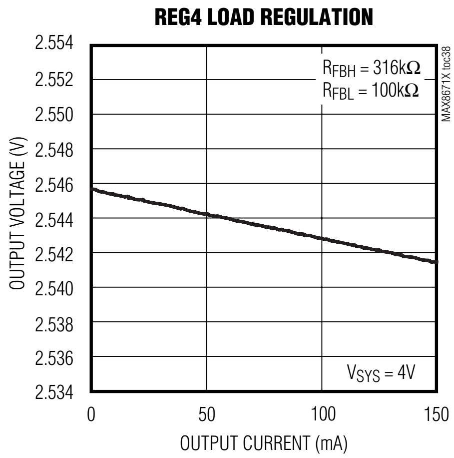
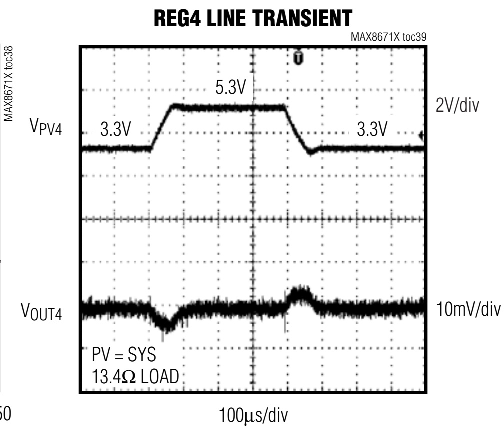
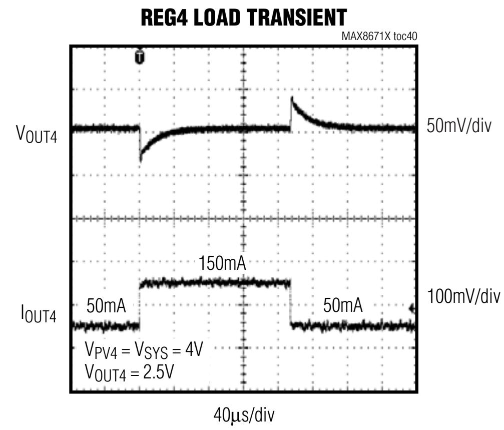
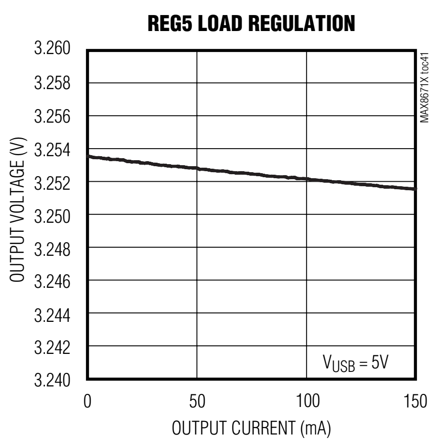
Typical Operating Characteristics (continued)

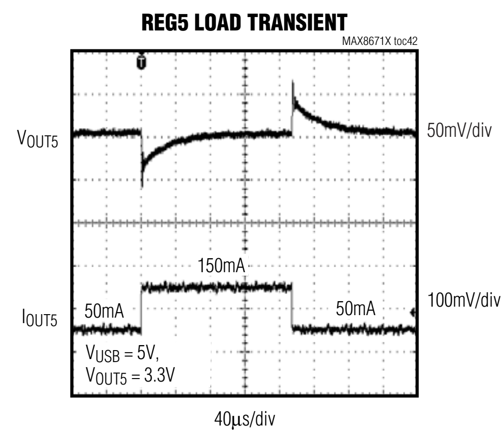
(Circuit of Figure 1, I_{VL} = 0mA, T_A = +25°C, unless otherwise noted.)











PMIC with Integrated Charger and Smart Power Selector for Handheld Devices

Pin Description

PIN	NAME	FUNCTION
1	USUS	USB Suspend Digital Input. As shown in Table 1, driving USUS high suspends the DC or USB inputs if they are configured as a USB power input.
2	DC	DC Power Input. DC is capable of delivering 1A to SYS. DC supports both AC adaptors and USB inputs. As shown in Table 1, the DC current limit is controlled by PEN1, PEN2, USUS, and R_{DISET}.
3	USB	USB Power Input. USB is capable of delivering 0.5A to SYS. As shown in Table 1, the USB current limit is controlled by PEN1, PEN2, and USUS.
4	FB5	Feedback Input for REG5. Connect FB5 to the center of a resistor voltage-divider from OUT5 to AGND to set the REG5 output voltage from 0.6V to V_{PV5}.
5	PV5	Power Input for REG5. Connect PV5 to SYS, or a supply between 1.7V and V_{SYS}. Bypass PV5 to power ground with a 1µF ceramic capacitor.
6	OUT5	Linear Regulator Power Output. OUT5 is internally pulled to AGND by 1kΩ in shutdown.
7	PG2	Power Ground for the REG2 Step-Down Regulator
8	LX2	Inductor Switching Node for REG2. LX2 is internally pulled to PG2 by 1kΩ in shutdown.
9	PV2	Power Input for the REG2 Step-Down Regulator. Connect PV2 to SYS. Bypass PV2 to PG2 with a 4.7µF ceramic capacitor.
10	$\overline{CEN}$	Active-Low Charger Enable Input. Pull $\overline{CEN}$ low to enable the charger, or drive $\overline{CEN}$ high to disable charging. The battery charger is also disabled when USUS is high.
11	FB2	Feedback Input for REG2. Connect FB2 to the center of a resistor voltage-divider from the REG2 output capacitors to AGND to set the output voltage from 1V to V_{SYS}.
12	$\overline{DOK}$	Active-Low, Open-Drain DC Power-OK Output. $\overline{DOK}$ is low when V_{DC} is within its valid operating range.
13	FB4	Feedback Input for REG4. Connect FB4 to the center of a resistor voltage-divider from the REG4 output capacitors to AGND to set the output voltage from 0.6V to V_{PV4}.
14	BP	Reference Noise Bypass. Bypass BP with a low-leakage 0.01µF ceramic capacitor for reduced noise on the LDO outputs.
15	OUT4	Linear Regulator Power Output. OUT4 is internally pulled to AGND in shutdown.
16	PV4	Power Input for REG4. Connect PV4 to SYS, or a supply between 1.7V and V_{SYS}. Bypass PV4 to power ground with a 1µF ceramic capacitor.
17	BVSET	Battery Regulation Voltage Set Node. Drive BVSET low to set the regulation voltage to 4.1V. Connect BVSET to VL or leave unconnected to set the regulation voltage to 4.2V. Connect BVSET to AGND through a 50kΩ resistor to set the regulation voltage to 4.350V.
18	AGND	Ground. AGND is the low-noise ground connection for the internal circuitry.
19	FB1	Feedback Input for REG1. Connect FB1 to the center of a resistor voltage-divider from the REG1 output capacitors to AGND to set the output voltage from 1V to V_{SYS}.
20	EN	Regulator Enable Input. Drive EN high to enable all regulator outputs. The sequencing is shown in Figure 11. Drive EN low to disable the regulators.
21	PWM	Forced-PWM Input. Connect PWM high for forced-PWM operation on REG1, REG2, and REG3. Connect PWM low for auto PWM operation. **Do not change PWM on-the-fly.** See the *PWM* section for more information.
22	PV1	Power Input for the REG1 Step-Down Regulator. Connect PV1 to SYS. Bypass PV1 to PG1 with a 4.7µF ceramic capacitor.

Pin Description (continued)

PIN	NAME	FUNCTION
23	LX1	Inductor Switching Node for REG1. LX1 is internally pulled to PG1 by 1kΩ in shutdown.
24	PG1	Power Ground for the REG1 Step-Down Regulator
25	PG3	Power Ground for the REG3 Step-Down Regulator
26	LX3	Inductor Switching Node for REG3. LX3 is internally pulled to PG3 by 1kΩ in shutdown.
27	PV3	Power Input for the REG3 Step-Down Regulator. Connect PV3 to SYS. Bypass PV3 to PG3 with a 4.7µF ceramic capacitor.
28	VL	IC Supply Output. VL is an LDO output that powers the MAX8671X internal battery-charger circuitry. VL provides 3.3V at 3mA to power external circuitry when DC or USB is present. Connect a 0.1µF capacitor from VL to AGND.
29	FB3	Feedback Input for REG3. Connect FB3 to the center of a resistor voltage-divider from the REG3 output capacitors to AGND to set the output voltage from 1V to V_{SYS}.
30	DISET	DC Input Current-Limit Select Input. Connect a resistor from DISET to AGND (R_{DISET}) to set the DC current limit. See Table 2 for more information.
31	CISET	Charge Rate Select Input. Connect a resistor from CISET to AGND (R_{CISET}) to set the fast-charge current limit, prequalification-charge current limit, and top-off threshold.
32	CT	Charge Timer Programming Node. Connect a capacitor from CT to AGND (C_{CT}) to set the time required for a fault to occur in fast-charge or prequalification modes. Connect CT to AGND to disable the fast-charge and prequalification timers.
33	THM	Thermistor Input. Connect a negative temperature coefficient (NTC) thermistor that has a good thermal contact with the battery from THM to AGND. Connect a resistor equal to the thermistor resistance at +25°C from THM to VL. Charging is suspended when the battery is outside the hot or cold limits.
34	BAT	Positive Battery Terminal Connection. Connect BAT to the positive terminal of a single-cell Li+/Li-Poly battery.
35	SYS	System Supply Output. Bypass SYS to power ground with a 10µF ceramic capacitor. When a valid voltage is present at USB or DC and not suspended (USUS = low), SYS is limited to 5.3V ($V_{SYS-REG}$). When the system load (I_{SYS}) exceeds the input current limit, SYS drops below V_{BAT} by V_{BSREG} allowing both the external power source and the battery service SYS. SYS is connected to BAT through an internal system load switch (R_{BS}) when a valid source is not present at USB or DC.
36	PEN1	Input Current-Limit Control 1. See Table 1 for more information.
37	CST2	Open-Drain Charger Status Output 2. CST1 and CST2 indicate four different charger states. See Table 3 for more information.
38	$\overline{UOK}$	Active-Low, Open-Drain USB Power-OK Output. $\overline{UOK}$ is low when V_{USB} is within its valid operating range.
39	CST1	Open-Drain Charger Status Output 1. CST1 and CST2 indicate four different charger states. See Table 3 for more information.
40	PEN2	Input Current-Limit Control 2. See Table 1 for more information.
—	EP	Exposed Paddle. Connect the exposed paddle to AGND. Connecting the exposed paddle does not remove the requirement for proper ground connections to AGND, PG1, PG2, and PG3.

PMIC with Integrated Charger and Smart Power Selector for Handheld Devices

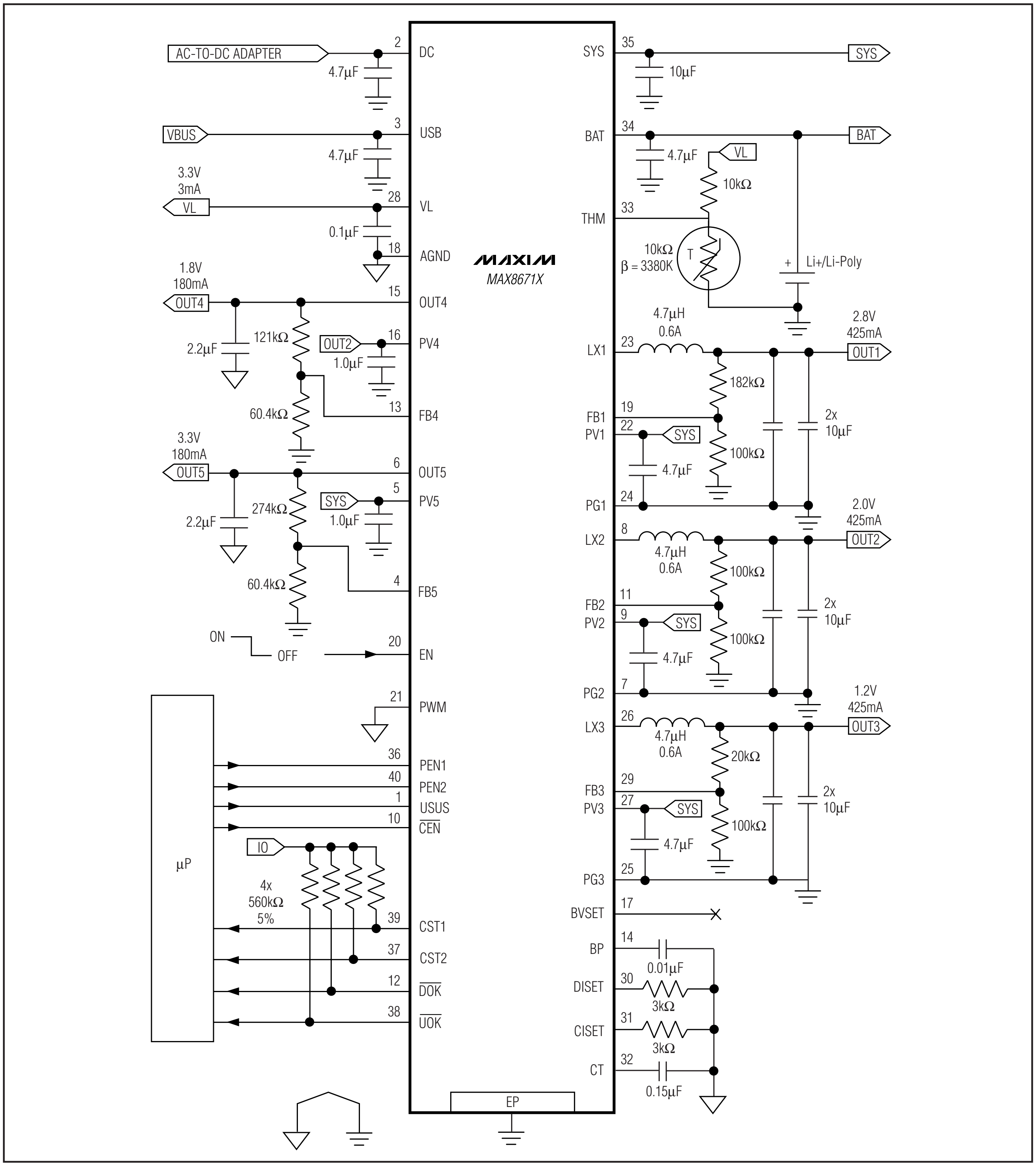


Figure 1. MAX8671X Typical Application Circuit

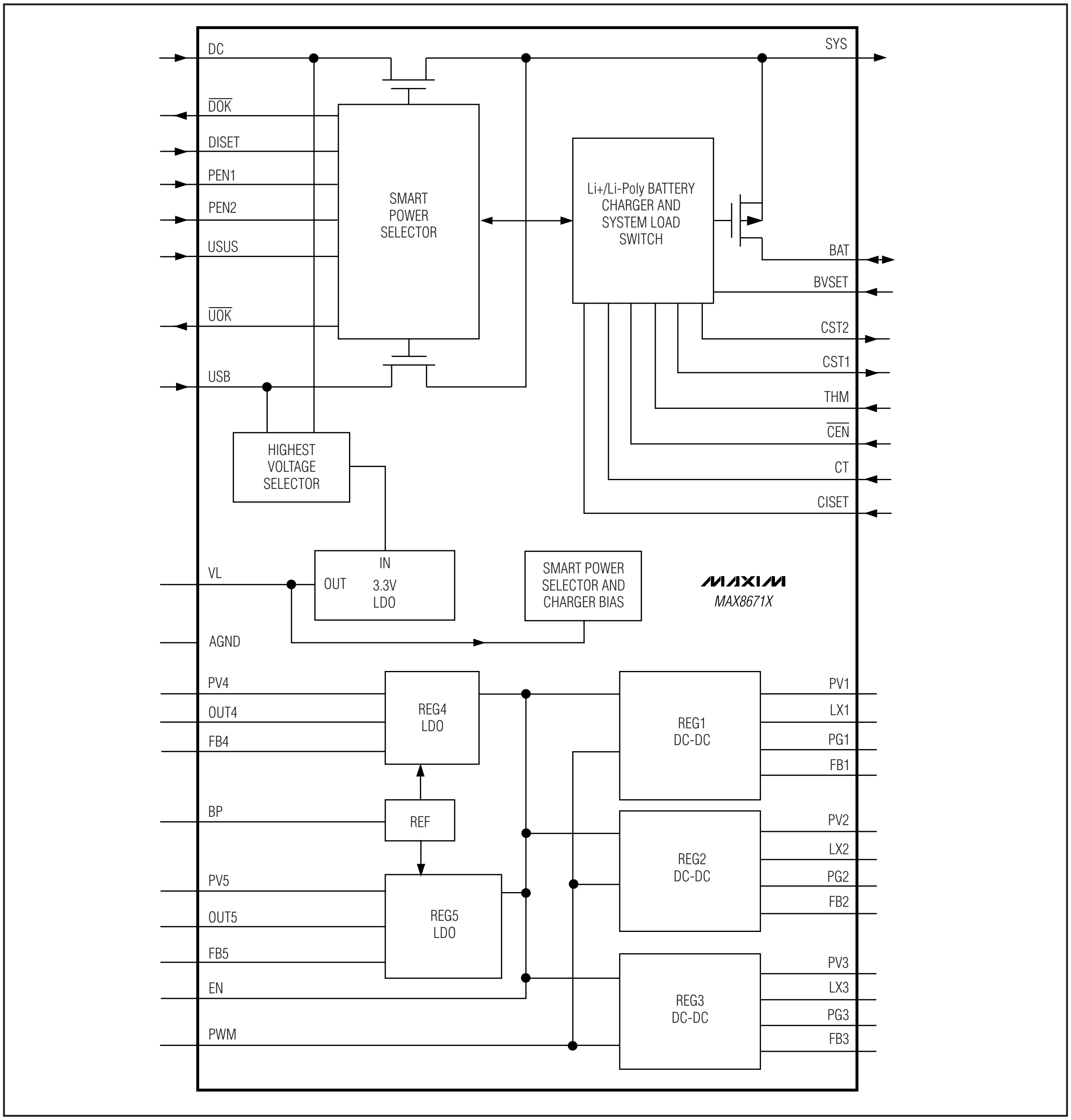


Figure 2. Functional Diagram

PMIC with Integrated Charger and Smart Power Selector for Handheld Devices

Detailed Description

The MAX8671X highly integrated PMIC is ideally suited for use in portable audio player and handheld applications. As shown in Figure 2, the MAX8671X integrates USB power input, AC-to-DC adapter power input (DC), Li+/Li-Poly battery charger, three step-down regulators, two linear regulators, and various monitoring and status outputs. The MAX8671X offers adjustable output voltages for all outputs.

Smart Power Selector

The MAX8671X Smart Power Selector seamlessly distributes power between the two current-limited external inputs (USB and DC), the battery (BAT), and the system load (SYS). The basic functions performed are:

- With both an external power supply (USB or DC) and battery (BAT) connected:

  When the system load requirements are less than the input current limit, the battery is charged with residual power from the input.

  When the system load requirements exceed the input current limit, the battery supplies supplemental current to the load through the internal system load switch.
- When the battery is connected and there is no external power input, the system (SYS) is powered from the battery.
- When an external power input is connected and there is no battery, the system (SYS) is powered from the external power input.

The dual-input Smart Power Selector supports end products with dual and single external power inputs. For end products with dual external power inputs, connect these inputs directly to the DC and USB nodes of the MAX8671X. For end products with a single input, connect the single input to the DC node and connect USB to ground or leave it unconnected. In addition to AC-to-DC adapters current limits, the DC input also supports USB current limit to allow for end products

Table 1. Input Limiter Control Logic

POWER SOURCE	$\overline{DOK}$	$\overline{UOK}$	PEN1	PEN2	USUS	DC INPUT CURRENT LIMIT	USB INPUT CURRENT LIMIT	MAXIMUM CHARGE CURRENT*
AC-to-DC Adapter at DC Input	L	X	H	X	X	I_{DCLIM}	USB input off, DC input has priority	Lower of I_{CHGMAX} and I_{DCLIM}
USB Power at DC Input	L	X	L	L	L	100mA		Lower of I_{CHGMAX} and 100mA
	L	X	L	H	L	500mA		Lower of I_{CHGMAX} and 500mA
	L	X	L	X	H	Suspend		0
USB Power at USB Input, DC Unconnected	H	L	X	L	L	No DC input	100mA	Lower of I_{CHGMAX} and 100mA
	H	L	X	H	L		500mA	Lower of I_{CHGMAX} and 500mA
	H	L	X	X	H		Suspend	0
DC and USB Unconnected	H	H	X	X	X		No USB input	0

**Charge current cannot exceed the input current limit. Charge can be less than the maximum charge current if the total SYS load exceeds the input current limit.*

X = Don't care.

with a single power input to operate from either an AC-to-DC adapter or USB host (see Table 1).

A thermal-limiting circuit reduces the battery charger rate and external power-source current to prevent the MAX8671X from overheating.

System Load Switch

An internal 80mΩ (R_{BS}) MOSFET connects SYS to BAT when no voltage source is available at DC or USB. When an external source is detected at DC or USB, this switch is opened and SYS is powered from the valid input source through the Smart Power Selector.

When the system load requirements exceed the input current limit, the battery supplies supplemental current to the load through the internal system load switch. If the system load continuously exceeds the input current limit, the battery does not charge, even though external power is connected. This is not expected to occur in most cases because high loads usually occur only in short peaks. During these peaks, battery energy is used, but at all other times the battery charges.

USB Power Input (USB)

USB is a current-limited power input that supplies the system (SYS) up to 500mA. The USB to SYS switch is a linear regulator designed to operate in dropout. This linear regulator prevents the SYS voltage from exceeding 5.3V. USB is typically connected to the V_{BUS} line of the universal serial bus (USB) interface. As shown in Table 1, USB supports three different current limits that are set with the PEN2 and USUS digital inputs. These current limits are ideally suited for use with USB power.

The operating voltage range for USB is 4.1V to 6.6V, but it can tolerate up to 14V without damage. When the USB input voltage is below the undervoltage threshold (V_{USBL}, 4V typ) it is considered invalid. Similarly, if the USB voltage is above the overvoltage threshold (V_{USBH}, 6.9V typ) it is considered invalid. When the USB voltage is below the battery voltage, it is considered invalid. The USB power input is disconnected when the USB voltage is invalid. As shown in Table 1, when power is available at the DC input, it has priority over the USB input. Bypass USB to ground with at least a 4.7μF capacitor.

To support USB power sources at the USB input drive PEN2 and USUS to select between three internally set USB-related current limits as shown in Table 1. Choose 100mA for low-power USB mode. Choose 500mA for high-power USB mode. Choose suspend to reduce the USB current to 0.11mA (typ) for both USB suspend mode and unconfigured OTG mode. To comply with the USB 2.0 specification, each device must be initially configured for low power. After USB enumeration, the device can switch from low power to high power if given permission from the USB host. The MAX8671X does not perform enumeration. It is expected that the system communicates with the USB host and commands the MAX8671X through its PEN1, PEN2, and USUS inputs. When the load exceeds the input current limit, SYS drops to 82mV below BAT and the battery supplies supplemental load current.

The MAX8671X reduces the USB current limit by 5%/°C when the die temperature exceeds +100°C. The system load (I_{SYS}) has priority over the charger current, so input current is first reduced by lowering charge current. If the junction temperature still reaches +120°C in spite of charge current reduction, no input current is drawn from USB; the battery supplies the entire load and SYS is regulated below BAT by V_{BSREG}. Note that this on-chip thermal-limiting circuit is not related to and operates independently from the thermistor input.

If the USB power input is not required, connect USB to ground or leave it unconnected. When both DC and USB inputs are powered, the DC input has priority.

USB Power-OK Output ($\overline{UOK}$)

As shown Figure 3, the USB power-OK output ($\overline{UOK}$) is an active-low open-drain output. The $\overline{UOK}$ output pulls low when the voltage from USB to AGND (V_{USB}) is between V_{USBH} (typically 6.9V) and V_{USBL} (typically 4.0V).

The USB power-OK circuitry remains active in thermal overload and USB suspend. If the USB power-OK output feature is not required, connect $\overline{UOK}$ to ground or leave unconnected.

USB Suspend (USUS)

As shown in Table 1, driving USUS high suspends the DC or USB inputs if they are configured as a USB power input. The suspend current is 110µA when USUS is driven high allowing the MAX8671X to comply with the USB 1.1/2.0 specification for USB suspend as well as the USB OTG specification for an unconfigured device. If an external input (USB or DC) is connected to the MAX8671X and suspended, the SYS node is supported by the battery. The DOK, UOK, and VL circuits remain active in USB suspend mode.

A common assumption is that REG5 is disabled in USB suspend. This is not true. REG5 is not affected by the USB suspend mode. While in suspend, a USB device must provide the 3.3V termination to the USB transceivers' pullup resistors. This 3.3V termination can come from the MAX8671X's VL output or REG5. Both remain enabled in USB suspend.

DC Power Input (DC)

DC is a current-limited power input that supplies the system (SYS) up to 1A. The DC-to-SYS switch is a linear regulator designed to operate in dropout. This linear regulator prevents the SYS voltage from exceeding 5.3V. As shown in Table 1, DC supports four different current limits that are set with the PEN1, PEN2, and USUS digital inputs. These current limits are ideally suited for use with AC-to-DC wall adapters and USB power. The operating voltage range for DC is 4.1V to 6.6V, but it can tolerate up to 14V without damage. When the DC input voltage is below the undervoltage threshold (V_{DCL}, 4V typ), it is considered invalid. Similarly, if the DC voltage is above the overvoltage threshold (V_{DCH}, 6.9V typ), it is considered invalid. When the DC voltage is below the battery voltage, it is considered invalid. The DC power input is disconnected when the DC voltage is invalid. As shown in Table 1, when power is available at the DC input, it has priority over the USB input. Bypass DC to ground with at least a 4.7µF capacitor.

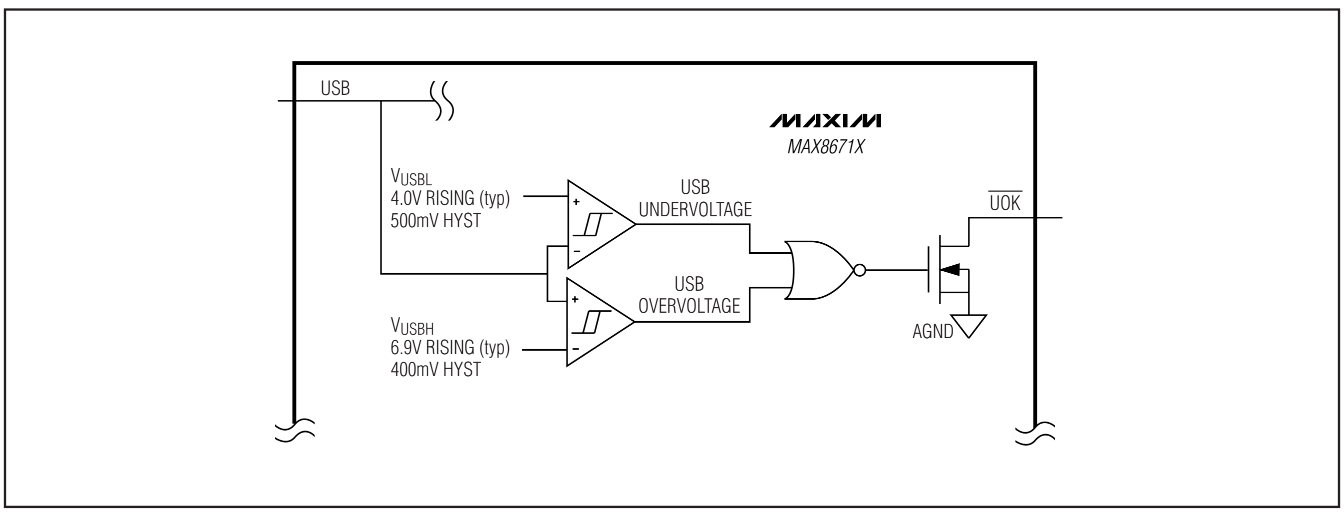


Figure 3. USB Power-OK Logic

To support common 500mA to 1000mA wall adapters at the DC input, pull PEN1 high. With PEN1 pulled high, the DC current limit is set by an external resistor from DISET to AGND (R_{DISET}). Choose R_{DISET} based on the current capability of the AC-to-DC adapter (I_{ADPTR}) as follows:

$$R_{DISET} \geq 2000 \times \frac{1.5V}{I_{ADPTR}}$$

For the selected value of R_{DISET}, calculate the DC current limit (I_{DCLIM}) as follows (Table 2, Figure 4):

$$I_{DCLIM} = 2000 \times \frac{1.5V}{R_{DISET}}$$

To support USB power sources at the DC input, pull PEN1 low. With PEN1 low, drive PEN2 and USUS to select between three internally set USB-related current limits as shown in Table 1. Choose 100mA for low-power USB mode. Choose 500mA for high-power USB mode. Choose suspend to reduce the DC current to 0.11mA (typ) for both USB suspend mode and unconfigured OTG mode. To comply with the USB 2.0 specification, each device must be initially configured for low power. After USB enumeration, the device can switch from low power to high power if given permission from the USB host. When the load exceeds the current limit, SYS drops below BAT by V_{BSREG} and the battery supplies supplemental load current.

If the DC power input is not required, connect DC to ground or leave it unconnected.

The MAX8671X reduces the USB and DC current limits by 5%/°C when the die temperature exceeds +100°C. The system load (I_{SYS}) has priority over the charger current, so input current is first reduced by lowering charge current. If the junction temperature still reaches +120°C in spite of charge-current reduction, no input current is drawn from USB and DC; the battery supplies the entire load and SYS is regulated below BAT by V_{BSREG}. Note that this on-chip thermal-limiting circuit is not related to and operates independently from the thermistor input.

DC Power-OK Output ($\overline{DOK}$)

As shown in Figure 5, the DC power-OK output ($\overline{DOK}$) is an open-drain, active-low output. The $\overline{DOK}$ output pulls low when the voltage from DC to AGND (V_{DC}) is between V_{DCH} (typically 6.9V) and V_{DCL} (typically 4.0V).

Table 2. DC Current Limit for Standard Values of R_{DISET}

R_{DISET} (kΩ)	I_{DCLIM} (mA)	R_{DISET} (kΩ)	I_{DCLIM} (mA)
3.01	997	4.32	694
3.09	971	4.42	679
3.16	949	4.53	662
3.24	926	4.64	647
3.32	904	4.75	632
3.40	882	4.87	616
3.48	862	4.99	601
3.57	840	5.11	587
3.65	822	5.23	574
3.74	802	5.36	560
3.83	783	5.49	546
3.92	765	5.62	534
4.02	746	5.76	521
4.12	728	5.90	508
4.22	711	6.04	497

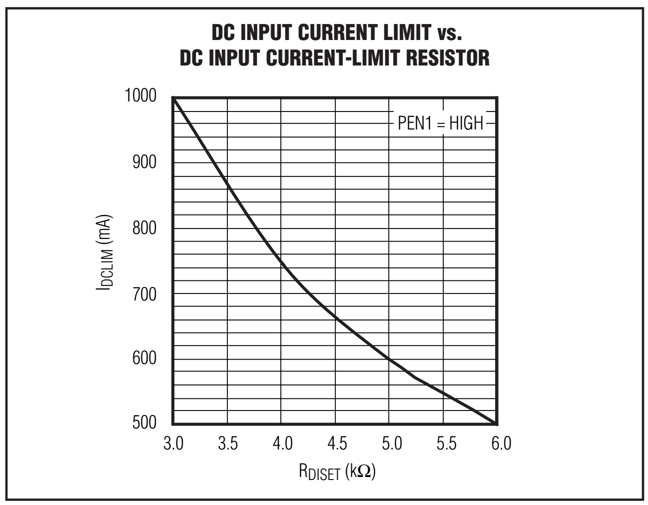


Figure 4. Programming DC Current Limit

The DC power-OK circuitry remains active in thermal overload and DC suspend. If the DC power-OK output feature is not required, connect $\overline{DOK}$ to ground or leave disconnected.

PMIC with Integrated Charger and Smart Power Selector for Handheld Devices

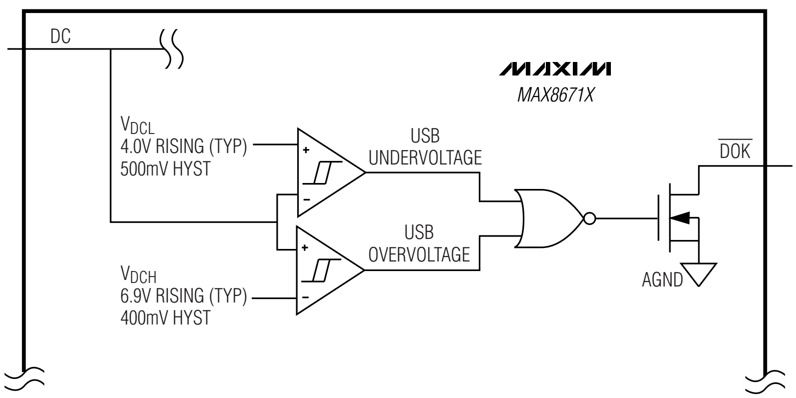


Figure 5. DC Power-OK Logic

Battery Charger

Figure 6 shows the typical Li+/Li-Poly charge profile for the MAX8671X, and Figure 7 shows the battery charger state diagram.

With a valid DC and/or USB input, the battery charger initiates a charge cycle when the charger is enabled. It first detects the battery voltage. If the battery voltage is less than the prequalification threshold (3.0V), the charger enters prequalification mode in which the battery charges at 10% of the maximum fast-charge current while deeply discharged. Once the battery voltage rises to 3.0V, the charger transitions to fast-charge mode and applies the maximum charge current. As charging continues, the battery voltage rises until it approaches the battery regulation voltage (selected with BVSET) where charge current starts tapering down. When charge current decreases to 4% of the maximum fast-charge current, the charger enters a brief 15s top-off state and then charging stops. If the battery voltage subsequently drops below the battery regulation voltage by $V_{BATRCHG}$, charging restarts and the timers reset.

The battery charge rate is set by several factors:

- Battery voltage
- USB/DC input current limit
- Charge setting resistor, R_{CISET}
- System load (I_{SYS})
- Die temperature

The MAX8671X automatically reduces charge current to prevent input overload. MAX8671X also reduces charge current when in thermal regulation (see the *Thermal Limiting and Overload Protection* section for more information).

Battery Regulation Voltage (BVSET)

BVSET allows the maximum battery charge voltage to be set to 4.1V, 4.2V, or 4.350V. Drive BVSET low to set the regulation voltage to 4.1V. Connect BVSET to VL or leave unconnected to set the regulation voltage to 4.2V. Connect BVSET to AGND through a 45kΩ to 55kΩ resistor (R_{BVSET}) to set the regulation voltage to 4.350V. R_{BVSET} accuracy is not critical. A 51kΩ ±5% resistor is acceptable.

Charge Enable Input ($\overline{CEN}$)

$\overline{CEN}$ is a digital input. Driving $\overline{CEN}$ high disables the battery charger. $\overline{CEN}$ does not affect the USB or DC current limit. Driving USUS high also disables the battery charger when charging from a USB source (PEN1 = low).

In many systems, there is no need for the system controller (typically a microprocessor (μP)) to disable the charger because the MAX8671X independently manages the charger power path. In these situations, $\overline{CEN}$ can be connected to ground. Do not leave $\overline{CEN}$ unconnected.

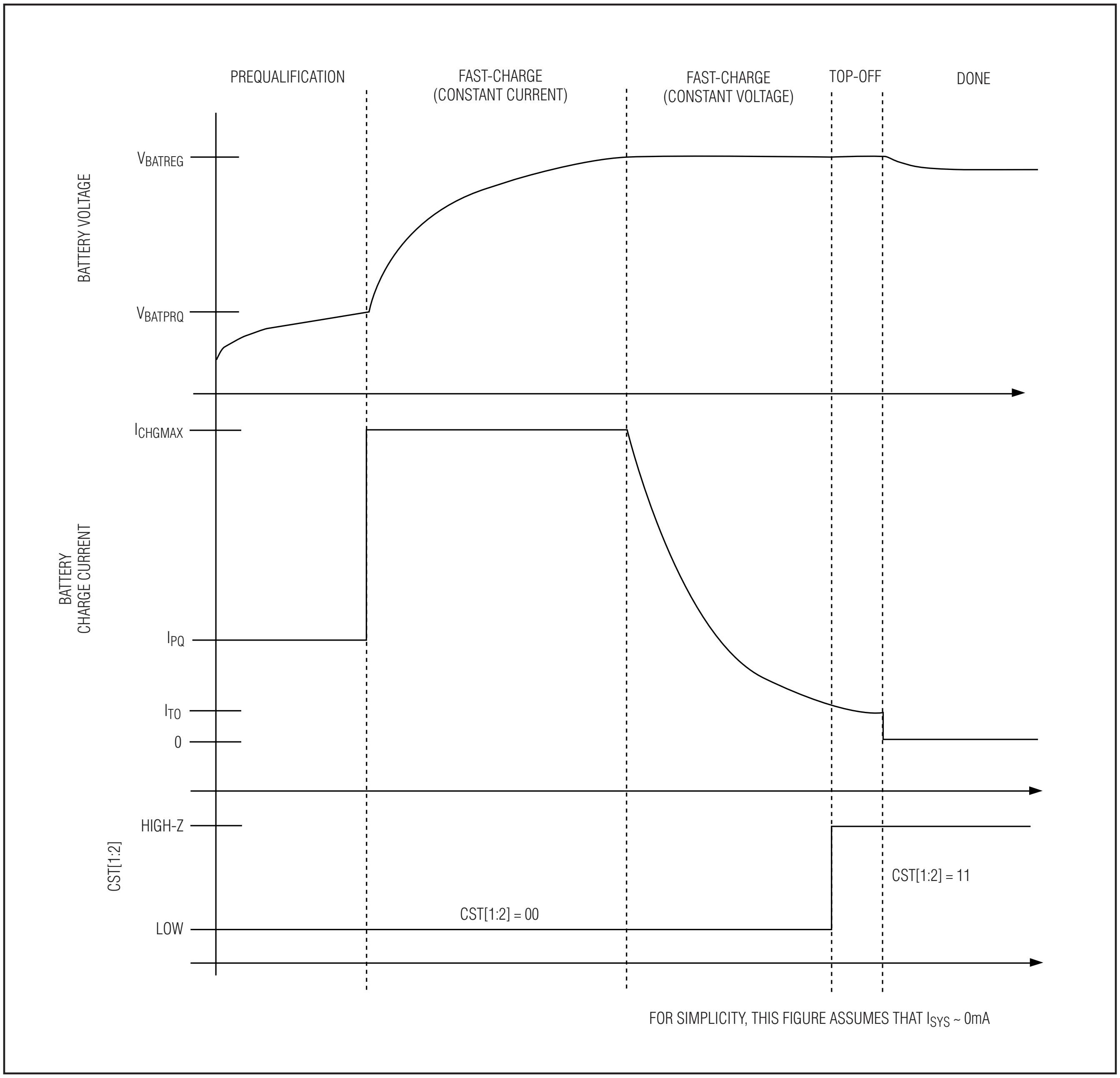


Figure 6. Li+/Li-Poly Charge Profile

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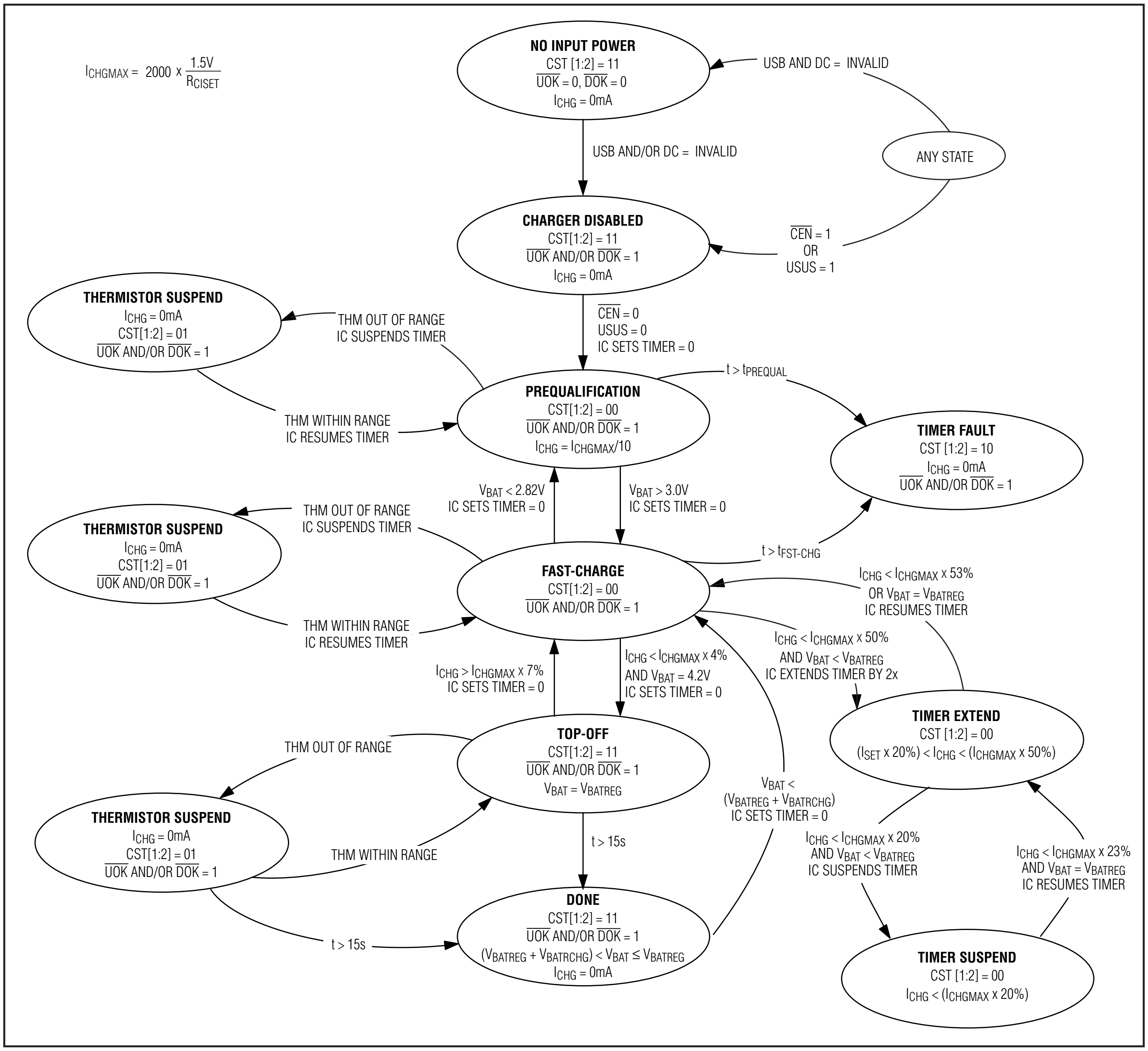

Figure 7. Charger State Diagram

Charge Status Outputs (CST1, CST2)

CST1 and CST2 are open-drain charger status outputs. Their function is shown in Table 3 and Figure 7. When the MAX8671X is used with a µP, pull CST1 and CST2 up to the system logic voltage with resistors to indicate charge status to the µP. Alternatively, CST1 and CST2 sink up to 20mA each for LED charge indicators.

If the charge status output feature is not required, connect CST1 and CST2 to ground or leave them unconnected.

Table 3. Charge Status Outputs

CST1	CST2	CHARGING	STATE
0	0	Yes	Prequalification or fast charge
0	1	No	Thermistor suspend
1	0	No	Timer fault
1	1	No	No input power or top-off or done

Note: *CST1 and CST2 are active-low, open-drain outputs. "0" indicates that the output device is pulling low. "1" indicates that the output is high impedance.*

Charge Timer (CT)

As shown in Figure 7, a fault timer prevents the battery from charging indefinitely. In prequalification and fast-charge modes, the timer is controlled by the capacitance at CT (C_{CT}). The MAX8671X supports values of C_{CT} from 0.01µF to 1µF. Calculate the prequalification and fast-charge times as follows (Table 4, Figure 8):

$$t_{PQ} = 33\text{min} \times \frac{C_{CT}}{0.15\mu F}$$

$$t_{FC} = 660\text{min} \times \frac{C_{CT}}{0.15\mu F}$$

When the charger exits fast-charge mode, a fixed 15s top-off mode is entered:

$$t_{TO} = 15s$$

While in the constant-current fast-charge mode (Figure 6), if the MAX8671X reduces the battery charge current due to its internal die temperature or large system loads, it slows down the charge timer. This feature eliminates nuisance charge timer faults. When the battery charge current is between 100% and 50% of its programmed fast-charge level, the fast-charge timer runs at full speed. When the battery charge current is between 50% and 20% of the programmed fast-charge level, the fast-charge timer is slowed by 2x. Similarly, when the battery charge current is below 20% of the programmed fast-charge level, the fast-charge timer is paused. The fast-charge timer is not slowed or paused when the charger is in the constant voltage portion of its fast-charge mode (Figure 6) where charge current reduces normally.

Table 4. Charge Times vs. C_{CT}

C_{CT} (nF)	t_{PQ} (min)	t_{FC} (min) 100% to 50%	t_{FC} (min) 50% to 20%
68	15.0	299	598
100	22.0	440	880
150	33.0	660	1320
220	48.4	968	1936
470	103.4	2068	4136

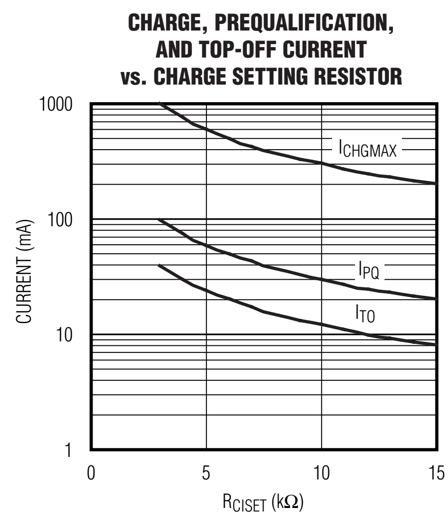

Figure 8. Programming Charge Current

Connect CT to AGND to disable the prequalification and fast-charge timers. With the internal timers of the MAX8671X disabled, an external device, such as a µP, can control the charge time through the $\overline{CEN}$ input.

Setting the Charger Currents (CISET)

As shown in Table 5 and Figure 9, a resistor from CISET to ground (R_{CISET}) sets the maximum fast-charge current (I_{CHGMAX}), the charge current in prequalification mode (I_{PQ}), and the top-off threshold (I_{TO}). The MAX8671X supports values of I_{CHGMAX} from 200mA to 1000mA. Select the R_{CISET} as follows:

$$R_{CISET} = 2000 \times \frac{1.5V}{I_{CHGMAX}}$$

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Table 5. Ideal Charge Currents vs. Charge Setting Resistor

R_{CISET} (kΩ)	I_{CHGMAX} (mA)	I_{PQ} (mA)	I_{TO} (mA)
3.01	1000	100	40
4.02	746	75	30
4.99	601	60	24
6.04	497	50	20
6.98	430	43	17
8.06	372	37	15
9.09	330	33	13
10.0	300	30	12
11.0	273	27	11
12.1	248	25	10
13.0	231	23	9
14.0	214	21	9
15.0	200	20	8

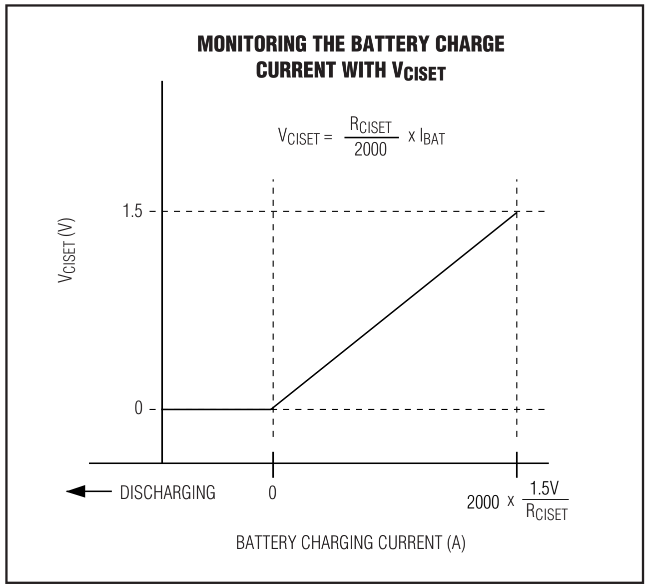

Figure 9. Monitoring the Battery Charge Current with the Voltage from CISET to AGND

Determine I_{CHGMAX} by considering the characteristics of the battery. It is not necessary to limit the charge current based on the capabilities of the expected AC-to-DC adapter or USB charging input, the system load, or thermal limitations of the PCB. The MAX8671X automatically lowers the charging current as necessary to accommodate these factors.

For the selected value of R_{CISET}, calculate I_{CHGMAX}, I_{PQ}, and I_{TO} as follows:

$$I_{CHGMAX} = 2000 \times \frac{1.5V}{R_{CISET}}$$

$$I_{PQ} = 10\% \times I_{CHGMAX}$$

$$I_{TO} = 4\% \times I_{CHGMAX}$$

In addition to setting the charge current, CISET also provides a means to monitor battery charge current. The CISET output voltage tracks the charge current delivered to the battery, and can be used to monitor the charge rate, as shown in Figure 9. A 1.5V output indicates the battery is being charged at the maximum set fast-charge current, and 0V indicates no charging. This voltage is also used by the charger control circuitry to set and monitor the battery current. Avoid adding capacitance directly to the CISET pin that exceeds 10pF. If filtering of the charge current monitor is necessary, include a resistor of 100kΩ or more between CISET and the filter capacitor to preserve charger stability.

Step-Down Converters (REG1, REG2, REG3)

REG1, REG2, and REG3 are high-efficiency 2MHz current-mode, step-down converters with adjustable outputs. Each REG1, REG2, and REG3 step-down converter delivers at least 425mA.

The step-down regulator power inputs (PV_) must be connected to SYS. The step-down regulators operate with V_{SYS} from 2.6V to 5.5V. Undervoltage lockout ensures that the step-down regulators do not operate with SYS below 2.6V (typ).

See the *Enable/Disable (EN) and Sequencing* section for how to enable and disable the step-down converters. When enabled, the MAX8671X gradually ramps each output up during a soft-start time. Soft-start eliminates input current surges when regulators are enabled.

See the *PWM* section for information about the step-down converters control scheme.

The MAX8671X uses external resistor-dividers to set the step-down output voltages between 1V and V_{SYS}. Use at least 10µA of bias current in these dividers to ensure no change in the stability of the closed-loop system. To set the output voltage, select a value for the resistor connected between FB_ and AGND (R_{FBL}). The recommended value is 100kΩ. Next, calculate the value of the resistor connected from FB_ to the output (R_{FBH}):

$$R_{FBH} = R_{FBL} \times \left(\frac{V_{OUT}}{1.0V} - 1 \right)$$

REG1, REG2, and REG3 are optimized for high, medium, and low output voltages, respectively. The highest overall efficiency occurs with V1 set to the highest output voltage and V3 set to the lowest output voltage.

PWM

The MAX8671X operates in either auto-PWM or forced-PWM modes. At light load, auto PWM switches only as needed to supply the load to improve light-load efficiency of the step-down converter. At higher load currents (~100mA), the step-down converter transitions to fixed 2MHz switching. Forced PWM always operates with a constant 2MHz switching frequency regardless of the load. This is useful in low-noise applications. Permanently connect PWM high for forced-PWM applications or low for auto-PWM applications. **Do not change PWM on-the-fly.**

Step-Down Dropout and Minimum Duty Cycle

All the step-down regulators are capable of operating in 100% duty-cycle dropout; however, REG1 has been optimized for this mode of operation. During 100% duty-cycle operation, the high-side p-channel MOSFET turns on constantly, connecting the input to the output through the inductor. The dropout voltage (V_{DO}) is calculated as follows:

$$V_{DO} = I_{LOAD} (R_P + R_L)$$

where:

R_P = p-channel power switch $R_{DS(ON)}$
R_L = external inductor ESR

The minimum duty cycle for all step-down regulators is 12.5% (typ), allowing a regulation voltage as low as 1V over the full SYS operating range. REG3 is optimized for low duty-cycle operation.

Step-Down Input Capacitors

The input capacitor in a step-down converter reduces current peaks drawn from the power source and reduces switching noise in the controller. The impedance of the input capacitor at the switching frequency must be less than that of the source impedance of the supply so that high-frequency switching currents do not pass through the input source.

The step-down regulator power inputs are critical discontinuous current paths that require careful bypassing. In the PCB layout, place the step-down regulator input bypass capacitors as close as possible to each pair of switching regulator power input pins (PV_ to PG_) to minimize parasitic inductance. If making connections to these caps through vias, be sure to use multiple vias to ensure that the layout does not insert excess inductance or resistance between the bypass cap and the power pins.

The input capacitor must meet the input ripple current requirement imposed by the step-down converter. Ceramic capacitors are preferred due to their low ESR and resilience to power-up surge currents. Choose the input capacitor so that its temperature rise due to input ripple current does not exceed about +10°C. For a step-down DC-DC converter, the maximum input ripple current is half of the output current. This maximum input ripple current occurs when the step-down converter operates at 50% duty factor ($V_{IN} = 2 \times V_{OUT}$).

Bypass each step-down regulator input with a 4.7µF ceramic capacitor from PV_ to PG_. Use capacitors that maintain their capacitance over temperature and DC bias. Ceramic capacitors with an X7R or X5R temperature characteristic generally perform well. The capacitor voltage rating should be 6.3V or greater.

Step-Down Output Capacitors

The output capacitance keeps output ripple small and ensures control loop stability. The output capacitor must have low impedance at the switching frequency. Ceramic, polymer, and tantalum capacitors are suitable, with ceramic exhibiting the lowest ESR and lowest high-frequency impedance. The MAX8671X requires at least 20µF of output capacitance, which is best achieved with two 10µF ceramic capacitors in parallel.

As the case sizes of ceramic surface-mount capacitors decrease, their capacitance vs. DC bias voltage characteristic becomes poor. Due to this characteristic, it is possible for 0805 capacitors to perform well while 0603 capacitors of the same value might not. The MAX8671X requires a nominal output capacitance of 20µF; however, after their DC bias voltage derating, the output capacitance must be at least 15µF.

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Step-Down Inductor

Choose the step-down regulator inductance to be 4.7µH. The minimum recommended saturation current requirement is 600mA. In PWM mode, the peak inductor currents are equal to the load current plus one half of the inductor ripple current. The MAX8671X works well with physically small inductors. See Table 6 for suggested inductors.

The peak-to-peak inductor ripple current during PWM operation is calculated as follows:

$$I_{P-P} = \frac{V_{OUT}(V_{SYS} - V_{OUT})}{V_{SYS} \times f_S \times L}$$

where f_S is the 2MHz switching frequency.

The peak inductor current during PWM operation is calculated as follows:

$$I_{L\_PEAK} = I_{LOAD} + \frac{I_{P-P}}{2}$$

Step-Down Converter Output Current

The three MAX8671X step-down regulators each provide at least 425mA of output current when using a recommended inductor (Table 6). To calculate the maximum output current for a particular application and inductor use the following two-step process (as shown in Figure 10):

1) Use the following equation to calculate the approximate duty cycle (D):

$$D = \frac{V_{OUT} + I_{OUTTAR}(R_N + R_L)}{V_{IN} + I_{OUTTAR}(R_N - R_P)}$$

where:

V_{OUT} = output voltage

I_{OUTTAR} = target (desired) output current—cannot be more than the minimum p-channel current-limit threshold

R_N = n-channel on-resistance

R_P = p-channel on-resistance

R_L = external inductor's ESR

V_{IN} = input voltage—MAXIMUM

2) Use the following equation to calculate the maximum output current (I_{OUTMAX}):

$$I_{OUTMAX} = \frac{I_{LIM} - \frac{V_{OUT}(1-D)}{2 \times f \times L}}{1 + (R_N + R_L)\frac{1-D}{2 \times f \times L}}$$

where:

I_{LIM} = p-channel current-limit threshold—MINIMUM

V_{OUT} = output voltage

D = approximate duty cycle derived from step 1

f = oscillator frequency—MINIMUM

L = external inductor's inductance—MINIMUM

R_N = n-channel on-resistance

R_L = external inductor's ESR

Table 6. Suggested Inductors

MANUFACTURER	SERIES	INDUCTANCE (µH)	ESR (Ω)	CURRENT RATING (mA)	DIMENSIONS (mm)
Sumida	CDRH2D11HP	4.7	190	750	3.0 x 3.0 x 1.2 = 10.8mm^3
	CDH2D09	4.7	218	700	3.0 x 3.0 x 1.0 = 9.0mm^3
Taiyo Yuden	NR3012	4.7	130	770	3.0 x 3.0 x 1.2 = 10.8mm^3
	NR3010	4.7	190	750	3.0 x 3.0 x 1.0 = 9.0mm^3
TDK	VLF3012	4.7	160	740	2.8 x 2.6 x 1.2 = 8.7mm^3
	VLF3010	4.7	240	700	2.8 x 2.6 x 1.0 = 7.3mm^3
TOKO	DE2812C	4.7	130	880	3.0 x 2.8 x 1.2 = 10.8mm^3
	DE2810C	4.7	180	640	3.0 x 2.8 x 1.0 = 8.4mm^3

TO FIND THE MAXIMUM OUTPUT CURRENT FOR REG3 WITH $V_{IN} = 3.2V$ TO $5.3V$, $V_{OUT} = 1.2V$, $L = 4.7\mu H$ $\pm 20\%$, AND $R_L = 130m\Omega$:

$$D = \frac{V_{OUT} + I_{OUTTAR}(R_N + R_L)}{V_{IN} + I_{OUTTAR}(R_N - R_P)} = \frac{1.2V + 0.425A(0.12\Omega + 0.13\Omega)}{5.3V + 0.425A(0.12\Omega - 0.23\Omega)} = 0.249$$

$$I_{OUTMAX} = \frac{I_{LIM} - \dfrac{V_{OUT}(1-D)}{2 \times f \times L}}{1 + (R_N + R_L)\dfrac{1-D}{2 \times f \times L}} = \frac{0.555A - \dfrac{1.2V(1-0.249)}{2 \times (1.8 \times 10^6 Hz) \times (4.7 \times 10^{-6} H \times 0.8)}}{1 + (0.12\Omega + 0.13\Omega)\dfrac{1-0.249}{2 \times (1.8 \times 10^6 Hz) \times (4.7 \times 10^{-6} H \times 0.8)}} = 0.482A$$

Figure 10. Step-Down Converter Maximum Output Current Example

Linear Regulators (REG4, REG5)

The REG4 and REG5 linear regulators have low quiescent current, and low output noise. Each regulator supplies up to 180mA to its load. Bypass each LDO output with a 2.2µF or greater capacitor to ground. If V4 or V5 is set to less than 1.5V, bypass the output with 3.3µF or greater.

Each linear regulator has an independent power input (PV4 and PV5) with an input voltage range from 1.7V to V_{SYS} (V_{SYS} can be up to 5.5V). Voltages below the input undervoltage lockout threshold (1.6V) are invalid. The regulator inputs can be driven from an efficient low-voltage source, such as a DC-DC output, to optimize efficiency (see the following equation). Bypass each LDO input with a 1µF or greater capacitor to ground:

$$Efficiency_{LDO} \approx \frac{V_{OUT}}{V_{IN}}$$

REG5 is intended to power the system USB transceiver circuitry and is only active when USB power is available. REG4 is powered from the battery when power is not available at DC or USB.

See the *Enable/Disable (EN) and Sequencing* section for how to enable and disable the linear regulators. When enabled, the linear regulators soft-start by ramping their outputs up to their target voltage in 3ms. Soft-start limits the inrush current when the regulators are enabled.

The MAX8671X uses external resistor-dividers to set the LDO output voltages between 0.6V and $V_{PV\_}$. Use at least 10µA of bias current in these dividers to ensure no change in the stability of the closed-loop system. To set the output voltage, select a value for the resistor connected between FB_ and AGND (R_{FBL}). The recommended value is 60.4kΩ. Next, calculate the value of the resistor connected from FB_ to the output (R_{FBH}):

$$R_{FBH} = R_{FBL} \times \left(\frac{V_{OUT}}{0.6V} - 1\right)$$

For REG4, an external 0.01µF bypass capacitor from BP to AGND in conjunction with a 150kΩ internal resistor creates a 110Hz lowpass filter for noise reduction. BP is a high-impedance node and requires a low-leakage capacitor. For example, a leakage of 40nA results in a 1% error.

VL Linear Regulator

VL is the output of a 3.3V linear regulator that powers MAX8671X internal circuitry. VL is internally powered from the higher of USB or DC and automatically powers up when either of these power inputs exceeds approximately 1.5V. When the higher of the DC and USB supply is between 1.5V and 3.3V, VL operates in dropout. VL automatically powers down when both the USB and DC power inputs are removed. Bypass VL to AGND with a 0.1µF capacitor.

VL remains on even when USB and/or DC are in overvoltage or undervoltage lockout, when SYS is in undervoltage lockout, and also during thermal faults.

VL sources up to 3mA for external loads. If VL is not used for external loads, the MAX8671X's USB/DC current limit guarantees compliance with the USB 2.0 input current specifications. If VL is used for external loads, USB/DC currents increase and might exceed the limits outlined in the USB 2.0 specification. For example, if the USB to SYS current is limited to 95mA and VL is sourcing 3mA, I_{USB} is 98mA. Similarly, if the USB input is suspended and VL is sourcing 3mA, I_{USB} is 3mA.

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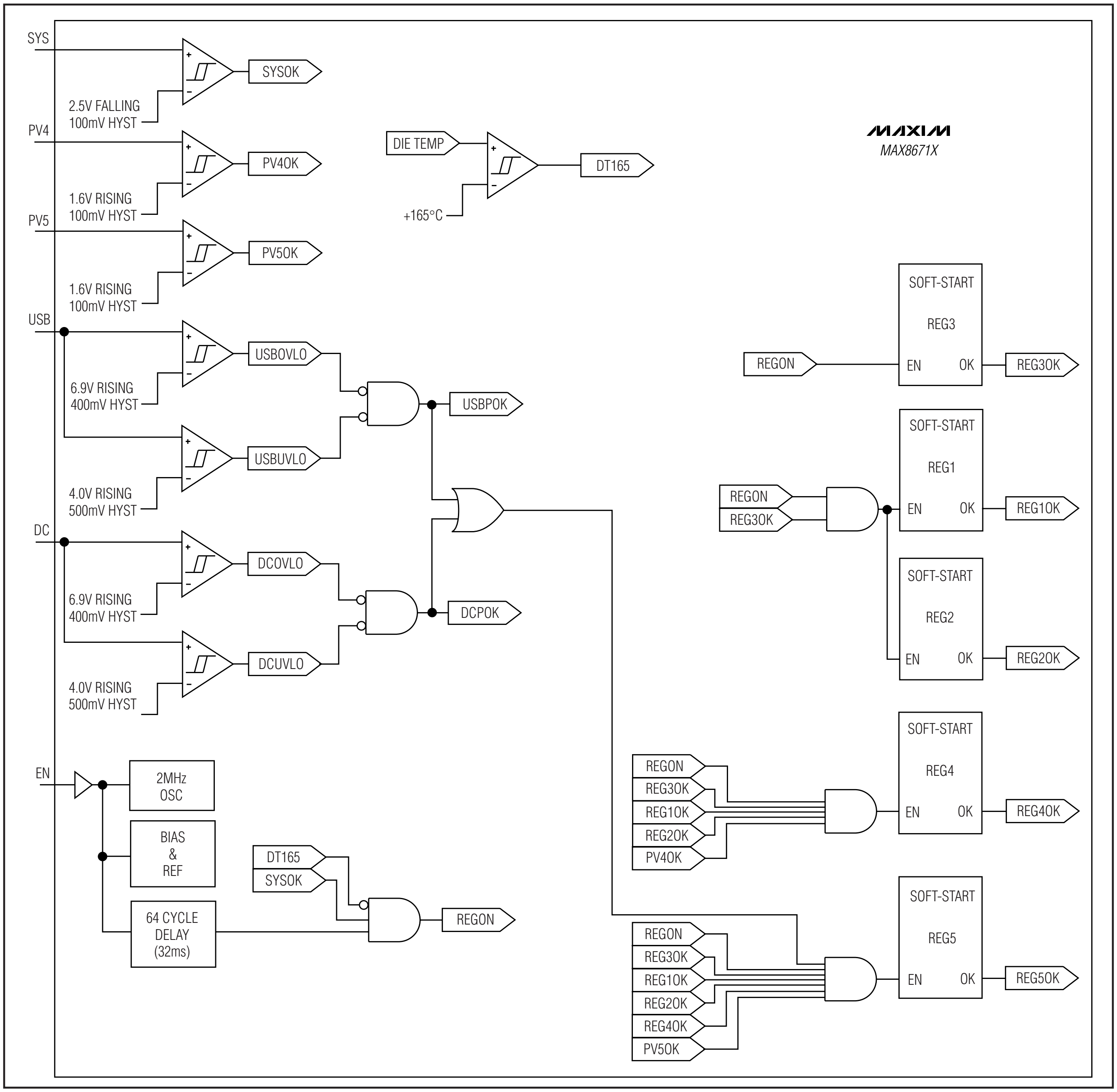


Figure 11. Enable/Disable Logic

Enable/Disable (EN) and Sequencing

Figures 11, 12, and 13 show how the five MAX8671X regulators are enabled and disabled. With a valid SYS voltage and die temperature, asserting EN high enables REG1–REG4. Pulling EN low disables REG1–REG5. REG5 is intended to power the system USB transceiver circuitry, which is only active when USB power is available. Therefore, a valid source must be on either the USB or DC input for REG5 to enable.

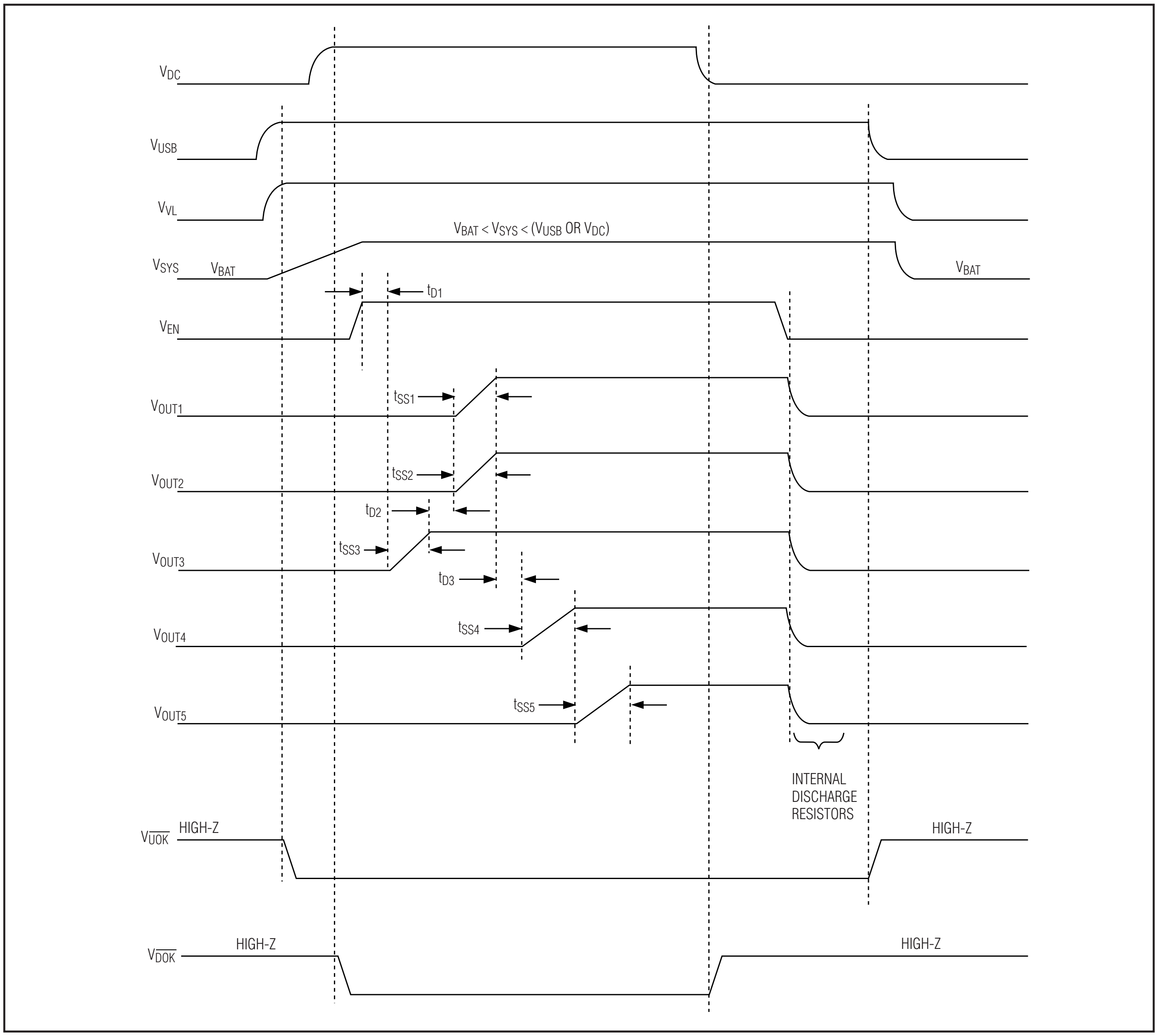


Figure 12. Enable and Disable Waveforms

The VL regulator is not controlled by EN. It is powered from the higher of USB or DC and automatically powers up when either of the power inputs exceeds approximately 1.5V. Similarly, VL automatically powers down when both the USB and DC power inputs are removed.

Soft-Start/Inrush Current

The MAX8671X implements soft-start on many levels to control inrush current, to avoid collapsing supply voltages, and to fully comply with the USB 2.0 specifications. All USB, DC, and charging functions implement soft-start. The USB and DC nodes only require 4.7µF of input capacitance. Furthermore, all regulators implement soft-start to avoid transient overload of power inputs (Figure 12).

Active Discharge in Shutdown

Each MAX8671X regulator (REG1–REG5) has an internal 1kΩ resistor that discharges the output capacitor when the regulator is off. The discharge resistors ensure that the load circuitry powers down completely. The internal discharge resistors are connected when a regulator is disabled and when the device is in UVLO with an input voltage greater than 1.0V. With an input voltage less than 1.0V, the internal discharge resistors are not activated.

Undervoltage and Overvoltage Lockout

USB/DC UVLO

Undervoltage lockout (UVLO) prevents an input supply from being used when its voltage is below the operating range. When the USB voltage is less than the USB UVLO threshold (4.0V typ), the USB input is disconnected from SYS, and $\overline{UOK}$ goes high impedance. When the DC voltage is less than the DC UVLO threshold (4.0V typ), the DC input is disconnected from SYS, and $\overline{DOK}$ goes high impedance. In addition, when both USB and DC are in UVLO, the battery charger is disabled, and BAT is connected to SYS through the internal system load switch. REG1–REG4 are allowed to operate from the battery without power at USB or DC. REG5 is intended to power the system USB transceiver circuitry, which is only active when USB power is available. Therefore, a valid source must be present on either the USB or DC input for REG5 to enable.

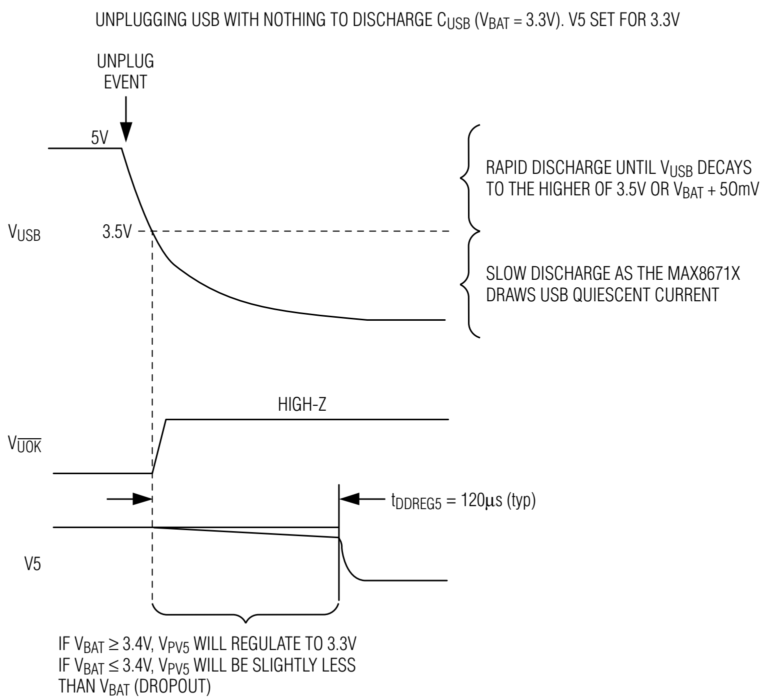


Figure 13. REG5 Disable Detail

USB/DC OVLO

Overvoltage lockout (OVLO) prevents an input supply from being used when its voltage exceeds the operating range. Both USB and DC withstand input voltages up to 14V. When the USB voltage is greater than the USB OVLO threshold (6.9V typ), the USB input is disconnected from SYS, and $\overline{UOK}$ goes high impedance. When the DC voltage is greater than the DC OVLO threshold (6.9V typ), the DC input is disconnected from SYS, and $\overline{DOK}$ goes high impedance. In addition, when both DC and USB are in OVLO, the battery charger is disabled, and BAT is connected to SYS through the internal system load switch. REG1–REG4 are allowed to operate from the battery when USB and DC are in overvoltage lockout. The VL supply remains active in OVLO. REG5 is intended to power the system USB transceiver circuitry, which is only active when USB power is available. A valid source must be present on either the USB or DC input for REG5 to enable.

SYS UVLO

A UVLO circuit monitors the voltage from SYS to ground (V_{SYS}). When V_{SYS} falls below V_{UVLO_SYS} (2.5V typ), REG1–REG5 are disabled. V_{UVLO_SYS} has a 100mV hysteresis. The VL supply remains active in SYS UVLO.

REG4/REG5 UVLO

A UVLO circuit monitors the PV4 and PV5 LDO power inputs. When the PV_ voltage is below 1.6V, it is invalid and the LDO is disabled.

Thermal Limiting and Overload Protection

The MAX8671X is packaged in a 5mm x 5mm x 0.8mm 40-pin thin QFN. Table 7 shows the thermal characteristics of this package. The MAX8671X has several mechanisms to control junction temperature in the event of a thermal overload.

Table 7. 5mm x 5mm x 0.8mm Thin QFN Thermal Characteristics

	SINGLE-LAYER PCB	MULTILAYER PCB
Continuous Power Dissipation	1777.8mW Derate 22.2mW/°C above +70°C	2857.1mW Derate 35.7mW/°C above +70°C
*θ_{JA}	45°C/W	28°C/W
θ_{JC}	1.7°C/W	1.7°C/W

**θ_{JA} is specified according to the JESD51 standard.*

Smart Power Selector Thermal-Overload Protection

The MAX8671X reduces the USB and DC current limits by 5%/°C when the die temperature exceeds +100°C. The system load (I_{SYS}) has priority over the charger current, so input current is first reduced by lowering charge current. If the junction temperature still reaches +120°C in spite of charge-current reduction, no input current is drawn from USB and DC; the battery supplies the entire load and SYS is regulated 82mV (V_{BSREG}) below BAT. Note that this on-chip thermal-limiting circuit is not related to and operates independently from the thermistor input.

Regulator Thermal-Overload Shutdown

The MAX8671X disables all regulator outputs (except VL) when the junction temperature rises above +165°C, allowing the device to cool. When the junction temperature cools by approximately 15°C, the regulators resume the state indicated by the enable input (EN) by repeating their soft-start sequence. Note that this thermal-overload shutdown is a fail-safe mechanism; proper thermal design should ensure that the junction temperature of the MAX8671X never exceeds the absolute maximum rating of +150°C.

Battery Charger Thermistor Input (THM)

The THM input connects to an external negative temperature coefficient (NTC) thermistor to monitor battery or system temperature. Charging is suspended when the thermistor temperature is out of range. Additionally, the charge timers are suspended and charge status indicators report that the charger is in thermistor suspend (CST[1:2] = 01). When the thermistor comes back into range, charging resumes and the charge timer continues from where it left off. Table 8 shows THM temperature limits for various thermistor material constants. If the battery temperature monitor is not required, bias THM midway between V_L and AGND with a resistive divider—100kΩ ±5% resistors are recommended. Biasing THM midway between V_L and AGND bypasses this function.

Table 8. Trip Temperatures for Different Thermistors

THERMISTOR BETA (ß [K])	3000	3250	3500	3750	4250	4250
R_{TB} (kΩ)	10	10	10	10	10	10
R_{TP} (kΩ)	Open	Open	Open	Open	Open	120
R_{TS} (kΩ)	Short	Short	Short	Short	Short	Short
Resistance at +25°C [kΩ]	10	10	10	10	10	10
Resistance at +50°C [kΩ]	4.59	4.30	4.03	3.78	3.32	3.32
Resistance at 0°C [kΩ]	25.14	27.15	29.32	31.66	36.91	36.91
Nominal Hot Trip Temperature [°C]	55	53	51	49	46	45
Nominal Cold Trip Temperature [°C]	-3	-1	0	2	5	0

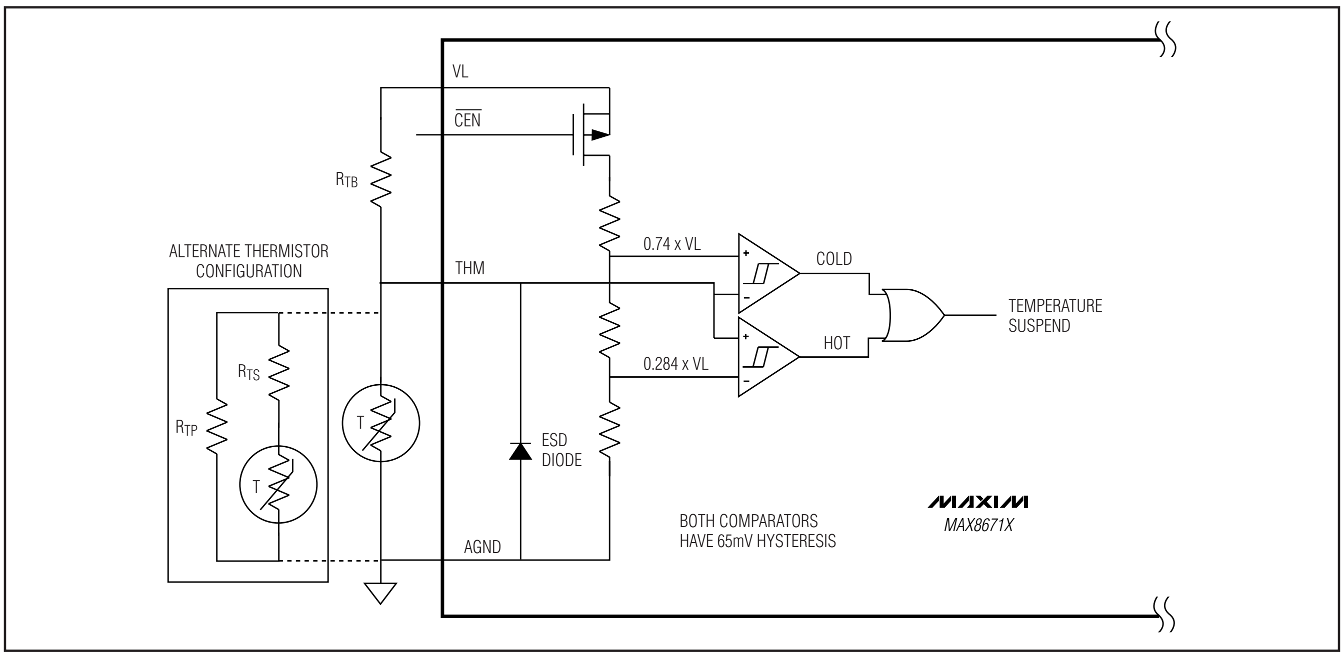


Figure 14. Thermistor Input

Since the thermistor monitoring circuit employs an external bias resistor from THM to VL (R_{TB} in Figure 14), any resistance thermistor can be used as long as the value of R_{TB} is equivalent to the thermistor's +25°C resistance. For example, with a 10kΩ at +25°C thermistor, use 10kΩ at R_{TB}, and with a 100kΩ at +25°C thermistor, use 100kΩ at R_{TB}. The general relation of thermistor resistance to temperature is defined by the following equation:

$$R_T = R_{25} \times e\left\{\beta\left(\frac{1}{T+273} - \frac{1}{298}\right)\right\}$$

where:

R_T = The resistance in ohms of the thermistor at temperature T in Celsius

R_{25} = The resistance in ohms of the thermistor at +25°C

β = The material constant of the thermistor that typically ranges from 3000K to 5000K

T = The temperature of the thermistor in °C that corresponds to R_T

THM threshold adjustment can be accommodated by changing R_{TB}, connecting a resistor in series and/or in parallel with the thermistor, or using a thermistor with different material constant (β). For example, a +45°C hot threshold and 0°C cold threshold can be realized by using a 10kΩ thermistor with a β of 4250K and connecting 120kΩ in parallel. Since the thermistor resistance near 0°C is much higher than it is near +50°C, a large parallel resistance lowers the cold threshold, while only slightly lowering the hot threshold. Conversely, a small series resistance raises the cold threshold, while only slightly raising the hot threshold. Raising R_{TB} lowers both the hot and cold thresholds, while lowering R_{TB} raises both thresholds.

PCB Layout and Routing

Good printed circuit board (PCB) layout is necessary to achieve optimal performance. Refer to the MAX8671 evaluation kit for Maxim's recommended layout.

Use the following guidelines for the best results:

- Use short and wide traces for high-current and discontinuous current paths.
- The step-down regulator power inputs are critical discontinuous current paths that require careful bypassing. Place the step-down regulator input bypass capacitors as close as possible to each switching regulator power input pair (PV_ to PG_).
- Minimize the area of the loops formed by the step-down converters' dynamic switching currents.
- The exposed paddle (EP) is the main path for heat to exit the IC. Connect EP to the ground plane with thermal vias to allow heat to dissipate from the device.
- The MAX8671X regulator feedback nodes are sensitive high-impedance nodes. Keep these nodes as short as possible and away from the inductors.
- The thermistor node is high impedance and should be routed with care.
- Make power ground connections to a power ground plane. Make analog ground connections to an analog ground plane. Connect the ground planes at a single point.

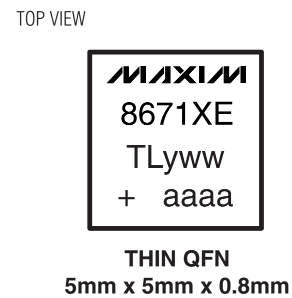


Figure 15. Package Marking Example

- The REG4 LDO is a high-performance LDO with high PSRR and low noise and care should be used in the layout to obtain the high performance. Generally, the REG4 LDO is powered from a step-down regulator output, and therefore, its input capacitor should be bypassed to the power ground plane. However, its output capacitor should be bypassed to the analog ground plane.
- BP is a high impedance node and leakage current into or out of BP can affect the LDO output accuracy.

Package Marking

The top of the MAX8671X package is laser etched as shown in Figure 15:

- "8671XETL" is the product identification code. The full part number is MAX8671XETL; however, in this case, the "MAX" prefix is omitted due to space limitations.
- "yww" is a date code. "y" is the last number in the Gregorian calendar year. "ww" is the week number in the Gregorian calendar. For example:

  "801" is the first week of 2008; the week of January 1st, 2008

  "052" is the fifty-second week of 2010; the week of December 27th, 2010.

  "aaaa" is an assembly code and lot code.

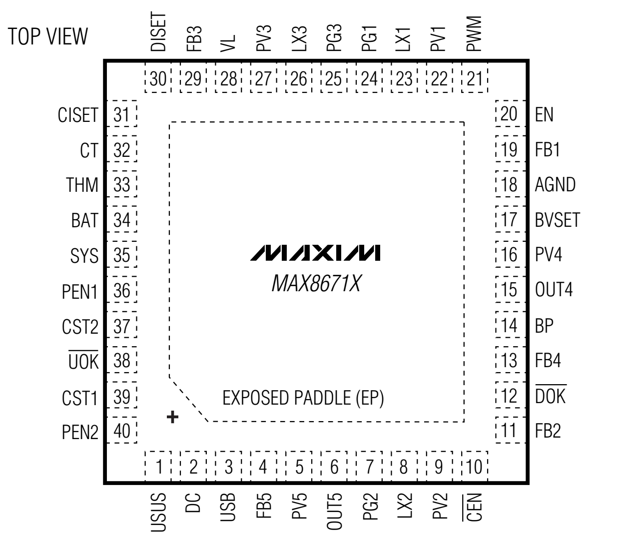
  "+" denotes lead-free packaging and marks the pin 1 location.

Chip Information

PROCESS: BiCMOS

PMIC with Integrated Charger and Smart Power Selector for Handheld Devices

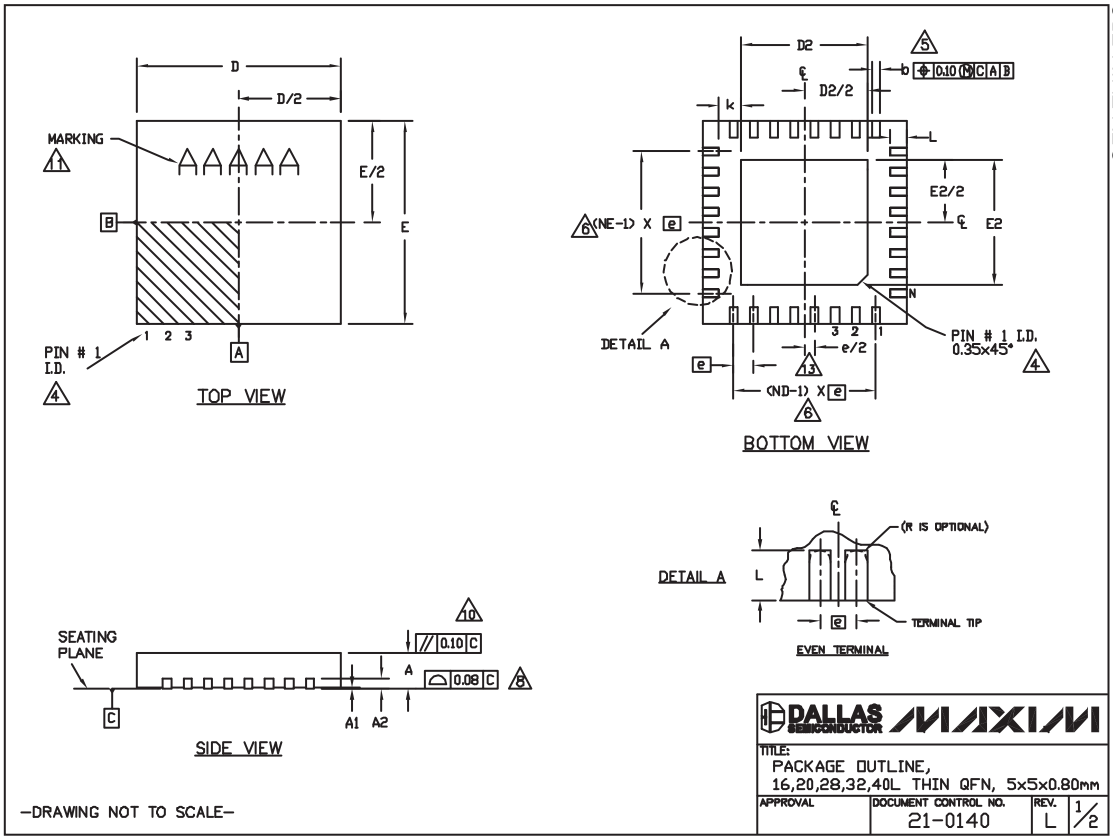
Pin Configuration



THIN QFN
5mm x 5mm x 0.8mm

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)



PMIC with Integrated Charger and Smart Power Selector for Handheld Devices

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

COMMON DIMENSIONS															
PKG.	16L 5x5			20L 5x5			28L 5x5			32L 5x5			40L 5x5		
SYMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05
A2	0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.		
b	0.25	0.30	0.35	0.25	0.30	0.35	0.20	0.25	0.30	0.20	0.25	0.30	0.15	0.20	0.25
D	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
E	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
e	0.80 BSC.			0.65 BSC.			0.50 BSC.			0.50 BSC.			0.40 BSC.		
k	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-
L	0.30	0.40	0.50	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50	0.30	0.40	0.50
N	16			20			28			32			40		
ND	4			5			7			8			10		
NE	4			5			7			8			10		
JEDEC	WHHB			WHHC			WHHD-1			WHHD-2			-----		

EXPOSED PAD VARIATIONS						
PKG. CODES	D2			E2		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
T1655-2	3.00	3.10	3.20	3.00	3.10	3.20
T1655-3	3.00	3.10	3.20	3.00	3.10	3.20
T1655N-1	3.00	3.10	3.20	3.00	3.10	3.20
T2055-3	3.00	3.10	3.20	3.00	3.10	3.20
T2055-4	3.00	3.10	3.20	3.00	3.10	3.20
T2055-5	3.15	3.25	3.35	3.15	3.25	3.35
T2055MN-5	3.15	3.25	3.35	3.15	3.25	3.35
T2855-3	3.15	3.25	3.35	3.15	3.25	3.35
T2855-4	2.60	2.70	2.80	2.60	2.70	2.80
T2855-5	2.60	2.70	2.80	2.60	2.70	2.80
T2855-6	3.15	3.25	3.35	3.15	3.25	3.35
T2855-7	2.60	2.70	2.80	2.60	2.70	2.80
T2855-8	3.15	3.25	3.35	3.15	3.25	3.35
T2855N-1	3.15	3.25	3.35	3.15	3.25	3.35
T3255-3	3.00	3.10	3.20	3.00	3.10	3.20
T3255-4	3.00	3.10	3.20	3.00	3.10	3.20
T3255M-4	3.00	3.10	3.20	3.00	3.10	3.20
T3255-5	3.00	3.10	3.20	3.00	3.10	3.20
T3255N-1	3.00	3.10	3.20	3.00	3.10	3.20
T4055-1	3.40	3.50	3.60	3.40	3.50	3.60
T4055-2	3.40	3.50	3.60	3.40	3.50	3.60
T4055MN-1	3.40	3.50	3.60	3.40	3.50	3.60

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.

⚠4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.

⚠5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.

⚠6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.

7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.

⚠8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.

9. DRAWING CONFORMS TO JEDEC MO220, EXCEPT EXPOSED PAD DIMENSION FOR T2855-3, T2855-6, T4055-1 AND T4055-2.

⚠10. WARPAGE SHALL NOT EXCEED 0.10 mm.

11. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
12. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.

⚠13. LEAD CENTERLINES TO BE AT TRUE POSITION AS DEFINED BY BASIC DIMENSION "e", ±0.05.

14. ALL DIMENSIONS APPLY TO BOTH LEADED AND PbFREE PARTS.

-DRAWING NOT TO SCALE-

DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE, 16,20,28,32,40L THIN QFN, 5x5x0.80mm

APPROVAL | DOCUMENT CONTROL NO. 21-0140 | REV. L | 2/2