- **3-State I/O-Type Read-Back Inputs**
- **Bus-Structured Pinout**
- **Choice of True or Inverting Logic**
  - **SN74ALS666 . . . True Outputs**
  - **SN74ALS667 . . . Inverted Outputs**
- **Preset and Clear Inputs**
- **Package Options Include Plastic Small-Outline (DW) Packages and Standard Plastic (NT) 300-mil DIPs**

SN74ALS666 . . . DW OR NT PACKAGE
(TOP VIEW)

$\overline{OERB}$	1	24 V_{CC}
$\overline{OE1}$	2	23 $\overline{OE2}$
1D	3	22 1Q
2D	4	21 2Q
3D	5	20 3Q
4D	6	19 4Q
5D	7	18 5Q
6D	8	17 6Q
7D	9	16 7Q
8D	10	15 8Q
$\overline{CLR}$	11	14 $\overline{PRE}$
GND	12	13 LE

SN74ALS667 . . . DW OR NT PACKAGE
(TOP VIEW)

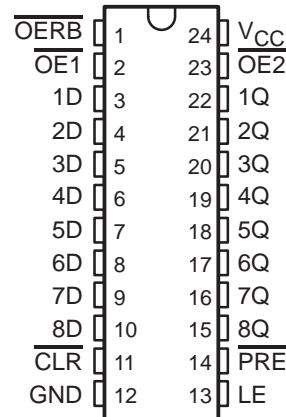|		
$\overline{OERB}$	1	24 V_{CC}
$\overline{OE1}$	2	23 $\overline{OE2}$
1D	3	22 $1\overline{Q}$
2D	4	21 $2\overline{Q}$
3D	5	20 $3\overline{Q}$
4D	6	19 $4\overline{Q}$
5D	7	18 $5\overline{Q}$
6D	8	17 $6\overline{Q}$
7D	9	16 $7\overline{Q}$
8D	10	15 $8\overline{Q}$
$\overline{CLR}$	11	14 $\overline{PRE}$
GND	12	13 LE

description

These 8-bit D-type transparent latches are designed specifically for storing the contents of the input data bus, plus reading back the stored data onto the input data bus. In addition, they provide a 3-state buffer-type output and are easily utilized in bus-structured applications.

While the latch enable (LE) is high, the Q outputs of the SN74ALS666 follow the data (D) inputs. The $\overline{Q}$ outputs of the SN74ALS667 provide the inverse of the data applied to its D inputs. The Q or $\overline{Q}$ output of both devices is in the high-impedance state if either output-enable ($\overline{OE1}$ or $\overline{OE2}$) input is at a high logic level.
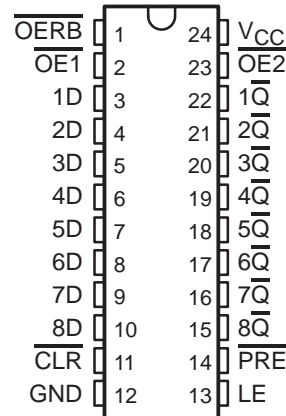
Read back is provided through the read-back control ($\overline{OERB}$) input. When $\overline{OERB}$ is taken low, the data present at the output of the data latches passes back onto the input data bus. When $\overline{OERB}$ is taken high, the output of the data latches is isolated from the D inputs. $\overline{OERB}$ does not affect the internal operation of the latches; however, caution should be exercised to avoid a bus conflict.

The SN74ALS666 and SN74ALS667 are characterized for operation from 0°C to 70°C.

![Texas Instruments logo] **TEXAS INSTRUMENTS**

logic symbols†

SN74ALS666

SN74ALS667

† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagrams (positive logic)

SN74ALS666

1D   3

To Seven Other Channels

SN74ALS667

1D   3

To Seven Other Channels

timing diagram
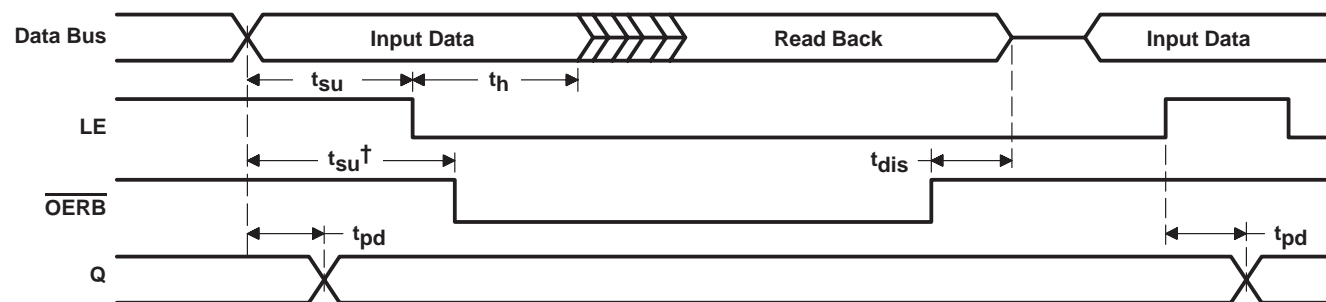
$\overline{\text{CLR}}$ = H, $\overline{\text{PRE}}$ = H, $\overline{\text{OE1}}$ = L, $\overline{\text{OE2}}$ = L.
† This setup time ensures the read-back circuit does not create a conflict on the input data bus.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, V_{CC} .... 7 V
Input voltage, V_I (all inputs except D inputs) .... 7 V
Voltage applied to D inputs and to disabled 3-state outputs .... 5.5 V
Operating free-air temperature range, T_A: SN74ALS666, SN74ALS667 .... 0°C to 70°C
Storage temperature range .... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN74ALS666 SN74ALS667			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current	Q			−2.6	mA
		D			−0.4	
I_{OL}	Low-level output current	Q			24	mA
		D			8	
t_w	Pulse duration	LE high	10			ns
		$\overline{\text{CLR}}$ low	10			
		$\overline{\text{PRE}}$ low	10			
t_{su}	Setup time	Data before LE↓	10			ns
		Data before $\overline{\text{OERB}}$↓	10			
t_h	Hold time, data after LE↓		5			ns
T_A	Operating free-air temperature		0		70	°C

TEXAS
INSTRUMENTS
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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN74ALS666 SN74ALS667 MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2	V
V_{OH}	All outputs	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V
	Q or $\overline{Q}$	V_{CC} = 4.5 V,	I_{OH} = −2.6 mA	2.4	3.2		
V_{OL}	D inputs	V_{CC} = 4.5 V	I_{OL} = 4 mA		0.25	0.4	V
			I_{OL} = 8 mA		0.35	0.5	
	Q or $\overline{Q}$	V_{CC} = 4.5 V	I_{OL} = 12 mA		0.25	0.4	
			I_{OL} = 24 mA		0.35	0.5	
I_{OZH}	Q or $\overline{Q}$	V_{CC} = 5.5 V,	V_O = 2.7 V			20	µA
I_{OZL}	Q or $\overline{Q}$	V_{CC} = 5.5 V,	V_O = 0.4 V			−20	µA
I_I	D inputs	V_{CC} = 5.5 V	V_I = 5.5 V			0.1	mA
	All others		V_I = 7 V			0.1	
I_{IH}	D inputs‡	V_{CC} = 5.5 V,	V_I = 2.7 V			20	µA
	All others					20	
I_{IL}	D inputs‡	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1	mA
	All others					−0.1	
I_O§		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	mA
I_{CC}	SN74ALS666	V_{CC} = 5.5 V, $\overline{OERB}$ high	Q outputs high		25	50	mA
			Q outputs low		40	73	
			Q outputs disabled		30	55	
	SN74ALS667	V_{CC} = 5.5 V, $\overline{OERB}$ high	$\overline{Q}$ outputs high		25	50	
			$\overline{Q}$ outputs low		45	79	
			$\overline{Q}$ outputs disabled		30	60	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ For I/O ports (Q_A through Q_H), the parameters I_{IH} and I_{IL} include the off-state output current.
§ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, T_A = MIN to MAX[†] SN74ALS666		UNIT
			MIN	MAX	
t_{PLH}	D	Q	3	14	ns
t_{PHL}			4	18	
t_{PLH}	LE	Q	6	21	ns
t_{PHL}			8	27	
t_{PHL}	$\overline{CLR}$	Q	9	29	ns
		D	11	32	
t_{PLH}	$\overline{PRE}$	Q	7	22	ns
t_{PHL}		D	9	28	
t_{en}[‡]	$\overline{OERB}$	D	4	21	ns
	$\overline{OE1}$, $\overline{OE2}$	Q	4	21	
t_{dis}[§]	$\overline{OERB}$	D	1	14	ns
	$\overline{OE1}$, $\overline{OE2}$	Q	1	14	

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
[‡] t_{en} = t_{PZH} or t_{PZL}
[§] t_{dis} = t_{PHZ} or t_{PLZ}

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, T_A = MIN to MAX[†] SN74ALS667		UNIT
			MIN	MAX	
t_{PLH}	D	$\overline{Q}$	6	20	ns
t_{PHL}			4	15	
t_{PLH}	LE	$\overline{Q}$	9	28	ns
t_{PHL}			7	22	
t_{PHL}	$\overline{CLR}$	$\overline{Q}$	7	24	ns
		D	8	26	
t_{PLH}	$\overline{PRE}$	$\overline{Q}$	8	25	ns
t_{PHL}		D	9	28	
t_{en}[‡]	$\overline{OERB}$	D	4	21	ns
	$\overline{OE1}$, $\overline{OE2}$	$\overline{Q}$	4	21	
t_{dis}[§]	$\overline{OERB}$	D	1	14	ns
	$\overline{OE1}$, $\overline{OE2}$	$\overline{Q}$	1	14	

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
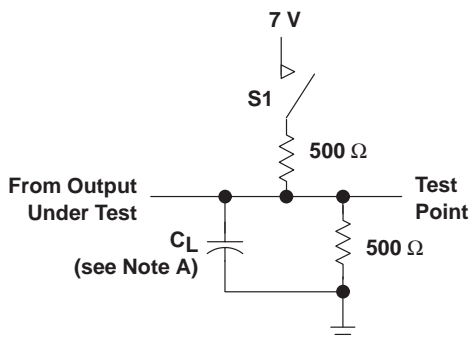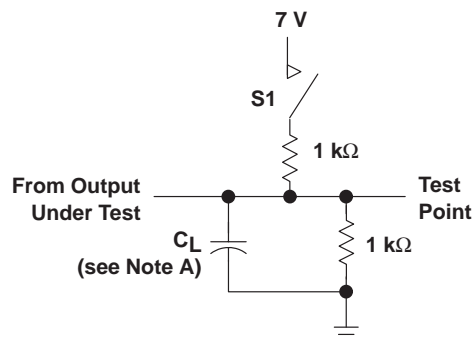[‡] t_{en} = t_{PZH} or t_{PZL}
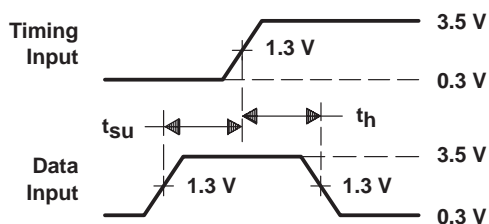[§] t_{dis} = t_{PHZ} or t_{PLZ}

PARAMETER MEASUREMENT INFORMATION

LOAD CIRCUIT FOR Q OR $\overline{Q}$ OUTPUTS

LOAD CIRCUIT FOR D OUTPUTS

VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES
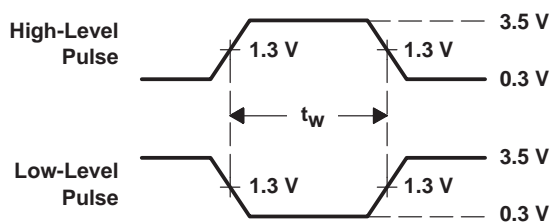
VOLTAGE WAVEFORMS
PULSE DURATIONS
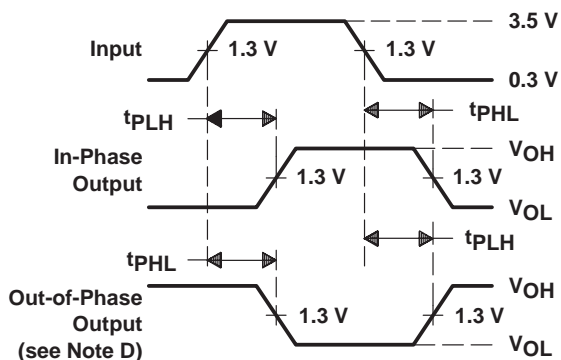
VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
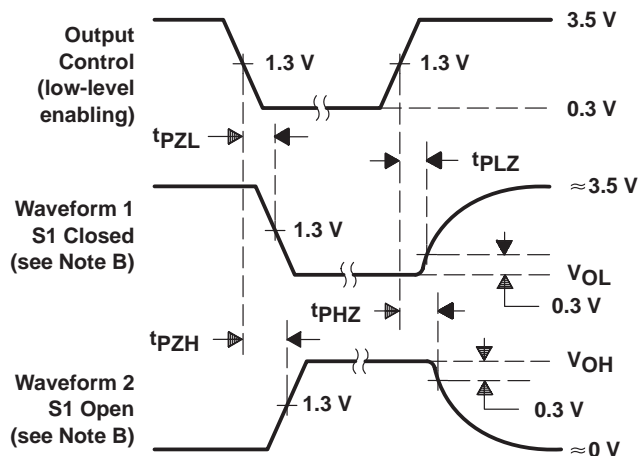
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance.
  B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
      Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  C. All input pulses have the following characteristics: PRR ≤ 1 MHz, $t_r = t_f = 2$ ns, duty cycle = 50%.
  D. When measuring propagation delay times of 3-state outputs, switch S1 is open.

Figure 1. Load Circuits and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
SN74ALS666DW	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS666DWE4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS666DWR	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS666DWRE4	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS666NSR	ACTIVE	SO	NS	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS666NSRE4	ACTIVE	SO	NS	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS666NT	ACTIVE	PDIP	NT	24	15	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74ALS666NTE4	ACTIVE	PDIP	NT	24	15	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74ALS667DW	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS667DWE4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS667DWR	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS667DWRE4	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS667NSR	ACTIVE	SO	NS	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS667NSRE4	ACTIVE	SO	NS	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS667NT	ACTIVE	PDIP	NT	24	15	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74ALS667NT3	OBSOLETE	PDIP	NT	24		TBD	Call TI	Call TI
SN74ALS667NTE4	ACTIVE	PDIP	NT	24	15	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check
http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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NT (R-PDIP-T**)   PLASTIC DUAL-IN-LINE PACKAGE

24 PINS SHOWN
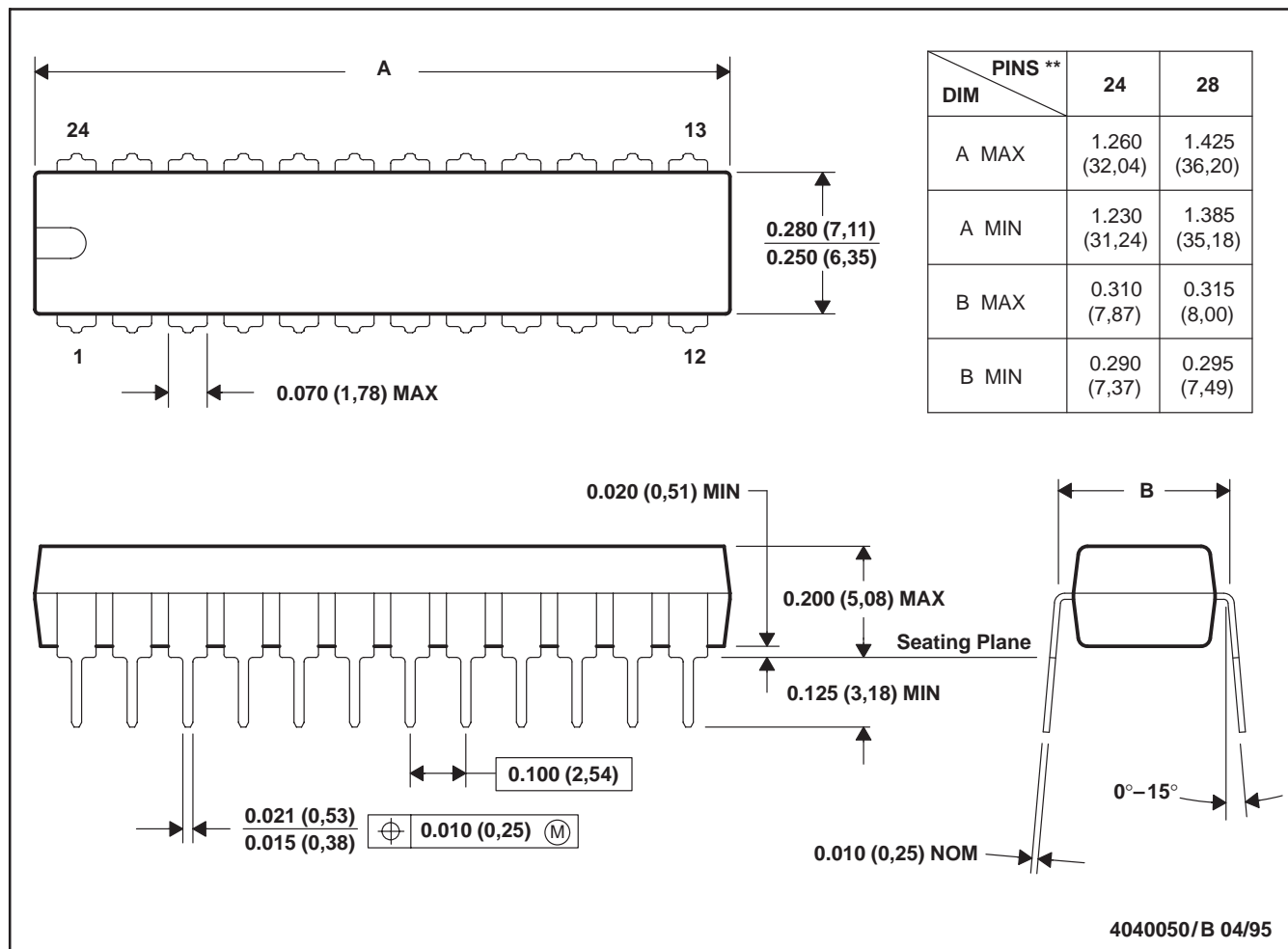
PINS ** DIM	24	28
A MAX	1.260 (32,04)	1.425 (36,20)
A MIN	1.230 (31,24)	1.385 (35,18)
B MAX	0.310 (7,87)	0.315 (8,00)
B MIN	0.290 (7,37)	0.295 (7,49)

A

24   13

0.280 (7,11)
0.250 (6,35)

1   12

0.070 (1,78) MAX

0.020 (0,51) MIN

0.200 (5,08) MAX

Seating Plane

0.125 (3,18) MIN

B

0°–15°

0.010 (0,25) NOM

0.100 (2,54)

0.021 (0,53)
0.015 (0,38)   ⊕   0.010 (0,25) Ⓜ

4040050/ B 04/95

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.

DW (R−PDSO−G24)   PLASTIC SMALL−OUTLINE PACKAGE

0.614 (15,60)
0.598 (15,20)

24

13

0.419 (10,63)
0.393 (9,97)

0.299 (7,60)
0.291 (7,40)

1

12

Pin 1
Index Area

0.050 (1,27)

0.020 (0,51)
0.012 (0,31)

⊕ 0.010 (0,25) Ⓜ

0.104 (2,65) Max

0.012 (0,30)
0.004 (0,10)

0.013 (0,33)
0.008 (0,20)

Gauge Plane

⌂ 0.004 (0,10)

Seating Plane

0.010 (0,25)

0°−8°

0.050 (1,27)
0.016 (0,40)

4040000−5/F 06/2004

NOTES: A.   All linear dimensions are in inches (millimeters).
         B.   This drawing is subject to change without notice.
         C.   Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
         D.   Falls within JEDEC MS−013 variation AD.

MECHANICAL DATA

DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES: A.   All linear dimensions are in millimeters.
         B.   This drawing is subject to change without notice.
         C.   Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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