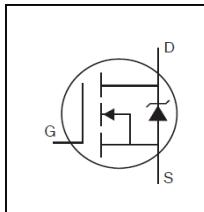
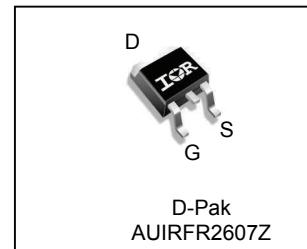


**Features**

- Advanced Process Technology
- Ultra Low On-Resistance
- 175°C Operating Temperature
- Fast Switching
- Repetitive Avalanche Allowed up to  $T_{jmax}$
- Lead-Free, RoHS Compliant
- Automotive Qualified \*



$V_{DSS}$	75V
$R_{DS(on)}$	typ. 17.6mΩ
	max. 22mΩ
$I_D$ (Silicon Limited)	45A④
$I_D$ (Package Limited)	42A



<b>G</b>	<b>D</b>	<b>S</b>
Gate	Drain	Source

**Description**

Specifically designed for Automotive applications, this HEXFET® Power MOSFET utilizes the latest processing techniques to achieve extremely low on-resistance per silicon area. Additional features of this design are a 175°C junction operating temperature, fast switching speed and improved repetitive avalanche rating. These features combine to make this design an extremely efficient and reliable device for use in Automotive applications and a wide variety of other applications.

Base part number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
AUIRFR2607Z	D-Pak	Tube	75	AUIRFR2607Z
		Tape and Reel Left	3000	AUIRFR2607ZTRL

**Absolute Maximum Ratings**

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only; and functional operation of the device at these or any other condition beyond those indicated in the specifications is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions. Ambient temperature (TA) is 25°C, unless otherwise specified.

Symbol	Parameter	Max.	Units	
$I_D$ @ $T_C = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS}$ @ 10V (Silicon Limited)	45④	A	
$I_D$ @ $T_C = 100^\circ\text{C}$	Continuous Drain Current, $V_{GS}$ @ 10V (Silicon Limited)	32		
$I_D$ @ $T_C = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS}$ @ 10V (Package Limited)	42		
$I_{DM}$	Pulsed Drain Current ①	180		
$P_D$ @ $T_C = 25^\circ\text{C}$	Maximum Power Dissipation	110	W	
	Linear Derating Factor	0.72	W/°C	
$V_{GS}$	Gate-to-Source Voltage	± 20	V	
$E_{AS}$	Single Pulse Avalanche Energy (Thermally Limited) ②	96	mJ	
$E_{AS}$ (Tested)	Single Pulse Avalanche Energy Tested Value ⑥	96		
$I_{AR}$	Avalanche Current ①	See Fig.15,16, 12a, 12b		
$E_{AR}$	Repetitive Avalanche Energy ⑤			
$T_J$	Operating Junction and	-55 to + 175	°C	
$T_{STG}$	Storage Temperature Range			
	Soldering Temperature, for 10 seconds (1.6mm from case)	300		

**Thermal Resistance**

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ⑧	—	1.38	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB Mount) ⑦	—	50	
$R_{\theta JA}$	Junction-to-Ambient	—	110	

HEXFET® is a registered trademark of Infineon.

\*Qualification standards can be found at [www.infineon.com](http://www.infineon.com)

**Static @  $T_J = 25^\circ\text{C}$  (unless otherwise specified)**

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(\text{BR})\text{DSS}}$	Drain-to-Source Breakdown Voltage	75	—	—	V	$V_{\text{GS}} = 0\text{V}$ , $I_D = 250\mu\text{A}$
$\Delta V_{(\text{BR})\text{DSS}}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.074	—	V/ $^\circ\text{C}$	Reference to $25^\circ\text{C}$ , $I_D = 1\text{mA}$
$R_{\text{DS}(\text{on})}$	Static Drain-to-Source On-Resistance	—	17.6	22	$\text{m}\Omega$	$V_{\text{GS}} = 10\text{V}$ , $I_D = 30\text{A}$ ③
$V_{\text{GS}(\text{th})}$	Gate Threshold Voltage	2.0	—	4.0	V	$V_{\text{DS}} = V_{\text{GS}}$ , $I_D = 50\mu\text{A}$
$g_{\text{fs}}$	Forward Trans conductance	36	—	—	S	$V_{\text{DS}} = 25\text{V}$ , $I_D = 30\text{A}$
$I_{\text{DSS}}$	Drain-to-Source Leakage Current	—	—	20	$\mu\text{A}$	$V_{\text{DS}} = 75\text{ V}$ , $V_{\text{GS}} = 0\text{V}$
		—	—	250		$V_{\text{DS}} = 75\text{V}$ , $V_{\text{GS}} = 0\text{V}$ , $T_J = 125^\circ\text{C}$
$I_{\text{GSS}}$	Gate-to-Source Forward Leakage	—	—	200	nA	$V_{\text{GS}} = 20\text{V}$
	Gate-to-Source Reverse Leakage	—	—	-200		$V_{\text{GS}} = -20\text{V}$

**Dynamic Electrical Characteristics @  $T_J = 25^\circ\text{C}$  (unless otherwise specified)**

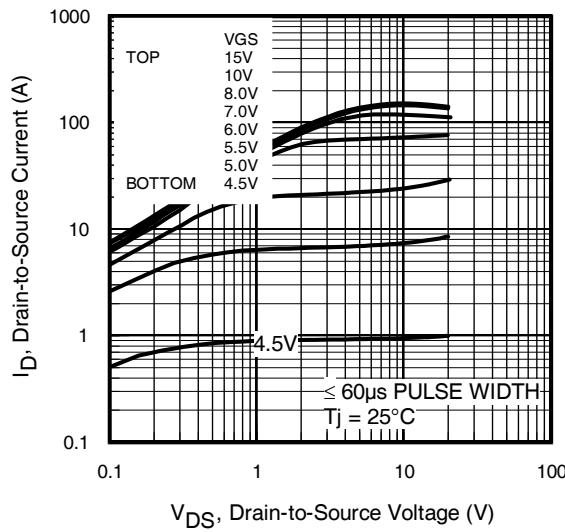
$Q_g$	Total Gate Charge	—	34	51	nC	$I_D = 30\text{A}$ $V_{\text{DS}} = 60\text{V}$ $V_{\text{GS}} = 10\text{V}$ ③
$Q_{\text{gs}}$	Gate-to-Source Charge	—	8.9	—		$V_{\text{DD}} = 38\text{V}$
$Q_{\text{gd}}$	Gate-to-Drain Charge	—	14	—		$I_D = 30\text{A}$
$t_{\text{d}(\text{on})}$	Turn-On Delay Time	—	14	—		$R_G = 15\Omega$
$t_r$	Rise Time	—	59	—		$V_{\text{GS}} = 10\text{V}$ ③
$t_{\text{d}(\text{off})}$	Turn-Off Delay Time	—	39	—	ns	
$t_f$	Fall Time	—	28	—		
$L_D$	Internal Drain Inductance	—	4.5	—		Between lead, 6mm (0.25in.) from package and center of die contact
$L_S$	Internal Source Inductance	—	7.5	—		
$C_{\text{iss}}$	Input Capacitance	—	1440	—	pF	$V_{\text{GS}} = 0\text{V}$
$C_{\text{oss}}$	Output Capacitance	—	190	—		$V_{\text{DS}} = 25\text{V}$
$C_{\text{rss}}$	Reverse Transfer Capacitance	—	110	—		$f = 1.0\text{MHz}$
$C_{\text{oss}}$	Output Capacitance	—	720	—		$V_{\text{GS}} = 0\text{V}$ , $V_{\text{DS}} = 1.0\text{V}$ $f = 1.0\text{MHz}$
$C_{\text{oss}}$	Output Capacitance	—	130	—		$V_{\text{GS}} = 0\text{V}$ , $V_{\text{DS}} = 60\text{V}$ $f = 1.0\text{MHz}$
$C_{\text{oss eff.}}$	Effective Output Capacitance	—	230	—		$V_{\text{GS}} = 0\text{V}$ , $V_{\text{DS}} = 0\text{V}$ to $60\text{V}$ ④

**Diode Characteristics**

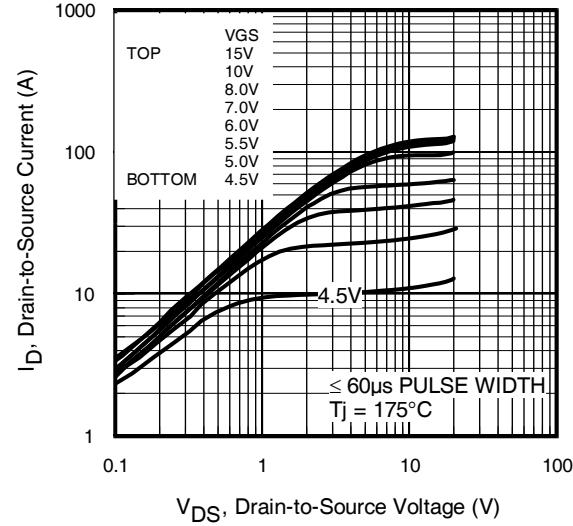
	Parameter	Min.	Typ.	Max.	Units	Conditions
$I_S$	Continuous Source Current (Body Diode)	—	—	45⑨	A	MOSFET symbol showing the integral reverse p-n junction diode.
$I_{\text{SM}}$	Pulsed Source Current (Body Diode) ①	—	—	180		
$V_{\text{SD}}$	Diode Forward Voltage	—	—	1.3		$T_J = 25^\circ\text{C}$ , $I_S = 30\text{A}$ , $V_{\text{GS}} = 0\text{V}$ ③
$t_{\text{rr}}$	Reverse Recovery Time	—	30	45		$T_J = 25^\circ\text{C}$ , $I_F = 30\text{A}$ , $V_{\text{DD}} = 38\text{V}$
$Q_{\text{rr}}$	Reverse Recovery Charge	—	28	42		$\text{di/dt} = 100\text{A}/\mu\text{s}$ ③
$t_{\text{on}}$	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S + L_D$ )				

**Notes:**

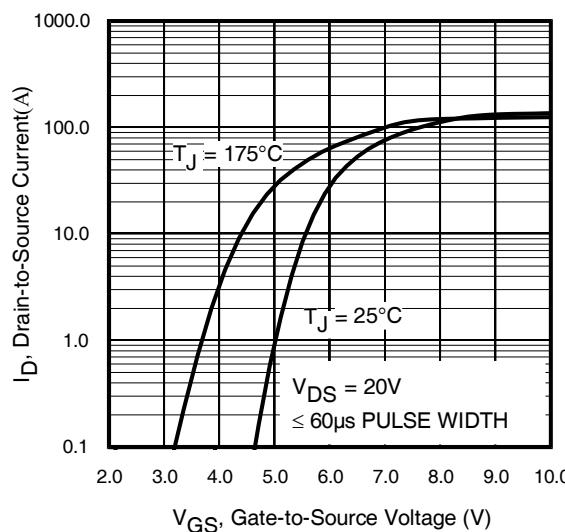
- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)
- ② Limited by  $T_{\text{Jmax}}$ , starting  $T_J = 25^\circ\text{C}$ ,  $L = 0.21\text{mH}$ ,  $R_G = 25\Omega$ ,  $I_{\text{AS}} = 30\text{A}$ ,  $V_{\text{GS}} = 10\text{V}$ . Part not recommended for use above this value.
- ③ Pulse width  $\leq 1.0\text{ms}$ ; duty cycle  $\leq 2\%$ .
- ④  $C_{\text{oss eff.}}$  is a fixed capacitance that gives the same charging time as  $C_{\text{oss}}$  while  $V_{\text{DS}}$  is rising from 0 to 80%  $V_{\text{DSS}}$
- ⑤ Limited by  $T_{\text{Jmax}}$ , see Fig.12a, 12b, 15, 16 for typical repetitive avalanche performance.
- ⑥ This value determined from sample failure population. 100% tested to this value in production.
- ⑦ When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994
- ⑧  $R_\theta$  is measured at  $T_J$  approximately  $90^\circ\text{C}$
- ⑨ Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 42A.



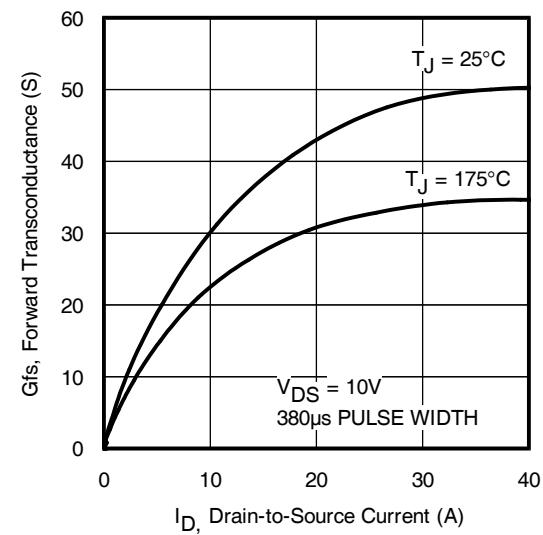
**Fig. 1** Typical Output Characteristics



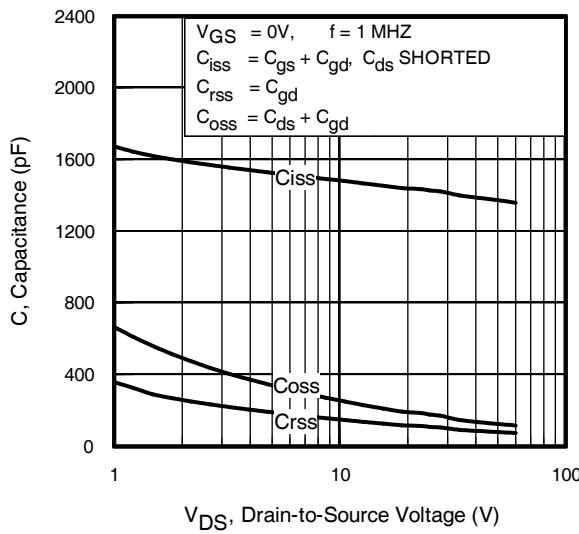
**Fig. 2** Typical Output Characteristics



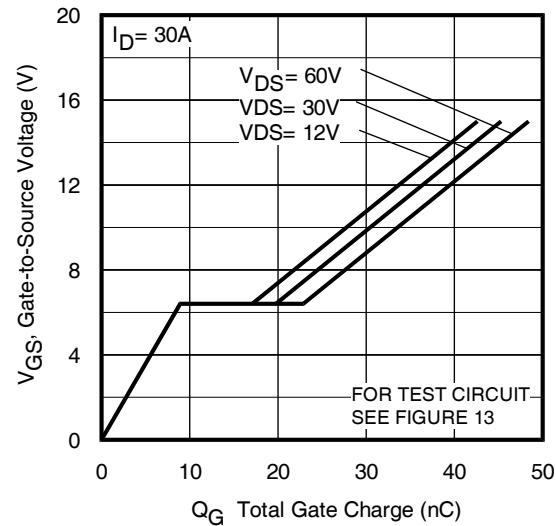
**Fig. 3** Typical Transfer Characteristics



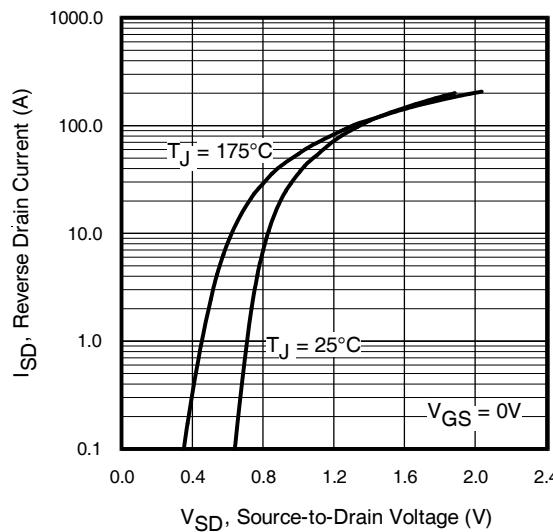
**Fig. 4** Typical Forward Transconductance Vs. Drain Current



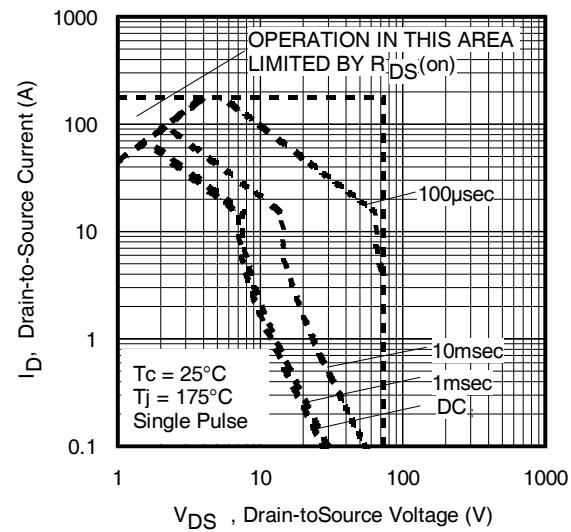
**Fig 5.** Typical Capacitance vs.  
Drain-to-Source Voltage



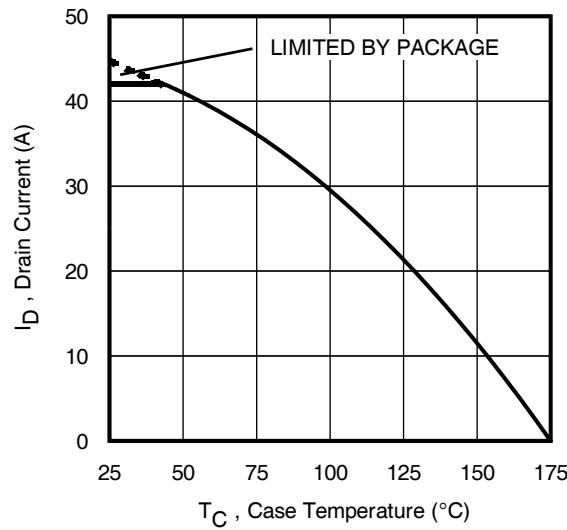
**Fig 6.** Typical Gate Charge vs.  
Gate-to-Source Voltage



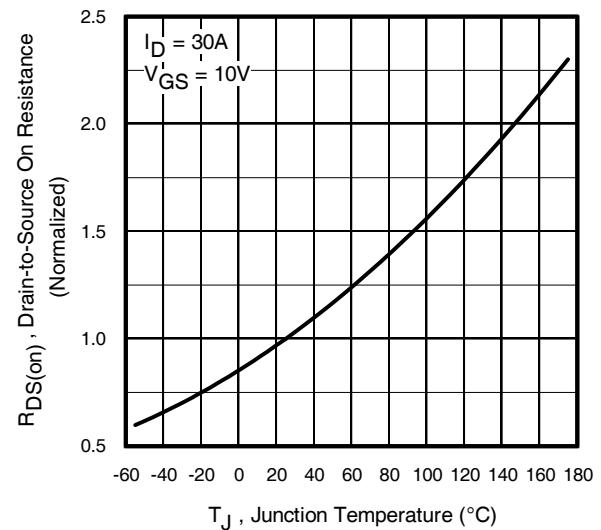
**Fig. 7** Typical Source-to-Drain Diode  
Forward Voltage



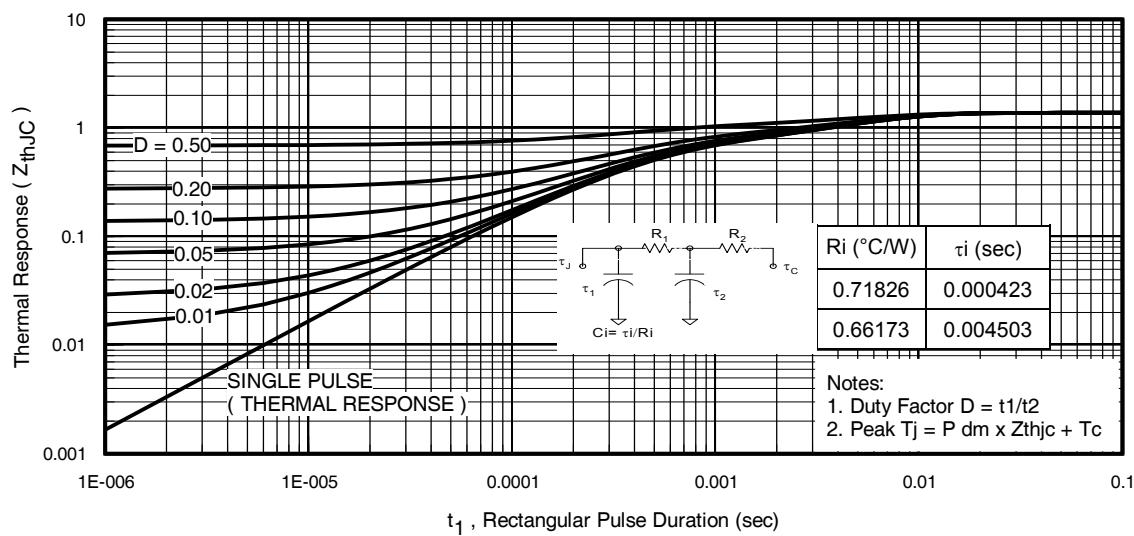
**Fig 8.** Maximum Safe Operating Area



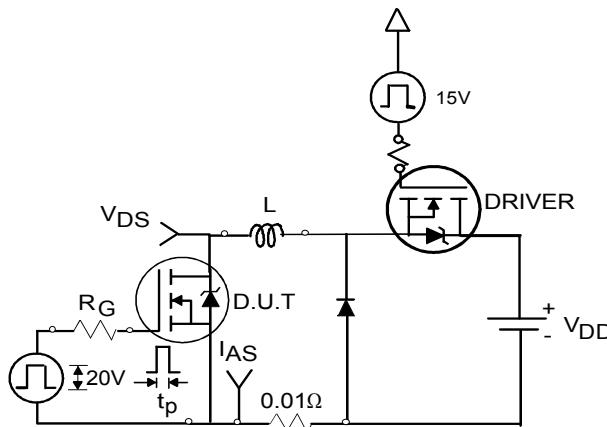
**Fig 9.** Maximum Drain Current Vs. Case Temperature



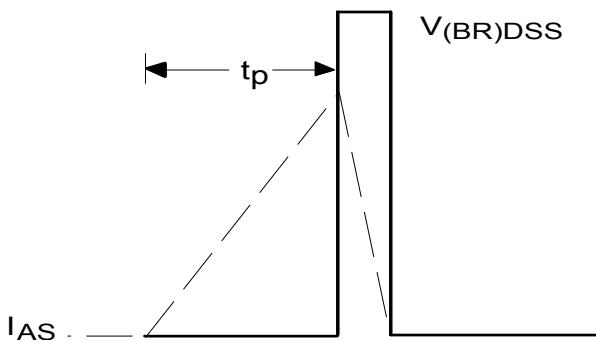
**Fig 10.** Normalized On-Resistance Vs. Temperature



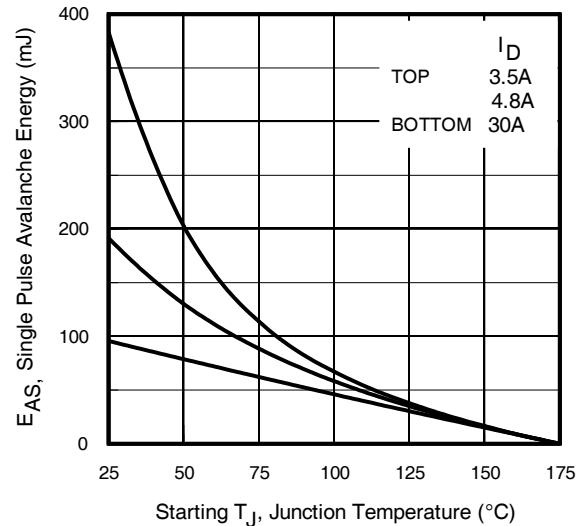
**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case



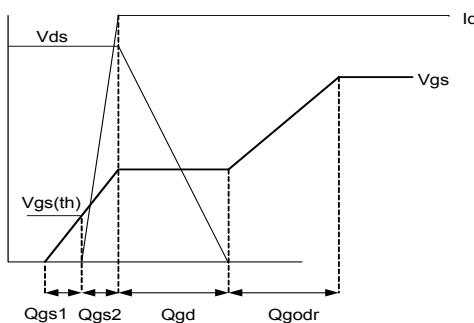
**Fig 12a.** Unclamped Inductive Test Circuit



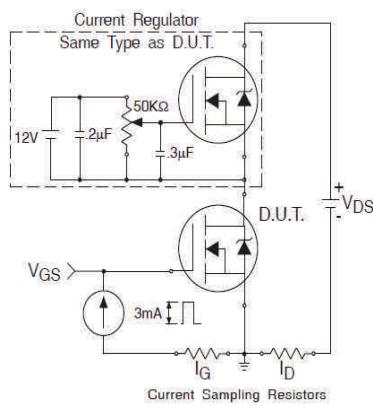
**Fig 12b.** Unclamped Inductive Waveforms



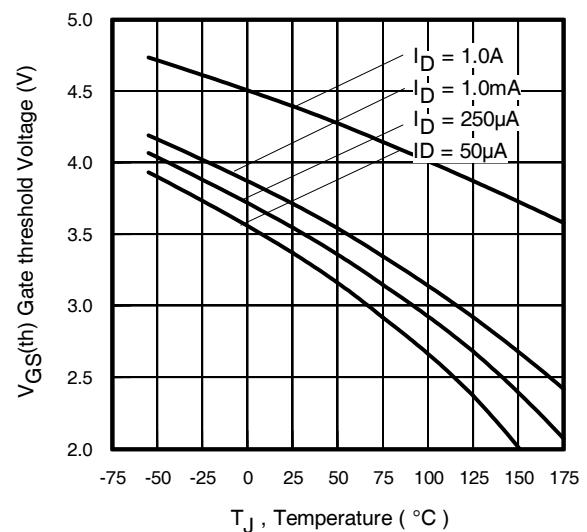
**Fig 12c.** Maximum Avalanche Energy vs. Drain Current



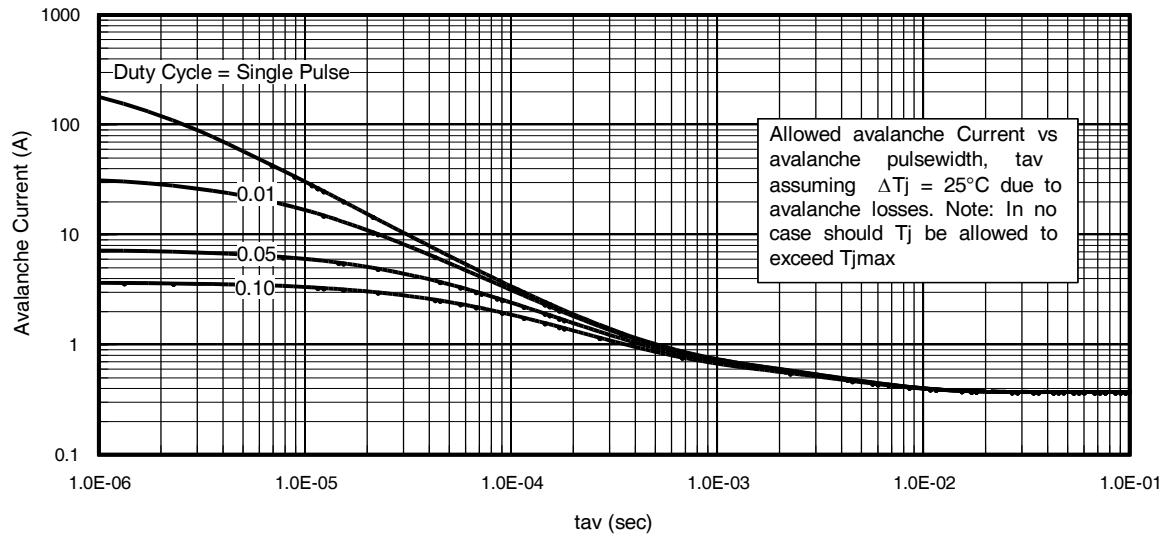
**Fig 13a.** Gate Charge Waveform



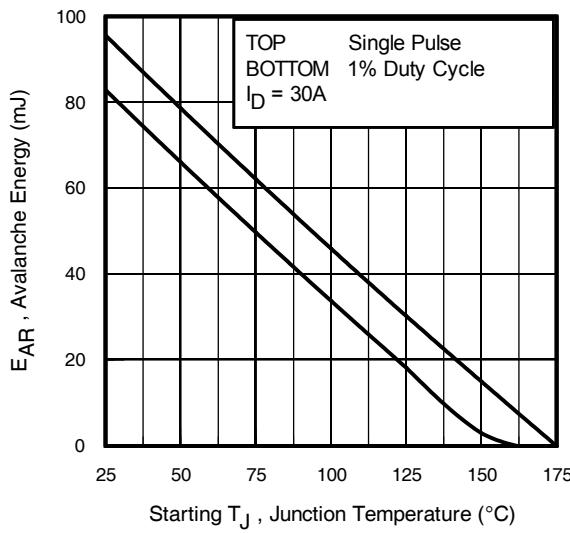
**Fig 13b.** Gate Charge Test Circuit



**Fig 14.** Threshold Voltage Vs. Temperature



**Fig 15.** Typical Avalanche Current Vs.Pulsewidth



**Fig 16.** Maximum Avalanche Energy Vs. Temperature

#### Notes on Repetitive Avalanche Curves , Figures 15, 16:

(For further info, see AN-1005 at [www.infineon.com](http://www.infineon.com))

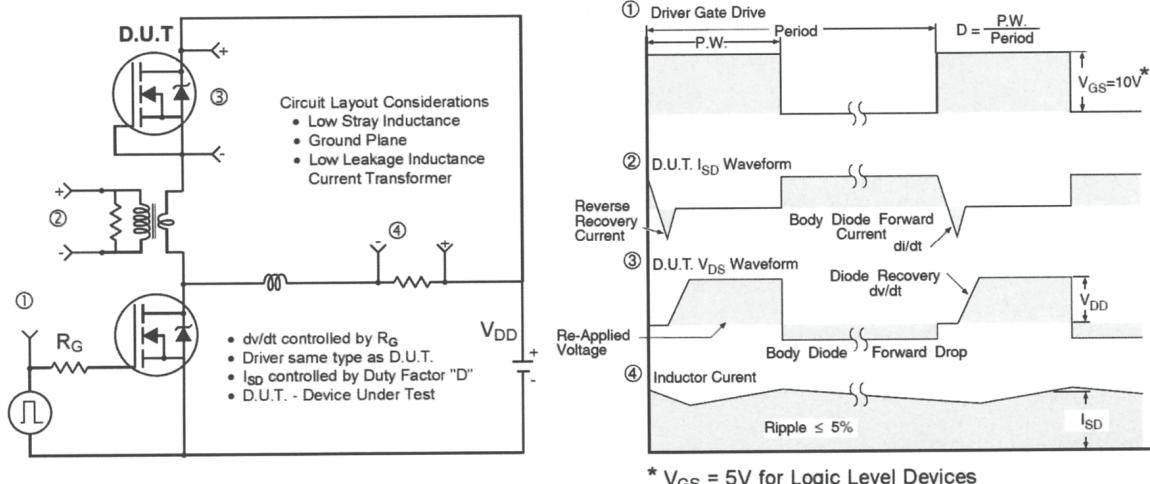
1. Avalanche failures assumption:  
Purely a thermal phenomenon and failure occurs at a temperature far in excess of  $T_{jmax}$ . This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as  $T_{jmax}$  is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 12a, 12b.
4.  $P_{D(ave)}$  = Average power dissipation per single avalanche pulse.
5.  $BV$  = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6.  $I_{av}$  = Allowable avalanche current.
7.  $\Delta T$  = Allowable rise in junction temperature, not to exceed  $T_{jmax}$  (assumed as  $25^\circ\text{C}$  in Figure 15, 16).

tav = Average time in avalanche.  
 $D$  = Duty cycle in avalanche =  $t_{av} \cdot f$   
 $Z_{thJC}(D, tav)$  = Transient thermal resistance, see Figures 13)

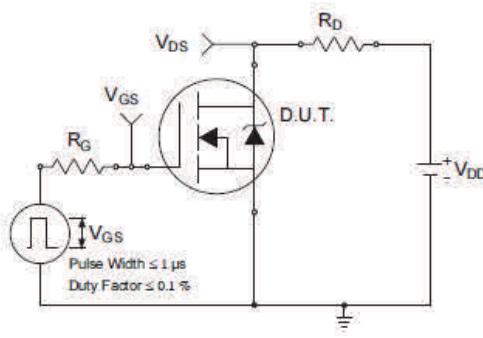
$$P_{D(ave)} = 1/2 (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$

$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$

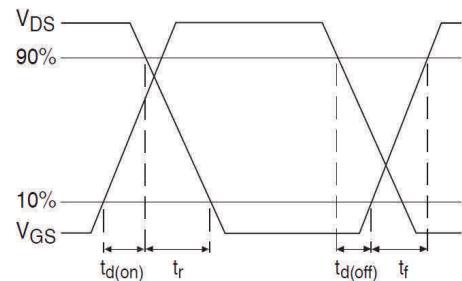
$$E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$$



**Fig 17.** Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

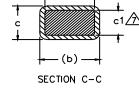
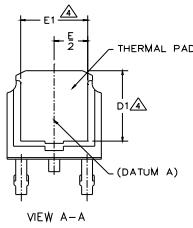
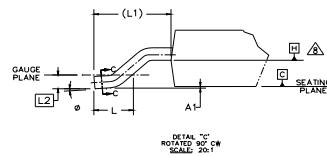
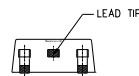
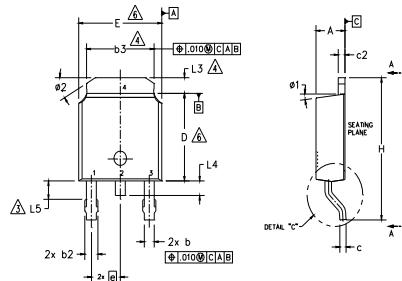


**Fig 18a.** Switching Time Test Circuit



**Fig 18b.** Switching Time Waveforms

## D-Pak (TO-252AA) Package Outline (Dimensions are shown in millimeters (inches))



## NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. DIMENSION ARE SHOWN IN INCHES [MILLIMETERS].
3. LEAD DIMENSION UNCONTROLLED IN L5.
4. DIMENSION D1, E1, L3 & b3 ESTABLISH A MINIMUM MOUNTING SURFACE FOR THERMAL PAD.
5. SECTION C-C DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .005 AND 0.10 [0.13 AND 0.25] FROM THE LEAD TIP.
6. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005 [0.13] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
7. DIMENSION b1 & c1 APPLIED TO BASE METAL ONLY.
8. DATUM A & B TO BE DETERMINED AT DATUM PLANE H.
9. OUTLINE CONFORMS TO JEDEC OUTLINE TO-252AA.

S Y M B O L	DIMENSIONS				N O T E S	
	MILLIMETERS		INCHES			
	MIN.	MAX.	MIN.	MAX.		
A	2.18	2.39	.086	.094		
A1	—	0.13	—	.005		
b	0.64	0.89	.025	.035		
b1	0.65	0.79	.025	.031	7	
b2	0.76	1.14	.030	.045		
b3	4.95	5.46	.195	.215	4	
c	0.46	0.61	.018	.024		
c1	0.41	0.56	.016	.022	7	
c2	0.46	0.89	.018	.035		
D	5.97	6.22	.235	.245	6	
D1	5.21	—	.205	—	4	
E	6.35	6.73	.250	.265	6	
E1	4.32	—	.170	—	4	
e	2.29	BSC	.090	BSC		
H	9.40	10.41	.370	.410		
L	1.40	1.78	.055	.070		
L1	2.74	BSC	.108	REF.		
L2	0.51	BSC	.020	BSC		
L3	0.89	1.27	.035	.050	4	
L4	—	1.02	—	.040		
L5	1.14	1.52	.045	.060	3	
Ø	0°	10°	0°	10°		
Ø1	0°	15°	0°	15°		
Ø2	25°	35°	25°	35°		

## LEAD ASSIGNMENTS

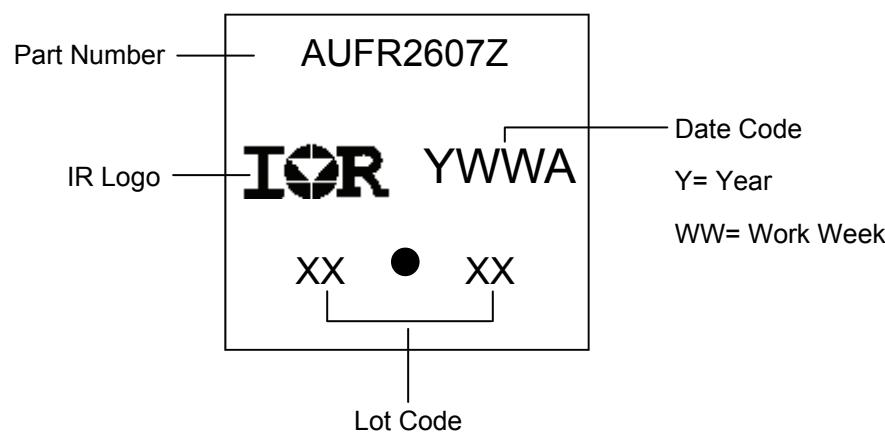
## HEXFET

1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

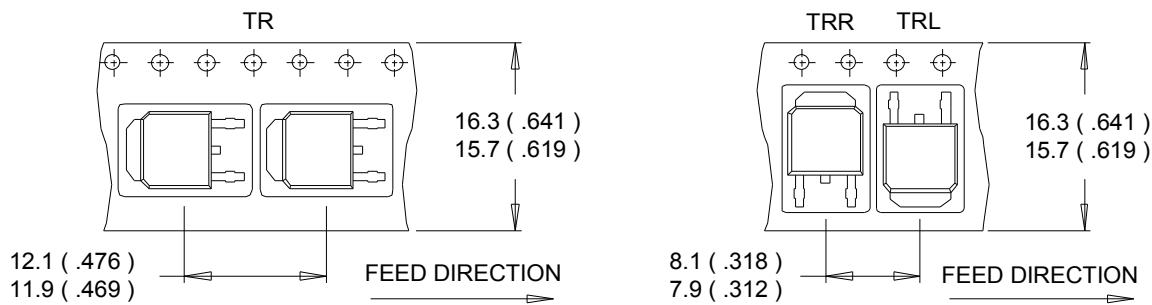
## IGBT &amp; CoPAK

1. GATE
2. COLLECTOR
3. Emitter
4. COLLECTOR

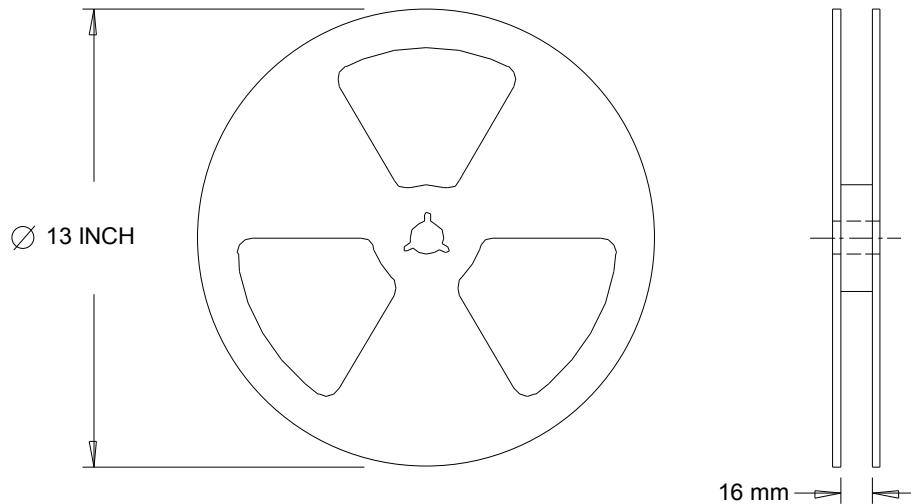
## D-Pak (TO-252AA) Part Marking Information



Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

**D-Pak (TO-252AA) Tape & Reel Information (Dimensions are shown in millimeters (inches))****NOTES :**

1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS ( INCHES ).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.

**NOTES :**

1. OUTLINE CONFORMS TO EIA-481.

Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

## Qualification Information

Qualification Level		Automotive (per AEC-Q101)	
		Comments: This part number(s) passed Automotive qualification. Infineon's Industrial and Consumer qualification level is granted by extension of the higher Automotive level.	
Moisture Sensitivity Level		D-Pak	MSL1
ESD	Machine Model	Class M4 (+/- 425V) <sup>†</sup> AEC-Q101-002	
	Human Body Model	Class H1B (+/- 1000V) <sup>†</sup> AEC-Q101-001	
	Charged Device Model	Class C5 (+/- 1125V) <sup>†</sup> AEC-Q101-005	
RoHS Compliant		Yes	

<sup>†</sup> Highest passing voltage.

## Revision History

Date	Comments
10/12/2015	<ul style="list-style-type: none"> <li>• Updated datasheet with corporate template</li> <li>• Corrected ordering table on page 1.</li> </ul>

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