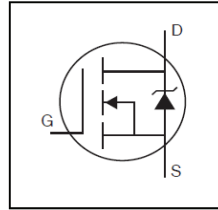


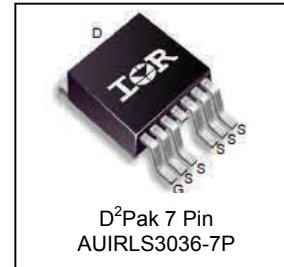
**Features**

- Advanced Process Technology
- Ultra Low On-Resistance
- Logic Level Gate Drive
- Dynamic dv/dt Rating
- 175°C Operating Temperature
- Fast Switching
- Repetitive Avalanche Allowed up to Tjmax
- Lead-Free, RoHS Compliant
- Automotive Qualified \*



HEXFET® Power MOSFET

$V_{DSS}$	<b>60V</b>
$R_{DS(on)}$ <b>typ.</b>	<b>1.5mΩ</b>
	<b>max.</b>
$I_D$ (Silicon Limited)	<b>300A</b> Ⓞ
$I_D$ (Package Limited)	<b>240A</b>



G	D	S
Gate	Drain	Source

**Description**

Specifically designed for Automotive applications, this HEXFET® Power MOSFET utilizes the latest processing techniques to achieve extremely low on-resistance per silicon area. Additional features of this design are a 175°C junction operating temperature, fast switching speed and improved repetitive avalanche rating. These features combine to make this design an extremely efficient and reliable device for use in Automotive applications and a wide variety of other applications.

Base Part Number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
AUIRLS3036-7P	D <sup>2</sup> Pak 7 Pin	Tube	50	AUIRLS3036-7P
		Tape and Reel Left	800	AUIRLS3036-7TRL

**Absolute Maximum Ratings**

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only; and functional operation of the device at these or any other condition beyond those indicated in the specifications is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions. Ambient temperature (TA) is 25°C, unless otherwise specified.

Symbol	Parameter	Max.	Units
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$ (Silicon Limited)	300Ⓞ	A
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$ (Silicon Limited)	210	
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$ (Package Limited)	240	
$I_{DM}$	Pulsed Drain Current ②	1000	
$P_D @ T_C = 25^\circ C$	Maximum Power Dissipation	380	W
	Linear Derating Factor	2.5	W/°C
$V_{GS}$	Gate-to-Source Voltage	± 16	V
$E_{AS}$	Single Pulse Avalanche Energy (Thermally Limited) ③	300	mJ
$I_{AR}$	Avalanche Current ②	See Fig.14,15, 22a, 22b	A
$E_{AR}$	Repetitive Avalanche Energy ②		mJ
dv/dt	Peak Diode Recovery ④	8.1	V/ns
$T_J$	Operating Junction and Storage Temperature Range	-55 to + 175	°C
$T_{STG}$			
	Soldering Temperature, for 10 seconds (1.6mm from case)	300	

**Thermal Resistance**

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ⑨⑩	—	0.40	°C/W
$R_{\theta JA}$	Junction-to-Ambient ⑧	—	40	

HEXFET® is a registered trademark of Infineon.

\*Qualification standards can be found at [www.infineon.com](http://www.infineon.com)

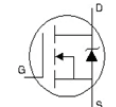
**Static @ T<sub>J</sub> = 25°C (unless otherwise specified)**

	Parameter	Min.	Typ.	Max.	Units	Conditions
V <sub>(BR)DSS</sub>	Drain-to-Source Breakdown Voltage	60	—	—	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA
ΔV <sub>(BR)DSS</sub> /ΔT <sub>J</sub>	Breakdown Voltage Temp. Coefficient	—	0.059	—	V/°C	Reference to 25°C, I <sub>D</sub> = 5mA ②
R <sub>DS(on)</sub>	Static Drain-to-Source On-Resistance	—	1.5	1.9	mΩ	V <sub>GS</sub> = 10V, I <sub>D</sub> = 180A ⑤
		—	1.7	2.2		V <sub>GS</sub> = 4.5V, I <sub>D</sub> = 150A ⑤
V <sub>GS(th)</sub>	Gate Threshold Voltage	1.0	—	2.5	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA
g <sub>fs</sub>	Forward Trans conductance	390	—	—	S	V <sub>DS</sub> = 10V, I <sub>D</sub> = 180A
R <sub>G</sub>	Gate Resistance	—	1.9	—	Ω	
I <sub>DSS</sub>	Drain-to-Source Leakage Current	—	—	20	μA	V <sub>DS</sub> = 60V, V <sub>GS</sub> = 0V
		—	—	250		V <sub>DS</sub> = 60V, V <sub>GS</sub> = 0V, T <sub>J</sub> = 125°C
I <sub>GSS</sub>	Gate-to-Source Forward Leakage	—	—	100	nA	V <sub>GS</sub> = 16V
	Gate-to-Source Reverse Leakage	—	—	-100		V <sub>GS</sub> = -16V

**Dynamic Electrical Characteristics @ T<sub>J</sub> = 25°C (unless otherwise specified)**

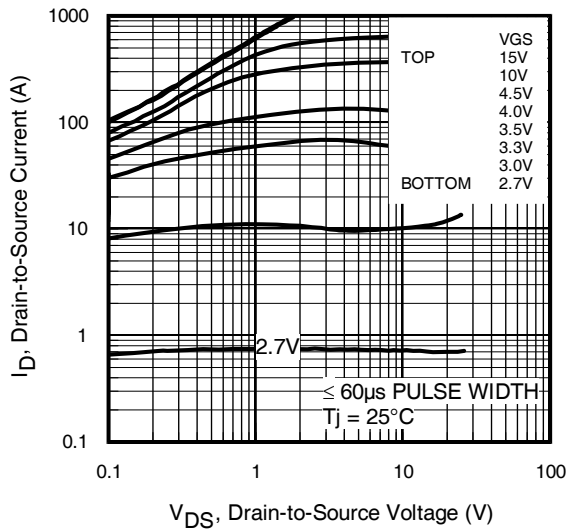
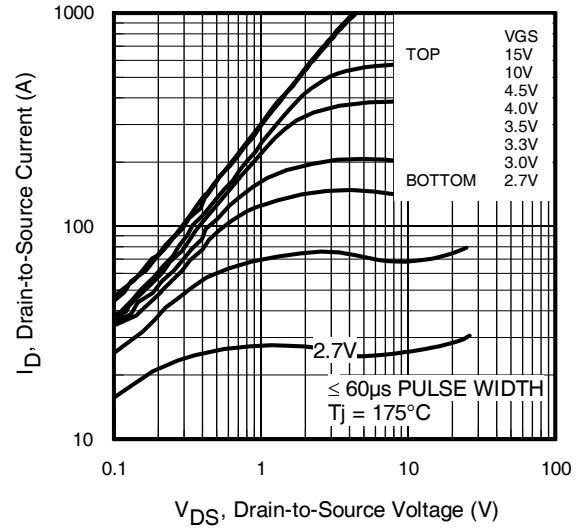
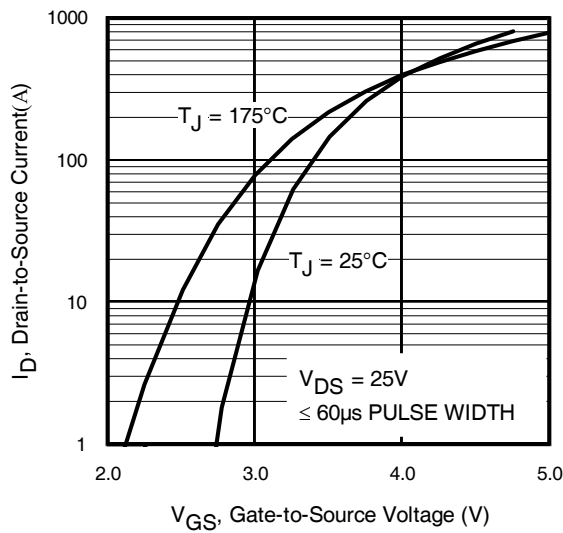
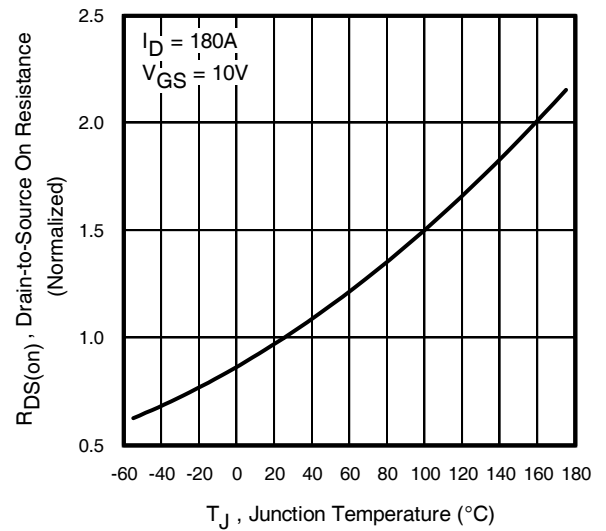
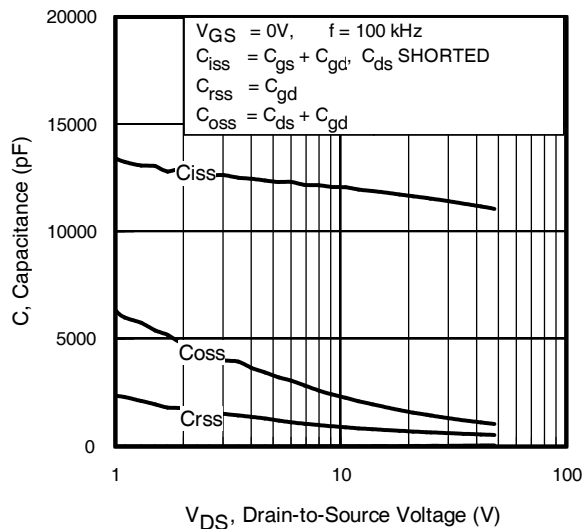
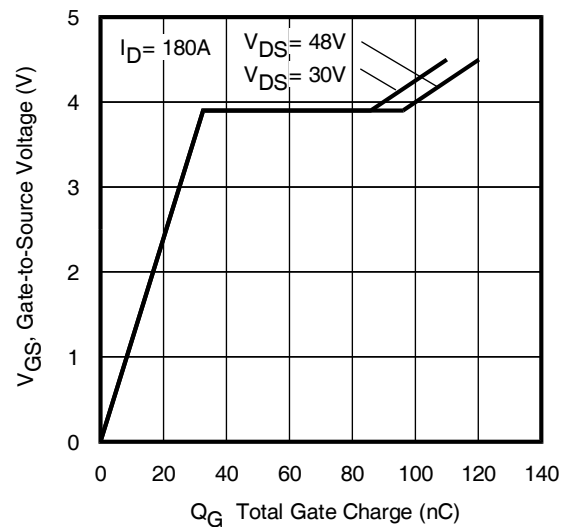
Q <sub>g</sub>	Total Gate Charge	—	110	160	nC	I <sub>D</sub> = 180A V <sub>DS</sub> = 30V V <sub>GS</sub> = 4.5V ⑤
Q <sub>gs</sub>	Gate-to-Source Charge	—	33	—		
Q <sub>gd</sub>	Gate-to-Drain Charge	—	53	—		
Q <sub>sync</sub>	Total Gate Charge Sync. (Q <sub>g</sub> - Q <sub>gd</sub> )	—	57	—		
t <sub>d(on)</sub>	Turn-On Delay Time	—	81	—	ns	V <sub>DD</sub> = 39V I <sub>D</sub> = 180A R <sub>G</sub> = 2.1Ω V <sub>GS</sub> = 4.5V ⑤
t <sub>r</sub>	Rise Time	—	540	—		
t <sub>d(off)</sub>	Turn-Off Delay Time	—	89	—		
t <sub>f</sub>	Fall Time	—	170	—		
C <sub>iss</sub>	Input Capacitance	—	11270	—	pF	V <sub>GS</sub> = 0V V <sub>DS</sub> = 50V f = 1.0MHz
C <sub>oss</sub>	Output Capacitance	—	1025	—		
C <sub>rss</sub>	Reverse Transfer Capacitance	—	520	—		
C <sub>oss eff.(ER)</sub>	Effective Output Capacitance (Energy Related)	—	1460	—		
C <sub>oss eff.(TR)</sub>	Effective Output Capacitance (Time Related)	—	1630	—		

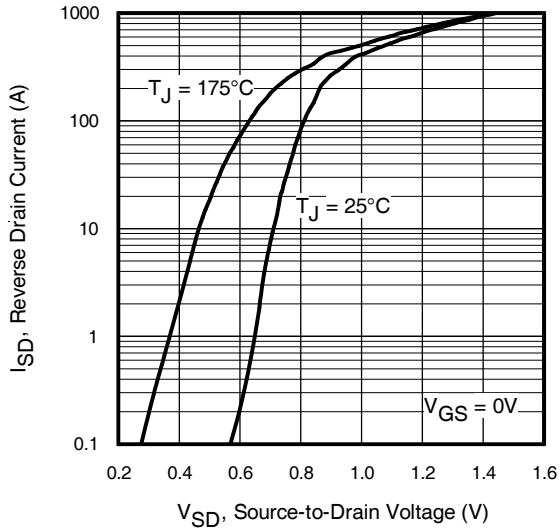
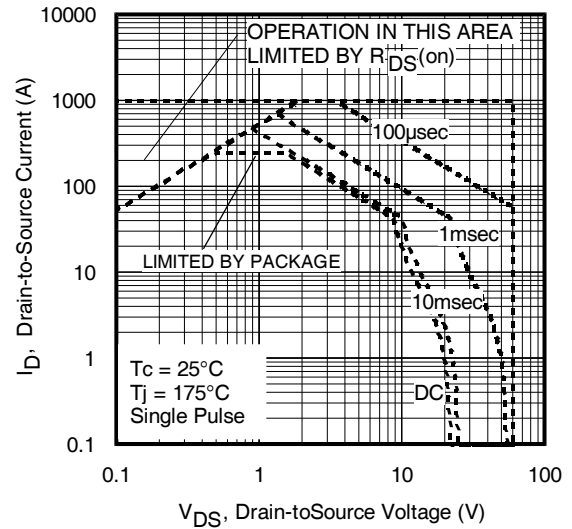
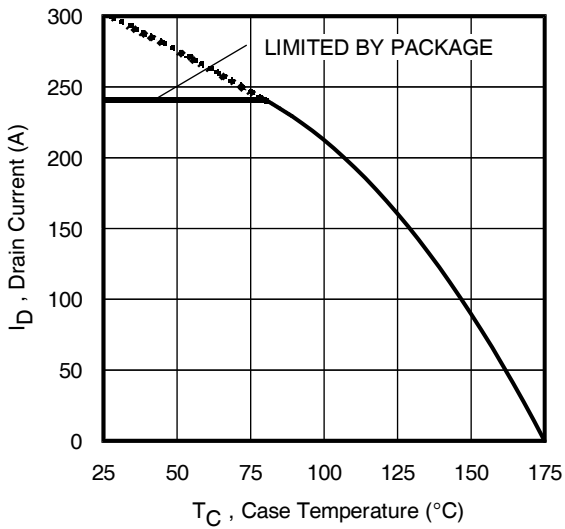
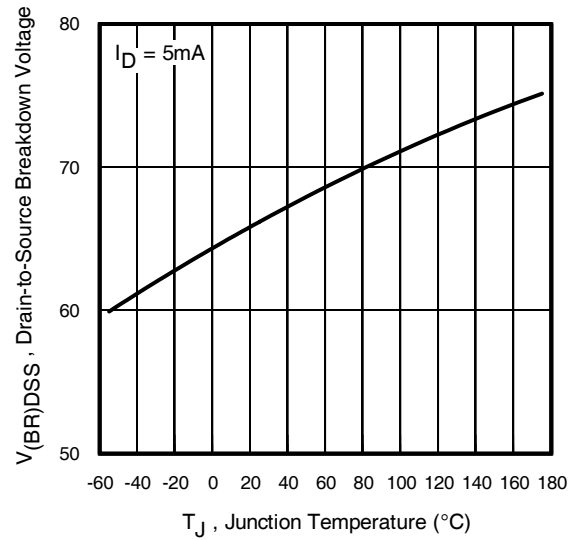
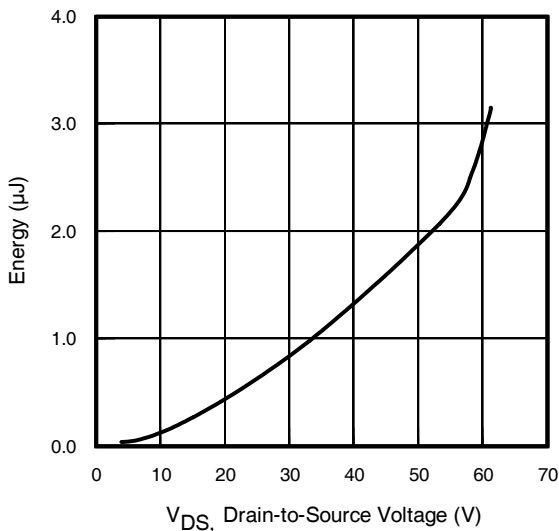
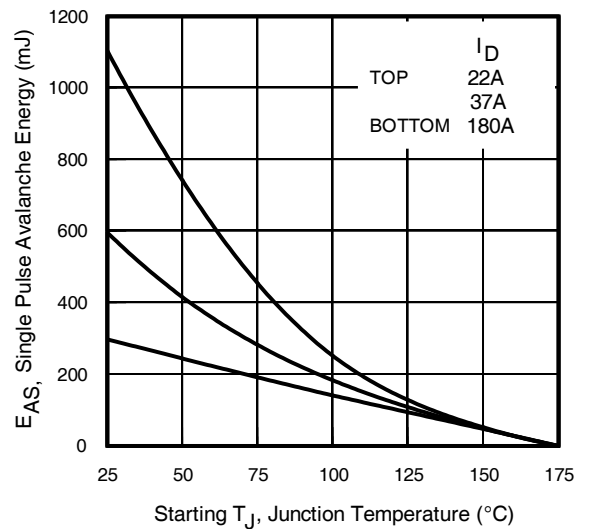
**Diode Characteristics**

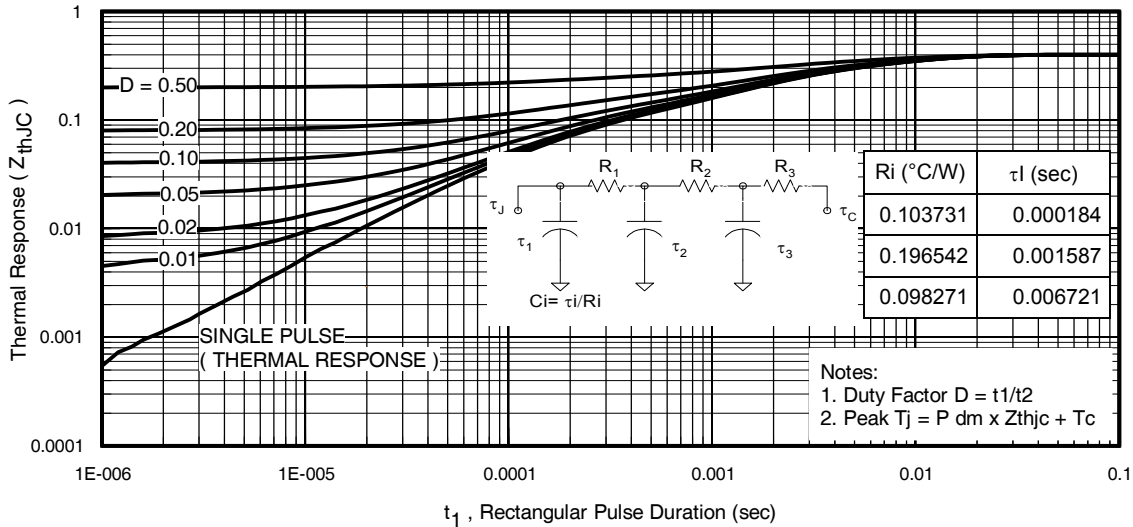
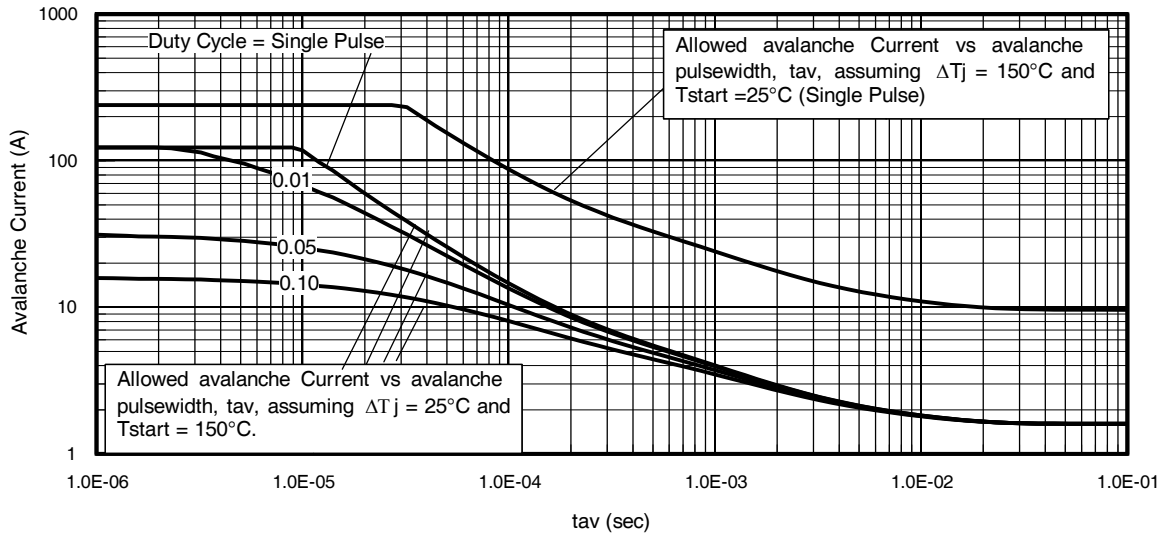
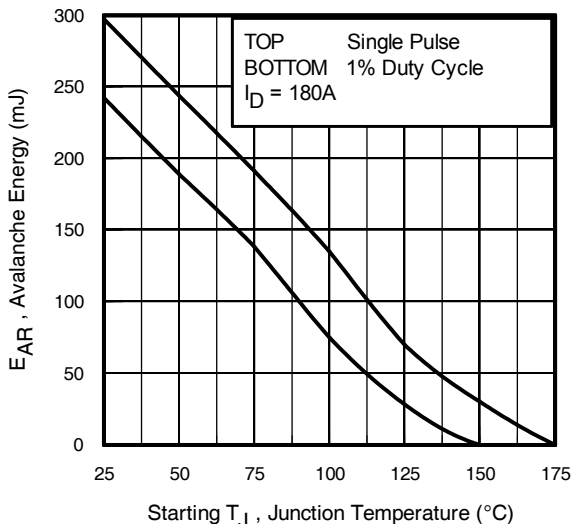
	Parameter	Min.	Typ.	Max.	Units	Conditions
I <sub>S</sub>	Continuous Source Current (Body Diode)	—	—	300 ①	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I <sub>SM</sub>	Pulsed Source Current (Body Diode) ②	—	—	1000		
V <sub>SD</sub>	Diode Forward Voltage	—	—	1.3	V	T <sub>J</sub> = 25°C, I <sub>S</sub> = 180A, V <sub>GS</sub> = 0V ③
t <sub>rr</sub>	Reverse Recovery Time	—	57	—	ns	T <sub>J</sub> = 25°C V <sub>DD</sub> = 51V
		—	60	—		T <sub>J</sub> = 125°C I <sub>F</sub> = 180A,
Q <sub>rr</sub>	Reverse Recovery Charge	—	140	—	nC	T <sub>J</sub> = 25°C di/dt = 100A/μs ⑤
		—	160	—		T <sub>J</sub> = 125°C
I <sub>RSM</sub>	Reverse Recovery Current	—	4.6	—	A	T <sub>J</sub> = 25°C
t <sub>on</sub>	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L <sub>S</sub> +L <sub>D</sub> )				

**Notes:**

- ① Calculated continuous current based on maximum allowable junction temperature. Bond wire current limit is 240A. Note that current limitations arising from heating of the device leads may occur with some lead mounting arrangements.
- ② Repetitive rating; pulse width limited by max. junction temperature.
- ③ Limited by T<sub>Jmax</sub>, starting T<sub>J</sub> = 25°C, L = 0.018mH, R<sub>G</sub> = 25Ω, I<sub>AS</sub> = 180A, V<sub>GS</sub> = 10V. Part not recommended for use above this value.
- ④ I<sub>SD</sub> ≤ 180A, di/dt ≤ 1070A/μs, V<sub>DD</sub> ≤ V<sub>(BR)DSS</sub>, T<sub>J</sub> ≤ 175°C.
- ⑤ Pulse width ≤ 400μs; duty cycle ≤ 2%.
- ⑥ C<sub>oss eff. (TR)</sub> is a fixed capacitance that gives the same charging time as C<sub>oss</sub> while V<sub>DS</sub> is rising from 0 to 80% V<sub>DSS</sub>.
- ⑦ C<sub>oss eff. (ER)</sub> is a fixed capacitance that gives the same energy as C<sub>oss</sub> while V<sub>DS</sub> is rising from 0 to 80% V<sub>DSS</sub>.
- ⑧ When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994
- ⑨ R<sub>θ</sub> is measured at T<sub>J</sub> approximately 90°C.
- ⑩ R<sub>θJC</sub> value shown is at time zero.


**Fig. 1** Typical Output Characteristics

**Fig. 2** Typical Output Characteristics

**Fig. 3** Typical Transfer Characteristics

**Fig. 4** Normalized On-Resistance vs. Temperature

**Fig. 5.** Typical Capacitance vs. Drain-to-Source Voltage

**Fig. 6.** Typical Gate Charge vs. Gate-to-Source Voltage


**Fig. 7** Typical Source-to-Drain Diode Forward Voltage

**Fig 8.** Maximum Safe Operating Area

**Fig 9.** Maximum Drain Current vs. Case Temperature

**Fig 10.** Drain-to-Source Breakdown Voltage

**Fig 11.** Typical Coss Stored Energy

**Fig 12.** Maximum Avalanche Energy vs. Drain Current


**Fig 13. Maximum Effective Transient Thermal Impedance, Junction-to-Case**

**Fig 14. Avalanche Current vs. Pulse width**

**Notes on Repetitive Avalanche Curves , Figures 14, 15:  
 (For further info, see AN-1005 at www.infineon.com)**

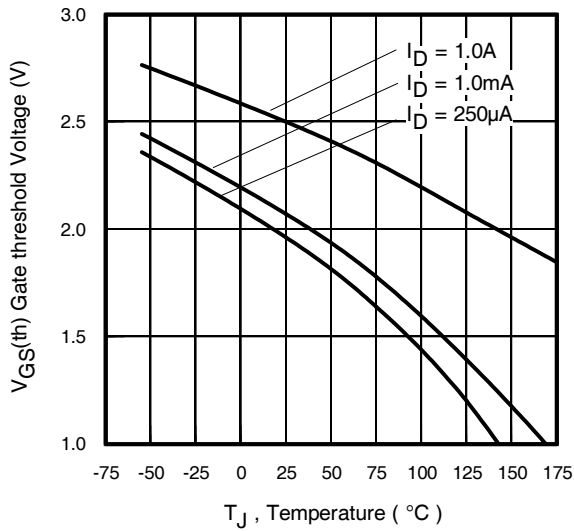
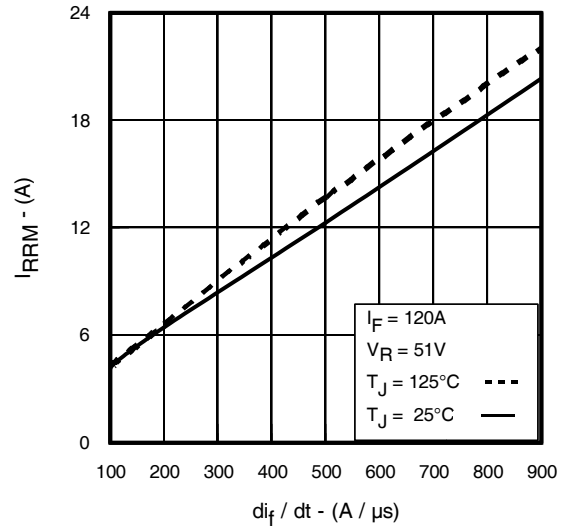
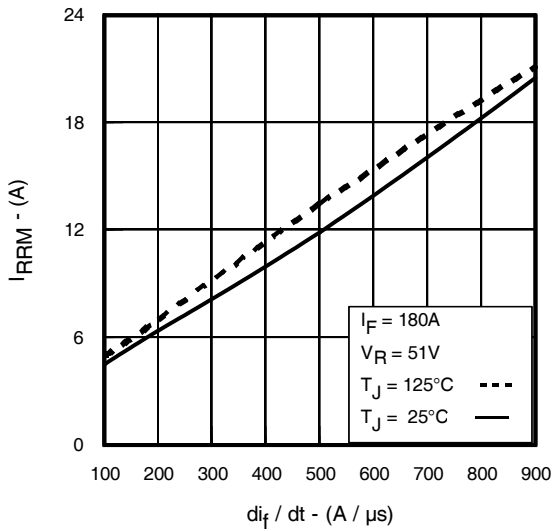
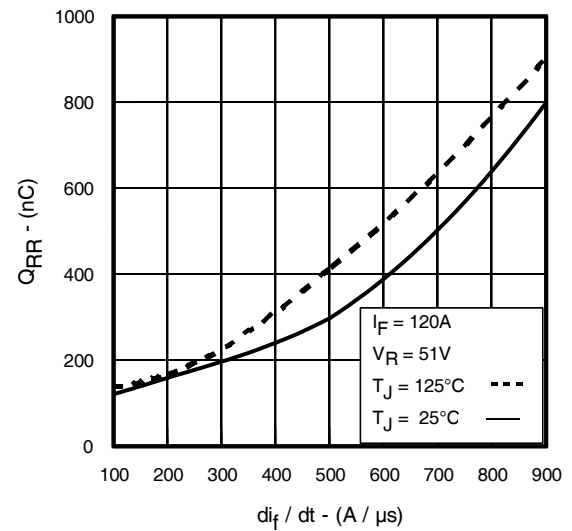
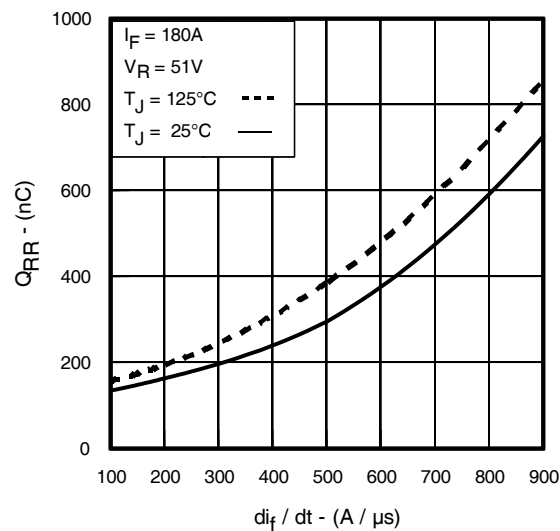
1. Avalanche failures assumption:  
Purely a thermal phenomenon and failure occurs at a temperature far in excess of  $T_{jmax}$ . This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as  $T_{jmax}$  is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 22a, 22b.
4.  $P_{D(ave)}$  = Average power dissipation per single avalanche pulse.
5.  $BV$  = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6.  $I_{av}$  = Allowable avalanche current.
7.  $\Delta T$  = Allowable rise in junction temperature, not to exceed  $T_{jmax}$  (assumed as 25°C in Figure 13, 14).  
 $t_{av}$  = Average time in avalanche.  
 $D$  = Duty cycle in avalanche =  $t_{av} \cdot f$   
 $Z_{thJC}(D, t_{av})$  = Transient thermal resistance, see Figures 13)

$$P_{D(ave)} = 1/2 ( 1.3 \cdot BV \cdot I_{av} ) = \Delta T / Z_{thJC}$$

$$I_{av} = 2\Delta T / [ 1.3 \cdot BV \cdot Z_{th} ]$$

$$E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$$

**Fig 15. Maximum Avalanche Energy vs. Temperature**


**Fig. 16.** Threshold Voltage vs. Temperature

**Fig. 17 -** Typical Recovery Current vs.  $di/dt$ 

**Fig. 18 -** Typical Recovery Current vs.  $di/dt$ 

**Fig. 19 -** Typical Stored Charge vs.  $di/dt$ 

**Fig. 20 -** Typical Stored Charge vs.  $di/dt$

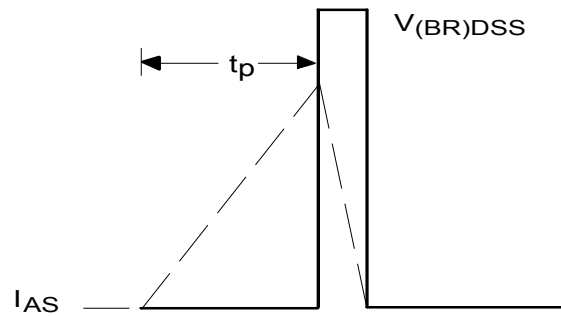


\*  $V_{GS} = 5V$  for Logic Level Devices

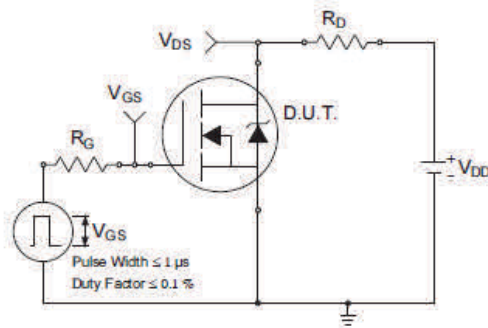
**Fig 21.** Peak Diode Recovery  $dv/dt$  Test Circuit for N-Channel HEXFET® Power MOSFETs



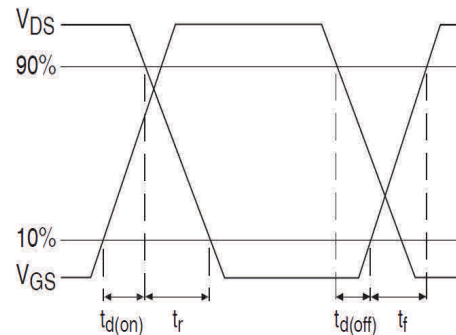
**Fig 22a.** Unclamped Inductive Test Circuit



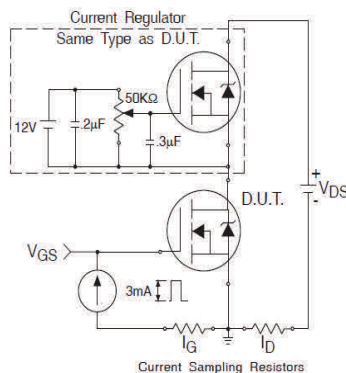
**Fig 22b.** Unclamped Inductive Waveforms



**Fig 23a.** Switching Time Test Circuit



**Fig 23b.** Switching Time Waveforms



**Fig 24a.** Gate Charge Test Circuit



**Fig 24b.** Gate Charge Waveform

## D<sup>2</sup>Pak - 7 Pin Package Outline (Dimensions are shown in millimeters (inches))

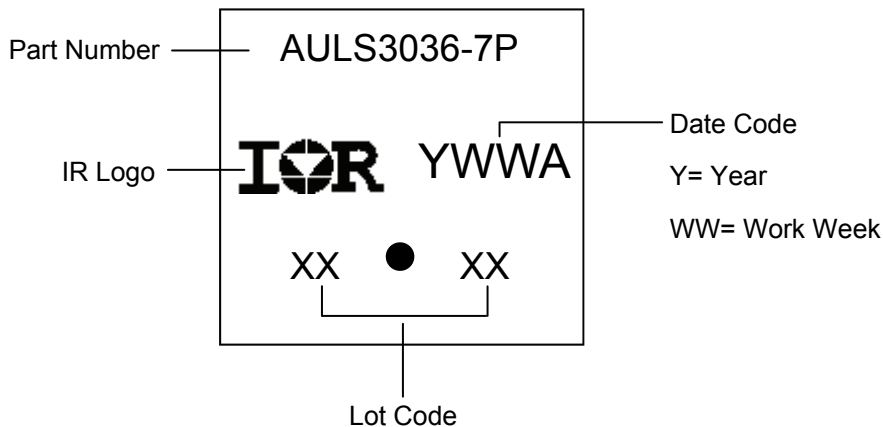


SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	
A1	—	0.254	—	.010	
b	0.51	0.99	.020	.036	
b1	0.51	0.89	.020	.032	5
c	0.38	0.74	.015	.029	
c1	0.38	0.58	.015	.023	5
c2	1.14	1.65	.045	.065	
D	8.38	9.65	.330	.380	3
D1	6.86	7.42	.270	.292	4
E	9.65	10.54	.380	.415	3,4
E1	6.22	8.48	.245	.334	4
e	1.27 BSC		.050 BSC		
H	14.61	15.88	.575	.625	
L	1.78	2.79	.070	.110	
L1	—	1.68	—	.066	4
L2	—	1.78	—	.070	
L3	0.25 BSC		.010 BSC		

### NOTES:

1. DIMENSIONING AND TOLERANCING AS PER ASME Y14.5M-1994
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [0.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
4. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSION E, L1, D1 & E1.
5. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
6. DATUM A & B TO BE DETERMINED AT DATUM PLANE H.
7. CONTROLLING DIMENSION: INCH.
8. OUTLINE CONFORMS TO JEDEC OUTLINE TO-263CB. EXCEPT FOR DIMS. E, E1 & D1.

## D<sup>2</sup>Pak - 7 Pin Part Marking Information



Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>



# D<sup>2</sup>Pak - 7 Pin Tape and Reel

NOTES, TAPE & REEL, LABELLING:

1. TAPE AND REEL.

- 1.1 REEL SIZE 13 INCH DIAMETER.
- 1.2 EACH REEL CONTAINING 800 DEVICES.
- 1.3 THERE SHALL BE A MINIMUM OF 42 SEALED POCKETS CONTAINED IN THE LEADER AND A MINIMUM OF 15 SEALED POCKETS IN THE TRAILER.
- 1.4 PEEL STRENGTH MUST CONFORM TO THE SPEC. NO. 71-9667.
- 1.5 PART ORIENTATION SHALL BE AS SHOWN BELOW.
- 1.6 REEL MAY CONTAIN A MAXIMUM OF TWO UNIQUE LOT CODE/DATE CODE COMBINATIONS. REWORKED REELS MAY CONTAIN A MAXIMUM OF THREE UNIQUE LOT CODE/DATE CODE COMBINATIONS. HOWEVER, THE LOT CODES AND DATE CODES WITH THEIR RESPECTIVE QUANTITIES SHALL APPEAR ON THE BAR CODE LABEL FOR THE AFFECTED REEL.

2. LABELLING (REEL AND SHIPPING BAG).

- 2.1 CUST. PART NUMBER (BAR CODE): IRFXXXXSTRL-7P
- 2.2 CUST. PART NUMBER (TEXT CODE): IRFXXXXSTRL-7P
- 2.3 I.R. PART NUMBER: IRFXXXXSTRL-7P
- 2.4 QUANTITY:
- 2.5 VENDOR CODE: IR
- 2.6 LOT CODE:
- 2.7 DATE CODE:



Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

**Qualification Information**

<b>Qualification Level</b>		Automotive (per AEC-Q101)	
		Comments: This part number(s) passed Automotive qualification. Infineon's Industrial and Consumer qualification level is granted by extension of the higher Automotive level.	
<b>Moisture Sensitivity Level</b>		D <sup>2</sup> -Pak 7 Pin	MSL1
<b>ESD</b>	Machine Model	Class M4 (+/- 800V) <sup>†</sup> AEC-Q101-002	
	Human Body Model	Class H3A (+/- 6000V) <sup>†</sup> AEC-Q101-001	
	Charged Device Model	Class C5 (+/- 2000V) <sup>†</sup> AEC-Q101-005	
<b>RoHS Compliant</b>		Yes	

† Highest passing voltage.

**Revision History**

Date	Comments
4/2/2014	<ul style="list-style-type: none"> <li>Added "Logic Level Gate Drive" bullet in the features section on page 1</li> <li>Updated part marking on page 8</li> <li>Updated typo on the fig.19 and fig.20, unit of y-axis from "A" to "nC" on page 6.</li> <li>Updated data sheet with new IR corporate template</li> </ul>
11/4/2015	<ul style="list-style-type: none"> <li>Updated datasheet with corporate template</li> <li>Corrected ordering table on page 1.</li> </ul>

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