

## LP3879 Micropower 800mA Low Noise "Ceramic Stable" Voltage Regulator for Low Voltage Applications

Check for Samples: [LP3879](#)

### FEATURES

- **Standard Output Voltage:** 1.00V, 1.20V
- **Custom Voltages Available from 1.0V to 1.2V (50 mV Increments)**
- **Input Voltage:** 2.5 to 6V
- **1% Initial Output Accuracy**
- **Designed for Use with Low ESR Ceramic Capacitors**
- **Very Low Output Noise**
- **Sense Option Improves Load Regulation**
- **8-Lead SO PowerPad and WSON Surface Mount Packages**
- **<10  $\mu$ A Quiescent Current in Shutdown**
- **Low Ground Pin Current at all Loads**
- **High Peak Current Capability**
- **Over-Temperature/Over-Current Protection**
- **-40°C to +125°C Junction Temperature Range**

### DESCRIPTION

The LP3879 is a 800 mA fixed-output voltage regulator designed to provide high performance and low noise in applications requiring output voltages between 1.0V and 1.2V.

Using an optimized VIP (Vertically Integrated PNP) process, the LP3879 delivers superior performance:

**Ground Pin Current:** Typically 5.5 mA @ 800 mA load, and 200  $\mu$ A @ 100  $\mu$ A load.

**Low Power Shutdown:** The LP3879 draws less than 10  $\mu$ A quiescent current when shutdown pin is pulled low.

**Precision Output:** Ensured output voltage accuracy is 1% at room temperature.

**Low Noise:** Broadband output noise is only 18  $\mu$ V (typical) with 10 nF bypass capacitor.

### APPLICATIONS

- **ASIC Power Supplies In:**
  - Desktops, Notebooks and Graphic Cards
  - Set Top Boxes, Printers and Copiers
- **DSP and FPGA Power Supplies**
- **SMPS Post-Regulator**
- **Medical Instrumentation**



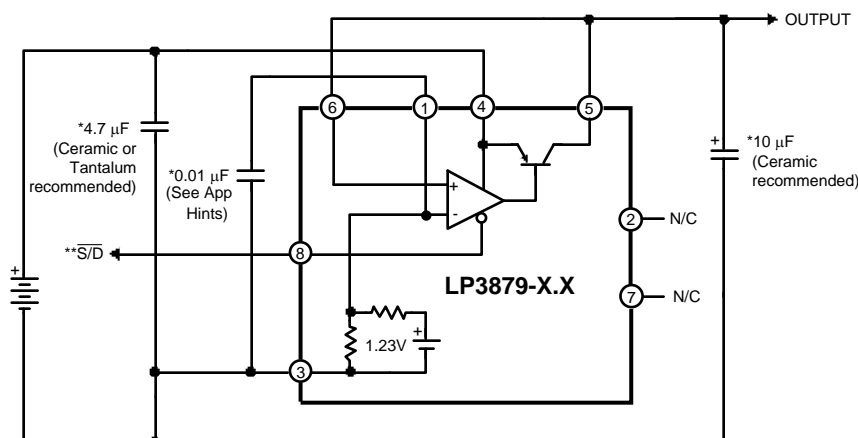
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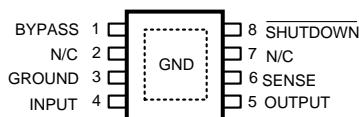
## Basic Application Circuit



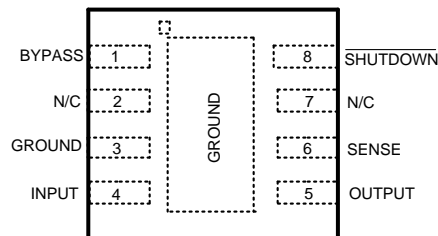
\*Capacitance values shown are minimum required to assure stability. Larger output capacitor provides improved dynamic response. Output capacitor must meet ESR requirements (see [Application Information](#)).

\*\*The Shutdown pin must be actively terminated (see [Application Information](#)). Tie to INPUT (Pin 4) if not used.

## Connection Diagram



**Figure 1. Top View  
8-Lead SO PowerPad  
See DDA0008B Package**



**Figure 2. Top View  
8-Lead WSON  
See NGT0008A Package**

## PIN DESCRIPTIONS

Pin	Name	Function
1	BYPASS	The capacitor connected between BYPASS and GROUND lowers output noise voltage level and is required for loop stability.
2	N/C	DO NOT CONNECT. This pin is used for post package test and must be left floating.
3	GROUND	Device ground.
4	INPUT	Input source voltage.
5	OUTPUT	Regulated output voltage.
6	SENSE	Remote Sense. Tie directly to output or remotely at point of load for best regulation.
7	N/C	No internal connection.
8	SHUTDOWN	Output is enabled above turn-on threshold voltage. Pull down to turn off regulator output.
SO PowerPad, WSON	SUBSTRATE GROUND	The exposed die attach pad should be connected to a thermal pad at ground potential. For additional information on using Texas Instruments' Non Pull Back WSON package, please refer to WSON application note <a href="#">SNOA401</a>



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## Absolute Maximum Ratings<sup>(1)(2)</sup>

Storage Temperature Range	–65°C to +150°C
Operating Junction Temperature Range	–40°C to +125°C
Lead Temperature (Soldering, 5 seconds)	260°C
ESD Rating <sup>(3)</sup>	2 kV
Shutdown Pin	1kV
Power Dissipation <sup>(4)</sup>	Internally Limited
Input Supply Voltage (Survival)	–0.3V to +16V
Input Supply Voltage (Typical Operating)	2.5V to +6V
SENSE Pin	–0.3V to +6V
Output Voltage (Survival) <sup>(5)</sup>	–0.3V to +6V
I <sub>OUT</sub> (Survival)	Short Circuit Protected
Input-Output Voltage (Survival) <sup>(6)</sup>	–0.3V to +16V

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Electrical specifications do not apply when operating the device outside of its rated operating conditions.
- (2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
- (3) ESD testing was performed using Human Body Model, a 100 pF capacitor discharged through a 1.5 kΩ resistor.
- (4) The maximum allowable power dissipation is a function of the maximum junction temperature, T<sub>J</sub>(MAX), the junction-to-ambient thermal resistance, θ<sub>J-A</sub>, and the ambient temperature, T<sub>A</sub>. The maximum allowable power dissipation at any ambient temperature is calculated using: 
$$P (MAX) = \frac{T_J (MAX) - T_A}{\theta_{J-A}}$$

The value of θ<sub>J-A</sub> for the WSON and SO PowerPad packages are specifically dependent on PCB trace area, trace material, and the number of layers and thermal vias. If a four layer board is used with maximum vias from the IC center to the heat dissipating copper layers, values of θ<sub>J-A</sub> which can be obtained are approximately 60°C/W for the SO PowerPad and 40°C/W for the WSON package. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown.
- (5) If used in a dual-supply system where the regulator load is returned to a negative supply, the LP3879 output must be diode-clamped to ground.
- (6) The output PNP structure contains a diode between the V<sub>IN</sub> and V<sub>OUT</sub> terminals that is normally reverse-biased. Forcing the output above the input will turn on this diode and may induce a latch-up mode which can damage the part (see Application Hints).

## Electrical Characteristics

Limits in standard typeface are for  $T_J = 25^\circ\text{C}$ , and limits in **boldface type** apply over the temperature range of  $-40^\circ\text{C}$  to  $125^\circ\text{C}$ . Limits are ensured through design, testing, or correlation. The limits are used to calculate the Average Outgoing Quality Level (AOQL). Unless otherwise specified:  $V_{IN} = 3.0\text{V}$ ,  $V_{OUT} = 1\text{V}$ ,  $I_L = 1\text{ mA}$ ,  $C_{OUT} = 10\text{ }\mu\text{F}$ ,  $C_{IN} = 4.7\text{ }\mu\text{F}$ ,  $V_{S/D} = 2\text{V}$ ,  $C_{BYPASS} = 10\text{ nF}$ .

Symbol	Parameter	Conditions	Min <sup>(1)</sup>	Typical <sup>(2)</sup>	Max <sup>(1)</sup>	Units
$V_O$	Output Voltage Tolerance		-1.0	1.00	1.0	% $V_{nom}$
		$1\text{ mA} \leq I_L \leq 800\text{ mA}$ , $3.0\text{V} \leq V_{IN} \leq 6\text{V}$	-2.0 <b>-3.0</b>	1.00	2.0 <b>3.0</b>	
$\frac{\Delta V_{OUT}}{\Delta V_{IN}}$	Output Voltage Line Regulation	$3.0\text{V} \leq V_{IN} \leq 6\text{V}$		0.007	0.014	% $V$
					<b>0.032</b>	
$V_{IN}(\text{min})$	Minimum Input Voltage Required To Maintain Output Regulation	$I_L = 800\text{ mA}$ , $V_{OUT} \geq V_{OUT(NOM)} - 1\%$		2.5	<b>3.1</b>	$V$
		$I_L = 800\text{ mA}$ , $V_{OUT} \geq V_{OUT(NOM)} - 1\%$ $0 \leq T_J \leq 125^\circ\text{C}$		2.5	<b>2.8</b>	
		$I_L = 750\text{ mA}$ , $V_{OUT} \geq V_{OUT(NOM)} - 1\%$		2.5	<b>3.0</b>	
$I_{GND}$	Ground Pin Current	$I_L = 100\text{ }\mu\text{A}$		200	250 <b>275</b>	$\mu\text{A}$
		$I_L = 200\text{ mA}$		1.5	2 <b>3.3</b>	$\text{mA}$
		$I_L = 800\text{ mA}$		5.5	8.5 <b>15</b>	
$I_O(\text{PK})$	Peak Output Current	$V_{OUT} \geq V_{OUT(NOM)} - 5\%$		1200		$\text{mA}$
$I_O(\text{MAX})$	Short Circuit Current	$R_L = 0$ (Steady State)		1400		
$e_n$	Output Noise Voltage (RMS)	$\text{BW} = 100\text{ Hz to }100\text{ kHz}$ $C_{BYPASS} = 10\text{ nF}$		18		$\mu\text{V(RMS)}$
$\frac{\Delta V_{OUT}}{\Delta V_{IN}}$	Ripple Rejection	$f = 1\text{ kHz}$		60		$\text{dB}$
<b>SHUTDOWN INPUT</b>						
$V_{S/D}$	S/D Input Voltage	$V_H = \text{Output ON}$		1.4	<b>1.6</b>	$V$
		$V_L = \text{Output OFF}$ , $I_{IN} \leq 10\text{ }\mu\text{A}$	<b>0.1</b>	0.50		
		$V_{OUT} \leq 10\text{ mV}$ , $I_{IN} \leq 50\text{ }\mu\text{A}$		0.6		
$I_{S/D}$	S/D Input Current	$V_{S/D} = 0$		0.02	<b>-1</b>	$\mu\text{A}$
		$V_{S/D} = 5\text{V}$		5	<b>15</b>	

- (1) Limits are ensured through testing, statistical correlation, or design.  
(2) Typical numbers represent the most likely norm for  $25^\circ\text{C}$  operation.

## Typical Performance Characteristics

Unless otherwise specified:  $V_{IN} = 3.3V$ ,  $V_{OUT} = 1V$ ,  $I_L = 1\text{ mA}$ ,  $C_{IN} = 4.7\text{ }\mu\text{F}$ ,  $C_{OUT} = 10\text{ }\mu\text{F}$ ,  $V_{SD} = 2V$ ,  $C_{BYP} = 10\text{ nF}$ ,  $T_J = 25^\circ\text{C}$ .

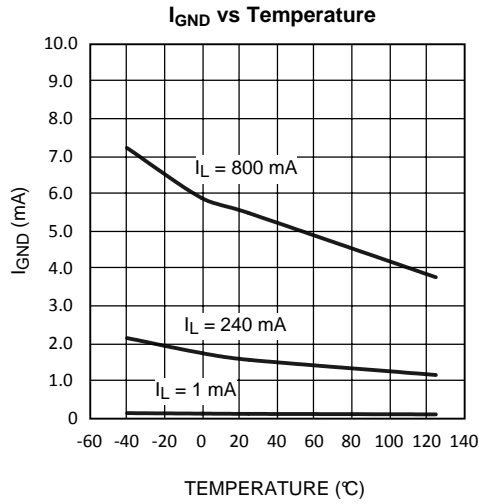


Figure 3.

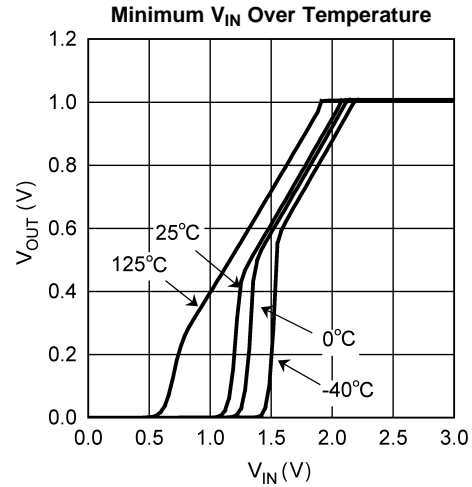


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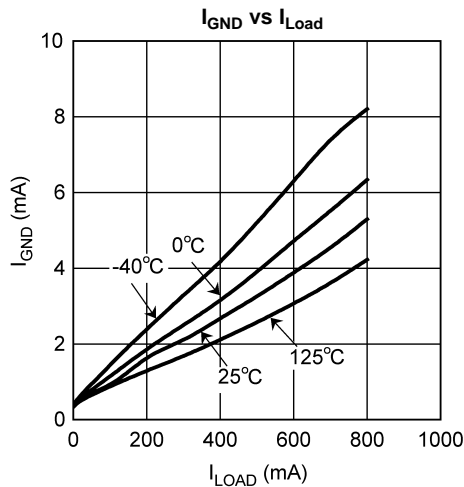


Figure 5.

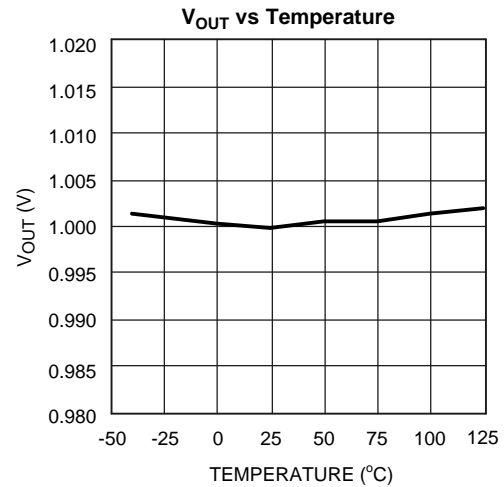


Figure 6.

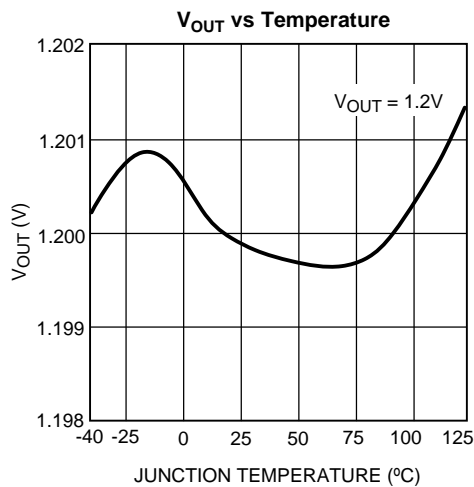


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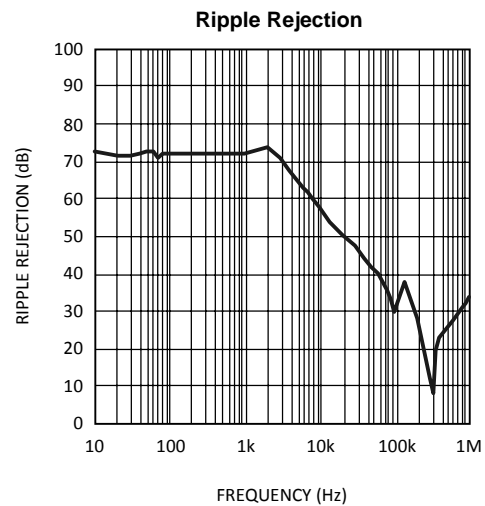


Figure 8.

### Typical Performance Characteristics (continued)

Unless otherwise specified:  $V_{IN} = 3.3V$ ,  $V_{OUT} = 1V$ ,  $I_L = 1\text{ mA}$ ,  $C_{IN} = 4.7\text{ }\mu\text{F}$ ,  $C_{OUT} = 10\text{ }\mu\text{F}$ ,  $V_{S/D} = 2V$ ,  $C_{BYP} = 10\text{ nF}$ ,  $T_J = 25^\circ\text{C}$ .

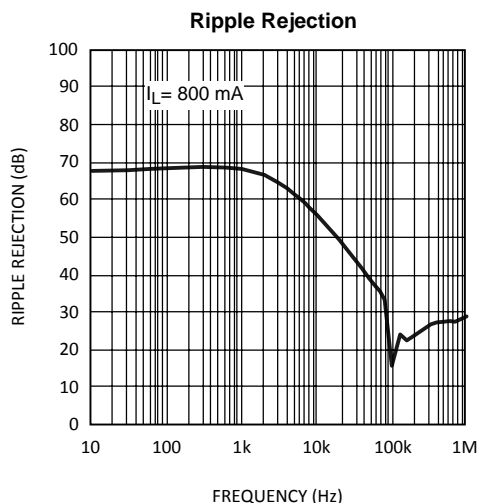


Figure 9.

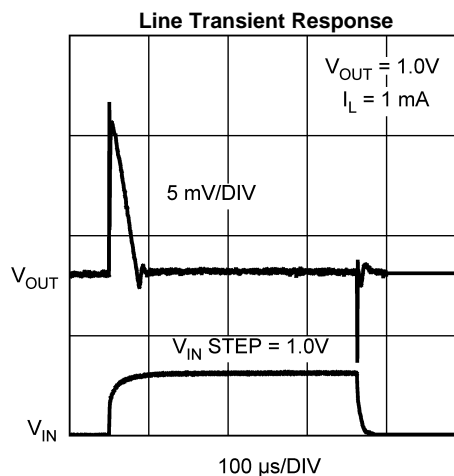


Figure 10.

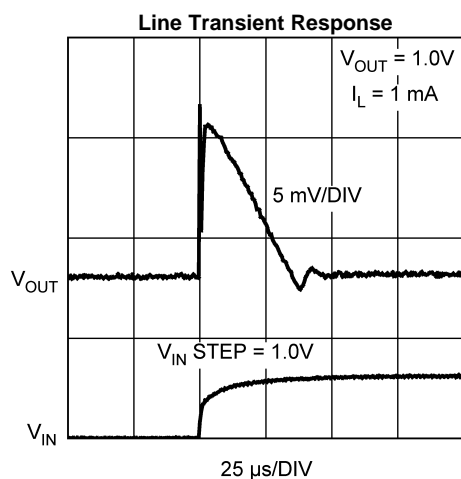


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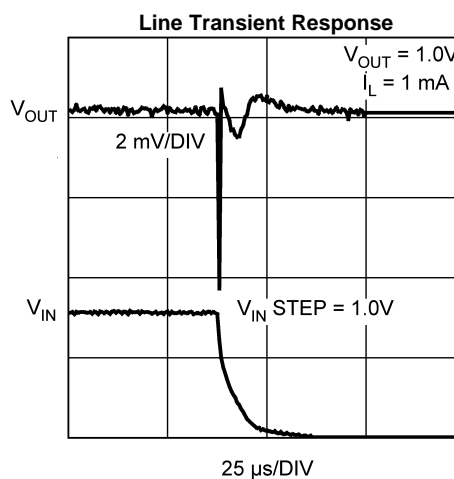


Figure 12.

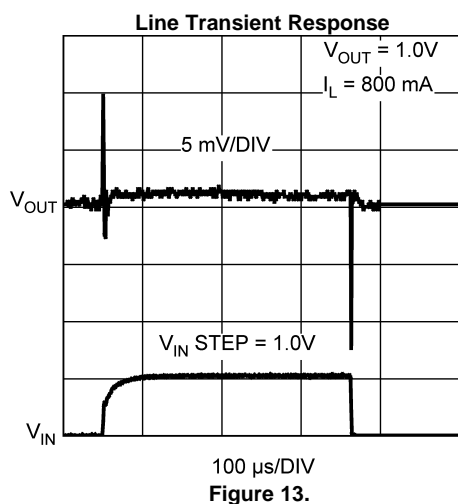


Figure 13.

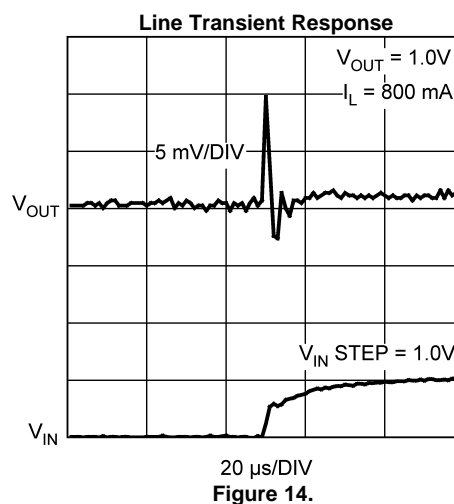
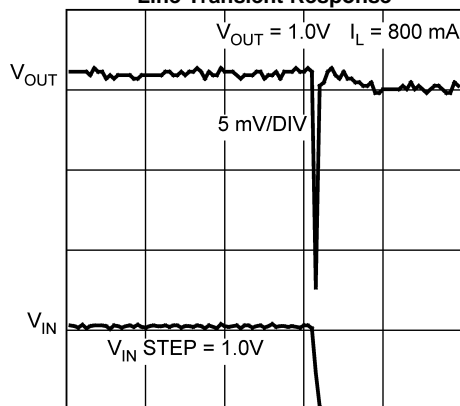


Figure 14.

## Typical Performance Characteristics (continued)

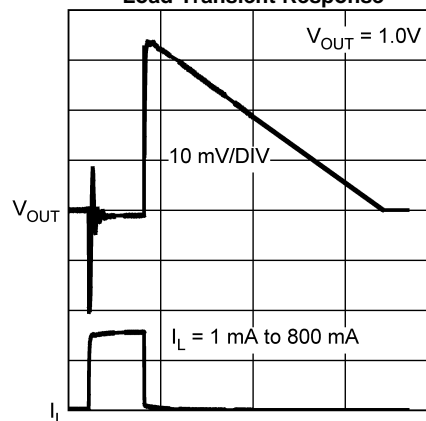
Unless otherwise specified:  $V_{IN} = 3.3V$ ,  $V_{OUT} = 1V$ ,  $I_L = 1\text{ mA}$ ,  $C_{IN} = 4.7\text{ }\mu\text{F}$ ,  $C_{OUT} = 10\text{ }\mu\text{F}$ ,  $V_{S/D} = 2V$ ,  $C_{BYP} = 10\text{ nF}$ ,  $T_J = 25^\circ\text{C}$ .

**Line Transient Response**



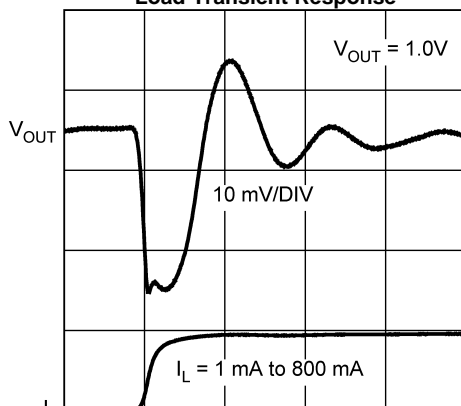
20  $\mu\text{s/DIV}$   
**Figure 15.**

**Load Transient Response**



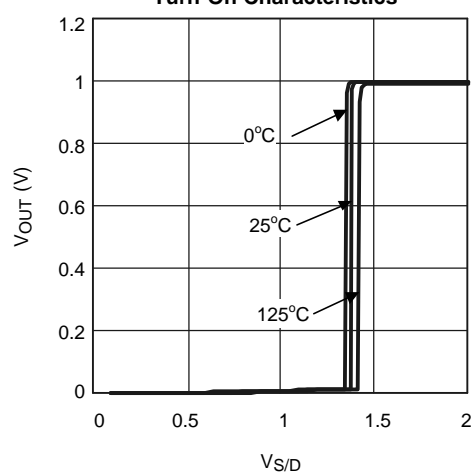
50  $\mu\text{s/DIV}$   
**Figure 16.**

**Load Transient Response**



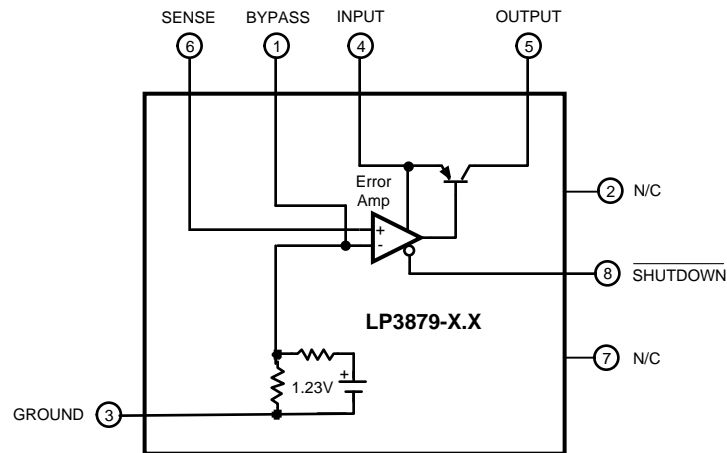
2  $\mu\text{s/DIV}$   
**Figure 17.**

**Turn-On Characteristics**



**Figure 18.**

## Block Diagram



## APPLICATION INFORMATION

### PACKAGE INFORMATION

The LP3879 is offered in the 8-lead SO PowerPad or WSON surface mount packages to allow for increased power dissipation compared to the SO-8 and Mini SO-8.

### EXTERNAL CAPACITORS

Like any low-dropout regulator, the LP3879 requires external capacitors for regulator stability. These capacitors must be correctly selected for good performance.

**INPUT CAPACITOR:** A capacitor whose value is at least 4.7  $\mu\text{F}$  ( $\pm 20\%$ ) is required between the LP3879 input and ground. A good quality X5R / X7R ceramic capacitor should be used.

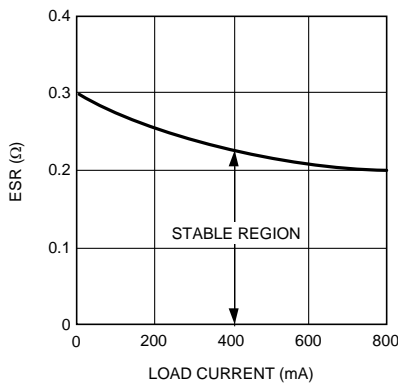
Capacitor tolerance and temperature variation must be considered when selecting a capacitor (see [Capacitor Characteristics](#) section) to assure the minimum requirement of input capacitance is met over all operating conditions.

The input capacitor must be located not more than 0.5" from the input pin and returned to a clean analog ground. Any good quality ceramic or tantalum capacitor may be used, assuming the minimum input capacitance requirement is met.

**OUTPUT CAPACITOR:** The LP3879 requires a ceramic output capacitor whose size is at least 10  $\mu\text{F}$  ( $\pm 20\%$ ). A good quality X5R / X7R ceramic capacitor should be used. Capacitance tolerance and temperature characteristics must be considered when selecting an output capacitor.

The LP3879 is designed specifically to work with ceramic output capacitors, utilizing circuitry which allows the regulator to be stable across the entire range of output current with an ultra low ESR output capacitor.

The output capacitor selected must meet the requirement for minimum amount of capacitance and also have an ESR (equivalent series resistance) value which is within the stable range. A curve is provided which shows the stable ESR range as a function of load current (see [Figure 19](#)).



**Figure 19. Stable Region For Output Capacitor ESR**

**Important:** The output capacitor must maintain its ESR within the stable region *over the full operating temperature range of the application* to assure stability.

The output capacitor ESR forms a zero which is required to add phase lead near the loop gain crossover frequency, typically in the range of 50kHz to 200 kHz. The ESR at lower frequencies is of no importance. Some capacitor manufacturers list ESR at low frequencies only, and some give a formula for Dissipation Factor which can be used to calculate a value for a term referred to as ESR. However, since the DF formula is usually at a much lower frequency than the range listed above, it will give an unrealistically high value. If good quality X5R or X7R ceramic capacitors are used, the actual ESR in the 50 kHz to 200 kHz range will not exceed 25 milli Ohms. If these are used as output capacitors for the LP3879, the regulator stability requirements are satisfied.

It is important to remember that capacitor tolerance and variation with temperature must be taken into consideration when selecting an output capacitor so that the minimum required amount of output capacitance is provided over the full operating temperature range. (See [Capacitor Characteristics](#) section).

The output capacitor must be located not more than 0.5" from the output pin and returned to a clean analog ground.

**NOISE BYPASS CAPACITOR:** The 10 nF capacitor on the Bypass pin significantly reduces noise on the regulator output and is required for loop stability. However, the capacitor is connected directly to a high-impedance circuit in the bandgap reference.

Because this circuit has only a few microamperes flowing in it, any significant loading on this node will cause a change in the regulated output voltage. For this reason, DC leakage current through the noise bypass capacitor must never exceed 100 nA, and should be kept as low as possible for best output voltage accuracy.

The types of capacitors best suited for the noise bypass capacitor are ceramic and film. High-quality ceramic capacitors with either NPO or COG dielectric typically have very low leakage. 10 nF polypropylene and polycarbonate film capacitors are available in small surface-mount packages and typically have extremely low leakage current.

## CAPACITOR CHARACTERISTICS

**CERAMIC:** The LP3879 was designed to work with ceramic capacitors on the output to take advantage of the benefits they offer: for capacitance values in the 10  $\mu$ F range, ceramics are the least expensive and also have the lowest ESR values (which makes them best for eliminating high-frequency noise). The ESR of a typical 10  $\mu$ F ceramic capacitor is in the range of 5 m $\Omega$  to 10 m $\Omega$ , which meets the ESR limits required for stability by the LP3879.

One disadvantage of ceramic capacitors is that their capacitance can vary with temperature. Many large value ceramic capacitors ( $\geq 2.2 \mu$ F) are manufactured with the Z5U or Y5V temperature characteristic, which results in the capacitance dropping by more than 50% as the temperature goes from 25°C to 85°C.

Another significant problem with Z5U and Y5V dielectric devices is that the capacitance drops severely with applied voltage. A typical Z5U or Y5V capacitor can lose 60% of its rated capacitance with half of the rated voltage applied to it.

For these reasons, X7R and X5R type ceramic capacitors must be used on the input and output of the LP3879.

## SHUTDOWN INPUT OPERATION

The LP3879 is shut off by pulling the Shutdown input low, and turned on by pulling it high. If this feature is not to be used, the Shutdown input should be tied to  $V_{IN}$  to keep the regulator output on at all times.

To assure proper operation, the signal source used to drive the Shutdown input must be able to swing above and below the specified turn-on/turn-off voltage thresholds listed in the [Electrical Characteristics](#) section under  $V_{ON/OFF}$ .

## REVERSE INPUT-OUTPUT VOLTAGE

The PNP power transistor used as the pass element in the LP3879 has an inherent diode connected between the regulator output and input.

During normal operation (where the input voltage is higher than the output) this diode is reverse-biased.

However, if the output is pulled above the input, this diode will turn ON and current will flow into the regulator output.

In such cases, a parasitic SCR can latch which will allow a high current to flow into  $V_{IN}$  (and out the ground pin), which can damage the part.

In any application where the output may be pulled above the input, an external Schottky diode must be connected from  $V_{IN}$  to  $V_{OUT}$  (cathode on  $V_{IN}$ , anode on  $V_{OUT}$ ), to limit the reverse voltage across the LP3879 to 0.3V (see [Absolute Maximum Ratings](#)).

## REVISION HISTORY

Changes from Revision A (April 2013) to Revision B	Page
• Changed layout of National Data Sheet to TI format .....	<a href="#">10</a>

## PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">LP3879MR-1.0/NOPB</a>	Active	Production	SO PowerPAD (DDA)   8	95   TUBE	Yes	SN	Level-3-260C-168 HR	-40 to 125	3879 MR1.0
LP3879MR-1.0/NOPB.B	Active	Production	SO PowerPAD (DDA)   8	95   TUBE	Yes	SN	Level-3-260C-168 HR	-40 to 125	3879 MR1.0
<a href="#">LP3879MR-1.2/NOPB</a>	Active	Production	SO PowerPAD (DDA)   8	95   TUBE	Yes	SN	Level-3-260C-168 HR	-40 to 125	LP3879 MR1.2
LP3879MR-1.2/NOPB.A	Active	Production	SO PowerPAD (DDA)   8	95   TUBE	Yes	SN	Level-3-260C-168 HR	-40 to 125	LP3879 MR1.2
LP3879MR-1.2/NOPB.B	Active	Production	SO PowerPAD (DDA)   8	95   TUBE	Yes	SN	Level-3-260C-168 HR	-40 to 125	LP3879 MR1.2
<a href="#">LP3879MRX-1.0/NOPB</a>	Active	Production	SO PowerPAD (DDA)   8	2500   LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 125	3879 MR1.0
LP3879MRX-1.0/NOPB.B	Active	Production	SO PowerPAD (DDA)   8	2500   LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 125	3879 MR1.0
<a href="#">LP3879MRX-1.2/NOPB</a>	Active	Production	SO PowerPAD (DDA)   8	2500   LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 125	LP3879 MR1.2
LP3879MRX-1.2/NOPB.A	Active	Production	SO PowerPAD (DDA)   8	2500   LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 125	LP3879 MR1.2
LP3879MRX-1.2/NOPB.B	Active	Production	SO PowerPAD (DDA)   8	2500   LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 125	LP3879 MR1.2
<a href="#">LP3879SD-1.0/NOPB</a>	Active	Production	WSON (NGT)   8	1000   SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	79SD1.0
LP3879SD-1.0/NOPB.B	Active	Production	WSON (NGT)   8	1000   SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	79SD1.0
<a href="#">LP3879SD-1.2/NOPB</a>	Active	Production	WSON (NGT)   8	1000   SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	79SD1.2
LP3879SD-1.2/NOPB.A	Active	Production	WSON (NGT)   8	1000   SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	79SD1.2
LP3879SD-1.2/NOPB.B	Active	Production	WSON (NGT)   8	1000   SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	79SD1.2

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

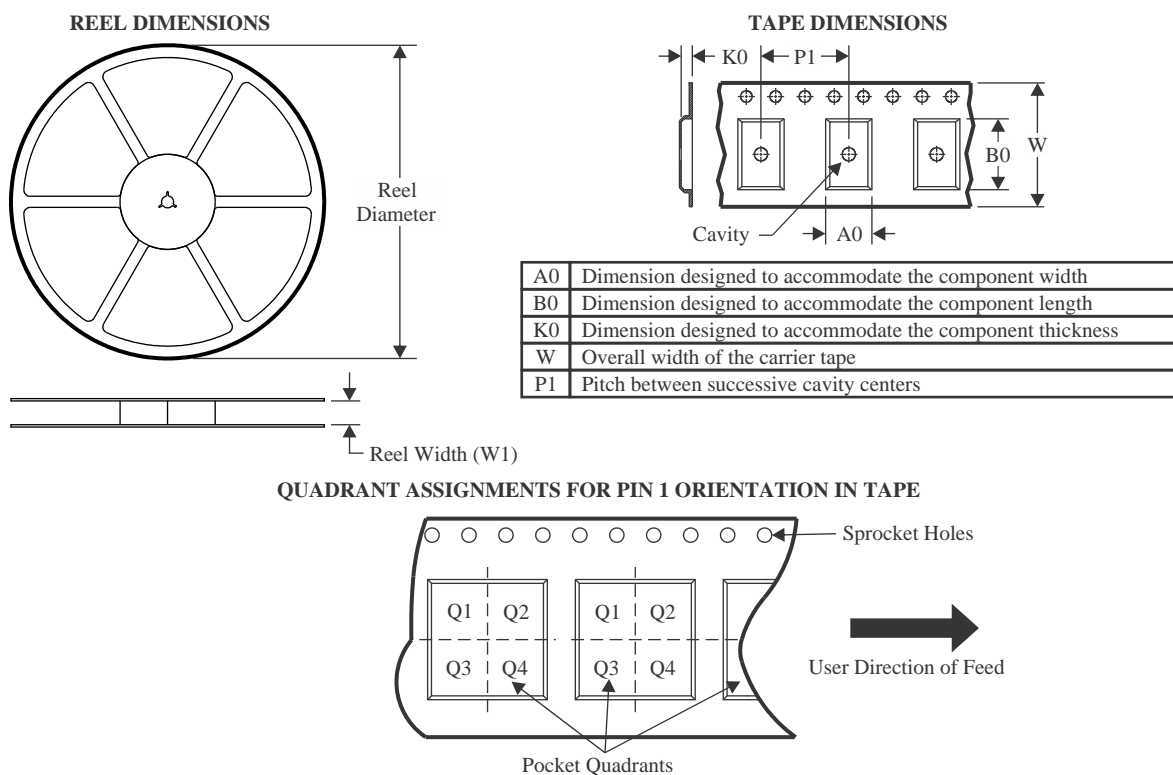
<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

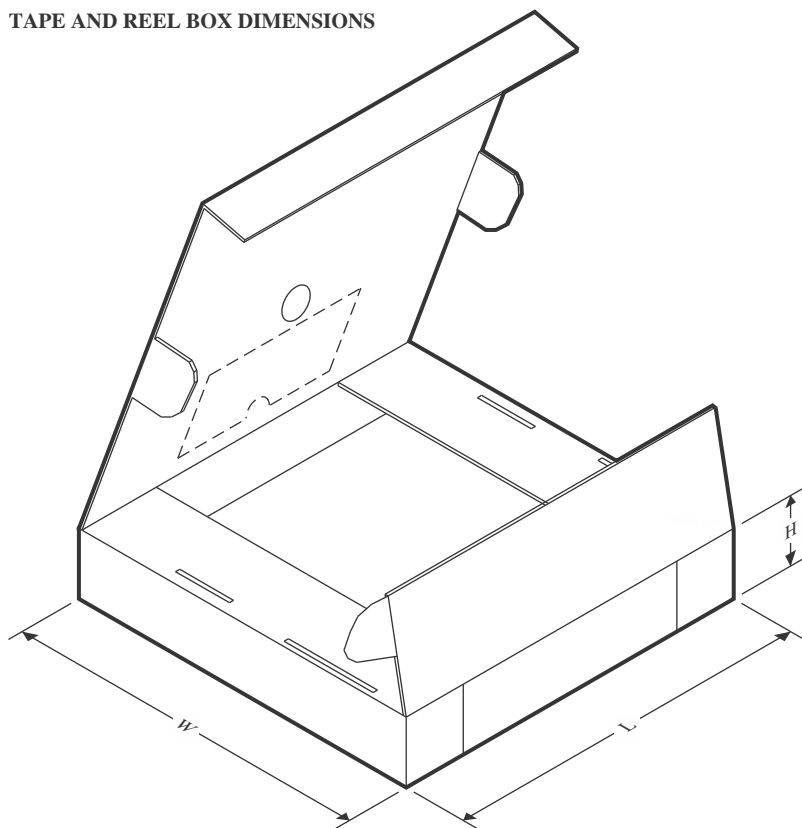
## TAPE AND REEL INFORMATION



\*All dimensions are nominal

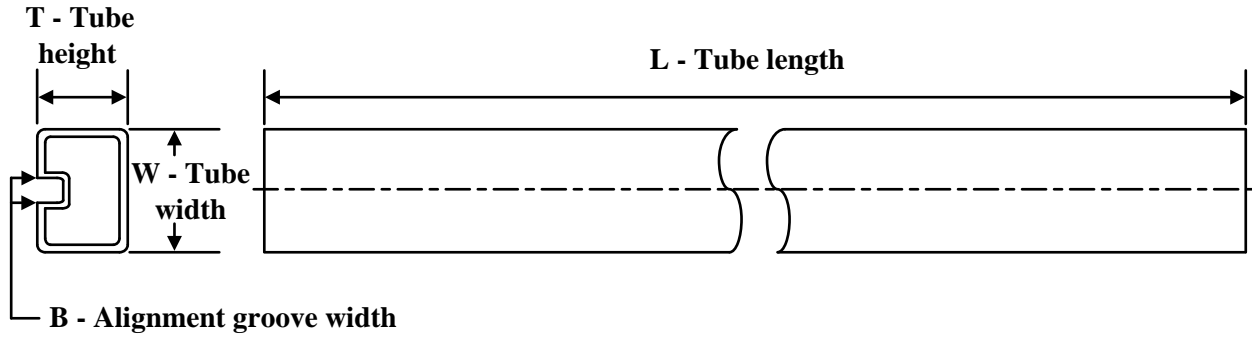
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP3879MRX-1.0/NOPB	SO PowerPAD	DDA	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LP3879MRX-1.2/NOPB	SO PowerPAD	DDA	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LP3879SD-1.0/NOPB	WSO	NGT	8	1000	177.8	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LP3879SD-1.2/NOPB	WSO	NGT	8	1000	177.8	12.4	4.3	4.3	1.3	8.0	12.0	Q1

## TAPE AND REEL BOX DIMENSIONS



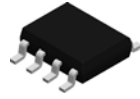
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP3879MRX-1.0/NOPB	SO PowerPAD	DDA	8	2500	356.0	356.0	36.0
LP3879MRX-1.2/NOPB	SO PowerPAD	DDA	8	2500	356.0	356.0	36.0
LP3879SD-1.0/NOPB	WSO	NGT	8	1000	208.0	191.0	35.0
LP3879SD-1.2/NOPB	WSO	NGT	8	1000	208.0	191.0	35.0

**TUBE**


\*All dimensions are nominal

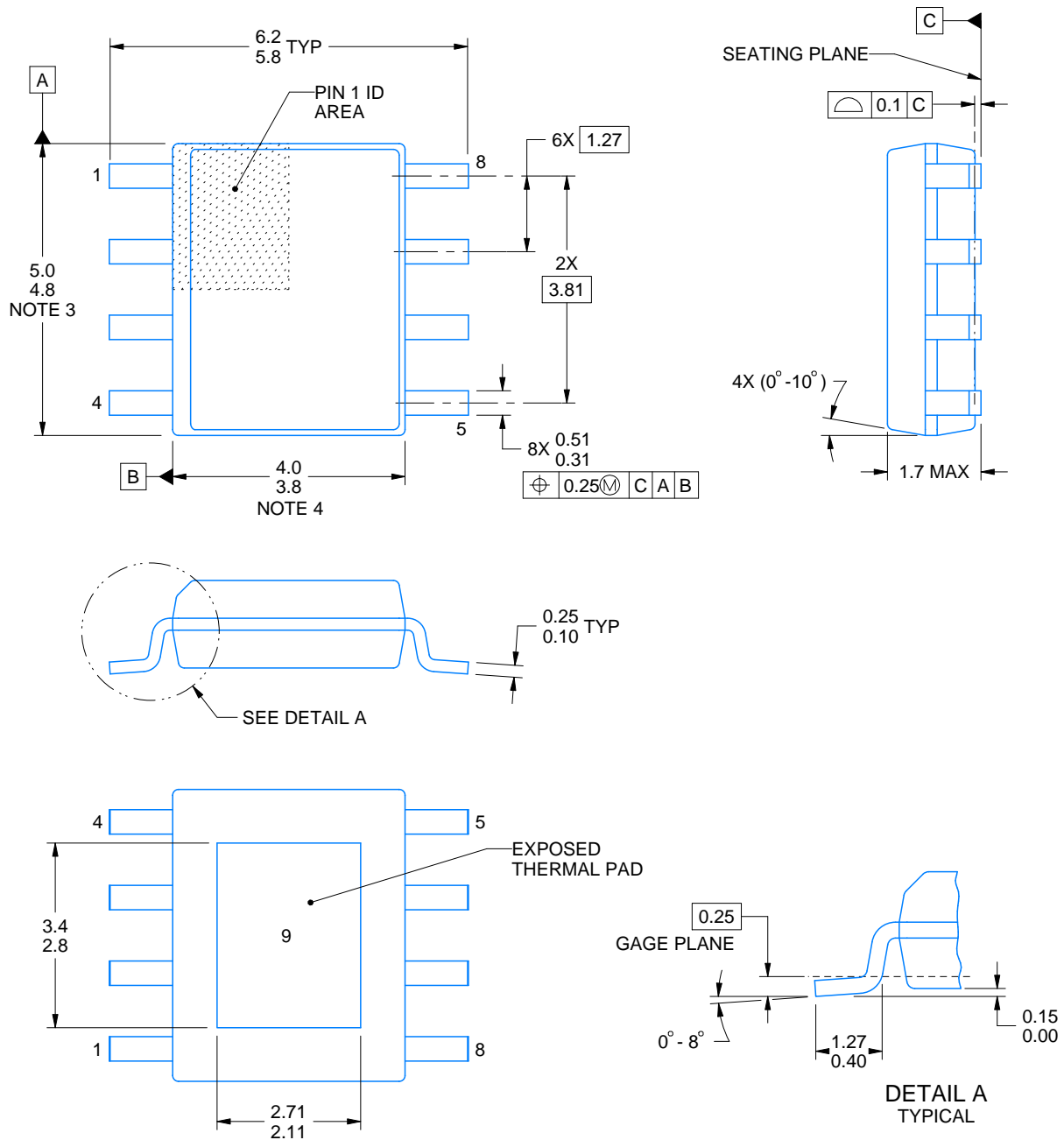
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
LP3879MR-1.0/NOPB	DDA	HSOIC	8	95	495	8	4064	3.05
LP3879MR-1.0/NOPB.B	DDA	HSOIC	8	95	495	8	4064	3.05
LP3879MR-1.2/NOPB	DDA	HSOIC	8	95	495	8	4064	3.05
LP3879MR-1.2/NOPB.A	DDA	HSOIC	8	95	495	8	4064	3.05
LP3879MR-1.2/NOPB.B	DDA	HSOIC	8	95	495	8	4064	3.05

**DDA0008B**

# PACKAGE OUTLINE

## PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



4214849/B 09/2025

**NOTES:**

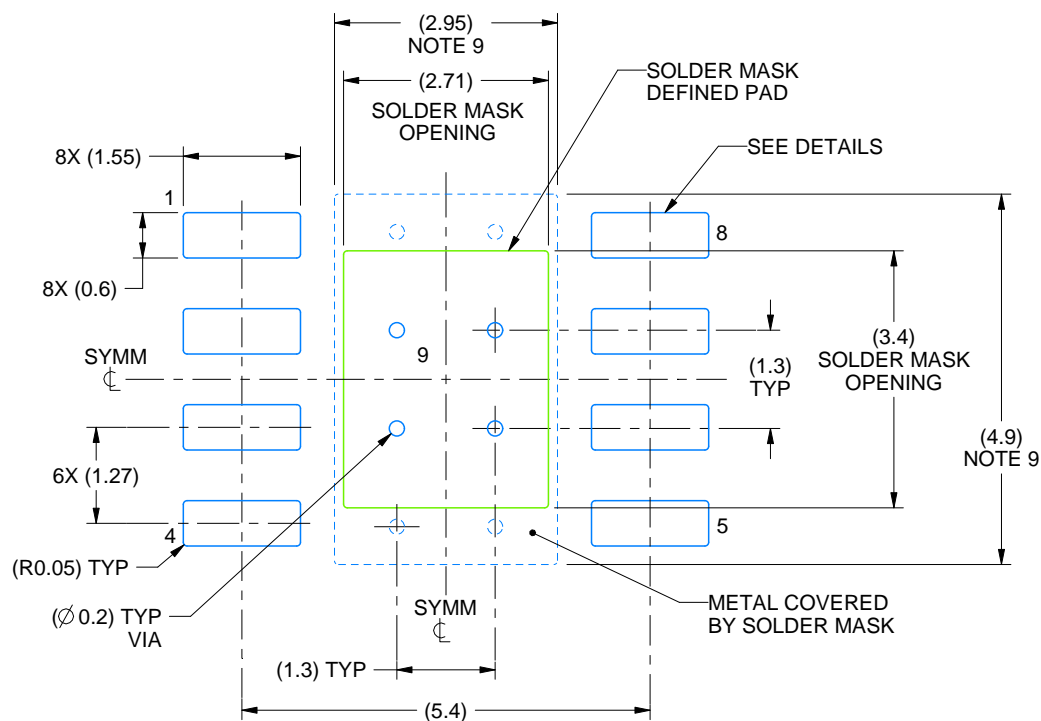
PowerPAD is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MS-012.

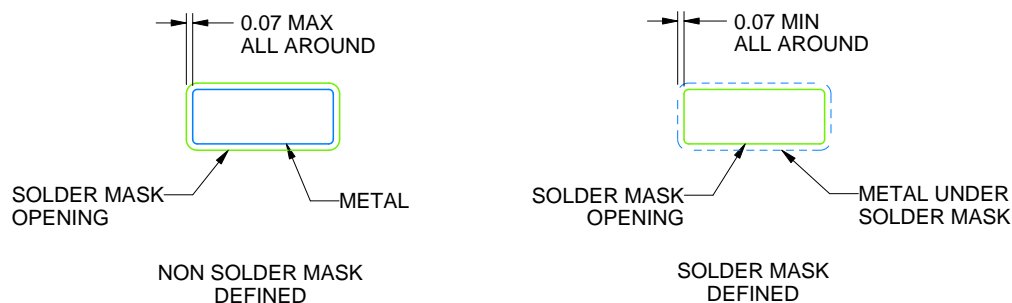
**DDA0008B**

## PowerPAD™ SOIC - 1.7 mm max height

## PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE  
SCALE:10X



## SOLDER MASK DETAILS

### PADS 1-8

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NOTES: (continued)

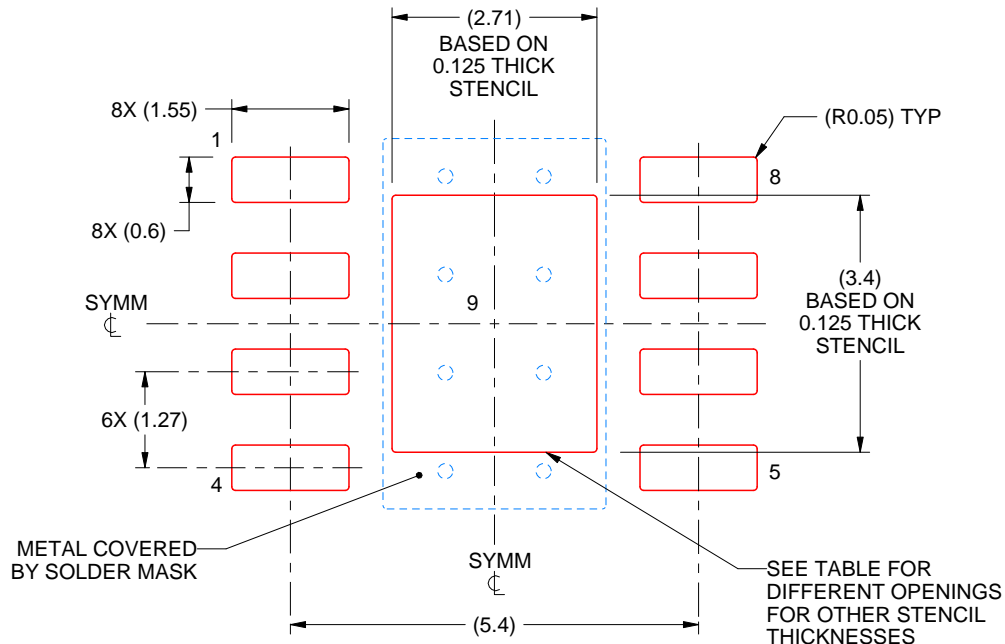
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 ([www.ti.com/lit/slma002](http://www.ti.com/lit/slma002)) and SLMA004 ([www.ti.com/lit/slma004](http://www.ti.com/lit/slma004)).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

DDA0008B

PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



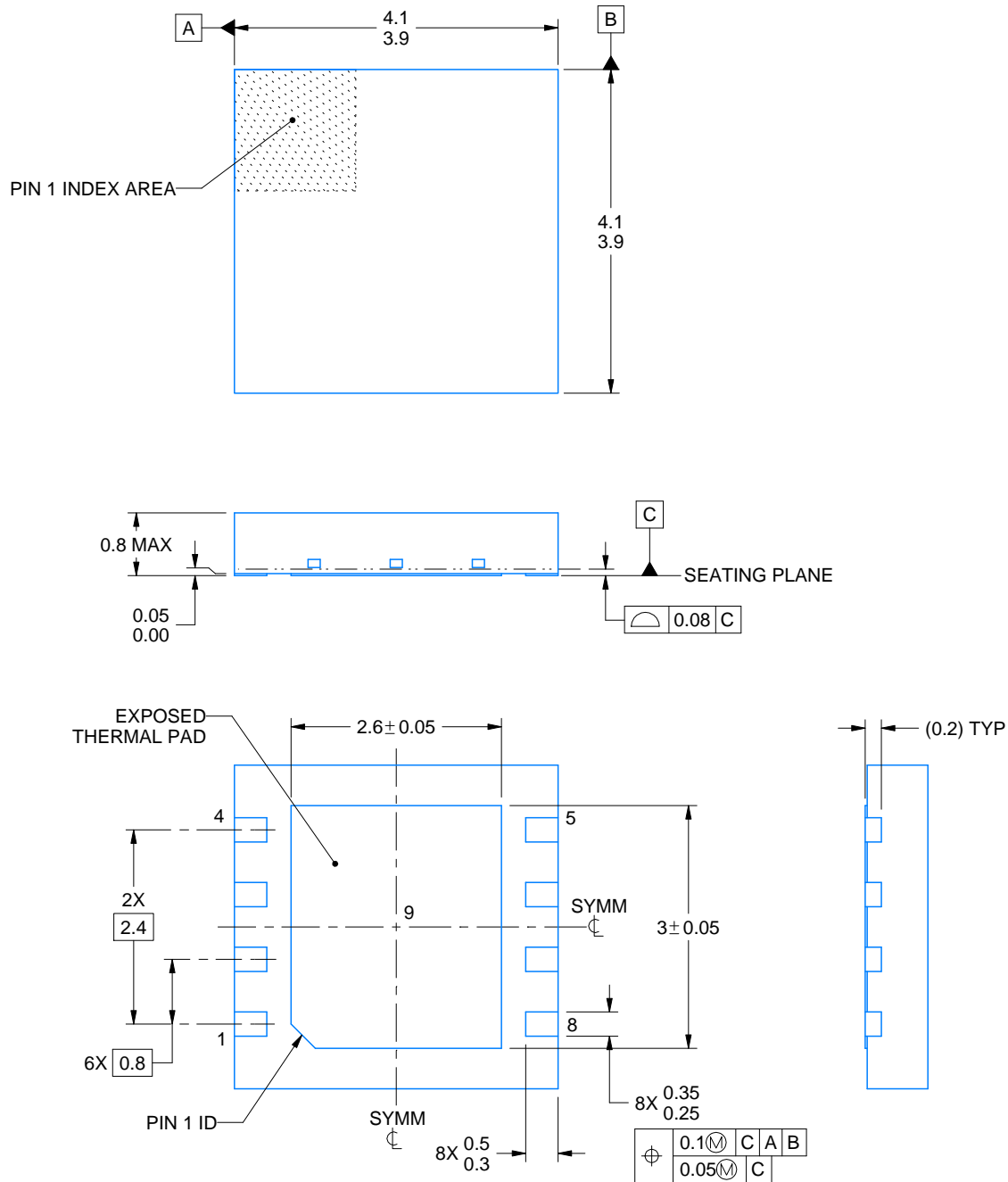
**SOLDER PASTE EXAMPLE**  
EXPOSED PAD  
100% PRINTED SOLDER COVERAGE BY AREA  
SCALE:10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.03 X 3.80
0.125	2.71 X 3.40 (SHOWN)
0.150	2.47 X 3.10
0.175	2.29 X 2.87

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NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.



4214935/A 08/2020

**NOTES:**

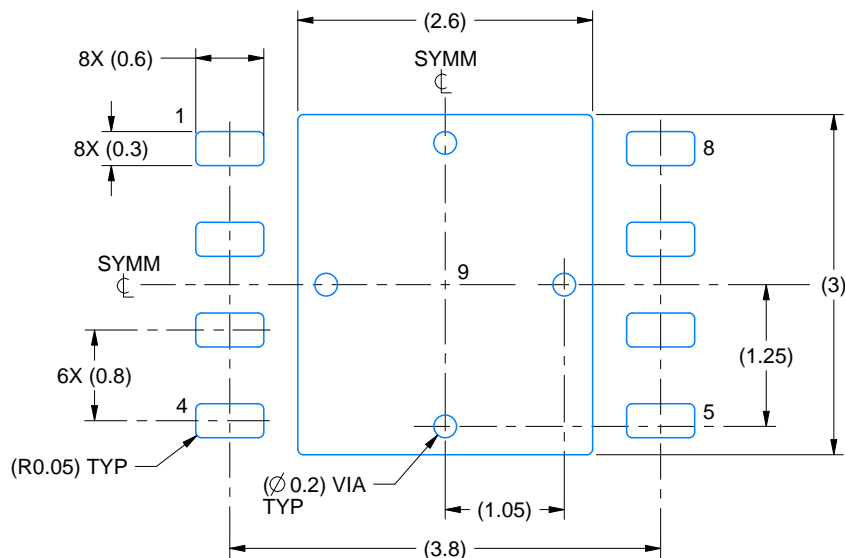
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

# EXAMPLE BOARD LAYOUT

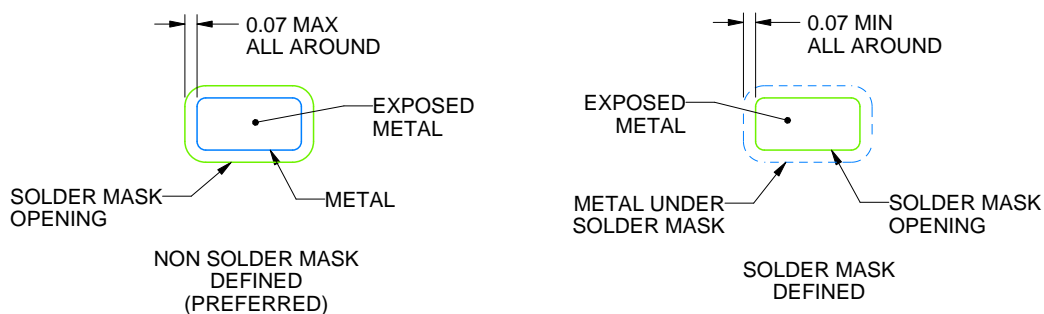
NGT0008A

WSN - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:15X



SOLDER MASK DETAILS

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NOTES: (continued)

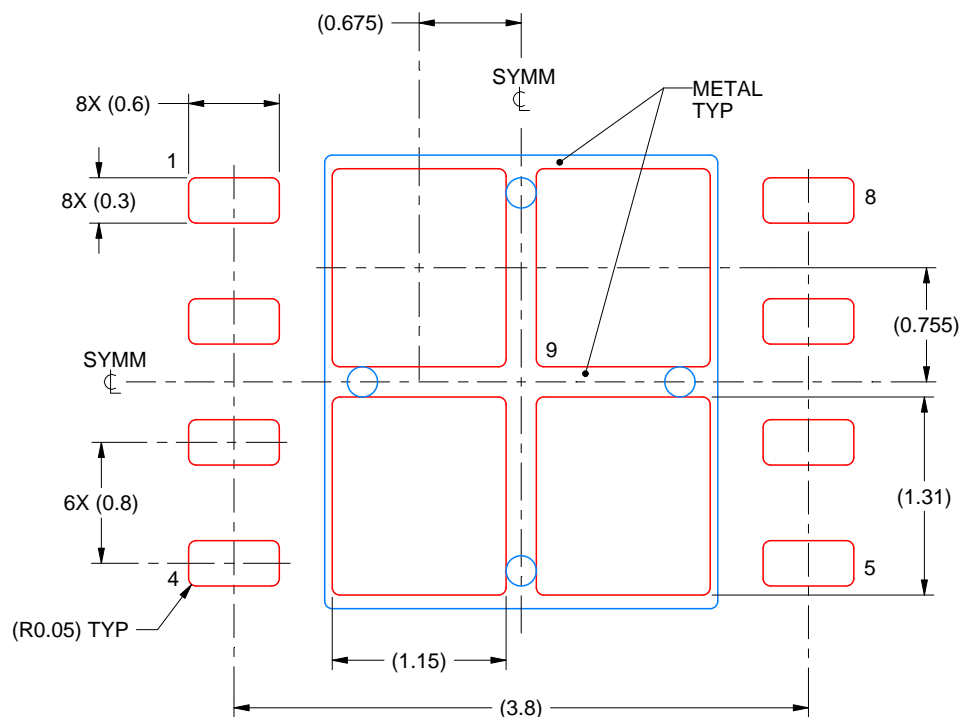
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slue271](http://www.ti.com/lit/slue271)).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

NGT0008A

WSN - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:  
77% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE  
SCALE:20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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