3.5MHz, 500mA Synchronous Step Down DC-DC Regulator

Features

- Input Voltage — 2.9V to 5.5V
- Output Voltage — 0.8V to 3.6V
- Output current capability — 500mA
- Efficiency up to 94%
- 15 Programmable output voltages
- High light-load efficiency via automatic PSAVE mode
- Fast transient response
- Temperature range — -40 to +85°C
- Oscillator frequency — 3.5MHz
- 100% duty cycle capability
- Quiescent current — 38µA typ
- Shutdown Current — 0.1µA typ
- Internal soft-start
- Over-voltage protection
- Current limit and short circuit protection
- Over-temperature protection
- Under-voltage lockout
- Floating control pin protection
- WLCSP8-0.80 X 0.80 X 0.375 (mm) package
- Pb free, halogen free, and RoHS/WEEE compliant

Applications

- Smart phones and cellular phones
- MP3/Personal media players
- Personal navigation devices
- Digital cameras
- Single Li-ion cell or 3 NiMH/NiCd cell devices
- Devices with 3.3V or 5V internal power rails

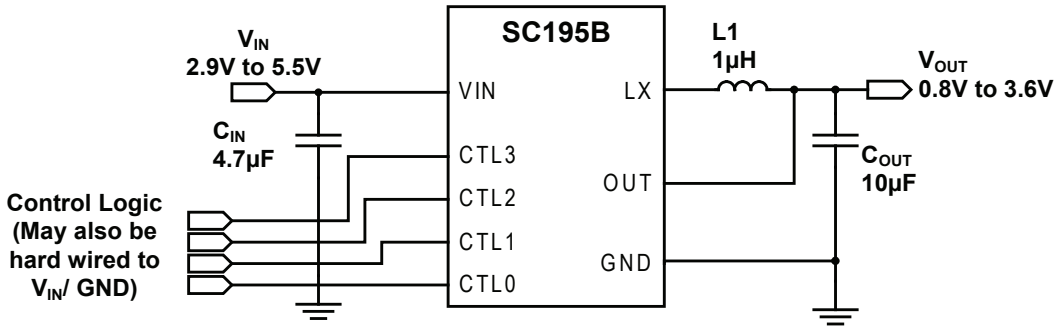
Description

The SC195B is a high efficiency, 500mA step down regulator designed to operate with an input voltage range of 2.9V to 5.5V. The input voltage range makes it ideal for battery operated applications with space limitations. The SC195B also includes fifteen programmable output voltage settings that can be selected using the four control pins, eliminating the need for external feedback resistors. The output voltage can be fixed to a single setting or dynamically switched between different levels. Pulling all four control pins low disables the output and puts the device into a low current shutdown state.

The SC195B operates at a fixed 3.5MHz switching frequency in normal PWM (Pulse-Width Modulation) mode. A variable frequency PSAVE (power-save) mode is used to optimize efficiency at light loads for each output setting. Built-in hysteresis prevents chattering between the two modes.

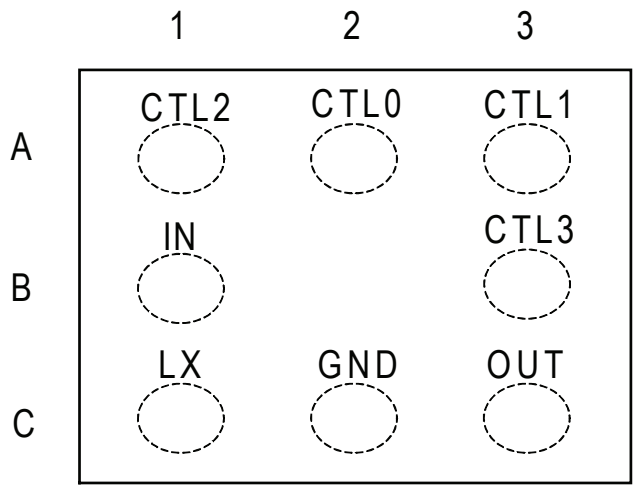
The SC195B provides several protection features to safeguard the device under stressed conditions. These include short circuit protection, over-temperature protection, over-voltage protection, under-voltage lockout, and soft-start to control in-rush current. These features coupled with the small 8-bump 0.80 X 0.80 X 0.375 (mm) package make it a versatile device ideal for step-down regulation in products needing high efficiency and a small PCB footprint.

Typical Application Circuit



Bump Configuration

Top View



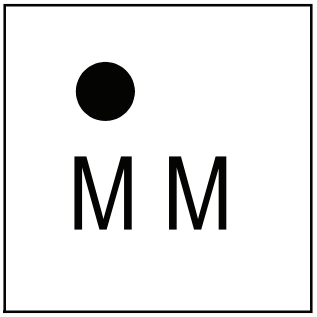
WLCSP8 0.80 X 0.80 (mm)
θ_{JA} = 107 °C/W

Ordering Information

Device	Package
SC195BCSTRT(1)(2)	WLCSP8-0.80X0.80X0.375
SC195BEVB	Evaluation Board

Notes:
(1) Available in tape and reel only. A reel contains 3,000 devices.
(2) Lead-free packaging only. Device is WEEE and RoHS compliant and halogen-free.

Marking Information



A1 Corner Bump and Part Number Marking Code

Table 1 – Output Voltage (CTL) Settings

CTL3	CTL2	CTL1	CTL0	Vout
0	0	0	0	Shutdown
0	0	0	1	0.80
0	0	1	0	1.00
0	0	1	1	1.10
0	1	0	0	1.20
0	1	0	1	1.35
0	1	1	0	1.50
0	1	1	1	1.60
1	0	0	0	1.80
1	0	0	1	2.00
1	0	1	0	2.50
1	0	1	1	2.80
1	1	0	0	3.00
1	1	0	1	3.30
1	1	1	0	3.40
1	1	1	1	3.60

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Absolute Maximum Ratings

IN (V) ..... -0.3 to +6.0
LX Voltage (V) ..... -1.0 to (V_{IN}+0.5)
Other Pins (V) ..... -0.3 to (V_{IN}+0.3)
Output Short Circuit to GND ..... Continuous
ESD Protection Level[1] (kV) 2.5

Recommended Operating Conditions

Input Voltage Range (V) ..... +2.9 to +5.5
Operating Temperature Range (°C) ..... -40 to +85

Thermal Information

Thermal Resistance, Junction to Ambient[2] (°C/W) 107
Junction Temperature Range (°C) ..... -40 to +150
Storage Temperature Range (°C) ..... -65 to +150

Exceeding the above specifications may result in permanent damage to the device or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not recommended.

NOTES:
(1) Tested according to JEDEC standard JESD22-A114.
(2) Calculated from package in still air, mounted to 3 x 4.5 (in), 4 layer FR4 PCB per JESD51 standards.

Electrical Characteristics

Unless otherwise specified: V_{IN}= 3.6V, C_{IN}=4.7µF, C_{OUT}=10µF, L_X=1µH, V_{OUT}=1.8V, $T_{J(MAX)}$=125°C, T_A= -40 to +85 °C. Typical values are T_A=+25 °C

Parameter	Symbol	Condition	Min	Typ	Max	Units
Output Voltage Range[1]	V_{OUT}		0.8		3.6	V
Output Voltage Tolerance [2]	V_{OUT_TOL}	Iout = 200mA, PWM Mode	-2.0		2.0	%
		PSAVE mode		1.5		
Line Regulation	$\Delta V_{LINEREG}$	2.9 ≤ V_{IN} ≤ 5.5V, PWM mode		0.3		%/V
Load Regulation	$\Delta V_{LOADREG}$	200mA ≤ Iout ≤ 500mA, PWM mode		-1		%/A
CTL Setting Regulation	ΔV_{CTLREG}	Relative to V_{OUT} at CTL =1000; Iout = 200mA, PWM mode		+/- 0.3		%
Output Current Capability	I_{OUT}		500			mA
Current Limit Threshold	I_{LIMIT}		800		1500	mA
Foldback Current Limit	I_{FB_LIM}	I_{LOAD} > $I_{LIMIT;}$ V_{OUT} forced to 1V		215		mA
Under-Voltage Lockout	V_{UVLO}	Rising V_{IN}			2.9	V
		Hysteresis		200		mV
Quiescent Current[3]	I_Q	No switching, I_{OUT} = 0mA, CTLx = V_{IN} or GND		38	60	µA
Shutdown Current	I_{SD}	$V_{CTL\ 0\text{-}3}$= 0V		0.1	1.0	µA
LX Leakage Current	I_{LX}	Into LX pin		0.1	1.0	µA

Electrical Characteristics (continued)

Parameter	Symbol	Condition	Min	Typ	Max	Units
High Side Switch Resistance(4)	R_{DSON_P}	I_{OUT}= 100mA, T_A=+25 °C	100	250	850	mΩ
Low Side Switch Resistance(5)	R_{DSON_N}	I_{OUT}= 100mA, T_A=+25 °C	200	350	900	
Switching Frequency	f_{SW}		2.8	3.5	4.2	MHz
Soft-Start	t_{SS}	V_{OUT} = 90% of final value		100	500	µs
Thermal Shutdown	T_{OT}	Rising temperature		160		°C
Thermal Shutdown Hysteresis	T_{HYST}			20		°C
Logic Inputs - CTL0, CTL1, CTL2, and CTL3(2)						
Input High Voltage	V_{IH}	2.9V < V_{IN} < 5.5V	1.6			V
Input Low Voltage	V_{IL}	2.9V < V_{IN} < 5.5V			0.4	V
Input High Current(3)	I_{IH}	$V_{CTL\ 0\text{-}3}$= V_{IN}	-1.0		1.0	µA
Input Low Current(3)	I_{IL}	$V_{CTL\ 0\text{-}3}$= GND	-1.0		1.0	µA

Notes

(1) Maximum output voltage is limited to V_{IN}.

(2) V_{IN} = 3.6V for $V_{OUT} \leq$ 3.0V. V_{IN} = 4.0V for V_{OUT} > 3.0V.

(3) Recommend connection for all CTLx inputs is V_{IN} or GND. Refer to "CTL Input Resistance" in the Applications Information.

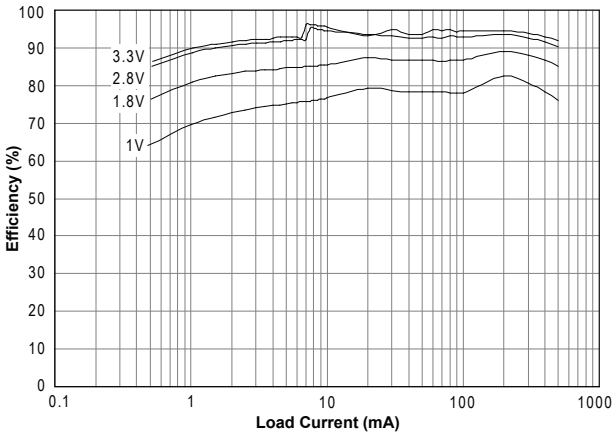
(4) Measured from IN to LX.

(5) Measured from LX to GND.

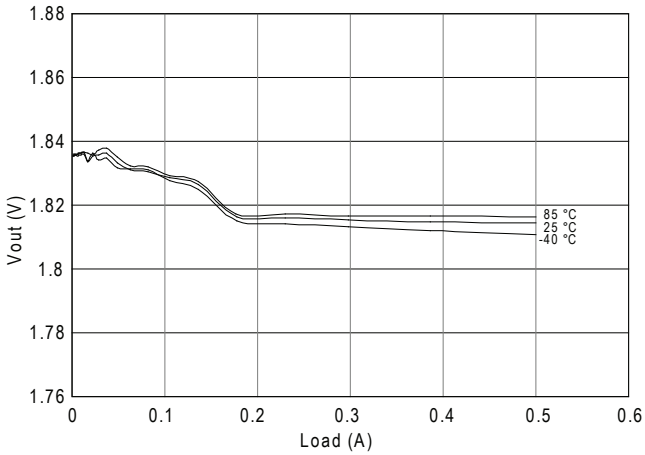
Typical Characteristics

V_{IN} = 4.0V for V_{OUT} = 3.3V, V_{IN} = 3.6V for all others. C_{IN} = 4.7µF, C_{OUT} = 10µF, L_X = 1µH, T_A = 25°C unless otherwise noted.

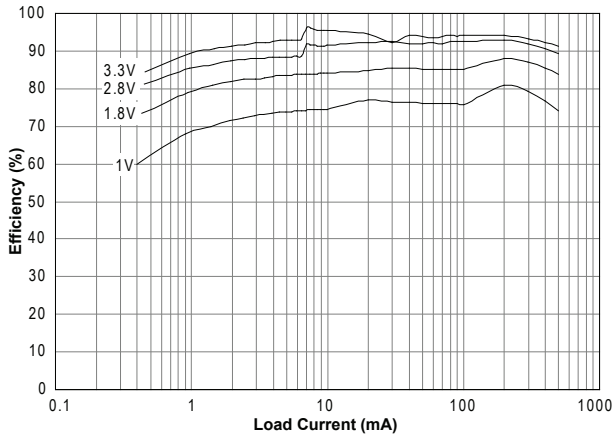
Efficiency vs. I_{OUT} (T_A = -40°C)



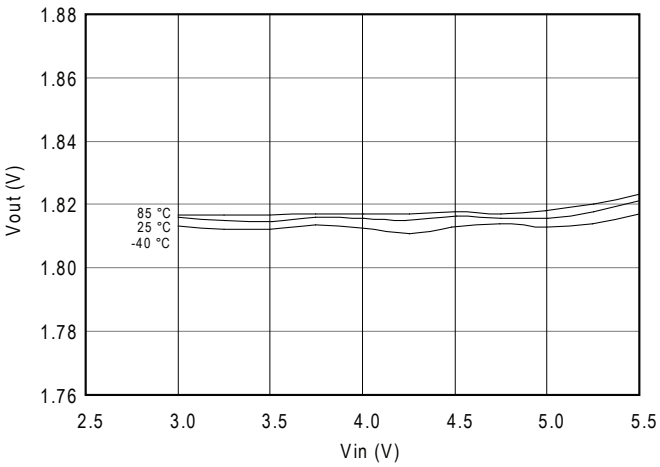
Load Regulation, Vout=1.8V



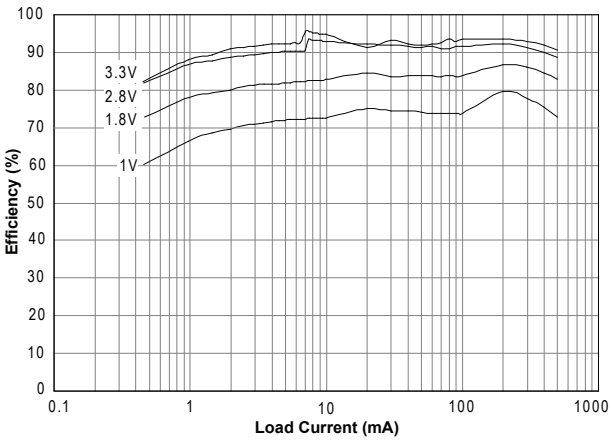
Efficiency vs. I_{OUT} (T_A = 25°C)



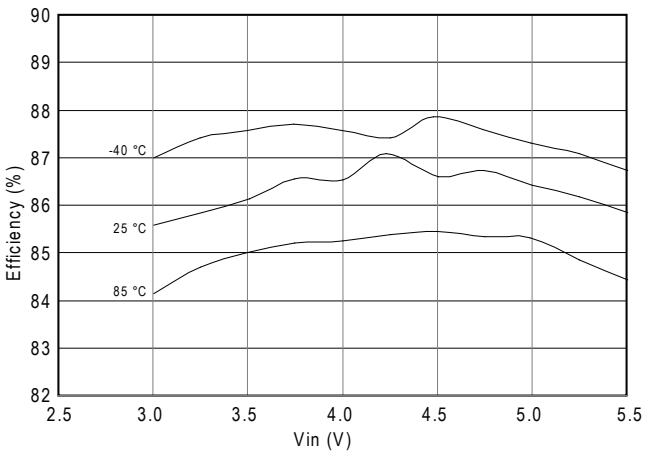
Line Regulation, Vout=1.8V/400mA



Efficiency vs. I_{OUT} (T_A = 85°C)

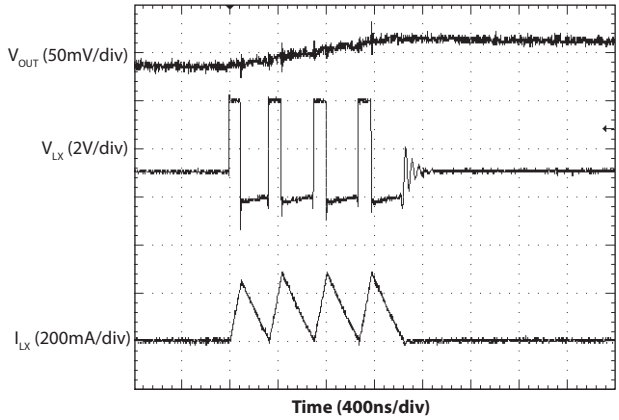


Efficiency vs. Vin, 1.8V/400mA

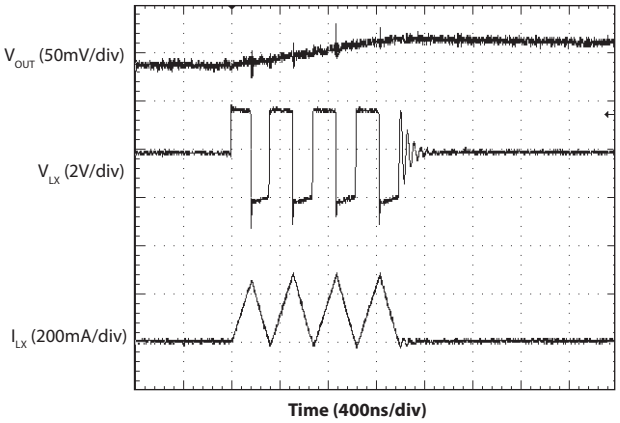


Typical Characteristics (continued)

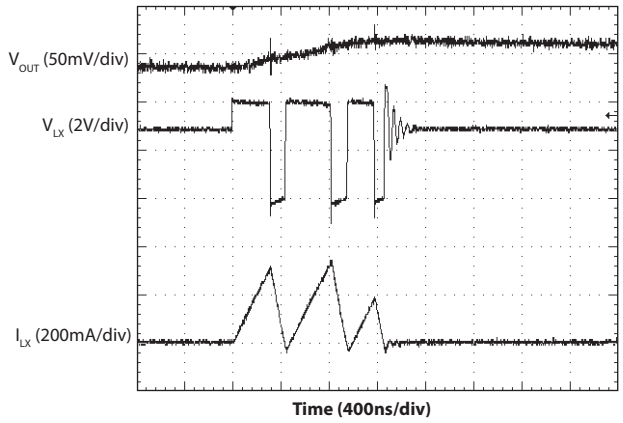
Light Load Switching — V_{OUT} = 1.0V



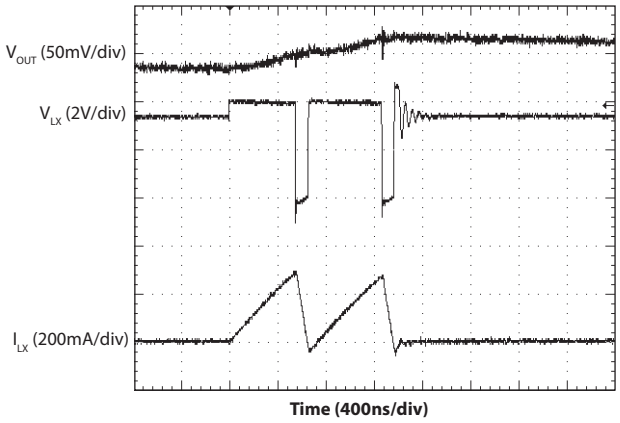
Light Load Switching — V_{OUT} = 1.8V



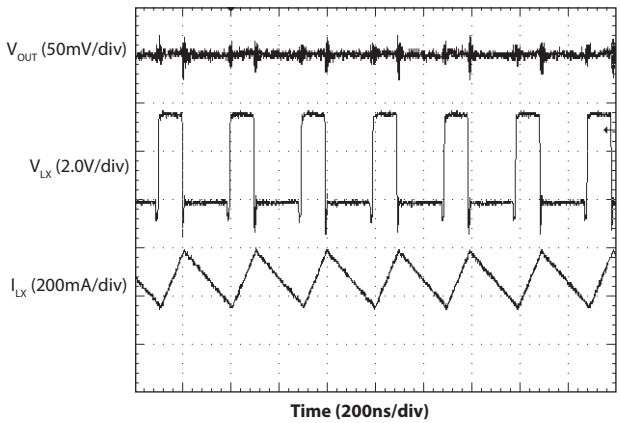
Light Load Switching — V_{OUT} = 2.8V



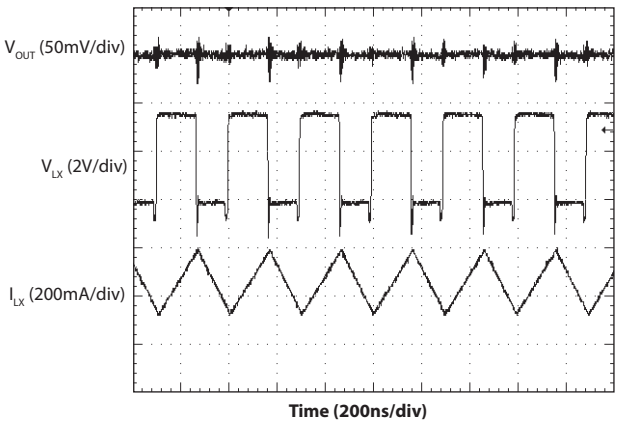
Light Load Switching — V_{OUT} = 3.3V



Heavy Load Switching — V_{OUT} = 1.0V

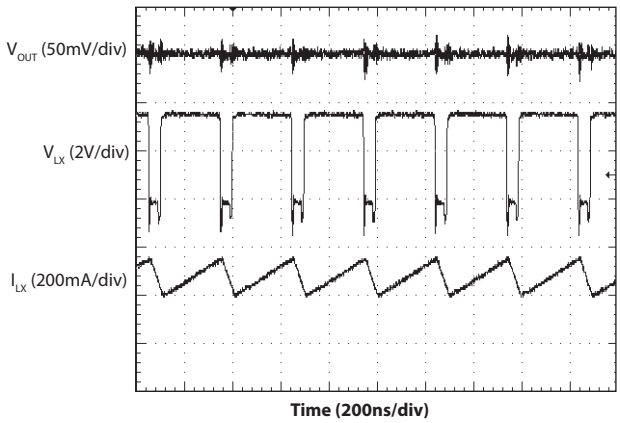


Heavy Load Switching — V_{OUT} = 1.8V

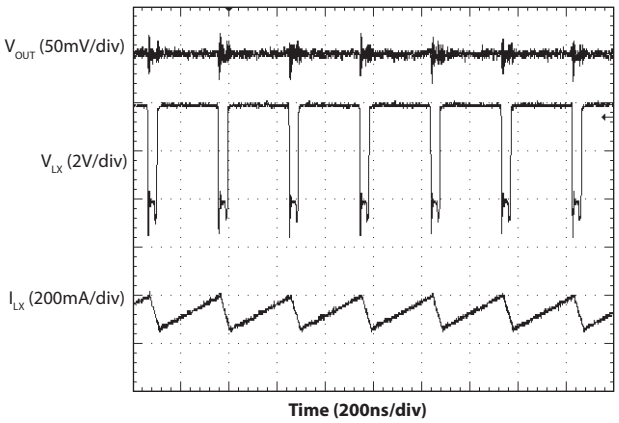


Typical Characteristics (continued)

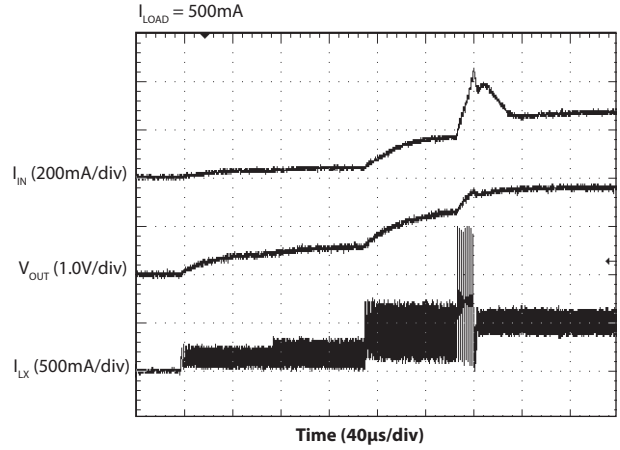
Heavy Load Switching — V_{OUT} = 2.8V



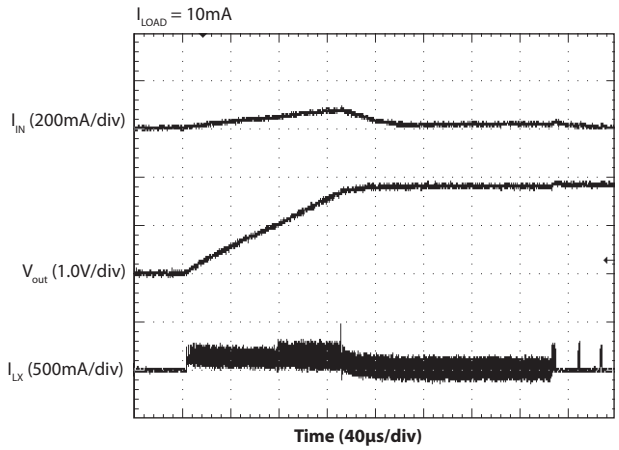
Heavy Load Switching — V_{OUT} = 3.3V



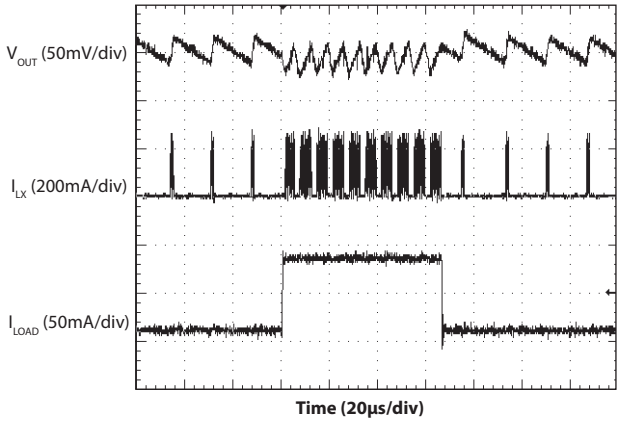
Heavy Load Soft-start



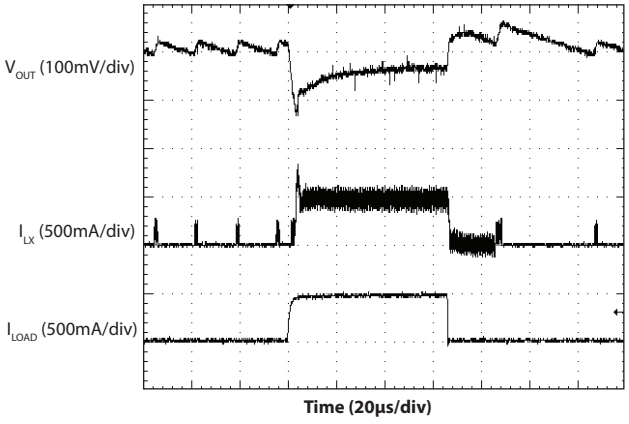
Light Load Soft-start



Load Transient Response — 10 to 80mA

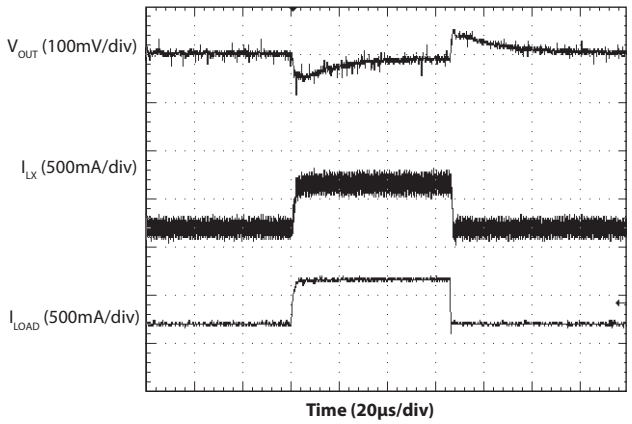


Load Transient Response — 10 to 500mA

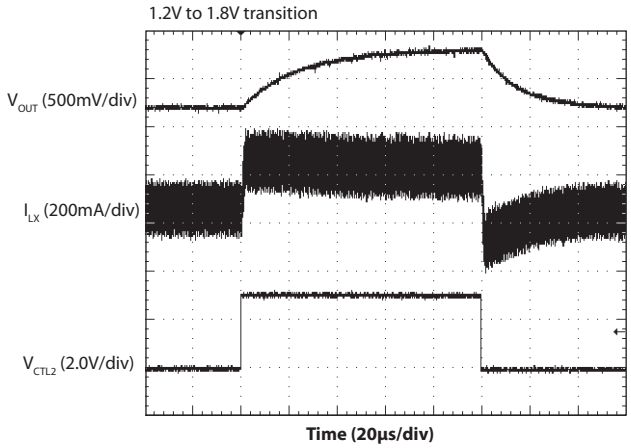


Typical Characteristics (continued)

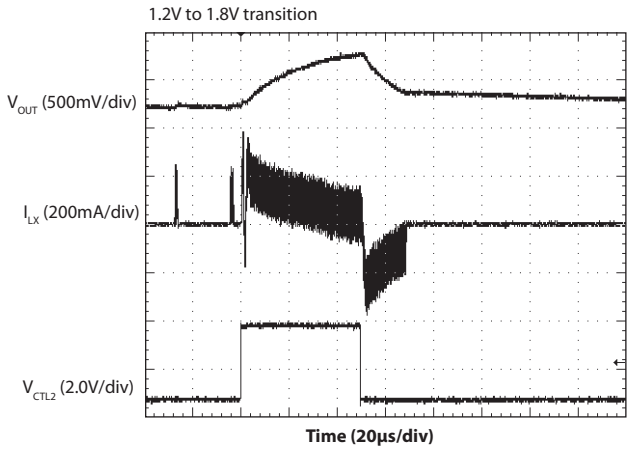
Load Transient Response — 200 to 500mA



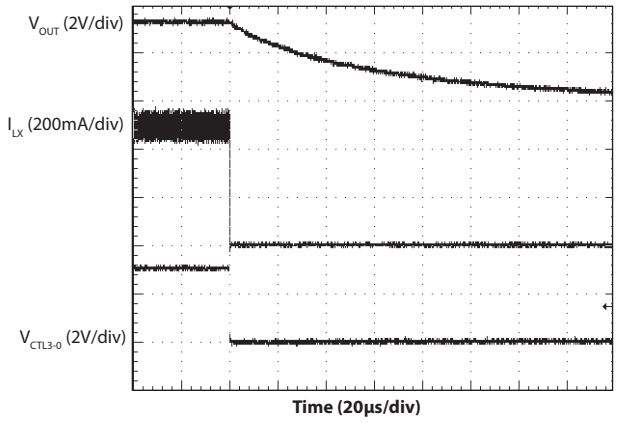
VID Transient Response — PWM



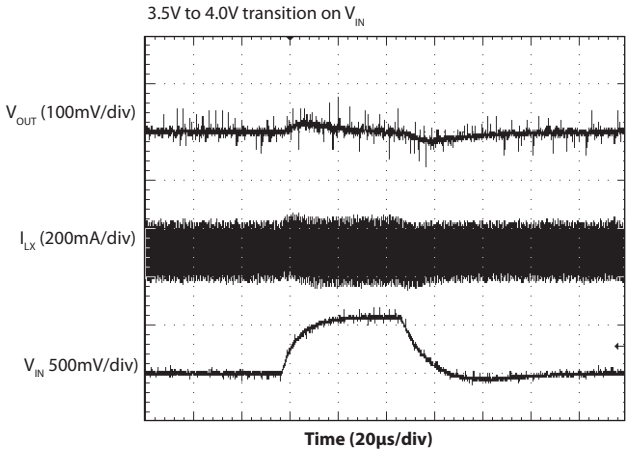
VID Transient Response — PSAVE



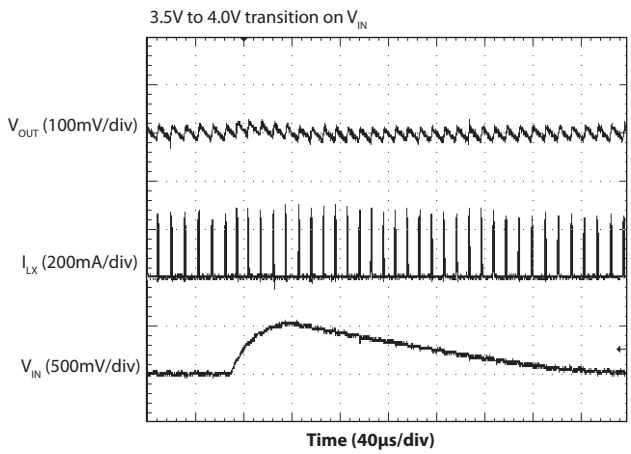
Shutdown Transient Response



Line Transient Response — PWM



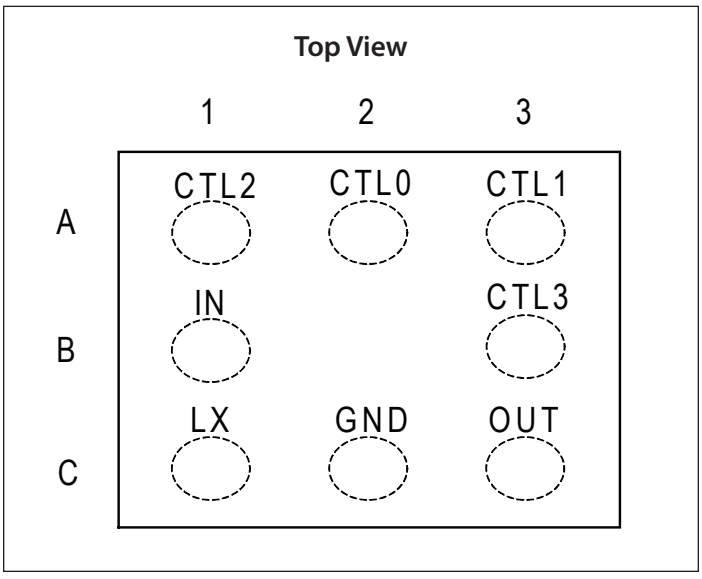
Line Transient Response — PSAVE



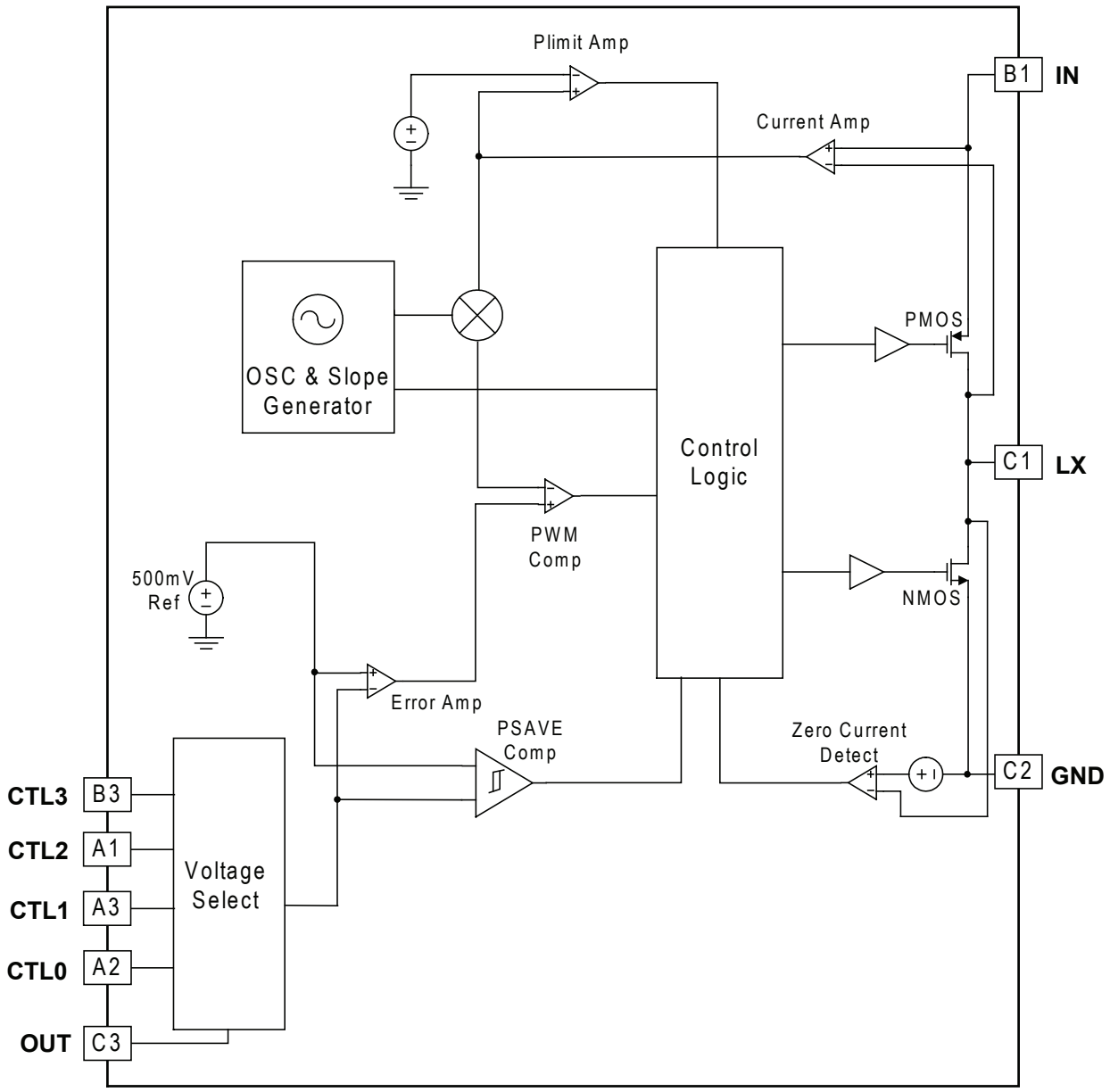
Bump Descriptions

Bump	Bump Name	Bump (Pin) Function
A1	CTL2	Control bit 2 — see Table 1, page 2, for decoding. This pin has a weak pull-down resistor (> 1MΩ) in place at reset that is removed when CTL2 is pulled above the logic high threshold.
A2	CTL0	Control bit 0 — see Table 1, page 2, for decoding. This pin has a weak pull-down resistor (> 1MΩ) in place at reset that is removed when CTL0 is pulled above the logic high threshold.
A3	CTL1	Control bit 1 — see Table 1, page 2, for decoding. This pin has a weak pull-down resistor (> 1MΩ) in place at reset that is removed when CTL1 is pulled above the logic high threshold.
B1	IN	Input power supply pin — connect a bypass capacitor from this pin to GND. 4.7µF minimum is recommended.
B3	CTL3	Control bit 3 — see Table 1, page 2, for decoding. This pin has a weak pull-down resistor (> 1MΩ) in place at reset that is removed when CTL3 is pulled above the logic high threshold.
C1	LX	Switching output — connect an inductor between this pin and the output capacitors and load to filter the LX switching pulses.
C2	GND	Ground reference and power ground.
C3	OUT	Output voltage sense pin — output voltage regulation point (connection node of inductor and output capacitor).

Bump Array Configuration



Block Diagram



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Applications Information

General Description

The SC195B is a synchronous step-down Pulse Width Modulated (PWM) DC-DC regulator utilizing a 3.5MHz fixed-frequency voltage mode architecture. The device is designed to operate in fixed-frequency PWM mode and enter power save (PSAVE) mode utilizing pulse frequency modulation under light load conditions to maximize efficiency. The device requires only two capacitors and a single inductor to be implemented in most systems. The switching frequency has been chosen to minimize the size of the inductor and capacitors while maintaining high efficiency. The output voltage is programmable, eliminating the need for external programming resistors. Loop compensation is also internal, eliminating the need for external components to control stability.

Programmable Output Voltage

The SC195B has 15 fixed output voltage levels which can be individually selected by programming the CTL control pins (CTL3-0 — see Table 1 on page 2 for settings). The device is disabled whenever all four CTL pins are pulled low and enabled whenever at least one of the CTL pins is pulled high. This configuration eliminates the need for a dedicated enable pin.

CTL Input Resistance

Each CTL pin is internally pulled down via 1MΩ at power up if V_{IN} is below 1.5V or if the voltage on the control pin is below the input high voltage. This ensures that the output is disabled when power is applied if there are no inputs to the CTL pins. Each 1MΩ pull-down is disabled whenever its pin is pulled high and remains disabled until all CTL pins are pulled low.

Output Voltage Setting

The output voltage can be set using different approaches. If a static output voltage is required, the CTL pins can be tied to either IN or GND to set the desired voltage whenever power is applied at IN. If enable control is required, each CTL pin can be tied to either GND or to a microprocessor I/O line to create the desired control code whenever the control signal is forced high. This approach is equivalent to using the CTL pins collectively as a single enable pin. A third option is to connect each of the four CTL pins to individual microprocessor I/O lines. Any of the 15 output voltages can be programmed using this approach. If only two output voltages are needed, the CTL pins can be combined in a way that will reduce the number of I/O lines to 1, 2, or 3, depending on the control code for each desired voltage. Other CTL pins could be hard wired to GND or IN. This option allows dynamic voltage adjustment for systems that reduce the supply voltage when entering sleep states. Note that applying all zeros to the CTL pins when changing the output voltages will temporarily disable the device, so it is important to avoid this combination when dynamically changing levels.

Dynamic Output Voltage Adjustment

Dynamically changing the CTL pins allows dynamic voltage adjustment for systems that reduce the supply voltage when entering sleep states. This should be done using specific procedures. Attention is required since applying all zeros in a very short period to the CTL pins when changing the output voltage will temporarily disable the device. Therefore it is important to avoid the combination of all zeros when dynamically changing the CTL levels. For example, when the CTLs change from 0001 to 0010 (0.8V to 1.0V), a transitional state of 0000 (shut down) state might occur for a very short period of time, which could result the device being disabled unintentionally. In order to achieve such operation, the correct logic transition stages can be arranged in this way: 0001--0011--0010 (0.8V--1.1V--1V). The very short transition state 0011 would keep the part in operation but not affect the voltage transition waveform.

When the CTL pins are changed to raise the output voltage, the regulator increases the inductor current to force the output voltage to slew up. A large change in the voltage setting could result in over-current due to charging the output capacitor. For large voltage steps it is recommended to use minimal output capacitors and to raise the voltage in smaller steps to reduce the transient inductor current.

When the CTL pins are changed to decrease the output voltage, the output response will vary depending on the operating mode. If the device is operating in PWM mode, the regulator will continue active switching and will bring the output capacitors down to match the new CTL setting. If the device is operating in PSAVE mode, the

Applications Information (continued)

regulator will stop switching; in this case the regulator relies on the load current to discharge the output capacitors and bring the output voltage down to the desired setting.

Note that if the commanded decrease in output voltage exceeds the Over-voltage threshold, the device will detect an Over-voltage condition regardless of whether the device is operation in PWM or PSAVE mode. All switching will stop and the output capacitors will discharge into the load. When the output voltage falls to the new CTL setting, previous switching operation will resume.

Voltage Selection

If an output voltage other than one of the 15 programmable settings is needed, external resistors can be added to adjust the output voltage setting. The resistor values can be determined using the following equation.

$$V_{OUT} = V_{SET} \times \left[\frac{R_{FB1} + R_{FB2}}{R_{FB2}} \right] + I_{LEAK} \times R_{FB1}$$

V_{OUT} is the desired output voltage, V_{SET} is the voltage setting from the CTL pins, R_{FB1} is the resistor between the output capacitor and the OUT pin, R_{FB2} is the resistor between the OUT pin and ground, and I_{LEAK} is the leakage current into the OUT pin during normal operation. The I_{LEAK} input current is typically 1µA, so the last term of the equation can be neglected if the current through R_{FB2} is much larger than 1µA. Selecting a resistor value of 10kΩ or lower will simplify the design. If I_{LEAK} is neglected and R_{FB2} is fixed, R_{FB1} can be determined using the equation

$$R_{FB1} = R_{FB2} \times \frac{V_{OUT} - V_{SET}}{V_{SET}}$$

Inserting resistance in the feedback loop will adversely affect the system's transient performance if feed-forward capacitance is not included in the circuit.

Figure 1 illustrates how the resistor divider and feed-forward capacitor can be added to the SC195B circuit.

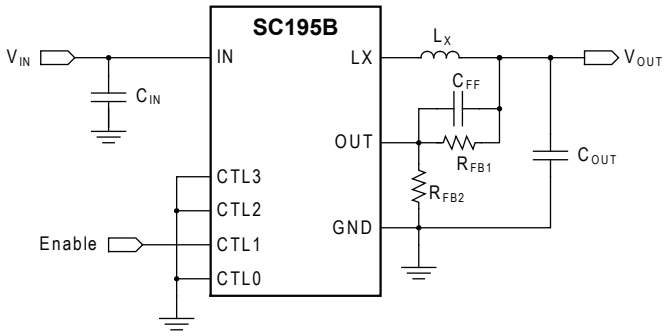


Figure 1 — Application Circuit with External Resistors

The value of feed-forward capacitance needed can be determined using the equation

$$C_{FF} = 4 \times 10^{-6} \times \frac{V_{SET}(V_{OUT} - 0.5)^2}{R_{FB1}(V_{OUT} - V_{SET})(V_{SET} - 0.5)}$$

V_{OUT} is the selected voltage using the CTL pins and V_{SET} is the final desired voltage. To simplify the design, it is recommended to program the output setting to 1.0V, use resistor values smaller than 10kΩ, and include a feed-forward capacitance calculated with the equation above. If V_{OUT} is set to 1.0V, the previous equation reduces to

$$C_{FF} = 8 \times 10^{-6} \times \frac{(V_{OUT} - 0.5)^2}{R_{FB1}(V_{OUT} - 1)}$$

Example:

An output voltage of 1.3V is desired, but this is not a programmable option. What external component values for Figure 1 are needed?

Solution: To keep the circuit simple, set R_{FB2} to 10kΩ so current into the OUT pin can be neglected and set the CTL3-0 pins to 0010 (1.0V setting). The necessary component values for this situation are

$$R_{FB1} = R_{FB2} \times \frac{V_{OUT} - V_{SET}}{V_{SET}} = 3k\Omega$$

$$C_{FF} = 8 \times 10^{-6} \times \frac{(V_{OUT} - 0.5)^2}{R_{FB1}(V_{OUT} - 1)} = 5.69nF$$

Applications Information (continued)

PWM Operation

Normal PWM operation occurs when the output load current exceeds the PSAVE threshold. In this mode, the PMOS high side switch is activated with the duty cycle required to produce the output voltage programmed by the CTL pins. An internal synchronous NMOS rectifier eliminates the need for an external Schottky diode on the LX pin. The duty cycle (percentage of time PMOS is active) increases as V_{IN} decreases to maintain output voltage regulation. As V_{IN} approaches the programmed output voltage, the duty cycle approaches 100% (PMOS always on) and the device enters a pass-through mode until the input voltage increases or the load decreases enough to allow PWM switching to resume.

Power Save Mode Operation

When the load current decreases below the PSAVE threshold, PWM switching stops and the device automatically enters PSAVE mode. This threshold varies depending on the input voltage and output voltage setting, optimizing efficiency for all possible load currents in PWM or PSAVE mode. While in PSAVE mode, output voltage regulation is controlled by a series of switching bursts. During a burst, the inductor current is limited to a peak value which controls the on-time of the PMOS switch. After reaching this peak, the PMOS switch is disabled and the NMOS switch is enabled, and the inductor current then decreases to near 0mA. Switching bursts continue until the output voltage climbs to the V_{OUT} +2.5% threshold. Switching is then stopped to eliminate switching losses and enhance overall efficiency. Switching resumes when the output voltage reaches the lower threshold of V_{OUT} and continues until the upper +2.5% threshold again is reached. Note that the output voltage is regulated hysteretically while in PSAVE mode between V_{OUT} and V_{OUT} + 2.5%. The period and duty cycle while in PSAVE mode are determined by V_{IN} and V_{OUT} until PWM mode resumes. This can result in the switching frequency being much lower than the PWM mode frequency.

If the output load current increases enough to cause V_{OUT} to decrease below the PSAVE exit threshold (V_{OUT} - 4%), the device automatically exits PSAVE and operates in continuous PWM mode. Figure 2 illustrates the transitions from PWM mode to PSAVE mode and back to PWM mode.

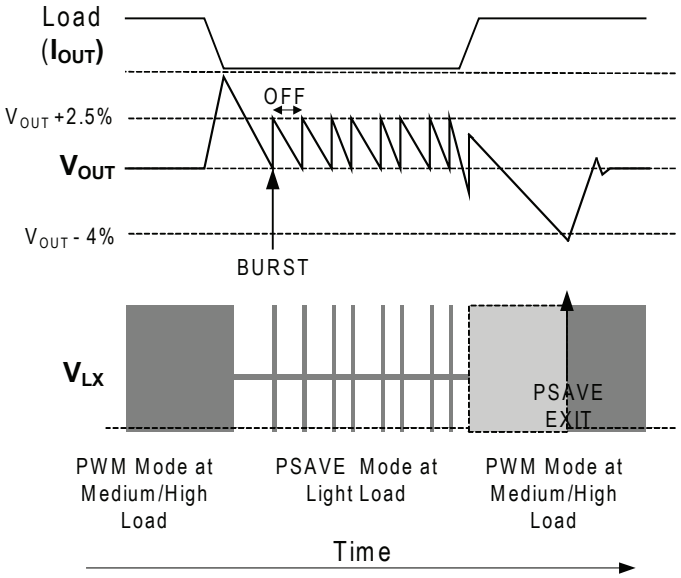


Figure 2 — Transitions Between PWM and PSAVE Modes

Protection Features

The SC195B provides these protection features:

- Soft-Start Operation
- Over-Voltage Protection
- Current Limit
- Thermal Shutdown
- Under-Voltage Lockout

Soft-Start

The soft-start sequence is activated by a transition from an all zeros CTL code to a non-zero CTL code, which enables the device. Switching begins after an internal 20µs start-up period. During switching, the PMOS current limit steps through four levels of 25%, 40%, 60%, and 100% of the Current Limit Threshold. Each current level is maintained for 256 clock cycles (73µs).

During each level, switching is not based on the internal 3.5MHz clock. Instead, the PMOS transistor is on until the current ramps up to the corresponding level. The PMOS then turns off and the low-side NMOS is on until the current returns to zero. The PMOS transistor then turns on and the pattern repeats. With this method, the inductor current is a series a triangular current pulses, at a frequency lower than the internal 3.5MHz clock, each pulse going from zero up to the corresponding level. Note that this operation is similar to the Power Save Mode Operation.

Applications Information (continued)

The full start-up period is 260µs, including the 20µs needed to initialize the internal circuitry. The output voltage may reach the regulation point before the full 260µs period has passed. If the internal feedback signal derived from V_{OUT} reaches 86% of the target during the soft-start sequence, the device will then switch to forced PWM operation until the sequence is completed. The switch-over point may correspond to a voltage lower than 86% as seen at V_{OUT} due to internal impedance connected between the V_{OUT} pin and the internal feedback signal. Note the V_{OUT} ripple in PSAVE mode can be larger than the ripple in PWM mode.

Note that the limited current available during Soft-Start will limit the maximum supportable capacitance and load. The inductor current must charge the output capacitor as well as provide any start-up load current. When the regulator reaches the end of the 4th current level (100%), the output capacitor must be charged sufficiently to prevent the regulator from going into Current Limit protection. If the Current Limit is reached and extends for 32 clock cycles, the regulator will enter Fold-back protection. Figure 3 shows a picture of this start-up behavior.

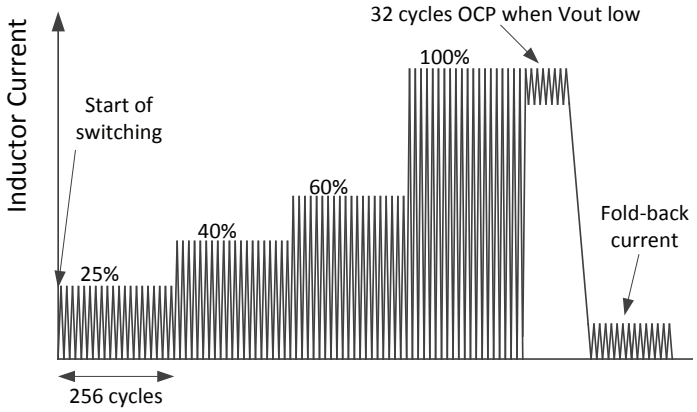


Figure 3 — Soft-start Cycle

For a selected Vout and load current, the maximum output capacitance can be determined from the following equation, with Load in amperes, V_{OUT} in volts and C_{OUT} in µF.

$$C_{OUT} = \frac{1}{V_{OUT}} \cdot \left(\frac{680}{10 - V_{OUT}} - 100 \cdot Load \right)$$

Over-Voltage Protection

Over-voltage protection disables the PWM drive when V_{OUT} exceeds the regulation voltage by 15%. When the output voltage falls below the 15% threshold the device resumes previous switching operation. If the device was operating in PSAVE mode then switching will be disabled until the voltage falls to lower hysteresis level used in PSAVE operation. If the device was operating in PWM mode, switching will resume to actively bring the output back to regulation.

Current Limit

The SC195B switching stage is protected by a current limit function. If the output load exceeds the PMOS current limit for 32 consecutive switching cycles, the device enters fold-back current limit mode and the output current is limited to approximately 215mA. Note that the fold-back current is moderately affected by the actual DC output voltage. During fold-back conditions, the output voltage will be the product of I_{FB-LIM} and the load resistance. The load must fall below I_{FB-LIM} for the device to exit fold-back current limit mode. This function makes the device capable of sustaining an indefinite short circuit on its output under fault conditions.

Thermal Shutdown

The SC195B has a thermal shutdown feature to protect the device if the junction temperature exceeds 160°C. During thermal shutdown, the PMOS and NMOS switches are both disabled, tri-stating the LX output. When the junction temperature drops by the hysteresis value (20°C), the device goes through the soft-start process and resumes normal operation.

Under-Voltage Lockout

Under-Voltage Lockout (UVLO) activates when the supply voltage drops below the UVLO threshold. This prevents the device from entering an ambiguous state in which regulation cannot be maintained. Hysteresis of approximately 200mV is included to prevent chattering near the threshold.

Inductor Selection

The SC195B is designed to operate with a 1µH inductor between the LX pin and the OUT pin. Other values may lead to instability, malfunction, or out-of-specification

Applications Information (continued)

performance. The specified current levels for PSAVE entry, PSAVE exit, and current limit are dependent on the inductor value.

The SC195B converter has internal loop compensation. The compensation is designed to work with a specific single-pole output filter corner frequency defined by the equation

$$f_C = \frac{1}{2\pi\sqrt{L \times C_{OUT}}}$$

where L = 1µH and C_{OUT} = 10µF.

When selecting output filter components, the LC product should not vary over a wide range. Selection of smaller inductor and capacitor values will move the corner frequency, potentially impacting system stability.

It is also important to consider the change in inductance with DC bias current when choosing an inductor. The inductor saturation current is specified as the current at which the inductance drops a specific percentage from the nominal value (approximately 30%). Except for short-circuit or other fault conditions, the peak current must always be less than the saturation current specified by the manufacturer. The peak current is the maximum load current plus one half of the inductor ripple current at the maximum input voltage. Load and/or line transients can cause the peak current to exceed this level for short durations. Maintaining the peak current below the inductor saturation specification keeps the inductor ripple current and the output voltage ripple at acceptable levels. Manufacturers often provide graphs of actual inductance and saturation characteristics versus applied inductor current. The saturation characteristics of the inductor can vary significantly with core temperature. Core and ambient temperatures should be considered when examining the core saturation characteristics.

When selecting the inductor, the DC resistance (DCR) must also be examined. Efficiency can be optimized by lowering the inductor's DCR as much as possible. Low DCR in an inductor requires either more surface area for the increased wire diameter or fewer turns to reduce the length of the copper winding. Fewer turns requires an inductor core with a larger cross-sectional area in order to maintain the same saturation characteristics. The inductor size must always be considered when examining the inductor DCR to determine the best compromise between DCR and component area on a PCB. Note that the ripple component of the inductor is a small percentage of the DC load. AC losses in the inductor core and winding do not contribute significantly to the total losses.

Magnetic fields associated with the output inductor can interfere with nearby circuitry. This can be minimized by the use of low-noise shielded inductors which use the minimum gap possible to limit the distance that magnetic fields can radiate from the inductor. Shielded inductors, however, typically have a higher DCR and are, therefore, less efficient than a similar sized non-shielded inductor.

Final inductor selection depends on various design considerations such as efficiency, EMI, size, and cost. Table 2 lists the manufacturers of recommended inductor options. The inductors with larger packages tend to provide better overall efficiency, while the smaller package inductors provide decent efficiency with reduced footprint or height. The saturation current ratings and DC characteristics are also shown.

Table 2 — Recommended Inductors

Manufacturer Part Number	L (µH)	DCR (Ω)	Saturation Current (mA)	L at 400mA (µH)	Dimensions LxWxH (mm)
Murata LQM21PN1R0MC0	1.0±20%	0.19	800	0.75	2.0x1.25x0.55
Murata LQM2HPN1R0MJ0	1.0±20%	0.09	1500	0.95	2.5x2.0x1.1
Murata LQM31PN1R0M00	1.0±20%	0.12	1200	0.95	3.2x1.6x0.85
Taiyo Yuden CKP25201R0M-T	1.0±20%	0.08	800	0.88	2.5x2.0x1.0
Toko MDT2012-CR1R0N	1.0±30%	0.08	1350	1.00	2.0x1.25x1.0
FDK MIPSZ2012D1R0	1.0±30%	0.09	1100	1.00	2.0x1.25x1.0
FDK MIPSU2520D1R0	1.0±30%	0.08	1300	0.78	2.5x2.0x0.5
Taiyo Yuden BRC1608T1R0M	1.0±20%	0.18	850	0.90	1.6x0.8x0.8

Applications Information (continued)

C_{OUT} Selection

The internal voltage loop compensation in the SC195B limits the minimum output capacitor value to 10µF. This is due to its influence on the loop crossover frequency, phase margin, and gain margin. Increasing the output capacitor above this minimum value will reduce the crossover frequency and provide greater phase margin. A capacitor between 10µF and 22µF will usually be adequate in stabilizing the output during large load transitions. Note that in some cases the maximum output capacitance may be limited due to load current that is applied during the Soft-Start sequence, as described in the Soft-Start section.

Capacitors with X7R or X5R ceramic dielectric are recommended for their low ESR and superior temperature and voltage characteristics. Y5V capacitors should not be used as their temperature coefficients make them unsuitable for this application.

In addition to ensuring stability, the output capacitor serves other important functions. This capacitor determines the output voltage ripple — as capacitance increases, ripple voltage decreases. It also supplies current during a large load step for a few switching cycles until the control loop responds (typically 3 switching cycles). Once the loop responds, regulation is restored and the desired output is reached. During the period prior to PWM operation resuming, the relationship between output voltage and output capacitance can be approximated using the equation

$$C_{OUT} = \frac{3 \times \Delta I_{LOAD}}{V_{DROOP} \times f}$$

This equation can be used to approximate the minimum output capacitance needed to ensure voltage does not droop below an acceptable level. For example, a load step from 200mA to 500mA requiring droop less than 40mV would require the minimum output capacitance to be

$$C_{OUT} = \frac{3 \times 0.3}{0.04 \times 3.5 \times 10^{6}} = 6.4\,\mu F$$

In this example, using a standard 10µF capacitor would be adequate to keep voltage droop below the desired limit. Note that if the voltage droop limit were decreased from 40mV to 20mV, the output capacitance would need to be increased to at least 12.8µF (twice as much capacitance for half the droop). Capacitance will decrease from the nominal value when a ceramic capacitor is biased with a DC voltage, so it is important to select a capacitor whose value exceeds the necessary capacitance value when biased at the programmed output voltage. Check the manufacturer's capacitance vs. DC voltage graphs when selecting an output capacitor to ensure the capacitance will be adequate. Table 3 lists the manufacturers of recommended output capacitor options.

Table 3 — Recommended Output Capacitors

Manufacturer Part Number	Value (µF)	Type	Rated Voltage (VDC)	Dimensions LxWxH (mm) Case Size
Murata GRM188R60J106ME47D	10±20%	X5R	6.3	1.6x0.8x0.8 0603
Murata GRM21BR60J106K	10±10%	X5R	6.3	2.0x1.25x1.25 0805
Taiyo Yuden JMK107BJ106MA-T	10±20%	X5R	6.3	1.6x0.8x0.8 0603
TDK C1608X5R0J106MT	10±20%	X5R	6.3	1.6x0.8x0.8 0603

C_{IN} Selection

The SC195B input source current will appear as a series of current pulses approximately equal to the load current. To prevent large input voltage ripple, a low ESR ceramic capacitor is required. A minimum value of 4.7µF should be used. It is important to consider the DC voltage coefficient characteristics when determining the actual required value. For example, a 10µF, 6.3V, X5R ceramic capacitor with 5V DC applied may exhibit a capacitance as low as 4.5µF. The value of required input capacitance is estimated by determining the acceptable input ripple voltage and calculating the minimum value required for C_{IN} using the equation

$$C_{IN} = \frac{\frac{V_{OUT}}{V_{IN}}\left(1 - \frac{V_{OUT}}{V_{IN}}\right)}{\left(\frac{\Delta V}{I_{OUT}} - ESR\right) f}$$

For a given V_{OUT} the input voltage ripple is maximum when the V_{IN} is twice V_{OUT}, (at 50% duty cycle).

Applications Information (continued)

The input capacitor provides a low impedance loop for the edges of pulsed current drawn by the PMOS switch. Low ESR/ESL X5R ceramic capacitors are recommended for this function. To minimize stray inductance, the capacitor should be placed as closely as possible to the IN and GND pins.

Table 4 lists the recommended input capacitor options from different manufacturers.

Table 4 — Recommended Input Capacitors

Manufacturer Part Number	Value (µF)	Type	Rated Voltage (VDC)	Dimensions LxWxH (mm) Case Size
Murata GRM188R60J475K	4.7±10%	X5R	6.3	1.6x0.8x0.8 0603
Murata GRM188R60J106K	10±10%	X5R	6.3	1.6x0.8x0.8 0603
Taiyo Yuden JMK107BJ475KA	4.7±10%	X5R	6.3	1.6x0.8x0.8 0603
TDK C1608X5R0J475KT	4.7±10%	X5R	6.3	1.6x0.8x0.8 0603

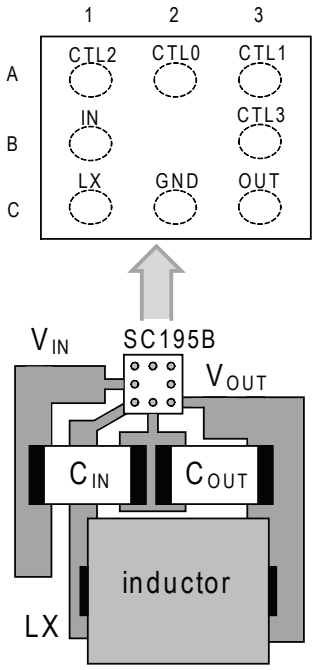
PCB Layout Considerations

Poor PCB layout can result in poor output voltage regulation and other noise problems.

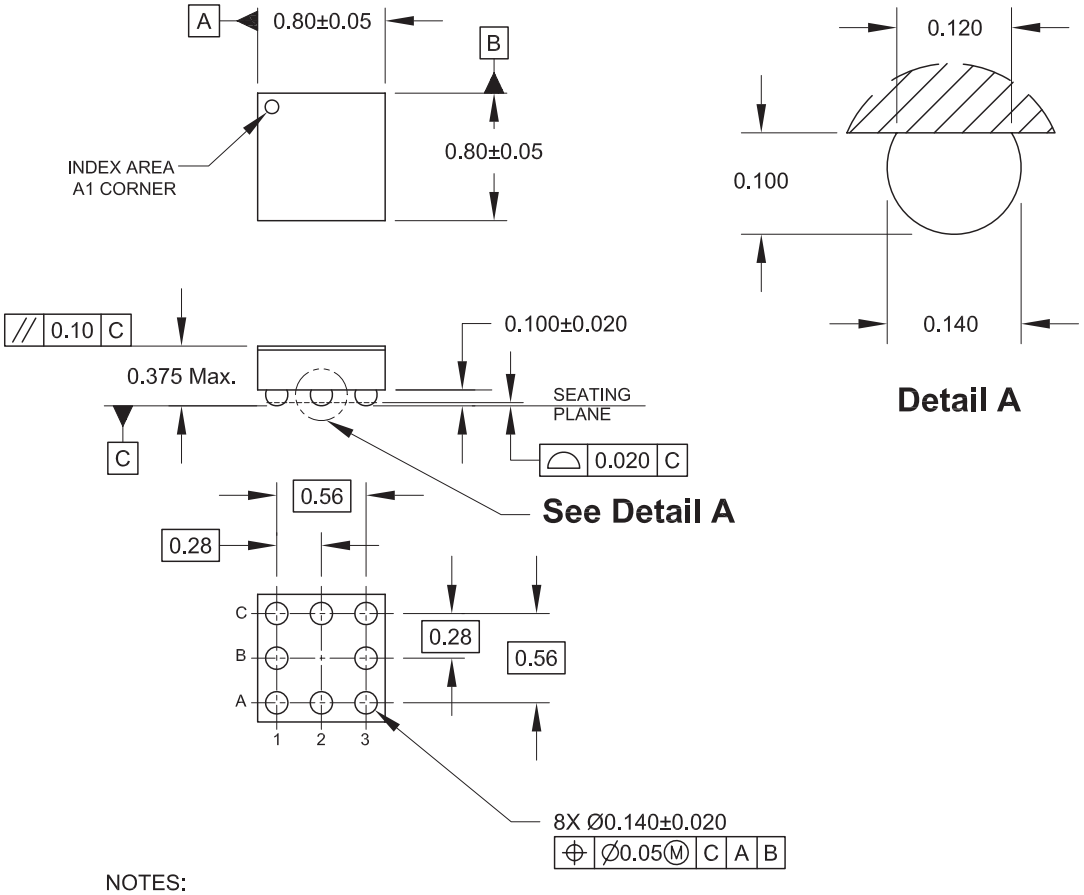
The following guidelines are recommended for designing a PCB layout and component placement, see Figure 4:

1. Place C_{IN} as close as possible to the IN and GND pins. This capacitor provides a low impedance loop for the pulsed currents present at the buck converter's input. Use short wide traces to minimize trace impedance. This will also minimize EMI and input voltage ripple by localizing the high frequency current pulses.
2. Place C_{OUT} close to the GND and OUT pins.
3. The LX trace can go underneath the input capacitor to one terminal of the inductor. The other terminal of the inductor connects to the V_{OUT} copper pad.
4. Use a ground plane to improve thermal performance.
5. Use a heavy copper trace to directly connect from the output capacitor to the load point to reduce the copper voltage drop. The regulation sense point for the SC195B is at the OUT pin.
6. Traces for the CTL pins should avoid these high noise traces: the LX trace between the inductor and the LX pin, the VIN trace between CIN and the IN pin, and the GND trace between and the GND pin.

Figure 4 — PCB Layout and Component Placement

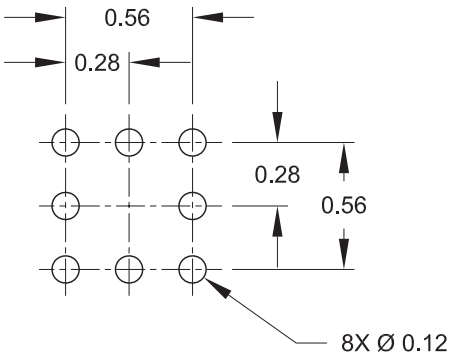


Outline Drawing — WLCSP8-0.80X0.80



NOTES:
1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS

Land Pattern — WLCSP8



NOTES:

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