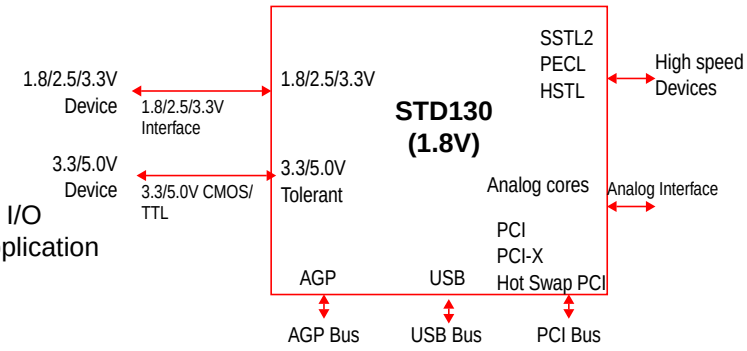
STD130 Standard Cell
0.18um System-On-Chip ASIC

Dec 2000, V2.0

Features

- L_{eff}= 0.15um, L_{drawn} = 0.18um
- Up to 23 million gates
- Power dissipation :24nW/MHz
- Gate Delay : 48ps @ 1.8V, 1SL
- 1.8/2.5/3.3V drive and 3.3/5V tolerant I/O
- Compilable SRAM for two different application
- 1.8V and 3.3V ADC,DAC and PLLs
- ARM920T/ARM940T, TeakLite/Teak



Description

STD130 is one of the Samsung ASIC library, which consists of standard cell products implemented in a 0.18um technology. STD130 utilizes six layers of interconnect metal having metal 4, 5 and 6 layer options for products. STD130 is diverse application specific digital and analog IPs for system-on-chip(SOC) application. Samsung provides a full range of products to address the challenges of producing ultra low power and high density devices that take advantage of SOC integration.

STD130 which reduced power dissipation and system cost by merging the logic and IPs as a whole and connecting internally from logic to memory data bus is ideal for high-performance products such as HDD, Network, and Display.

STD130 supports up to 23 million gates counts of logic providing 80% of usable gate. Gate delay is 30% faster than that of STD110, 0.25um library. Logic and compiled memory density are respectively 2.6 times and 3 timer denser than those of STD110.

STD130 also supports fully user-configurable compiled memory elements such as high-density and low-power applications. Each element is provided as a compiler. For high-capacity memory solution in SOC design, the repairable memory containing redundancy scheme is provided as a compiler.

Variety of IPs are provided in STD130 family including

- Processor Cores :
  ARM7T/ARM9T/940T/920T from ARM, Teaklite/TEAK from DSPG
- Memories
  Compiled SRAM with two different application and repairable SRAM with redundancy.
- Analog Cores :
  ADC, DAC, PLL, RAMDAC
- IO IPs

Samsung design methodology offers an comprehensive timing driven design flow including automated time budgeting, tight floorplan synthesis integration, powerful timing analysis and timing driven layout. Its advanced characterization flow provides accurate timing data and robust delay models for a 0.18um very deep-submicron technology. Static verification methods such as static timing analysis and formal equivalence checking provide an effective verification methodology with a variety of simulators. Samsung DFT methodology supports scan design, BIST and JTAG boundary scan. Samsung provides a full set of test-ready IPs with an efficient core test integration methodology.

Samsung ASIC Macros

Analog Cores

- Ultra low voltage analog cores : 1.8V
- High Resolution analog cores : 3.3V

Analog Cores	Bit	Supply Voltage	
		3.3V± 5%	1.8V± 5%
ADC	8	- 125MHz	- 250KHz
	10	-	- 30MHz
	12	- 250KHz - 10MHz	-
DAC	10	-	- 80MHz
	12	- 2MHz - 300MHz	-
CODEC	14	- 8K~11KHz (2.5V)	-
PLL			- 25~300MHz(FS) - 100~500MHz(FS) - 200MHz(SSCG)

Digital Cores

Application	Hard macro	Soft macro
CPU cores	- ARM7TDMI - ARM9TDMI - ARM940T - ARM920T	AMBA, AHB Wrapper
DSP cores	- Teaklite - Teak	-
Interface cores	-	USB1.1, USB2.0, IrDA UART(16C450,16C550) IEEE1284, P1394a LINK
Communica-tion cores	-	10/100 Ethernet MAC
Decoder	-	RS Decoder, Viterbi Decoder

Memory Compiler

- Fully compilable application specific SRAM
- High-density(HD) and low-power(LP)
- Single-port(1RW, 1R), dual-port(2RW), multi-port(1R1W~2R2W)
- Duty-free cycle and zero hold time in synchronous
- Bit-write feature available
- 2-bank architecture
- Up to 1M-bit high-capacity repairable SRAM with redundancy

Name	Availa-bility		Description
	HD	LP	
SPSRAM	O	O	- Single Port Synchronous static RAM - up to 512K bits
SPSRAMBW	O	O	- SPSRAM with Bit-Write - up to 512K bits
SPSRAMR	O	X	- SPSRAM with Redundancy - up to 1M bits
DPSRAM	O	O	- Dual Port Synchronous static RAM - up to 256K bits
DPSRAMBW	O	O	- DPSRAM with Bit-Write - up to 256K bits
SPARAM	O	O	- Single Port Asynchronous static RAM - up to 512K bits
SPARAMBW	O	O	- SPARAM with Bit-Write - up to 512K bits
DROM	O	X	- Synchronous Diffusion pro-grammable ROM - up to 512K bits
MROM	O	X	- synchronous Metal-2 pro-grammable ROM - up to 512K bits
ARFRAM	O	X	- multi-port Asynchronous Register File RAM - 1-to-2 write ports, 1-to-2 read ports - up to 16K bits
FIFO	O	X	- synchronous First-In First-Out memory - up to 64K bits
CAM	O	X	- synchronous Content Addressable Memory - up to 32K bits

X : Not Support

I/Os and I/O IPs

- 1.8V, 2.5V and 3.3V drive I/Os, 3.3V and 5V tolerant I/Os
- 3-level(high, medium, no) slew rate control
- Minimum wire bonded pad pitch
  - single in line(70um) I/Os
  - staggered(35/70um) I/Os
- Driving capability
  - 1,2,4,8,12,16,20,24mA(for drive I/Os)
  - 1,2,4,6mA (for tolerant I/Os)
- I/O IPs

Name	Description	Frequency(MHz)
PCI	2.1 compliant, 5V tolerant	33, 66
USB	1.1 compliant, Full speed/ Low speed	12/1.5
SSTL2	Class-I and II, SDRAM Interface	Up to 200
ATA	ATA4/UDMA66, 3.3/5V tolerant	
AGP	AGP2.0 compliant	66@1X,133@2X, 266@4X
PECL	ATM interface	200(single) 500(differential)
HSTL	1.5V, SRAM interface, programmable output impedance control	300
Hot Swap PCI	1V pre-charge, VIO pre-charge	33, 66
PCI-X	1.0 compliant, 3.3V	133

Recommended Operating Conditions

	Parameter	Rating		Unit
V_{DD}	DC supply voltage	1.8V I/O	1.65 to 1.95	V
		2.5V I/O	2.3 to 2.7	
		3.3V I/O	3.0 to 3.6	
		3.3V tolerant I/O	1.65 to 1.95	
		5V tolerant I/O	3.0 to 3.6	
	Analog Core DC supply voltage	3.3V core	3.3V± 5%	
		2.5V core	2.5V± 5%	
		1.8V core	1.8V± 5%	
T_A	Commercial temperature range		0 to 70	°C
	Industrial temperature range * If you want this range, please contact field application engineer in Samsung.		– 40 to 85	

ASIC Design Kit and EDA support

Design Flow	Design Kits
Logic Synthesis	Synopsys Design Compiler, Synopsys Physical Compiler
Logic Simulation	Cadence Verilog-XL, Cadence NC-Verilog, Viewlogic ViewSim, Mentor ModelSim-VHDL, Mentor ModelSim-Verilog, Synopsys VSS, Synopsys VCS
Scan Insertion and ATPG	Synopsys TestGen, Synopsys TestCompiler, Synopsys TetraMax, Mentor Fastscan
Static Timing Analysis	Synopsys PrimeTime
RC Analysis	Avant! Star-RC
Power Analysis	Synopsys DesignPower, CubicPower*
Formal Verification	Synopsys Formality, Chrysalis Design VERIFYer, Verplex Tuxedo-LEC
Fault Simulation	Cadence Verifault
Delay Calculator	CubicDelay*
Floorplanner	Avant! PlanetPL, Cadence DesignPlanner, CubicPlan*
P&R	Avant! Apollo, Cadence Silicon Ensemble
DRC and LVS	Dracula, Hercules, Calibre

* In-house tools

Package Availability

Package Type	# of Pins
QFP	256,208,176,160,144,128,100,80,64,48
Thin QFP	100,80
Power QFP	304,240,208,160,144,128,120,100
Plastic Leaded Chip Carrier	84,68,52,44,32,28,18
Plastic BGA	560,492,388,352,329,316,313,304,300, 292,272,256,225,208,196,153,119
Super BGA	696,648,540,352,304,256
Flat BGA	280,256,208,196,180,160,153,144,119, 64,48
Multi Chip Package	256,100,69,68,64,48,32

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