

TLC7524C, TLC7524E, TLC7524I 8-BIT MULTIPLYING DIGITAL-TO-ANALOG CONVERTERS

SLAS061D – SEPTEMBER 1986 – REVISED JUNE 2007

- Easily Interfaced to Microprocessors
- On-Chip Data Latches
- Monotonic Over the Entire A/D Conversion Range
- Segmented High-Order Bits Ensure Low-Glitch Output
- Interchangeable With Analog Devices AD7524, PMI PM-7524, and Micro Power Systems MP7524
- Fast Control Signaling for Digital Signal-Processor Applications Including Interface With TMS320
- CMOS Technology

KEY PERFORMANCE SPECIFICATIONS	
Resolution	8 Bits
Linearity error	1/2LSB Max
Power dissipation at $V_{DD} = 5V$	5mW Max
Setting time	100ns Max
Propagation delay time	80ns Max

description

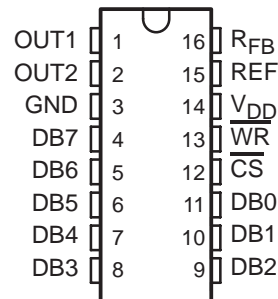
The TLC7524C, TLC7524E, and TLC7524I are CMOS, 8-bit, digital-to-analog converters (DACs) designed for easy interface to most popular microprocessors.

The devices are 8-bit, multiplying DACs with input latches and load cycles similar to the write cycles of a random access memory. Segmenting the high-order bits minimizes glitches during changes in the most significant bits, which produce the highest glitch impulse. The devices provide accuracy to 1/2LSB without the need for thin-film resistors or laser trimming, while dissipating less than 5mW typically.

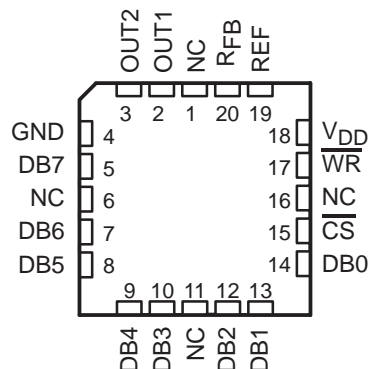
Featuring operation from a 5V to 15V single supply, these devices interface easily to most microprocessor buses or output ports. The 2- or 4-quadrant multiplying makes these devices an ideal choice for many microprocessor-controlled gain-setting and signal-control applications.

The TLC7524C is characterized for operation from 0°C to 70°C. The TLC7524I is characterized for operation from –25°C to +85°C. The TLC7524E is characterized for operation from –40°C to +85°C.

D, N, OR PW PACKAGE
(TOP VIEW)



FN PACKAGE
(TOP VIEW)



NC—No internal connection



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

All trademarks are the property of their respective owners.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

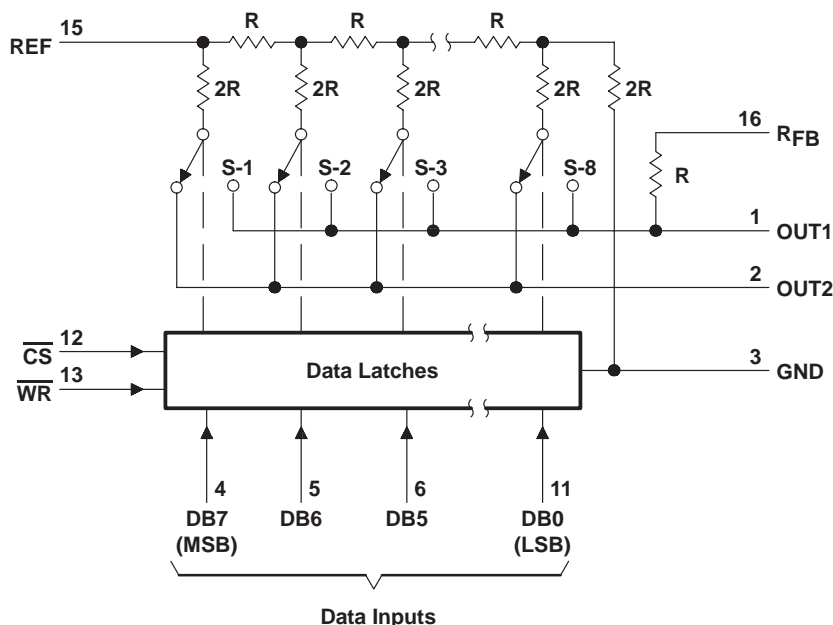
Copyright © 1998–2007, Texas Instruments Incorporated

TLC7524C, TLC7524E, TLC7524I

8-BIT MULTIPLYING DIGITAL-TO-ANALOG CONVERTERS

SLAS061D – SEPTEMBER 1986 – REVISED JUNE 2007

functional block diagram



Terminal numbers shown are for the D or N package.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V_{DD}	–0.3V to 16.5V
Digital input voltage range, V_I	–0.3V to $V_{DD} + 0.3V$
Reference voltage, V_{ref}	$\pm 25V$
Peak digital input current, I_I	10 μA
Operating free-air temperature range, T_A : TLC7524C	0°C to +70°C
TLC7524I	–25°C to +85°C
TLC7524E	–40°C to +85°C
Storage temperature range, T_{stg}	–65°C to +150°C
Case temperature for 10 seconds, T_C : FN package	+260°C
Lead temperature 1,6mm (1/16 inch) from case for 10 seconds: D, N, or PW package	+260°C

package/ordering information

For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

TLC7524C, TLC7524E, TLC7524I

8-BIT MULTIPLYING DIGITAL-TO-ANALOG CONVERTERS

SLAS061D – SEPTEMBER 1986 – REVISED JUNE 2007

recommended operating conditions

		V _{DD} = 5V			V _{DD} = 15V			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V _{DD}		4.75	5	5.25	14.5	15	15.5	V
Reference voltage, V _{ref}		±10			±10			V
High-level input voltage, V _{IH}		2.4			13.5			V
Low-level input voltage, V _{IL}		0.8			1.5			V
CS setup time, t _{su} (CS)		40			40			ns
CS hold time, t _h (CS)		0			0			ns
Data bus input setup time, t _{su} (D)		25			25			ns
Data bus input hold time, t _h (D)		10			10			ns
Pulse duration, $\overline{\text{WR}}$ low, t _w (WR)		40			40			ns
Operating free-air temperature, T _A	TLC7524C	0			+70			°C
	TLC7524I	−25			+85			
	TLC7524E	−40			+85			

electrical characteristics over recommended operating free-air temperature range, V_{ref} = ±10V, OUT1 and OUT2 at GND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{DD} = 5V			V _{DD} = 15V			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
I _{IH}	High-level input current	V _I = V _{DD}	10			10			μA
I _{IL}	Low-level input current	V _I = 0	−10			−10			μA
I _{lkg}	Output leakage current	OUT1 DB0–DB7 at 0V, \overline{WR} , \overline{CS} at 0V, V _{ref} = ±10V	±400			±200			nA
		OUT2 DB0–DB7 at V _{DD} , \overline{WR} , \overline{CS} at 0V, V _{ref} = ±10V	±400			±200			
I _{DD}	Supply current	Quiescent DB0–DB7 at V _{IH} min or V _{IL} max	1			2			mA
		Standby DB0–DB7 at 0V or V _{DD}	500			500			μA
k _{SVS}	Supply voltage sensitivity, Δgain/ΔV _{DD}		0.01 0.16			0.005 0.04			%FSR/%
C _i	Input capacitance, DB0–DB7, \overline{WR} , \overline{CS}		5			5			pF
C _o	Output capacitance	OUT1	30			30			pF
		OUT2	120			120			
		OUT1	120			120			
		OUT2	30			30			
Reference input impedance (REF to GND)			5	20		5	20		kΩ



TLC7524C, TLC7524E, TLC7524I

8-BIT MULTIPLYING DIGITAL-TO-ANALOG CONVERTERS

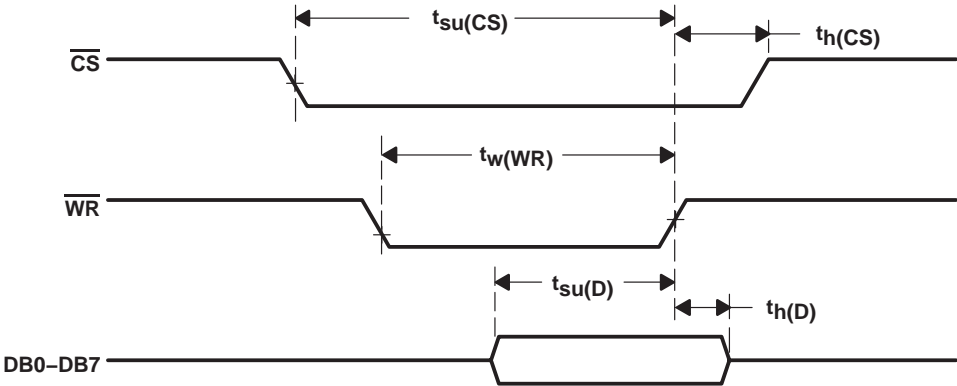
SLAS061D – SEPTEMBER 1986 – REVISED JUNE 2007

operating characteristics over recommended operating free-air temperature range, $V_{ref} = \pm 10V$, OUT1 and OUT2 at GND (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$V_{DD} = 5V$			$V_{DD} = 15V$			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
Linearity error				± 0.5			± 0.5	LSB
Gain error	See Note 1			± 2.5			± 2.5	LSB
Settling time (to 1/2 LSB)	See Note 2			100			100	ns
Propagation delay from digital input to 90% of final analog output current	See Note 2			80			80	ns
Feedthrough at OUT1 or OUT2	$V_{ref} = \pm 10V$ (100kHz sinewave) \overline{WR} and \overline{CS} at 0V, DB0–DB7 at 0V			0.5			0.5	%FSR
Temperature coefficient of gain	$T_A = +25^{\circ}C$ to MAX		± 0.004			± 0.001		%FSR/ $^{\circ}C$

NOTES: 1. Gain error is measured using the internal feedback resistor. Nominal full-scale range (FSR) = $V_{ref} - 1LSB$.
2. OUT1 load = 100Ω, $C_{ext} = 13pF$, \overline{WR} at 0V, \overline{CS} at 0V, DB0 – DB7 at 0V to V_{DD} or V_{DD} to 0V.

operating sequence



PRINCIPLES OF OPERATION

voltage-mode operation

It is possible to operate the current-multiplying DAC in these devices in a voltage mode. In the voltage mode, a fixed voltage is placed on the current output terminal. The analog output voltage is then available at the reference voltage terminal. Figure 1 is an example of a current-multiplying DAC, which is operated in voltage mode.

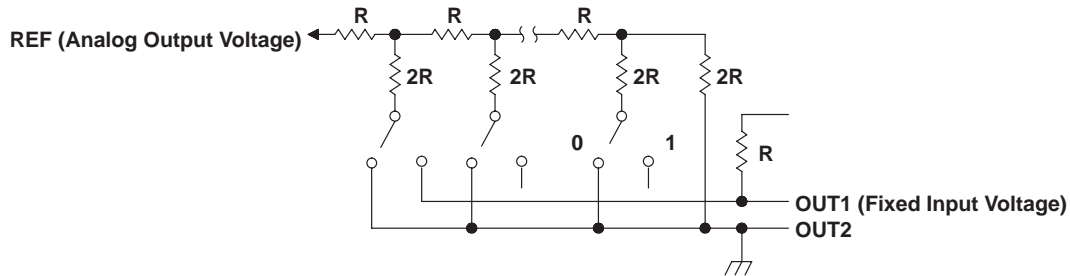


Figure 1. Voltage Mode Operation

The relationship between the fixed-input voltage and the analog-output voltage is given by the following equation:

$$V_O = V_I (D/256)$$

where

V_O = analog output voltage

V_I = fixed input voltage

D = digital input code converted to decimal

In voltage-mode operation, these devices meet the following specification:

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
Linearity error at REF	$V_{DD} = 5V$, $OUT1 = 2.5V$, $OUT2$ at GND, $T_A = +25^\circ C$		1	LSB

TLC7524C, TLC7524E, TLC7524I

8-BIT MULTIPLYING DIGITAL-TO-ANALOG CONVERTERS

SLAS061D – SEPTEMBER 1986 – REVISED JUNE 2007

PRINCIPLES OF OPERATION

The TLC7524C, TLC7524E, and TLC7524I are 8-bit multiplying DACs consisting of an inverted R-2R ladder, analog switches, and data input latches. Binary-weighted currents are switched between the OUT1 and OUT2 bus lines, thus maintaining a constant current in each ladder leg independent of the switch state. The high-order bits are decoded. These decoded bits, through a modification in the R-2R ladder, control three equally-weighted current sources. Most applications only require the addition of an external operational amplifier and a voltage reference.

The equivalent circuit for all digital inputs low is seen in Figure 2. With all digital inputs low, the entire reference current, I_{ref} , is switched to OUT2. The current source $I/256$ represents the constant current flowing through the termination resistor of the R-2R ladder, while the current source I_{lkg} represents leakage currents to the substrate. The capacitances appearing at OUT1 and OUT2 are dependent upon the digital input code. With all digital inputs high, the off-state switch capacitance (30pF maximum) appears at OUT2 and the on-state switch capacitance (120pF maximum) appears at OUT1. With all digital inputs low, the situation is reversed as shown in Figure 2. Analysis of the circuit for all digital inputs high is similar to Figure 2; however, in this case, I_{ref} would be switched to OUT1.

The DAC on these devices interfaces to a microprocessor through the data bus and the \overline{CS} and \overline{WR} control signals. When \overline{CS} and \overline{WR} are both low, analog output on these devices responds to the data activity on the DB0–DB7 data bus inputs. In this mode, the input latches are transparent and input data directly affects the analog output. When either the \overline{CS} signal or \overline{WR} signal goes high, the data on the DB0–DB7 inputs are latched until the \overline{CS} and \overline{WR} signals go low again. When \overline{CS} is high, the data inputs are disabled regardless of the state of the \overline{WR} signal.

These devices are capable of performing 2-quadrant or full 4-quadrant multiplication. Circuit configurations for 2-quadrant or 4-quadrant multiplication are shown in Figure 3 and Figure 4. Table 1 and Table 2 summarize input coding for unipolar and bipolar operation respectively.

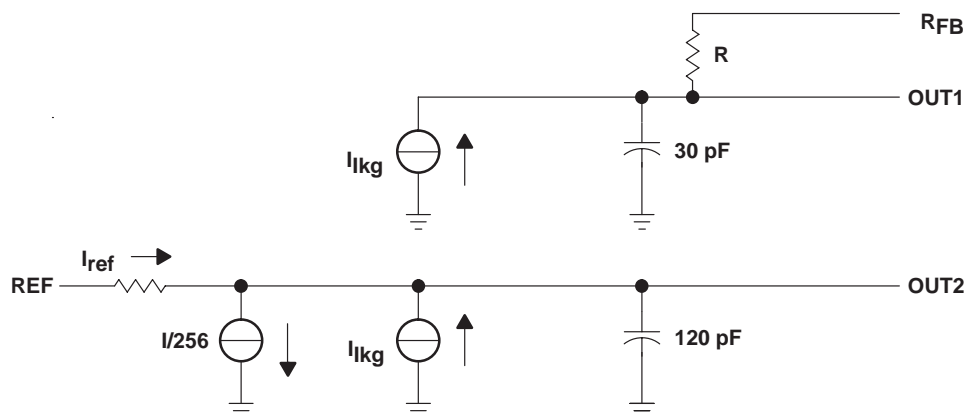


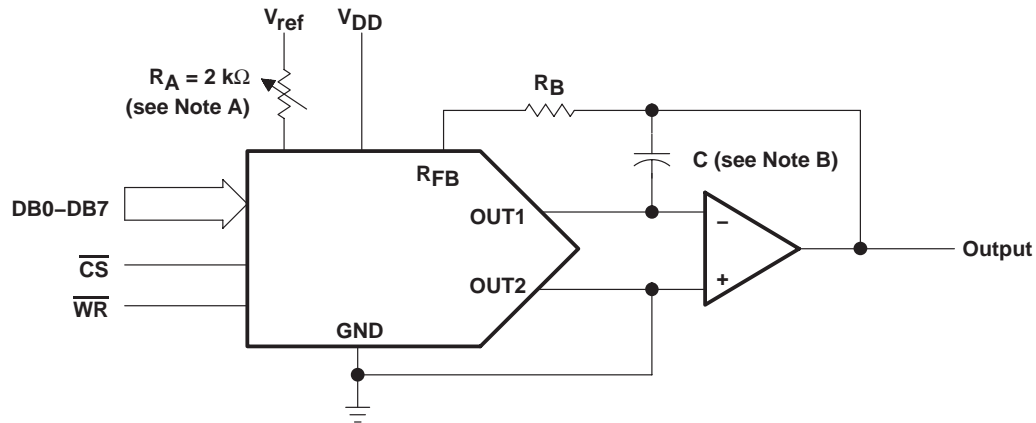
Figure 2. TLC7524 Equivalent Circuit With All Digital Inputs Low

TLC7524C, TLC7524E, TLC7524I

8-BIT MULTIPLYING DIGITAL-TO-ANALOG CONVERTERS

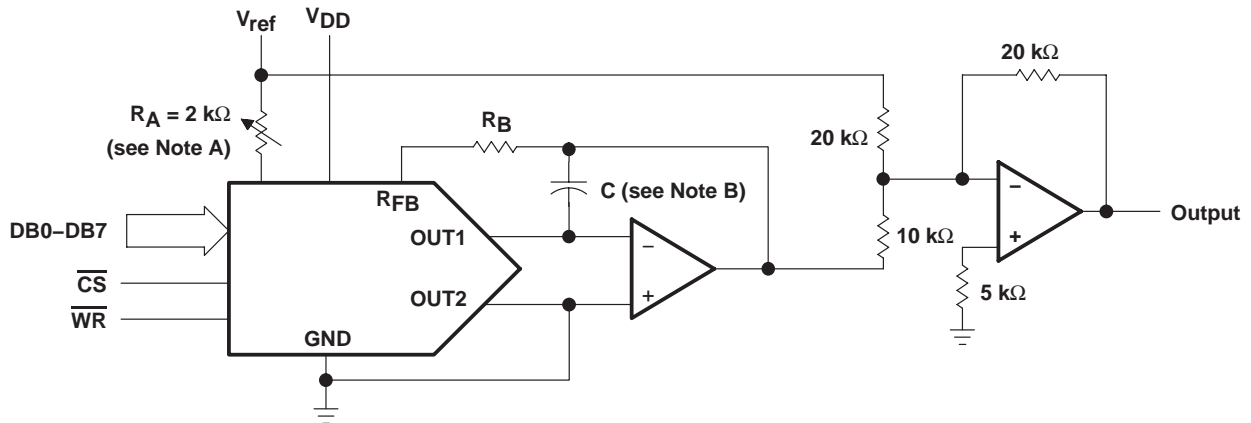
SLAS061D – SEPTEMBER 1986 – REVISED JUNE 2007

PRINCIPLES OF OPERATION



- NOTES: A. R_A and R_B used only if gain adjustment is required.
B. C phase compensation (10-15 pF) is required when using high-speed amplifiers to prevent ringing or oscillation.

Figure 3. Unipolar Operation (2-Quadrant Multiplication)



- NOTES: A. R_A and R_B used only if gain adjustment is required.
B. C phase compensation (10-15 pF) is required when using high-speed amplifiers to prevent ringing or oscillation.

Figure 4. Bipolar Operation (4-Quadrant Operation)

Table 1. Unipolar Binary Code		
DIGITAL INPUT (see Note 3)		ANALOG OUTPUT
MSB	LSB	
1	1	$-V_{ref} (255/256)$
1	0	$-V_{ref} (129/256)$
1	0	$-V_{ref} (128/256) = -V_{ref}/2$
0	1	$-V_{ref} (127/256)$
0	0	$-V_{ref} (1/256)$
0	0	0

NOTE 3: $LSB = 1/256 (V_{ref})$

Table 2. Bipolar (Offset Binary) Code		
DIGITAL INPUT (see Note 4)		ANALOG OUTPUT
MSB	LSB	
1	1	$V_{ref} (127/128)$
1	0	$V_{ref} (1/128)$
1	0	0
0	1	$-V_{ref} (1/128)$
0	0	$-V_{ref} (127/128)$
0	0	$-V_{ref}$

NOTE 4: $LSB = 1/128 (V_{ref})$

TLC7524C, TLC7524E, TLC7524I

8-BIT MULTIPLYING DIGITAL-TO-ANALOG CONVERTERS

SLAS061D – SEPTEMBER 1986 – REVISED JUNE 2007

PRINCIPLES OF OPERATION

microprocessor interfaces

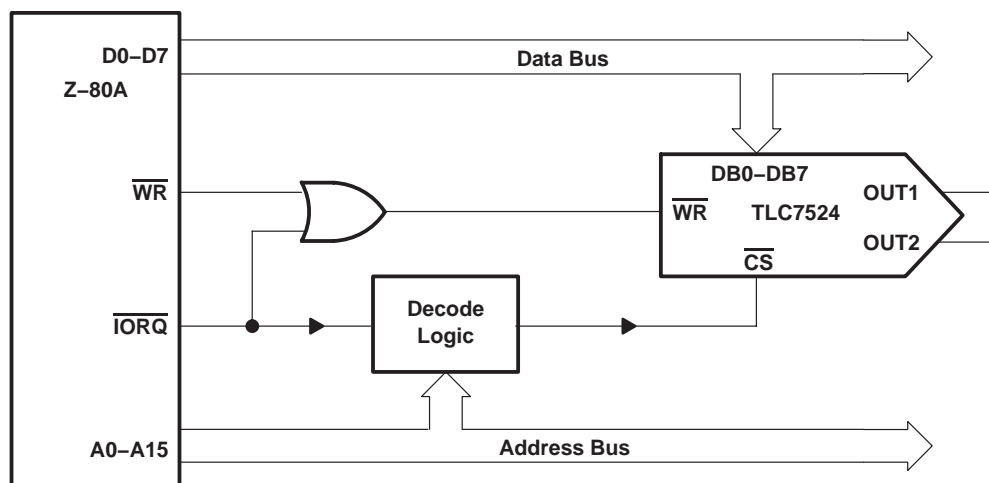


Figure 5. TLC7524: Z-80A Interface

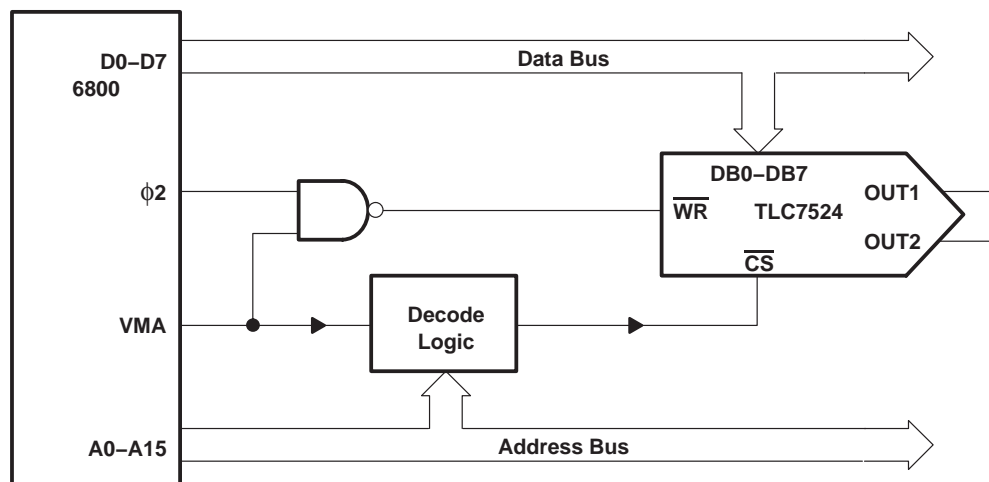


Figure 6. TLC7524: 6800 Interface

TLC7524C, TLC7524E, TLC7524I

8-BIT MULTIPLYING DIGITAL-TO-ANALOG CONVERTERS

SLAS061D – SEPTEMBER 1986 – REVISED JUNE 2007

PRINCIPLES OF OPERATION

microprocessor interfaces (continued)

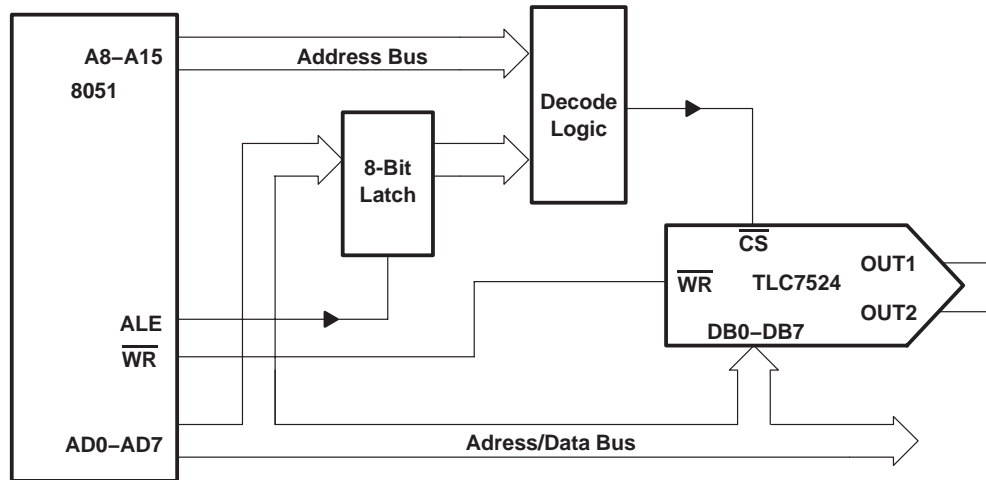


Figure 7. TLC7524: 8051 Interface

Revision History

DATE	REV	PAGE	SECTION	DESCRIPTION
6/07	D	Front Page	—	Deleted Available Options table.
		2	—	Inserted Package/Ordering information.

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLC7524CD	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TLC7524C	Samples
TLC7524CDG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TLC7524C	Samples
TLC7524CDR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TLC7524C	Samples
TLC7524CDRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TLC7524C	Samples
TLC7524CFN	ACTIVE	PLCC	FN	20	46	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 70	TLC7524C	Samples
TLC7524CFNR	ACTIVE	PLCC	FN	20	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 70	TLC7524C	Samples
TLC7524CN	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TLC7524CN	Samples
TLC7524CNE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TLC7524CN	Samples
TLC7524CNS	ACTIVE	SO	NS	16	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TLC7524	Samples
TLC7524CNSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TLC7524	Samples
TLC7524CPW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	P7524	Samples
TLC7524CPWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	P7524	Samples
TLC7524CPWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	P7524	Samples
TLC7524CPWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	P7524	Samples
TLC7524ED	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TLC7524E	Samples
TLC7524EDG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TLC7524E	Samples
TLC7524EDR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TLC7524E	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLC7524EDRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TLC7524E	Samples
TLC7524EN	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	TLC7524EN	Samples
TLC7524ENE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	TLC7524EN	Samples
TLC7524ID	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-25 to 85	TLC7524I	Samples
TLC7524IDG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-25 to 85	TLC7524I	Samples
TLC7524IDR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-25 to 85	TLC7524I	Samples
TLC7524IFN	ACTIVE	PLCC	FN	20	46	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-25 to 85	TLC7524I	Samples
TLC7524IFNG3	ACTIVE	PLCC	FN	20	46	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-25 to 85	TLC7524I	Samples
TLC7524IN	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-25 to 85	TLC7524IN	Samples
TLC7524INE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-25 to 85	TLC7524IN	Samples
TLC7524IPW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-25 to 85	Y7524	Samples
TLC7524IPWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-25 to 85	Y7524	Samples
TLC7524IPWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-25 to 85	Y7524	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC7524CDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
TLC7524CNSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
TLC7524CPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TLC7524EDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
TLC7524IDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
TLC7524IPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC7524CDR	SOIC	D	16	2500	367.0	367.0	38.0
TLC7524CNSR	SO	NS	16	2000	367.0	367.0	38.0
TLC7524CPWR	TSSOP	PW	16	2000	367.0	367.0	35.0
TLC7524EDR	SOIC	D	16	2500	367.0	367.0	38.0
TLC7524IDR	SOIC	D	16	2500	367.0	367.0	38.0
TLC7524IPWR	TSSOP	PW	16	2000	367.0	367.0	35.0

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- $\triangle C$ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- $\triangle D$ Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



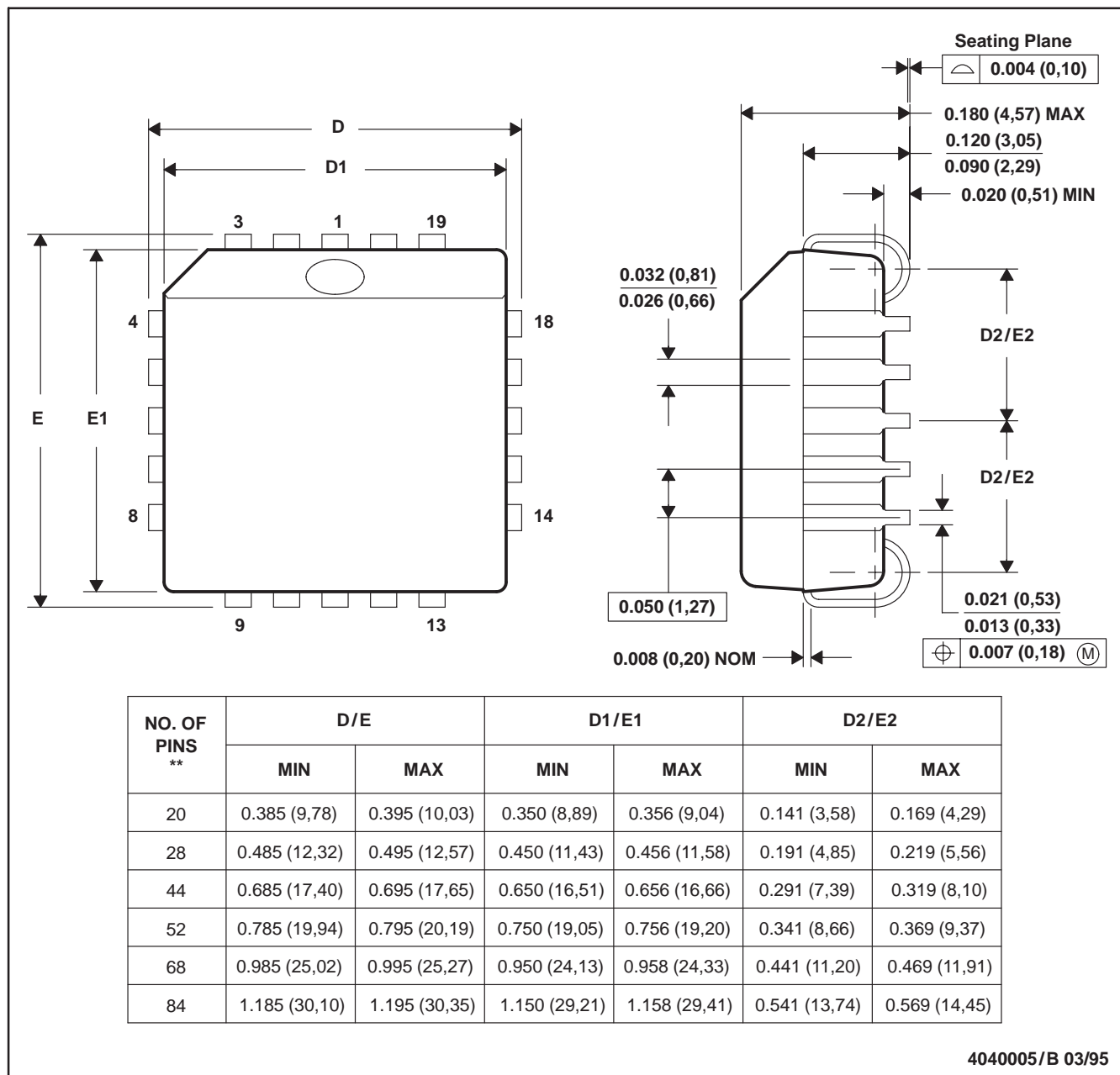
4211284-3/F 12/12

- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

FN (S-PQCC-J**)

PLASTIC J-LEADED CHIP CARRIER

20 PIN SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Falls within JEDEC MS-018

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products

Audio	www.ti.com/audio
Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DLP® Products	www.dlp.com
DSP	dsp.ti.com
Clocks and Timers	www.ti.com/clocks
Interface	interface.ti.com
Logic	logic.ti.com
Power Mgmt	power.ti.com
Microcontrollers	microcontroller.ti.com
RFID	www.ti-rfid.com
OMAP Applications Processors	www.ti.com/omap
Wireless Connectivity	www.ti.com/wirelessconnectivity

Applications

Automotive and Transportation	www.ti.com/automotive
Communications and Telecom	www.ti.com/communications
Computers and Peripherals	www.ti.com/computers
Consumer Electronics	www.ti.com/consumer-apps
Energy and Lighting	www.ti.com/energy
Industrial	www.ti.com/industrial
Medical	www.ti.com/medical
Security	www.ti.com/security
Space, Avionics and Defense	www.ti.com/space-avionics-defense
Video and Imaging	www.ti.com/video

TI E2E Community

e2e.ti.com