To our customers,

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Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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To all our customers

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Note : Mitsubishi Electric will continue the business operations of high frequency & optical devices and power devices.

Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

# M35017-XXXSP/FP

SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

## DESCRIPTION

The M35017-XXXSP/FP is a TV screen display control IC which can be used to display information such as program schedules, the data and messages on the TV screen.

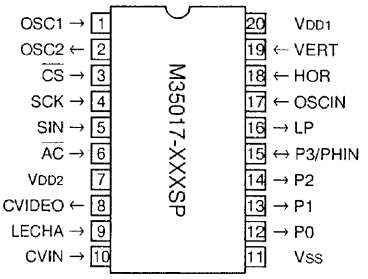
It uses a silicon gate CMOS process and M35017-XXXSP is housed in a 20-pin shrink DIP package, M35017-XXXFP is housed in a 20-pin shrink SOP package.

For M35017-001SP/FP that is a standard ROM version of M35017-XXXSP/FP respectively, the character pattern is also mentioned.

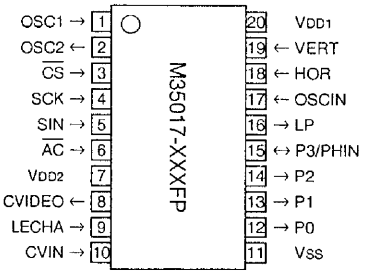
## FEATURES

- Screen composition ..... 24 columns × 10 lines
- Number of characters displayed ..... 240 (Max.)
- Character composition ..... 12 × 18 dot matrix
- Characters available ..... 128 characters
- Character sizes available ..... 4 (horizontal) × 4 (vertical)
- Display locations available
  - Horizontal direction ..... 62 locations
  - Vertical direction ..... 64 locations
- Blinking ..... Character units
  - Cycle : approximately 1 second, or approximately 0.5 seconds
  - Duty : 25%, 50%, or 75%
- Data input ..... By the serial input function
- Coloring
  - Background coloring (composite video signal)
- Blanking
  - Total blanking (14 × 18 dots)
  - Border size blanking
  - Character size blanking
- Synchronization signal
  - Composite synchronization signal generation (PAL, NTSC, M-PAL)
- Synchronized separation circuit ..... Built-in
- 4 output ports (2 digital lines)
- Oscillation stop function
  - Be possible to stop the oscillation for display
- Exclusion function ..... Built-in
- Built-in the oscillation for synchronized signal generation
- Reversed character display function
- Be possible to background coloring in superimpose (NTSC, PAL, M-PAL)
- Built-in polarity switching function at horizontal synchronized signal or vertical synchronized signal is input.

## PIN CONFIGURATION (TOP VIEW)




Outline 20P4B




Outline 20P2Q-A

## APPLICATION

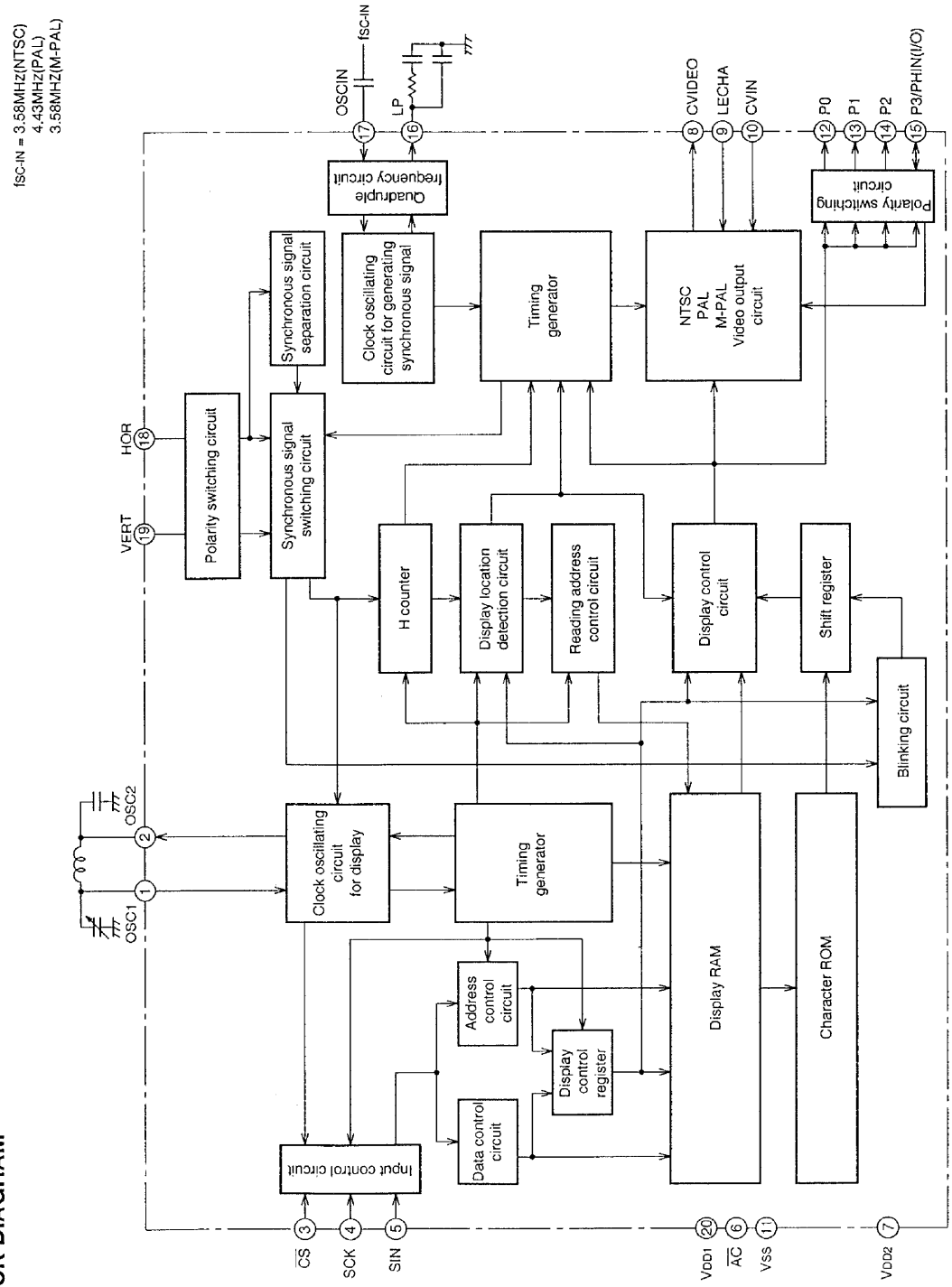
TV, VCR, Camcorder

## PIN DESCRIPTION

| Pin Number | Symbol | Pin name | Input/ Output | Function |
|---|---|---|---|---|
| 1 | OSC1 | Pins for attachment of external oscillator circuit | Input | There are the pins for attaching an external display oscillator circuit. The standard oscillation frequency is approximately 7 MHz. This oscillation frequency determines the horizontal position of the display on the TV screen and the width of the characters. |
| 2 | OSC2 | | Output | |
| 3 | $\overline{CS}$ | Chip select input | Input | This is the chip select pin, and when serial data transmission is being carried out, it goes to "L". Hysteresis input. Includes built-in pull-up resistor. |
| 4 | SCK | Serial clock input | Input | When $\overline{CS}$ pin is "L", SIN serial data is taken in when SCK rises. Hysteresis input. Built-in pull-up resistor is included. |
| 5 | SIN | Serial data input | Input | This is the pin for serial input of data and addresses for the display control register and the display data memory. Hysteresis input. Includes built-in pull-up resistor. |
| 6 | $\overline{AC}$ | Auto-clear input | Input | When "L", this pin resets the internal IC circuit. Hysteresis input. Includes built-in pull-up resistor. |
| 7 | $V_{DD2}$ | Power pin | – | Please connect to +5 V with the analog circuit power pin. |
| 8 | CVIDEO | Composite video signal output | Output | This is the output pin for composite video signals. It outputs 2Vp-p composite video signals. In superimpose mode, character output etc. is superimposed on the external composite video signals from CVIN. |
| 9 | LECHA | Character level input | Input | This is the input pin which determines the "white" character luminance level in the composite video signal. |
| 10 | CVIN | Composite video signal input | Input | This is the input pin for external composite video signals. In superimpose mode, character output etc. is superimposed on these external composite video signals. |
| 11 | $V_{SS}$ | Earthing pin | – | Please connect to GND using circuit earthing pin. |
| 12 | P0 | Port P0 output | Output | This pin can be toggled between port pin output and BLNK1 (character background) signal output. |
| 13 | P1 | Port P1 output | Output | This pin can be toggled between port pin output and CO1 (character) signal output. |
| 14 | P2 | Port P2 output | Output | This pin can be toggled between port pin output and BLNK2 (character background) signal output. |
| 15 | P3/PHIN | Port P3 output | I/O | This pin can be toggled between port pin output and CO2 (character) signal output. Superimposed colors on the PAL and M-PAL systems are controlled by the input terminal of the color burst select signal. |
| 16 | LP | Filter connection pin | Output | This pin connects filter circuit. |
| 17 | OSCIN | fsc input pin of oscillation circuit for generating the synchronization signal | Input | This is the subcarrier frequency (fsc) input pin for generating the synchronization signal (Note). This pin inputs the oscillation of 3.58 MHz at NTSC, 4.43 MHz at PAL and 3.58 MHz at M-PAL. |
| 18 | HOR | Horizontal synchronization signal input | Input | This pin inputs the horizontal synchronization signal. Hysteresis input. |
| 19 | VERT | Vertical synchronization signal input | Input | This pin inputs the vertical synchronization signal. Hysteresis input. |
| 20 | $V_{DD1}$ | Power pin | – | Please connect +5 V with the digital circuit power pin. |

Note : Refer to Note for other (Note for fsc signal input).

## BLOCK DIAGRAM



## MEMORY CONSTITUTION

Address 0016 to EF16 are assigned to the display RAM, address F016 to F816 are assigned to the display control registers.
The internal circuit is reset and all display control registers (address F016 to F816) are set to "0" and RAM is erased when the $\overline{AC}$ pin level is "L".

| Bit / Address | DA7 | DA6 | DA5 | DA4 | DA3 | DA2 | DA1 | DA0 | Remarks |
|---|---|---|---|---|---|---|---|---|---|
| 0016 | EXP | C6 | C5 | C4 | C3 | C2 | C1 | C0 | Display RAM |
| ⋮ | Expansion bit | Character code | | | | | | | |
| EF16 | EXP | C6 | C5 | C4 | C3 | C2 | C1 | C0 | |
| F016 | PTD 3 | PTD 2 | PTD 1 | PTD 0 | PTC 3 | PTC 2 | PTC 1 | PTC 0 | Port output specify |
| F116 | PLTV | PLTH | HP 5 | HP 4 | HP 3 | HP 2 | HP 1 | HP 0 | Horizontal display start position specify |
| F216 | $\overline{INT}$/NON | SEPV | VP 5 | VP 4 | VP 3 | VP 2 | VP 1 | VP 0 | Vertical display start position specify |
| F316 | VSZ 21 | VSZ 20 | VSZ 11 | VSZ 10 | HSZ 21 | HSZ 20 | HSZ 11 | HSZ 10 | Character size specify |
| F416 | DSP 7 | DSP 6 | DSP 5 | DSP 4 | DSP 3 | DSP 2 | DSP 1 | DSP 0 | Display mode specify |
| F516 | $\overline{N/P}$ | TEST 2 | TEST 1 | TEST 0 | EXP 1 | EXP 0 | DSP 9 | DSP 8 | Expansion |
| F616 | EQP | PAL H | MPAL | ALL 24 | SCOR | BLINK 2 | BLINK 1 | BLINK 0 | Blinking specify and so on |
| F716 | BLKHF | BB | BG | BR | LEVEL 0 | PHASE 2 | PHASE 1 | PHASE 0 | Raster color specify |
| F816 | DSP ON | CONT7F | STOP 1 | TEST A | RAM ERS | EX | BLK 1 | BLK 0 | Control display |

Fig. 1 Memory constitution

## SCREEN CONSTITUTION

The screen lines and rows are determined from each address of the display RAM. The screen constitution is shown in Figure 2.

| Line \ Row | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | 00₁₆ | 01₁₆ | 02₁₆ | 03₁₆ | 04₁₆ | 05₁₆ | 06₁₆ | 07₁₆ | 08₁₆ | 09₁₆ | 0A₁₆ | 0B₁₆ | 0C₁₆ | 0B₁₆ | 0E₁₆ | 0F₁₆ | 10₁₆ | 11₁₆ | 12₁₆ | 13₁₆ | 14₁₆ | 15₁₆ | 16₁₆ | 17₁₆ |
| 2 | 18₁₆ | 19₁₆ | 1A₁₆ | 1B₁₆ | 1C₁₆ | 1D₁₆ | 1E₁₆ | 1F₁₆ | 20₁₆ | 21₁₆ | 22₁₆ | 23₁₆ | 24₁₆ | 25₁₆ | 26₁₆ | 27₁₆ | 28₁₆ | 29₁₆ | 2A₁₆ | 2B₁₆ | 2C₁₆ | 2D₁₆ | 2E₁₆ | 2F₁₆ |
| 3 | 30₁₆ | 31₁₆ | 32₁₆ | 33₁₆ | 34₁₆ | 35₁₆ | 36₁₆ | 37₁₆ | 38₁₆ | 39₁₆ | 3A₁₆ | 3B₁₆ | 3C₁₆ | 3D₁₆ | 3E₁₆ | 3F₁₆ | 40₁₆ | 41₁₆ | 42₁₆ | 43₁₆ | 44₁₆ | 45₁₆ | 46₁₆ | 47₁₆ |
| 4 | 48₁₆ | 49₁₆ | 4A₁₆ | 4B₁₆ | 4C₁₆ | 4D₁₆ | 4E₁₆ | 4F₁₆ | 50₁₆ | 51₁₆ | 52₁₆ | 53₁₆ | 54₁₆ | 55₁₆ | 56₁₆ | 57₁₆ | 58₁₆ | 59₁₆ | 5A₁₆ | 5B₁₆ | 5C₁₆ | 5D₁₆ | 5E₁₆ | 5F₁₆ |
| 5 | 60₁₆ | 61₁₆ | 62₁₆ | 63₁₆ | 64₁₆ | 65₁₆ | 66₁₆ | 67₁₆ | 68₁₆ | 69₁₆ | 6A₁₆ | 6B₁₆ | 6C₁₆ | 6D₁₆ | 6E₁₆ | 6F₁₆ | 70₁₆ | 71₁₆ | 72₁₆ | 73₁₆ | 74₁₆ | 75₁₆ | 76₁₆ | 77₁₆ |
| 6 | 78₁₆ | 79₁₆ | 7A₁₆ | 7B₁₆ | 7C₁₆ | 7D₁₆ | 7E₁₆ | 7F₁₆ | 80₁₆ | 81₁₆ | 82₁₆ | 83₁₆ | 84₁₆ | 85₁₆ | 86₁₆ | 87₁₆ | 88₁₆ | 89₁₆ | 8A₁₆ | 8B₁₆ | 8C₁₆ | 8D₁₆ | 8E₁₆ | 8F₁₆ |
| 7 | 90₁₆ | 91₁₆ | 92₁₆ | 93₁₆ | 94₁₆ | 95₁₆ | 96₁₆ | 97₁₆ | 98₁₆ | 99₁₆ | 9A₁₆ | 9B₁₆ | 9C₁₆ | 9D₁₆ | 9E₁₆ | 9F₁₆ | A0₁₆ | A1₁₆ | A2₁₆ | A3₁₆ | A4₁₆ | A5₁₆ | A6₁₆ | A7₁₆ |
| 8 | A8₁₆ | A9₁₆ | AA₁₆ | AB₁₆ | AC₁₆ | AD₁₆ | AE₁₆ | AF₁₆ | B0₁₆ | B1₁₆ | B2₁₆ | B3₁₆ | B4₁₆ | B5₁₆ | B6₁₆ | B7₁₆ | B8₁₆ | B9₁₆ | BA₁₆ | BB₁₆ | BC₁₆ | BD₁₆ | BE₁₆ | BF₁₆ |
| 9 | C0₁₆ | C1₁₆ | C2₁₆ | C3₁₆ | C4₁₆ | C5₁₆ | C6₁₆ | C7₁₆ | C8₁₆ | C9₁₆ | CA₁₆ | CB₁₆ | CC₁₆ | CD₁₆ | CE₁₆ | CF₁₆ | D0₁₆ | D1₁₆ | D2₁₆ | D3₁₆ | D4₁₆ | D5₁₆ | D6₁₆ | D7₁₆ |
| 10 | D8₁₆ | D9₁₆ | DA₁₆ | DB₁₆ | DC₁₆ | DD₁₆ | DE₁₆ | DF₁₆ | E0₁₆ | E1₁₆ | E2₁₆ | E3₁₆ | E4₁₆ | E5₁₆ | E6₁₆ | E7₁₆ | E8₁₆ | E9₁₆ | EA₁₆ | EB₁₆ | EC₁₆ | ED₁₆ | EE₁₆ | EF₁₆ |

The hexadecimal numbers in the boxes show the display RAM address.

Fig. 2 Screen constitution

## REGISTERS DESCRIPTION

(1) Address F0₁₆

| DA | Register | Contents | | Remarks |
|---|---|---|---|---|
| | | Status | Function | |
| 0 | PTC0 | ⓪ | P0 output (port P0) | Port output control |
| | | 1 | BLNK1 output | |
| 1 | PTC1 | ⓪ | P1 output (port P1) | |
| | | 1 | CO1 output | |
| 2 | PTC2 | ⓪ | P2 output (port P2) | |
| | | 1 | BLNK2 output | |
| 3 | PTC3 | ⓪ | P3 output (port P3) | |
| | | 1 | CO2 output | |
| 4 | PTD0 | ⓪ | P0 output "L" | Port data control |
| | | 1 | P0 output "H" | |
| 5 | PTD1 | ⓪ | P1 output "L" | |
| | | 1 | P1 output "H" | |
| 6 | PTD2 | ⓪ | P2 output "L" | |
| | | 1 | P2 output "H" | |
| 7 | PTD3 | ⓪ | P3 output "L" | |
| | | 1 | P3 output "H" | |

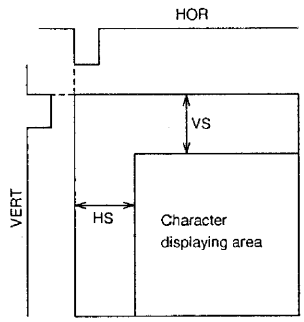
Note : The mark ⓪ around the status value means the reset status by the "L" level is input to $\overline{AC}$ pin.

(2) Address F1$_{16}$

<table>
<tr><th rowspan="2">DA</th><th rowspan="2">Register</th><th colspan="2">Contents</th><th rowspan="2">Remarks</th></tr>
<tr><th>Status</th><th>Function</th></tr>
<tr><td rowspan="2">0</td><td rowspan="2">HP0<br>(LSB)</td><td>◎</td><td rowspan="10">If HS is the horizontal display start location.<br><br>$HS = T \times (4 \sum_{n=0}^{5} 2^n HP_n + N)$.<br><br>T : The oscillation cycle of oscillator OSC1, OSC2<br><br><table><tr><th>HSZ11</th><th>HSZ10</th><th rowspan="2">N</th></tr><tr><th>HSZ21</th><th>HSZ20</th></tr><tr><td>0</td><td>0</td><td>9</td></tr><tr><td>0</td><td>1</td><td>10</td></tr><tr><td>1</td><td>0</td><td>11</td></tr><tr><td>1</td><td>1</td><td>12</td></tr></table></td><td rowspan="10">Horizontal display start location is specified using the 6 bits from HP5 to HP0.<br>Note : HP5 to 0 = (000000)$_2$ and (000001)$_2$ settings are forbidden.</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">1</td><td rowspan="2">HP1</td><td>◎</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">2</td><td rowspan="2">HP2</td><td>◎</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">3</td><td rowspan="2">HP3</td><td>◎</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">4</td><td rowspan="2">HP4</td><td>◎</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">5</td><td rowspan="2">HP5<br>(MSB)</td><td>◎</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">6</td><td rowspan="2">PLTH</td><td>◎</td><td>Input polarity of HOR pin is negative.</td><td rowspan="2">Set input polarity of HOR pin.</td></tr>
<tr><td>1</td><td>Input polarity of HOR pin is positive.</td></tr>
<tr><td rowspan="2">7</td><td rowspan="2">PLTV</td><td>◎</td><td>Input polarity of VERT pin is negative.</td><td rowspan="2">Set input polarity of VERT pin.</td></tr>
<tr><td>1</td><td>Input polarity of VERT pin is positive.</td></tr>
</table>

Note : The mark ◎ around the status value means the reset status by the "L" level is input to $\overline{AC}$ pin.

(3) Address F216

| DA | Register | Contents | | Remarks |
|---|---|---|---|---|
| | | Status | Function | |
| 0 | VP0 (LSB) | ⓪ | If VS is the vertical display start location.<br>$VS = H \times (4 \sum_{n=0}^{5} 2^n VP_n + 3)$.<br>H: Cycle with the horizontal synchronizing pulse<br>  <br> | The vertical start location is specified using the 6 bits from VP5 to VP0. |
| | | 1 | | |
| 1 | VP1 | ⓪ | | |
| | | 1 | | |
| 2 | VP2 | ⓪ | | |
| | | 1 | | |
| 3 | VP3 | ⓪ | | |
| | | 1 | | |
| 4 | VP4 | ⓪ | | |
| | | 1 | | |
| 5 | VP5 (MSB) | ⓪ | | |
| | | 1 | | |
| 6 | SEPV | ⓪ | Input both horizontal synchronization signal and vertical synchronization signal. | The contents of synchronization signal input in superimpose display is altered. |
| | | 1 | Input the horizontal (composite) synchronization signal only. | |
| 7 | $\overline{\text{INT}}$/NON | ⓪ | Interlace | Scanning lines control (only in internal synchronization) |
| | | 1 | Non-interlace | |

Note : The mark ○ around the status value means the reset status by the "L" level is input to $\overline{\text{AC}}$ pin.

(4) Address F316

<table>
<tr><th rowspan="2">DA</th><th rowspan="2">Register</th><th colspan="2">Contents</th><th rowspan="2">Remarks</th></tr>
<tr><th>Status</th><th>Function</th></tr>
<tr><td>0</td><td>HSZ10</td><td>Ⓞ<br>1</td><td rowspan="2"><table><tr><th>HSZ10 / HSZ11</th><th>0</th><th>1</th></tr><tr><td>0</td><td>1T/1dot</td><td>2T/1dot</td></tr><tr><td>1</td><td>3T/1dot</td><td>4T/1dot</td></tr></table></td><td rowspan="2">Character size setting in the horizontal direction for the first line.</td></tr>
<tr><td>1</td><td>HSZ11</td><td>Ⓞ<br>1</td></tr>
<tr><td>2</td><td>HSZ20</td><td>Ⓞ<br>1</td><td rowspan="2"><table><tr><th>HSZ20 / HSZ21</th><th>0</th><th>1</th></tr><tr><td>0</td><td>1T/1dot</td><td>2T/1dot</td></tr><tr><td>1</td><td>3T/1dot</td><td>4T/1dot</td></tr></table></td><td rowspan="2">Character size setting in the horizontal direction for the 2nd line to 10th line.</td></tr>
<tr><td>3</td><td>HSZ21</td><td>Ⓞ<br>1</td></tr>
<tr><td>4</td><td>VSZ10</td><td>Ⓞ<br>1</td><td rowspan="2"><table><tr><th>VSZ10 / VSZ11</th><th>0</th><th>1</th></tr><tr><td>0</td><td>1H/1dot</td><td>2H/1dot</td></tr><tr><td>1</td><td>3H/1dot</td><td>4H/1dot</td></tr></table></td><td rowspan="2">Character size setting in the vertical direction for the first line.</td></tr>
<tr><td>5</td><td>VSZ11</td><td>Ⓞ<br>1</td></tr>
<tr><td>6</td><td>VSZ20</td><td>Ⓞ<br>1</td><td rowspan="2"><table><tr><th>VSZ20 / VSZ21</th><th>0</th><th>1</th></tr><tr><td>0</td><td>1H/1dot</td><td>2H/1dot</td></tr><tr><td>1</td><td>3H/1dot</td><td>4H/1dot</td></tr></table></td><td rowspan="2">Character size setting in the vertical direction for the 2nd line to 10th line.</td></tr>
<tr><td>7</td><td>VSZ21</td><td>Ⓞ<br>1</td></tr>
</table>

Note : The mark Ⓞ around the status value means the reset status by the "L" level is input to $\overline{AC}$ pin.

(5) Address F416

| DA | Register | Contents | | Remarks |
|---|---|---|---|---|
| | | Status | Function | |
| 0 | DSP0 | ⓪ | Line 1 is in the display mode specified by BLK0 and BLK1. | DSP0 to DSP9 are each controlled independently. |
| | | 1 | Line 1 is in a different display mode. | |
| 1 | DSP1 | ⓪ | Line 2 is in the display mode specified by BLK0 and BLK1. | |
| | | 1 | Line 2 is in a different display mode. | |
| 2 | DSP2 | ⓪ | Line 3 is in the display mode specified by BLK0 and BLK1. | |
| | | 1 | Line 3 is in a different display mode. | |
| 3 | DSP3 | ⓪ | Line 4 is in the display mode specified by BLK0 and BLK1. | |
| | | 1 | Line 4 is in a different display mode. | |
| 4 | DSP4 | ⓪ | Line 5 is in the display mode specified by BLK0 and BLK1. | |
| | | 1 | Line 5 is in a different display mode. | |
| 5 | DSP5 | ⓪ | Line 6 is in the display mode specified by BLK0 and BLK1. | |
| | | 1 | Line 6 is in a different display mode. | |
| 6 | DSP6 | ⓪ | Line 7 is in the display mode specified by BLK0 and BLK1. | |
| | | 1 | Line 7 is in a different display mode. | |
| 7 | DSP7 | ⓪ | Line 8 is in the display mode specified by BLK0 and BLK1. | |
| | | 1 | Line 8 is in a different display mode. | |

| BLK1 | BLK0 | DSPn | Display mode for line n |
|---|---|---|---|
| 0 | 0 | 0 | Border (Note 1) |
| | | 1 | Character |
| 0 | 1 | 0 | Character |
| | | 1 | Border |
| 1 | 0 | 0 | Border |
| | | 1 | Matrix-outline |
| 1 | 1 | 0 | Matrix-outline |
| | | 1 | Character |

DSPn in the generic name for DSP0 to DSP9

Note 1: The display mode for line n is the border size, and for the other lines, the display mode is the character size.
If all DSPn (n : 0 to 9) are "0", the display mode is all line blanking OFF.
Note 2: DSP8 and DSP9 are assigned to address F516.

Note : The mark ○ around the status value means the reset status by the "L" level is input to $\overline{AC}$ pin.

(6) Address F5₁₆

<table>
<tr><th rowspan="2">DA</th><th rowspan="2">Register</th><th colspan="2">Contents</th><th rowspan="2">Remarks</th></tr>
<tr><th>Status</th><th>Function</th></tr>
<tr><td>0</td><td>DSP8</td><td>Ⓞ</td><td>Line 9 is in the display mode specified by BLK0 and BLK1.</td><td rowspan="4">See the remarks of DSP0 to DSP7 (address F4₁₆).</td></tr>
<tr><td></td><td>1</td><td>Line 9 is in the different display mode.</td></tr>
<tr><td>1</td><td>DSP9</td><td>Ⓞ</td><td>Line 10 is in the display mode specified by BLK0 and BLK1.</td></tr>
<tr><td></td><td>1</td><td>Line 10 is in the different display mode.</td></tr>
<tr><td>2</td><td>EXP0</td><td>Ⓞ</td><td rowspan="2"><table><tr><th>EXP1 \ EXP0</th><th>0</th><th>1</th></tr><tr><td>0</td><td>Normal character + Blinking</td><td>Reversed character (No blinking)</td></tr><tr><td>1</td><td>Normal character + Exclusion</td><td>Reversed character + Exclusion</td></tr></table></td><td rowspan="2">These registers are used to extend the function of the EXP bits in the addresses 0₁₆ to EF₁₆ of the display RAM.<br>Blinking function do not operate when register is a reversed character.</td></tr>
<tr><td></td><td>1</td></tr>
<tr><td>3</td><td>EXP1</td><td>Ⓞ</td></tr>
<tr><td></td><td>1</td></tr>
<tr><td>4</td><td>TEST0</td><td>Ⓞ</td><td rowspan="3">TEST0 to TEST2 = (000)₂ → Normal display<br>= (010)₂ → Space display</td><td rowspan="3"></td></tr>
<tr><td></td><td>1</td></tr>
<tr><td>5</td><td>TEST1</td><td>Ⓞ</td></tr>
<tr><td></td><td>1</td><td></td><td></td></tr>
<tr><td>6</td><td>TEST2</td><td>Ⓞ</td><td rowspan="2"></td><td rowspan="2"></td></tr>
<tr><td></td><td>1</td></tr>
<tr><td>7</td><td>$\overline{N}$/P</td><td>Ⓞ</td><td rowspan="2"><table><tr><th>$\overline{N}$/P \ M-PAL</th><th>0</th><th>1</th></tr><tr><td>0</td><td>NTSC</td><td>M-PAL</td></tr><tr><td>1</td><td>PAL</td><td>Do not use</td></tr></table></td><td rowspan="2">Synchronization signal is selected with this register and MPAL register (address F6₁₆).</td></tr>
<tr><td></td><td>1</td></tr>
</table>

Note : The mark Ⓞ around the status value means the reset status by the "L" level is input to $\overline{AC}$ pin.

(7) Address F616

<table>
<tr><th rowspan="2">DA</th><th rowspan="2">Register</th><th colspan="2">Contents</th><th rowspan="2">Remarks</th></tr>
<tr><th>Status</th><th>Function</th></tr>
<tr><td rowspan="2">0</td><td rowspan="2">BLINK0</td><td>0</td><td rowspan="3"><table><tr><th>BLINK1 \ BLINK0</th><th>0</th><th>1</th></tr><tr><td>0</td><td>Blinking OFF</td><td>Duty 25%</td></tr><tr><td>1</td><td>Duty 50%</td><td>Duty 75%</td></tr></table></td><td rowspan="3">Blinking duty ratio can be altered.</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">1</td><td rowspan="2">BLINK1</td><td>0</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">2</td><td rowspan="2">BLINK2</td><td>0</td><td>Division of vertical synchronization signal into 1/64.<br>Cycle approximately 1 second.</td><td rowspan="2">Blinking cycle can be altered.</td></tr>
<tr><td>1</td><td>Division of vertical synchronization signal into 1/32.<br>Cycle approximately 0.5 second.</td></tr>
<tr><td rowspan="2">3</td><td rowspan="2">SCOR</td><td>0</td><td>No coloring in superimpose (Black/white)</td><td rowspan="2">Control the coloring at superimpose. Available at only register EX=0 (external synchronization). (Notes 1,2)</td></tr>
<tr><td>1</td><td>Coloring in superimpose</td></tr>
<tr><td rowspan="2">4</td><td rowspan="2">ALL24</td><td>0</td><td>Blanking with all 24 characters in matrix-outline size.</td><td rowspan="2">Horizontal display range can be altered when all characters are in matrix-outline size (Note 3).</td></tr>
<tr><td>1</td><td>Horizontal display period blanked.</td></tr>
<tr><td rowspan="2">5</td><td rowspan="2">MPAL</td><td>0</td><td rowspan="3"><table><tr><th>$\overline{N/P}$ \ MPAL</th><th>0</th><th>1</th></tr><tr><td>0</td><td>NTSC</td><td>M-PAL</td></tr><tr><td>1</td><td>PAL</td><td>Do not use</td></tr></table></td><td rowspan="3">Synchronization signal is selected with this register and $\overline{N/P}$ register (address F516).</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">6</td><td rowspan="2">PALH</td><td>0</td></tr>
<tr><td>1</td><td>Interlace 2<br>Noninterlace 2</td><td>In NTSC mode, status is "0".</td></tr>
<tr><td rowspan="2">7</td><td rowspan="2">EQP</td><td>0</td><td>Not include the equivalent pulse</td><td rowspan="2">Setting the contents of composite synchronized signal at non-interlace.</td></tr>
<tr><td>1</td><td>Include the equivalent pulse</td></tr>
</table>

Notes 1 : When this register is set to "1", input an $f_{SC\text{-}IN}$ signal which has been synchronized with the color burst of the composite video signal (CVIN pin input) into the OSCIN terminal.

2 : Fix to "0" this register when internal synchronous mode.

3 : Fix to "0" this register when external synchronous mode.

(8) Address F7₁₆

<table>
<tr><th rowspan="2">DA</th><th rowspan="2">Register</th><th colspan="2">Contents</th><th rowspan="2">Remarks</th></tr>
<tr><th>Status</th><th>Function</th></tr>
<tr><td rowspan="2">0</td><td rowspan="2">PHASE0</td><td>Ⓞ</td><td rowspan="8">
<table>
<tr><th>PHASE2</th><th>PHASE1</th><th>PHASE0</th><th>NTSC Phase angle(color)</th><th>PAL Phase angle(color)</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>(Black)</td><td>(Black)</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>π /2 [rad.]</td><td>±π /2 [rad.]</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>7π /4 [rad.]</td><td>∓π /4 [rad.]</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>same phase</td><td>same phase</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>π [rad.]</td><td>±π [rad.]</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>3π /4 [rad.]</td><td>±3π /4 [rad.]</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>3π /2 [rad.]</td><td>∓π /2 [rad.]</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>(White)</td><td>(White)</td></tr>
</table>
</td><td rowspan="8">Raster color setting. Coloring by composite video signals means that the phase angle of the background color signals for the color burst signals can be varied. The angle can be varied in units of π /4 rad.<br>This differs from coloring by RGB output.</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">1</td><td rowspan="2">PHASE1</td><td>Ⓞ</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">2</td><td rowspan="2">PHASE2</td><td>Ⓞ</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">3</td><td rowspan="2">LEVEL0</td><td>Ⓞ</td><td>Internal bias OFF</td><td rowspan="2">Generation of composite video signal bias potential.</td></tr>
<tr><td>1</td><td>Internal bias ON</td></tr>
<tr><td rowspan="2">4</td><td rowspan="2">BR</td><td>Ⓞ</td><td rowspan="8">
<table>
<tr><th>BB</th><th>BG</th><th>BR</th><th>NTSC Phase angle(color)</th><th>PAL Phase angle(color)</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>(Black)</td><td>(Black)</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>π /2 [rad.]</td><td>±π /2 [rad.]</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>7π /4 [rad.]</td><td>∓7π /4 [rad.]</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>same phase</td><td>same phase</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>π [rad.]</td><td>±π [rad.]</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>3π /4 [rad.]</td><td>±3π /4 [rad.]</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>3π /2 [rad.]</td><td>∓3π /2 [rad.]</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>(White)</td><td>(White)</td></tr>
</table>
</td><td rowspan="8">Character background color setting.</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">5</td><td rowspan="2">BG</td><td>Ⓞ</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">6</td><td rowspan="2">BB</td><td>Ⓞ</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">7</td><td rowspan="2">BLKHF</td><td>Ⓞ</td><td>The halftone displaying "OFF" in superimpose</td><td rowspan="2">This register is available in the superimpose displaying only (Note 2).</td></tr>
<tr><td>1</td><td>The halftone displaying "ON" in superimpose</td></tr>
</table>

Notes 1 : The mark Ⓞ around the status value means the reset status by the "L" level is input to $\overline{AC}$ pin.

2 : Connecting 100Ω to 200Ω external register in series to external composite video signal input from CVIN terminal are needed.

(9) Address F816

| DA | Register | Contents | | Remarks |
|---|---|---|---|---|
| | | Status | Function | |
| 0 | BLK0 | ⓪ | <table><tr><td>BLK1 \ BLK0</td><td>0</td><td>1</td></tr><tr><td>0</td><td>Blanking OFF</td><td>Character size</td></tr><tr><td>1</td><td>Border size</td><td>Matrix-outline size</td></tr></table> | Display mode variable. |
| | | 1 | | |
| 1 | BLK1 | ⓪ | | |
| | | 1 | | |
| 2 | EX | ⓪ | External synchronization | Synchronization signal switching. (Note 2) |
| | | 1 | Internal synchronization | |
| 3 | RAMERS | ⓪ | RAM not erased | This register does not have the function as register. If RAM is erase continuously, set DSPON (address F816) to "0". |
| | | 1 | RAM erased | |
| 4 | TESTA | ⓪ | Normaly "0" setting | |
| | | 1 | Do not set | |
| 5 | STOP1 | ⓪ | Oscillation of OSC1, OSC2 for display. | OSC1 and OSC2 oscillation switching. To stop the oscillation, set $\overline{CS}$ pin to "H" level and DSPON (address F816) to "0". |
| | | 1 | Stop the oscillation OSC1, OSC2 for display. | |
| 6 | CONT7F | ⓪ | Normal write mode. | Usually "0" fix. Writing mode of the serial data input switching. |
| | | 1 | Continuously writing mode (character code 7F16) | |
| 7 | DSPON | ⓪ | Display OFF | Display can be altered. |
| | | 1 | Display ON | |

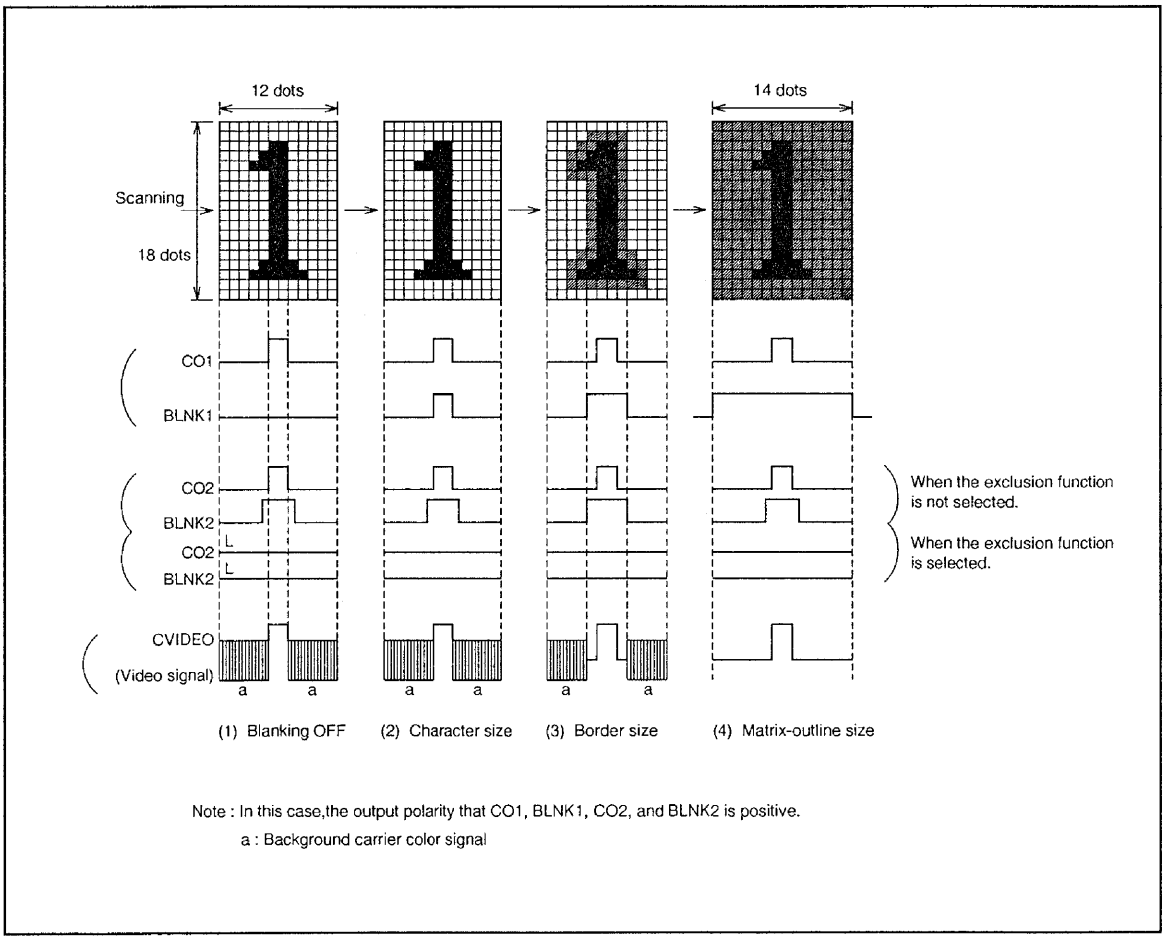
Notes 1 : The mark ⓪ around the status value means the reset status by the "L" level is input to $\overline{AC}$ pin.
2 : Cut off video signal input from the exterior at the outside of IC when internal synchronous mode. Leakage of input video signal from the exterior is able to be evaded.

## DISPLAY FORMS

M35017-XXXSP/FP has the following four display forms as the blanking function, when CO1, BLNK1, CO2, and BLNK2 are output.

(1) Blanking OFF : Blanking output signal (BLNK) is cut off.
(2) Character size : Blanking same as the character size.
(3) Border size : Blanking the background as a size from character.
(4) Matrix-outline size : Blanking the background as a size from all character font size (14 × 18 dots).

This display format allows each line (from the first line to the tenth line) to be controlled independently, so that two kinds of display formats can be combined on the same screen.




Note : In this case,the output polarity that CO1, BLNK1, CO2, and BLNK2 is positive.
a : Background carrier color signal

Fig. 3 Display forms at each display mode

## EXCLUSION FUNCTION

For M35017-XXXSP/FP, the function expansion that is set with the EXP1 and EXP0 registers (DA3 and DA2 of address F5$_{16}$) is performed when "1" is set to DA7 of display RAM (EXP bit).

Table1 Display form of M35017-XXXSP/FP

| Register | | Display form |
|---|---|---|
| EXP1 | EXP0 | |
| 0 | 0 | Normal character+Blinking |
| 0 | 1 | Reversed character (no blinking) |
| 1 | 0 | Normal character+Exclusion |
| 1 | 1 | Reversed character+Exclusion |

The figure 4 and 5 show the display examples using ports P0 to P3 (digital output).

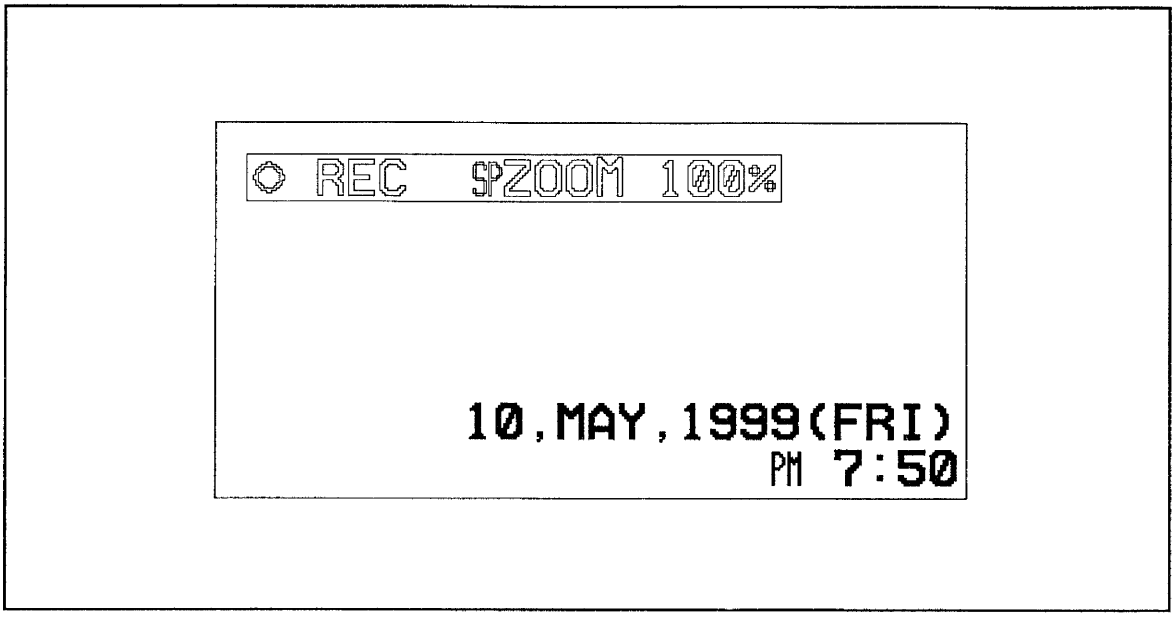



Fig. 4 Display example using ports P0(BLNK1) and P1(CO1)(display line)

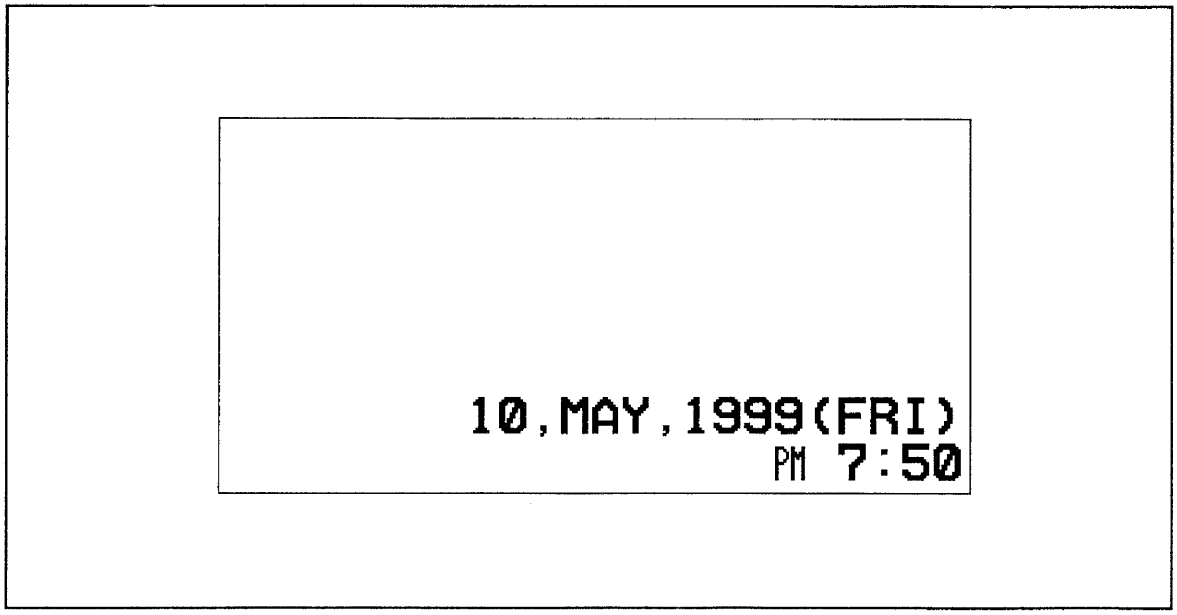



Fig. 5 Display example using ports P2(BLNK2) and P3(CO2)(record line)

## DATA INPUT EXAMPLE

Data of display RAM and display control registers can be set by the serial input function. Example of data setting at M35017-XXXSP/FP is shown in Figure 6.

| No. | Memory Contents | | DA 7 | DA 6 | DA 5 | DA 4 | DA 3 | DA 2 | DA 1 | DA 0 |
|---|---|---|---|---|---|---|---|---|---|---|
| | Address/Data | Addition | | | | | | | | |
| 1 | Address F8$_{16}$ | Display OFF | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 |
| 2 | Data(F8$_{16}$) | | 0 | 0 | 0 | 0 | 1 | X | X | X |
| 3 | Data(00$_{16}$) | Setting to display RAM (address 00$_{16}$ to EF$_{16}$) and registers (addresses F0$_{16}$ to F8$_{16}$) | BLINK | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| 4 | Data(01$_{16}$) | | BLINK | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| | ⋮ | | | | | | ⋮ | | | |
| 242 | Data(EF$_{16}$) | | BLINK | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| 243 | Data(F0$_{16}$) | | PTD 3 | PTD 2 | PTD 1 | PTD 0 | PTC 3 | PTC 2 | PTC 1 | PTC 0 |
| 244 | Data(F1$_{16}$) | | PLTV | PLTH | HP 5 | HP 4 | HP 3 | HP 2 | HP 1 | HP 0 |
| 245 | Data(F2$_{16}$) | | 0 | 0 | VP 5 | VP 4 | VP 3 | VP 2 | VP 1 | VP 0 |
| 246 | Data(F3$_{16}$) | | VSZ 21 | VSZ 20 | VSZ 11 | VSZ 10 | HSZ 21 | HSZ 20 | HSZ 11 | HSZ 10 |
| 247 | Data(F4$_{16}$) | | DSP 7 | DSP 6 | DSP 5 | DSP 4 | DSP 3 | DSP 2 | DSP 1 | DSP 0 |
| 248 | Data(F5$_{16}$) | | $\overline{N}$/P | 0 | 0 | 0 | EXP 1 | EXP 0 | DSP 9 | DSP 8 |
| 249 | Data(F6$_{16}$) | | EQP | PAL. H | MPAL | ALL 24 | 0 | BLINK 2 | BLINK 1 | BLINK 0 |
| 250 | Data(F7$_{16}$) | | BLKHF | BB | BG | BR | 1 | PHASE 2 | PHASE 1 | PHASE 0 |
| 251 | Data(F8$_{16}$) | Display ON | 1 | 0 | 0 | 0 | 0 | EX | BLK 1 | BLK 0 |

Fig. 6 Example of data setting by the serial input function

## SERIAL DATA INPUT TIMING

(1) Serial data should be input with the LSB first.
(2) The address consists of 8 bits.
(3) The data consists of 8 bits.
(4) The 8 bits in the SCK after the $\overline{CS}$ signal has fallen are the address, and for succeeding input data, the address is incremented every 8 bits.

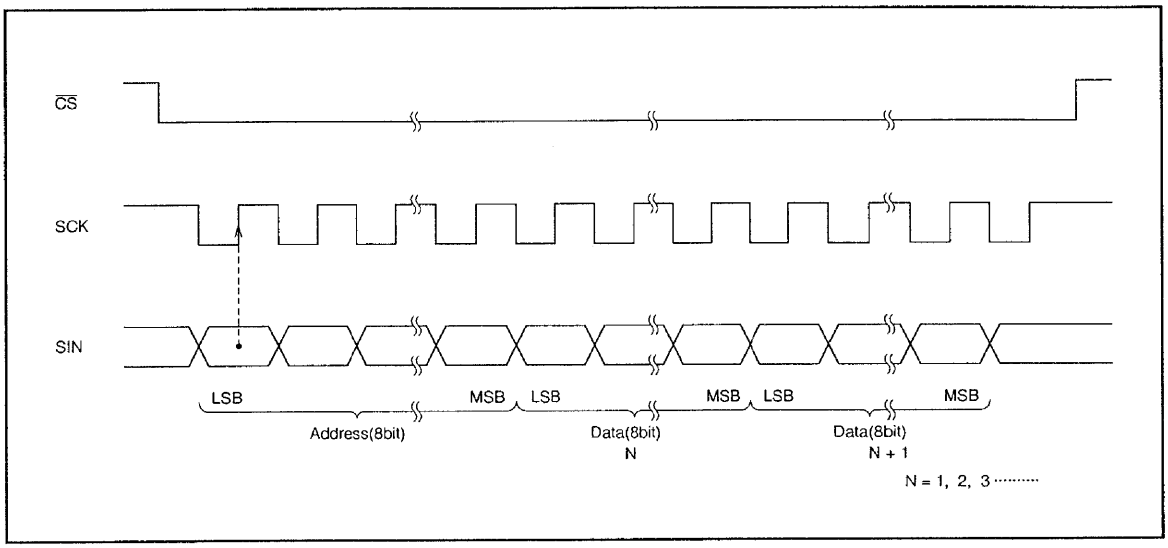



Fig. 7 Serial input timing

## CONT7F FUNCTION

When the register CONT7F (DA6 of address F8$_{16}$) is set to "1" and data input as the timing shown in Figure 8, the character code 7F$_{16}$ (blank) can be set to display RAM automatically. However, be necessary to set the hold time.

While this function is operating, never stop the display oscillation OSC1 and OSC2, and set the register STOP1 (DA5 of address F8$_{16}$) to "0".

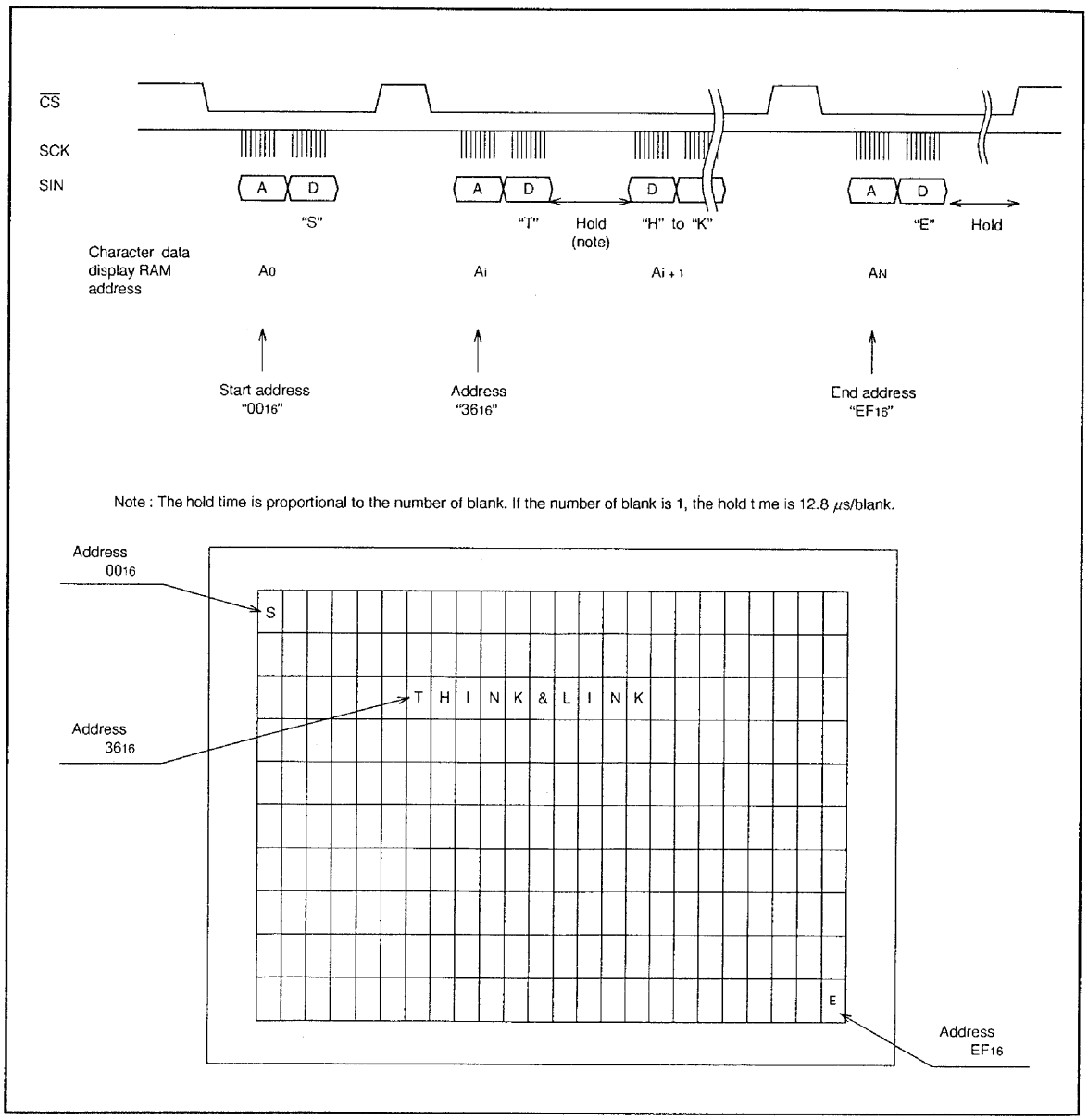



Fig. 8 CONT7F functional timing

## CHARACTER FONT

Images are composed on a 12 × 18 dot matrix, and characters can be linked vertically and horizontally with other characters to allow the display the continuous symbols.

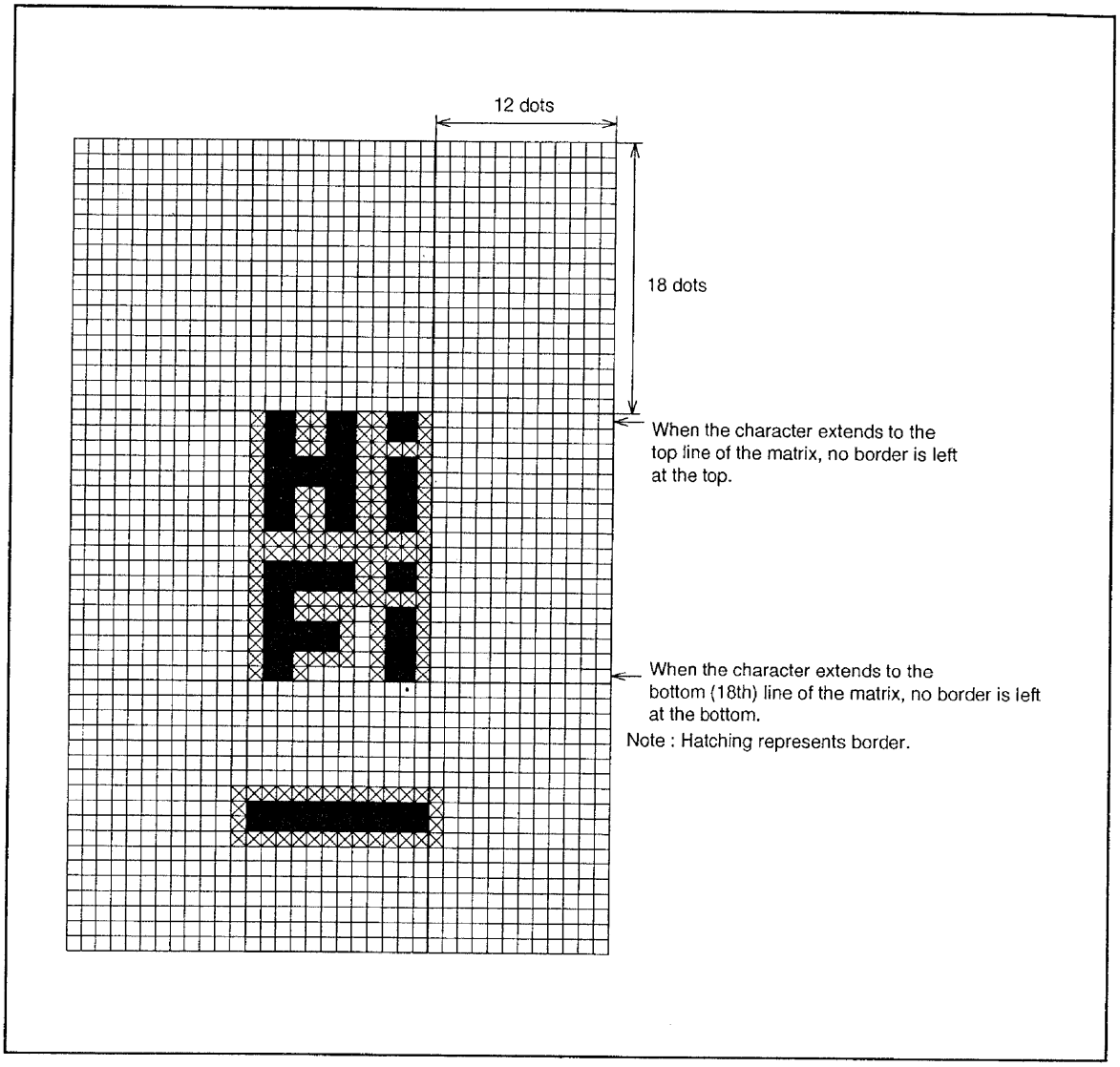



Fig. 9 Character font and border

Character code $7F_{16}$ is fixed as blank, without a background.

## TIMING REQUIREMENTS (Ta= −10 °C to + 70 °C, VDD=5 ± 0.25 V, unless otherwise noted)

### Serial data input

| Symbol | Parameter | Limits | | | Unit | Remarks |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| tw(SCK) | SCK width | 200 | – | – | ns | See Figure 10 |
| tsu($\overline{CS}$) | $\overline{CS}$ setup time | 200 | – | – | ns | |
| th($\overline{CS}$) | $\overline{CS}$ hold time | 2 | – | – | μs | |
| tsu(SIN) | SIN setup time | 200 | – | – | ns | |
| th(SIN) | SIN hold time | 200 | – | – | ns | |
| tword | 1 word writing time | 5 | – | – | μs | |

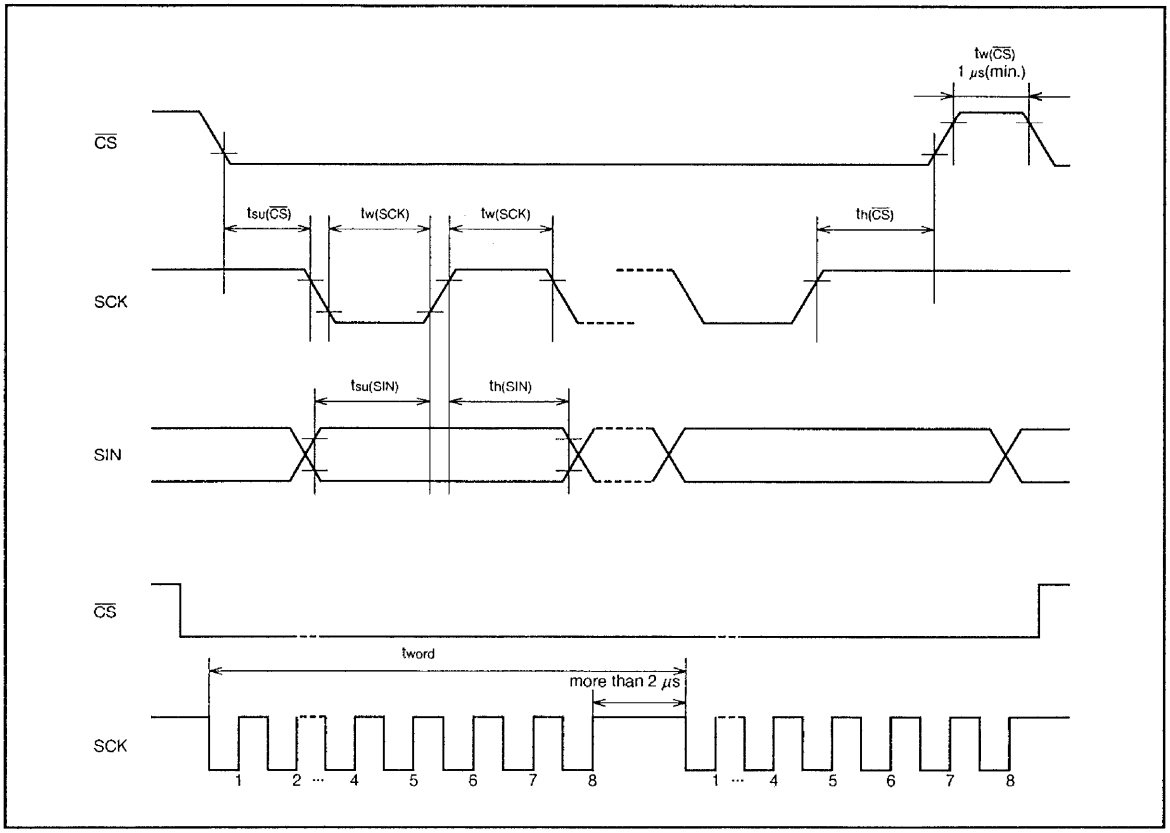



Fig. 10 Serial input timing requirements

## ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Conditions | Ratings | Unit |
|---|---|---|---|---|
| $V_{DD}$ | Supply voltage | With respect to Vss. | −0.3 to 6.0 | V |
| $V_I$ | Input voltage | | $V_{SS}-0.3 \leqq V_I \leqq V_{DD}+0.3$ | V |
| $V_O$ | Output voltage | | $V_{SS} \leqq V_O \leqq V_{DD}$ | V |
| $P_d$ | Power dissipation | Ta =25 °C | 300 | mW |
| $T_{opr}$ | Operating temperature | | −10 to 70 | °C |
| $T_{stg}$ | Storage temperature | | −40 to 125 | °C |

## RECOMMENDED OPERATING CONDITIONS ($V_{DD}$ = 5V, Ta = −10 to 70 °C, unless otherwise noted)

| Symbol | Parameter | Limits | | | Unit | Remarks |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| $V_{DD}$ | Supply voltage | 4.75 | 5.0 | 5.25 | V | |
| $V_{IH}$ | "H" level input voltage SIN, SCK, $\overline{CS}$, $\overline{AC}$, HOR, VERT | 0.8$V_{DD}$ | $V_{DD}$ | $V_{DD}$ | V | |
| $V_{IL}$ | "L" level input voltage SIN, SCK, $\overline{CS}$, $\overline{AC}$, HOR, VERT | 0 | 0 | 0.2 X $V_{DD}$ | V | |
| VCVIN | Composite-video signal input voltage CVIN | – | 2$V_{P-P}$ | — | V | |
| $f_{OSC1}$ | Oscillating frequency for display | 6.3 | 7.0 | 7.7 | MHz | |
| $f_{OSCIN}$ | Oscillating frequency for synchronized signal | — | 3.58<br>4.43<br>3.58 | — | MHz | — |
| $V_{OSCIN}$ | Input voltage OSCIN (DUTY 40 to 60 %) | 0.3 | — | 4.0 | $V_{P-P}$ | (Note) |

Note: Noise ingredient of $V_{OSCIN}$ is less than 30mV.

## ELECTRICAL CHARACTERISTICS ($V_{DD}$ = 5 V, $f_{OSC1}$ = 7.0 MHz, Ta = 25 °C, unless otherwise noted)

| Symbol | Parameter | Test conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| $V_{DD}$ | Supply voltage | Ta = −10 to 70 °C | 4.75 | 5.0 | 5.25 | V |
| $I_{DD}$ | Supply current | | – | 10 | 20 | mA |
| $V_{OH}$ | "H" level output voltage, P0 to P3 | $V_{DD}$ = 4.75 V, $I_{OH}$ = 0.4 mA | 3.75 | – | – | V |
| $V_{OL}$ | "L" level output voltage, P0 to P3 | $V_{DD}$ = 4.75 V, $I_{OL}$ = 0.4 mA | – | – | 0.4 | V |
| $R_I$ | Pull-up resistance SCK, $\overline{AC}$, $\overline{CS}$, SIN. | | 10 | 30 | 100 | kΩ |
| $Z_{OSCIN}$ | Input impedance of OSCIN pin | $V_{OSCIN}$ = 0.3 to 4.0 $V_{P-P}$ | 100 | 500 | – | kΩ |

## VIDEO SIGNAL INPUT CONDITIONS ($V_{DD}$ = 5 V, Ta = −10 to 70 °C, unless otherwise noted)

| Symbol | Parameter | Test conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| $V_{IN-SC}$ | Composite-video signal input clamp voltage | Sync-chip voltage | – | 1.5 | – | V |

## Note for Supplying Power

(1) Timing of power supplying to $\overline{AC}$ pin

The internal circuit of M35017-XXXSP/FP is reset when the level of the auto clear input pin $\overline{AC}$ is "L".

This pin is hysteresis input with the pull-up resistor. The timing about power supplying of $\overline{AC}$ pin is shown in Figure 11.

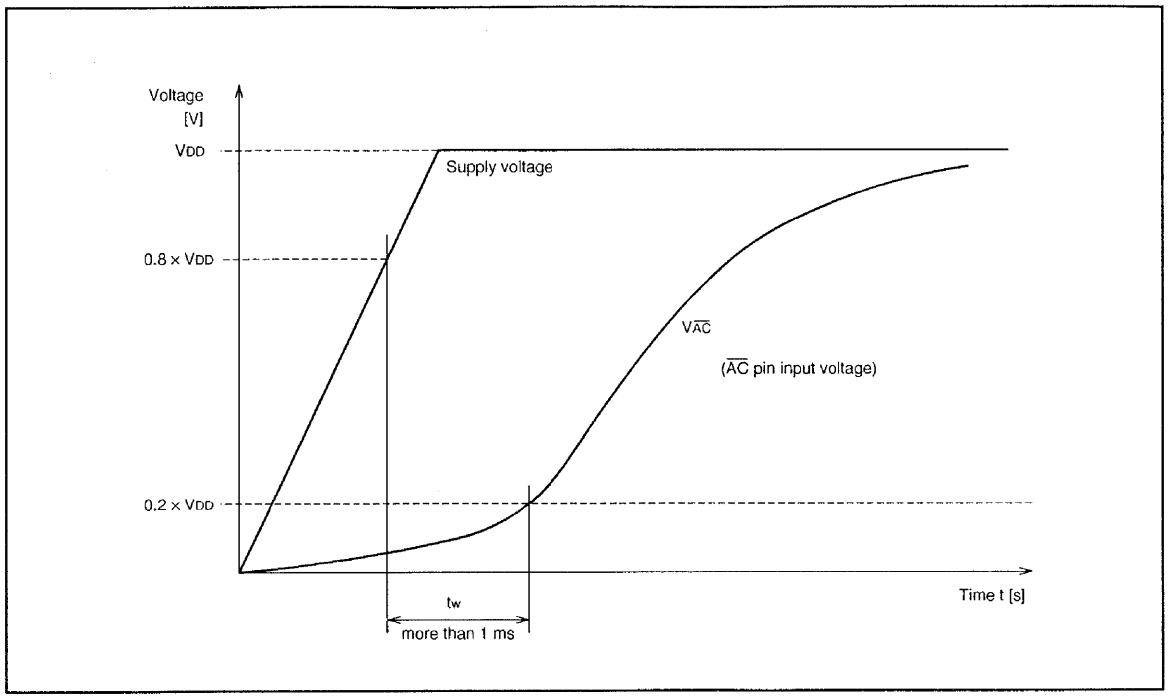



Fig.11 Timing of power supplying to $\overline{AC}$ pin

After supplying the power ($V_{DD}$ and $V_{SS}$) to M35017-XXXSP/FP and the supply voltage becomes more than 0.8 × $V_{DD}$, it needs to keep $V_{IL}$ time; tw of the $\overline{AC}$ pin for more than 1ms.

(2) Power supply timing about $V_{DD1}$ pin and $V_{DD2}$ pin.

The power need to supply to $V_{DD1}$ and $V_{DD2}$ at a time, though it is separated perfectly between the $V_{DD1}$ as the digital line and the $V_{DD2}$ as the analog line.

## PRECAUTION FOR USE

Notes on noise and latch-up

In order to avoid noise and latch-up, connect a bypass capacitor (≈0.1$\mu$ F) directly between the $V_{DD}$ pin and $V_{SS}$ pin using a heavy wire.

## DATA REQUIRED FOR MASK ROM ORDERING

Please send the following data for mask orders.

(1) M35017-XXXSP/FP mask ROM order confirmation form
(2) 20P4B, 20P2Q-A mask specification form
(3) ROM data (EPROM 3 sets)
(4) Floppy disks containing the character font generating program + character data

## Note for other

1. Note for when superimpose coloring mode

(1) Setting of register

Setting when superimpose coloring mode

Table 2. Setting when superimpose coloring mode

| Register / Broadcast system | PAL/$\overline{\text{NTSC}}$ | MPAL | EX | SCOR | State of P3/PHIN pin |
|---|---|---|---|---|---|
| NTSC | 0 | 0 | 0 | 1 | Output mode (Port output) |
| PAL | 1 | 0 | 0 | 1 | Refer to input mode (2) |
| M-PAL | 0 | 1 | 0 | 1 | Refer to input mode (2) |

(2) Signal input to P3/PHIN pin

P3/PHIN pin is input pin when PAL, M-PAL mode by register setting written in Table 2.

Then, other registers are output mode (port output).

With PAL and M-PAL systems, it is necessary to input a control signal for alternating color burst phase (CB1, CB2) every other scanning line.

Signal input timing to P3/PHIN pin is shown in Fig 13.

Input to P3/PHIN pin is able to be polarity select by register PTD3.

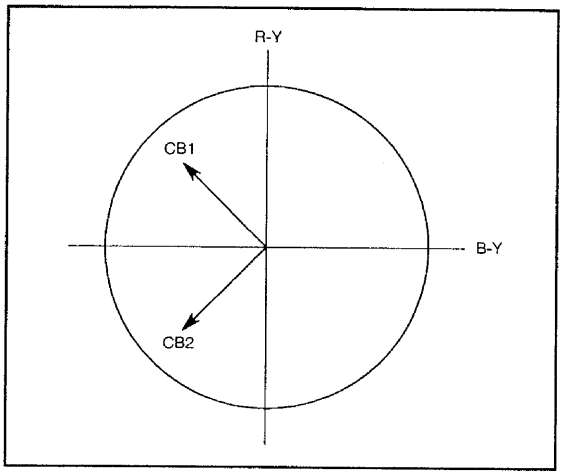
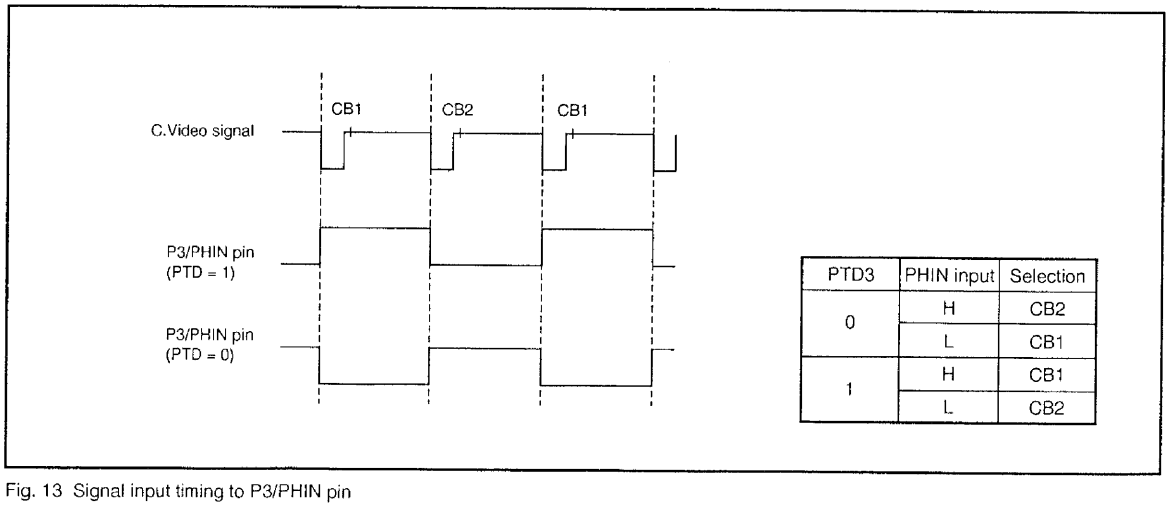



Fig. 12 Vector phase when PAL, M-PAL mode




| PTD3 | PHIN input | Selection |
|---|---|---|
| 0 | H | CB2 |
| | L | CB1 |
| 1 | H | CB1 |
| | L | CB2 |

Fig. 13 Signal input timing to P3/PHIN pin

2. Note for when fSC-IN signal input

(1)This IC amplifies the fSC signal (3.58 MHz for NTSC and M-PAL, 4.43 MHz for PAL) input into the OSCIN terminal. Internally, it generates the composite video signal.

The amplified fSC signal can be destabilized in the following cases.

(a)When the fSC signal is outside of recommended operating conditions

(b)When the waveform of the fSC signal is distorted

(c)When DC level in the fSC waveform fluctuates

When the amplified signal is unstable, the composite video signal generated inside the IC is also unstable in terms of synchronization with the subcarrier and phase.

Consequently, this results in color flicker and lost synchronization when the composite video signal is generated. Make note of the fact that this may prevent a stable blue background from being formed.

(2)When switching to internal synchronization from external synchronization (fSC signal is OFF), start fSC signal input 20 msec or more before the internal oscillator circuit stabilizes.

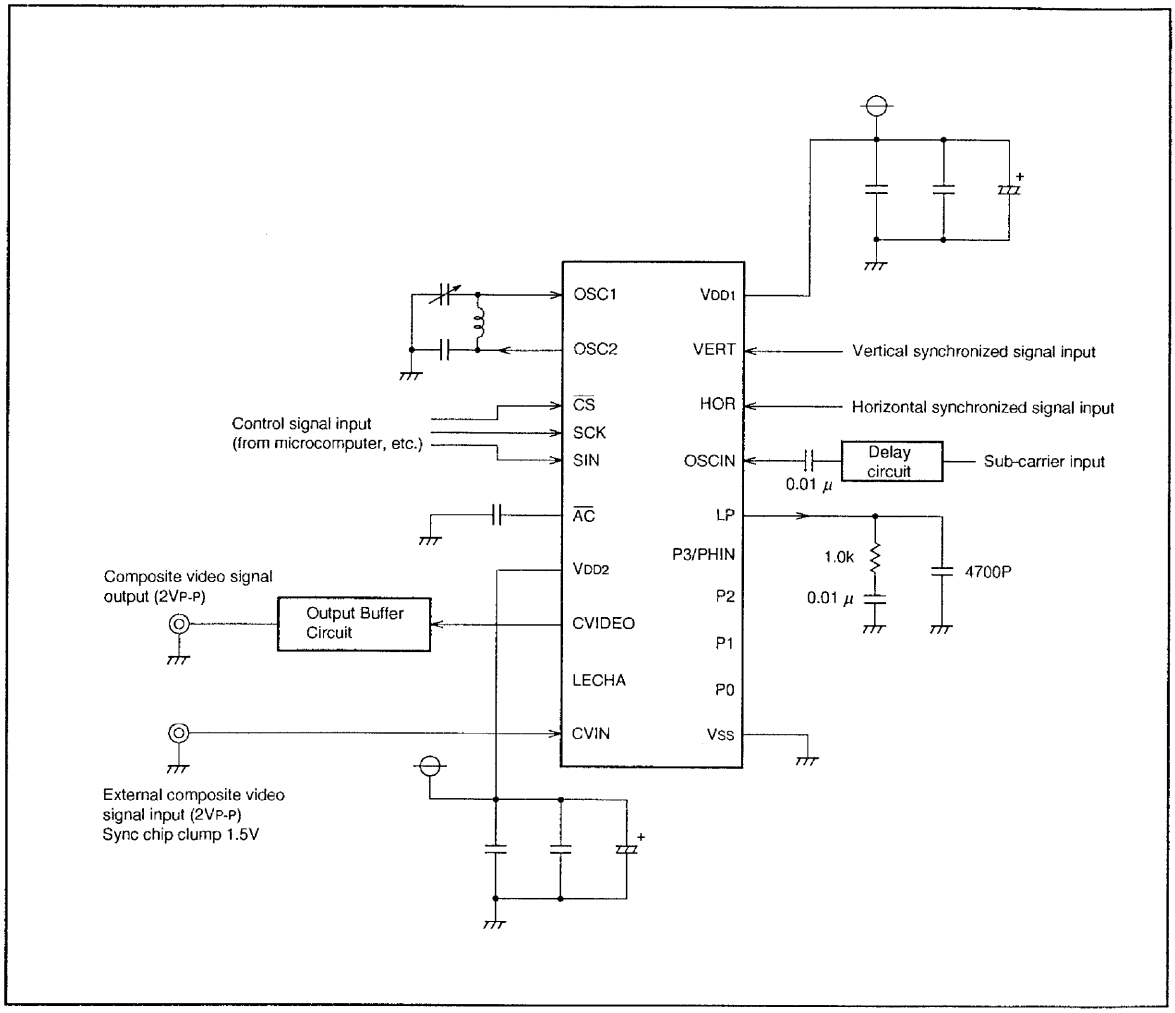



Fig. 14 Example of Peripheral circuit

## STANDARD ROM TYPE : M35017-001SP/FP

M35017-001SP/FP is a standard ROM type of M35017-XXXSP/FP. The input/output polarity and character patterns are fixed to the contents of Table 3 and Figure 17 to 19.

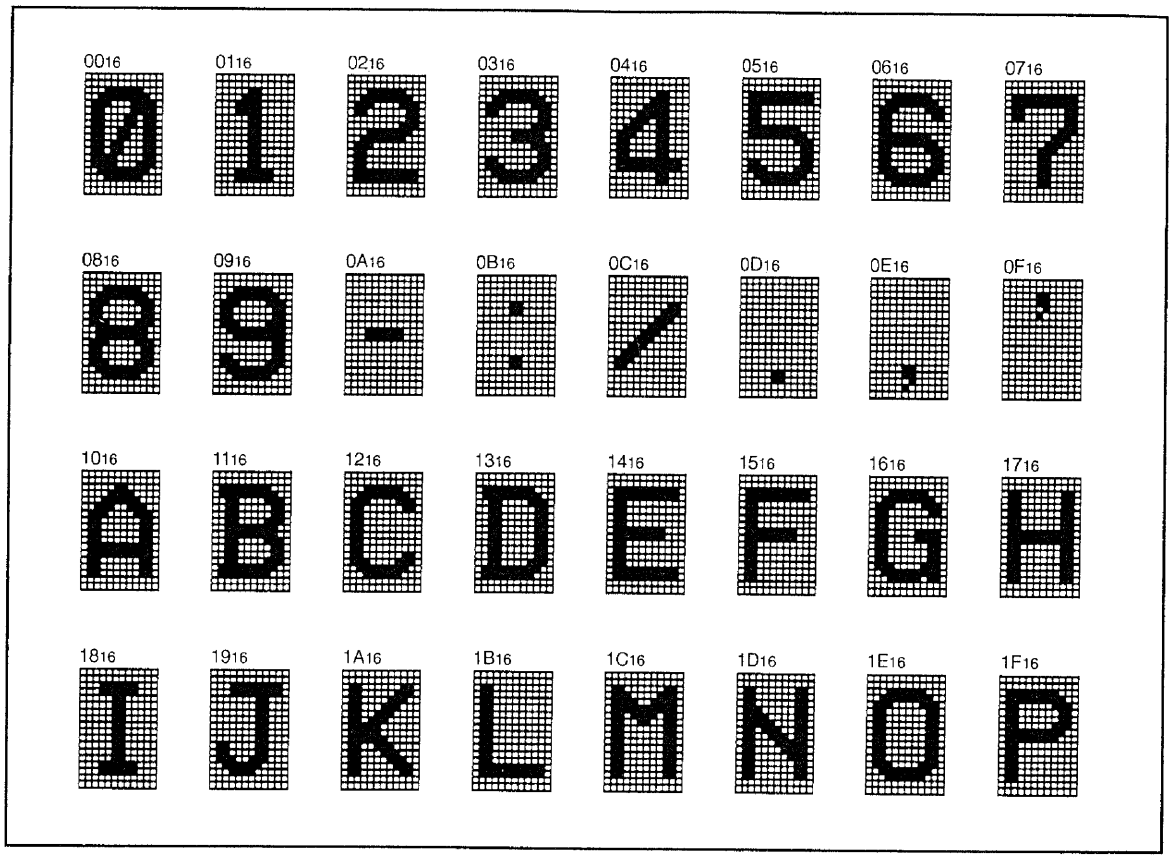



Fig. 15 M35017-001SP/FP character patterns (1)

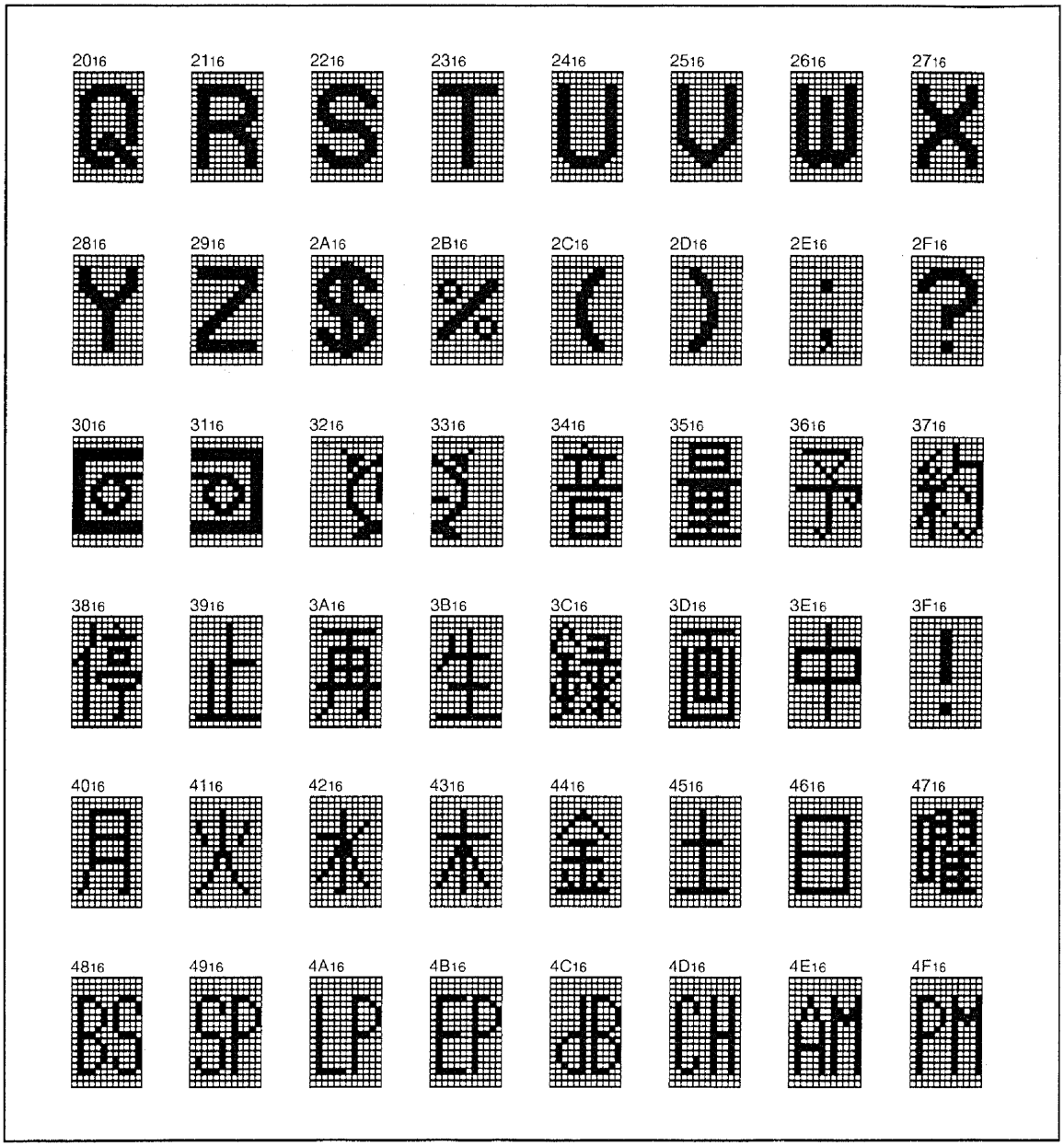



Fig. 16 M35017-001SP/FP character patterns (2)

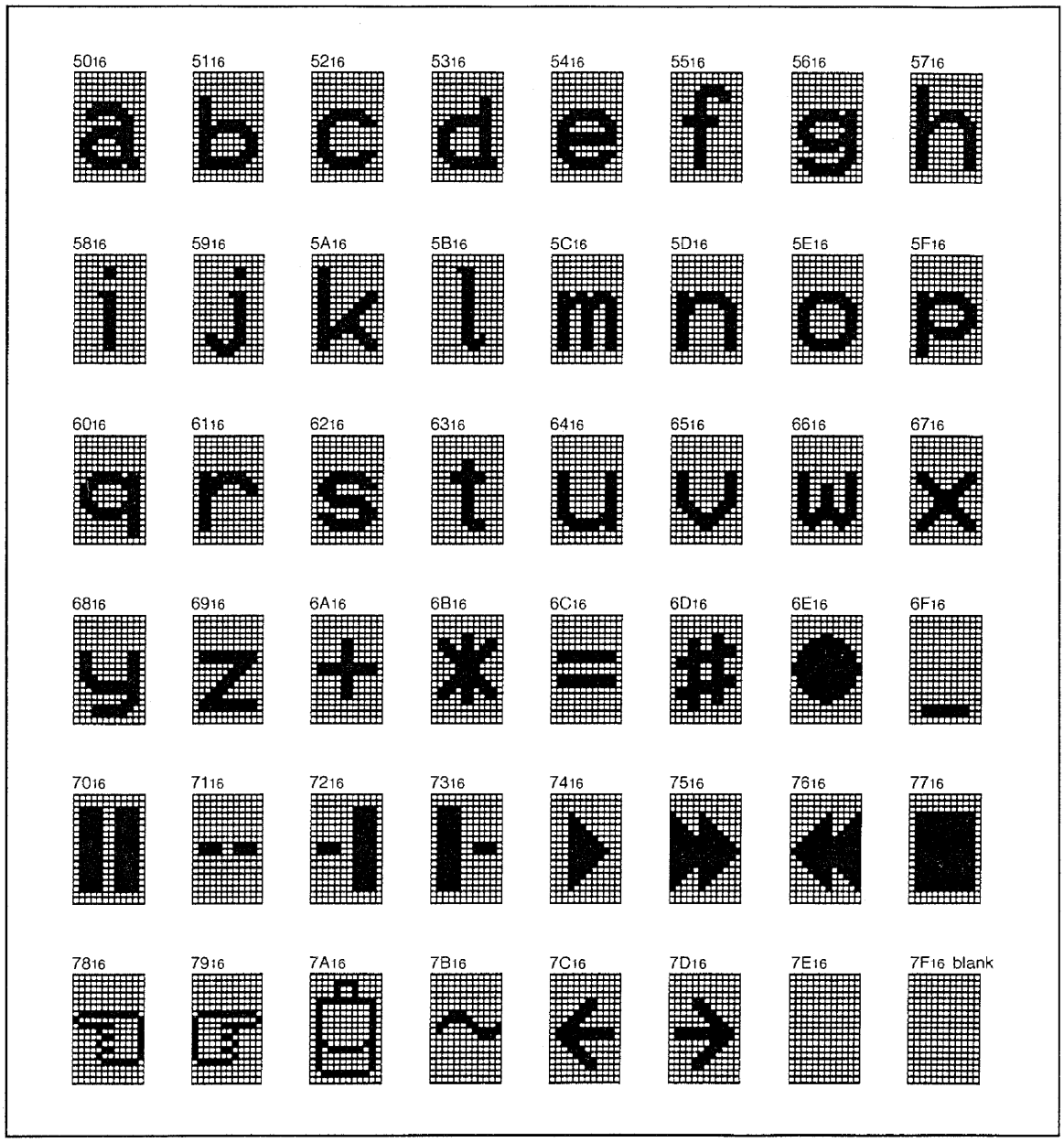



Fig. 17 M35017-001SP/FP character patterns (3)