



Pin Description

Pin No.	Name	Type	Description															
1, 49, 54, 65	VDD_SRC	PWR	3.3V power supply for outputs.															
2, 3, 50, 51, 52, 53, 55, 56, 58, 59, 60, 61, 63, 64, 66, 67, 69, 70	SRCT/C[1:9]	O, DIF	100-MHz Differential serial reference clocks.															
4, 68	VSS_SRC	GND	Ground for outputs.															
5, 6	CPUT2_ITP/SRCT10, CPUC2_ITP/SRCC10	O, DIF	Selectable differential CPU or SRC clock output. ITP_SEL = 0 @ VTT_PWRGD# assertion = SRC10 ITP_SEL = 1 @ VTT_PWRGD# assertion = CPU2															
7	VDDA	PWR	3.3V power supply for PLL.															
8	VSSA	GND	Ground for PLL.															
9	IREF	I	A precision resistor is attached to this pin which is connected to the internal current reference.															
10, 11, 13, 14	CPUT/C[0:1]	O, DIF	Differential CPU clock outputs.															
12	VDD_CPU	PWR	3.3V power supply for outputs.															
15	VSS_CPU	GND	Ground for outputs.															
16	SCLK	I	SMBus-compatible SCLOCK.															
17	SDATA	I/O, OD	SMBus-compatible SDATA.															
18	VDD_REF	PWR	3.3V power supply for outputs.															
19	XOUT	O, SE	14.318-MHz crystal output.															
20	XIN	I	14.318-MHz crystal input.															
21	VSS_REF	GND	Ground for outputs.															
22	REF1	O	Fixed 14.318-MHz clock output.															
23	REF0/FSC_TESTSEL	I/O,PD	Fixed 14.318 clock output / 3.3V-tolerant input for CPU frequency selection/Selects test mode if pulled to V_{IMFS_C} when VTT_PWRGD# is asserted LOW. <i>Refer to DC Electrical Specifications table for V_{ILFS_C}, V_{IMFS_C}, V_{IHFS_C} specifications.</i>															
24	CPU_STP#	I, PU	3.3V LVTTTL input for CPU_STP# active LOW.															
25	PCI_STP#	I, PU	3.3V LVTTTL input for PCI_STP# active LOW.															
26, 28, 29, 38, 46, 57, 62, 71, 72	CLKREQ[1:9]#	I, PU	3.3V LVTTTL input for enabling assigned SRC clock (active LOW).															
27, 32, 33	PCI[1:3]	O, SE	33-MHz clock outputs															
30, 36	VDD_PCI	PWR	3.3V power supply for outputs.															
31, 35	VSS_PCI	GND	Ground for outputs.															
34	PCI4/FCTSEL1	I/O, PD	33-MHz clock output / 3.3V LVTTTL input for selecting pins 47,48 (SRC[T/C]0, 100M[T/C]) and pins 43,44 (DOT96[T/C] and 27M Spread and Non-spread) (sampled on the VTT_PWRGD# assertion). <table border="1"><tr><td>FCTSEL1</td><td>Pin 43</td><td>Pin 44</td><td>Pin 47</td><td>Pin 48</td></tr><tr><td>0</td><td>DOT96T</td><td>DOT96C</td><td>96/100M_T</td><td>96/100M_C</td></tr><tr><td>1</td><td>27M_NSS</td><td>27M_SS</td><td>SRCT0</td><td>SRCC0</td></tr></table>	FCTSEL1	Pin 43	Pin 44	Pin 47	Pin 48	0	DOT96T	DOT96C	96/100M_T	96/100M_C	1	27M_NSS	27M_SS	SRCT0	SRCC0
FCTSEL1	Pin 43	Pin 44	Pin 47	Pin 48														
0	DOT96T	DOT96C	96/100M_T	96/100M_C														
1	27M_NSS	27M_SS	SRCT0	SRCC0														
37	ITP_SEL/PCIF0	I/O,PD, SE	3.3V LVTTTL input to enable SRC10 or CPU2_ITP / 33-MHz clock output. (sampled on the VTT_PWRGD# assertion). 1 = CPU2_ITP, 0 = SRC10															

Pin Description (continued)

Pin No.	Name	Type	Description
39	VTT_PWRGD#/PD	I, PD	3.3V LVTTTL input. This pin is a level sensitive strobe used to latch the FSA, FSB, FSC, FCTSEL1, and ITP_SEL. After VTT_PWRGD# (active LOW) assertion, this pin becomes a real-time input for asserting power down (active HIGH).
40	VDD_48	PWR	3.3V power supply for outputs.
41	48M/FSA	I/O	Fixed 48-MHz clock output / 3.3V-tolerant input for CPU frequency selection <i>Refer to DC Electrical Specifications table for Vil_FS and Vih_FS specifications.</i>
42	VSS_48	GND	Ground for outputs.
43, 44	DOT96T/ 27M_NSS DOT96C/ 27M_SS	O, DIF	Fixed 96-MHz clock output or 27 Mhz Spread and Non-spread output Selected via FCTSEL1 at VTT_PWRGD# assertion.
45	FSB/TEST_MODE	I	3.3V-tolerant input for CPU frequency selection. Selects Ref/N or Tri-state when in test mode 0 = Tri-state, 1 = Ref/N <i>Refer to DC Electrical Specifications table for Vil_FS and Vih_FS specifications.</i>
47, 48	SRC[T/C]0/ LCD100M[T/C]	O,DIF	100-MHz differential serial reference clock output / Differential 96/100-MHz SS clock for flat-panel display Selected via FCTSEL1 at VTT_PWRGD# assertion.

Frequency Select Pins (FSA, FSB, and FSC)

Host clock frequency selection is achieved by applying the appropriate logic levels to FSA, FSB, FSC inputs prior to VTT_PWRGD# assertion (as seen by the clock synthesizer). Upon VTT_PWRGD# being sampled LOW by the clock chip (indicating processor VTT voltage is stable), the clock chip samples the FSA, FSB, and FSC input values. For all logic levels of FSA, FSB, and FSC, VTT_PWRGD# employs a one-shot functionality in that once a valid LOW on VTT_PWRGD# has been sampled, all further VTT_PWRGD#, FSA, FSB, and FSC transitions will be ignored, except in test mode.

Serial Data Interface

To enhance the flexibility and function of the clock synthesizer, a two-signal serial interface is provided. Through the Serial Data Interface, various device functions, such as individual clock output buffers, can be individually enabled or disabled. The registers associated with the Serial Data Interface

initialize to their default setting upon power-up, and therefore use of this interface is optional. Clock device register changes are normally made upon system initialization, if any are required. The interface cannot be used during system operation for power management functions.

Data Protocol

The clock driver serial protocol accepts byte write, byte read, block write, and block read operations from the controller. For block write/read operation, the bytes must be accessed in sequential order from lowest to highest byte (most significant bit first) with the ability to stop after any complete byte has been transferred. For byte write and byte read operations, the system controller can access individually indexed bytes. The offset of the indexed byte is encoded in the command code, as described in *Table 2*.

The block write and block read protocol is outlined in *Table 3* while *Table 4* outlines the corresponding byte write and byte read protocol. The slave receiver address is 11010010 (D2h)

Table 1. Frequency Select Table FSA, FSB, and FSC^[1]

FSC	FSB	FSA	CPU	SRC	PCIF/PCI	27MHz	REF0	DOT96	USB
1	0	1	100 MHz	100 MHz	33 MHz	27 MHz	14.318 MHz	96 MHz	48 MHz
0	0	1	133 MHz	100 MHz	33 MHz	27 MHz	14.318 MHz	96 MHz	48 MHz
0	1	1	166 MHz	100 MHz	33 MHz	27 MHz	14.318 MHz	96 MHz	48 MHz
0	1	0	200 MHz	100 MHz	33 MHz	27 MHz	14.318 MHz	96 MHz	48 MHz

Table 2. Command Code Definition

Bit	Description
7	0 = Block read or block write operation, 1 = Byte read or byte write operation
(6:0)	Byte offset for byte read or byte write operation. For block read or block write operations, these bits should be '0000000'

Note:

1. 27-MHz and 96-MHz can not be output at the same time.

Table 3. Block Read and Block Write Protocol

Block Write Protocol		Block Read Protocol	
Bit	Description	Bit	Description
1	Start	1	Start
8:2	Slave address – 7 bits	8:2	Slave address – 7 bits
9	Write	9	Write
10	Acknowledge from slave	10	Acknowledge from slave
18:11	Command Code – 8 bits	18:11	Command Code – 8 bits
19	Acknowledge from slave	19	Acknowledge from slave
27:20	Byte Count – 8 bits (Skip this step if I ² C_EN bit set)	20	Repeat start
28	Acknowledge from slave	27:21	Slave address – 7 bits
36:29	Data byte 1 – 8 bits	28	Read = 1
37	Acknowledge from slave	29	Acknowledge from slave
45:38	Data byte 2 – 8 bits	37:30	Byte Count from slave – 8 bits
46	Acknowledge from slave	38	Acknowledge
....	Data Byte/Slave Acknowledges	46:39	Data byte 1 from slave – 8 bits
....	Data Byte N – 8 bits	47	Acknowledge
....	Acknowledge from slave	55:48	Data byte 2 from slave – 8 bits
....	Stop	56	Acknowledge
			Data bytes from slave / Acknowledge
			Data Byte N from slave – 8 bits
			NOT Acknowledge
			Stop

Table 4. Byte Read and Byte Write Protocol

Byte Write Protocol		Byte Read Protocol	
Bit	Description	Bit	Description
1	Start	1	Start
8:2	Slave address – 7 bits	8:2	Slave address – 7 bits
9	Write	9	Write
10	Acknowledge from slave	10	Acknowledge from slave
18:11	Command Code – 8 bits	18:11	Command Code – 8 bits
19	Acknowledge from slave	19	Acknowledge from slave
27:20	Data byte – 8 bits	20	Repeated start
28	Acknowledge from slave	27:21	Slave address – 7 bits
29	Stop	28	Read
		29	Acknowledge from slave
		37:30	Data from slave – 8 bits
		38	NOT Acknowledge
		39	Stop

Control Registers

Byte 0: Control Register 0

Bit	@Pup	Name	Description
7	1	SRC[T/C]7	SRC[T/C]7 Output Enable 0 = Disable (Tri-state), 1 = Enable
6	1	SRC[T/C]6	SRC[T/C]6 Output Enable 0 = Disable (Tri-state), 1 = Enable
5	1	SRC[T/C]5	SRC[T/C]5 Output Enable 0 = Disable (Tri-state), 1 = Enable
4	1	SRC[T/C]4	SRC[T/C]4 Output Enable 0 = Disable (Tri-state), 1 = Enable
3	1	SRC[T/C]3	SRC[T/C]3 Output Enable 0 = Disable (Tri-state), 1 = Enable
2	1	SRC[T/C]2	SRC[T/C]2 Output Enable 0 = Disable (Tri-state), 1 = Enable
1	1	SRC[T/C]1	SRC[T/C]1 Output Enable 0 = Disable (Tri-state), 1 = Enable
0	1	SRC[T/C]0 / LCD_96_100M[T/C] /LCD_96_100M[T/C]	SRC[T/C]0 / LCD_96_100M[T/C] Output Enable 0 = Disable (Hi-Z), 1 = Enable

Byte 1: Control Register 1

Bit	@Pup	Name	Description
7	1	PCIF0	PCIF0 Output Enable 0 = Disabled, 1 = Enabled
6	1	27M NSS / DOT_96[T/C]	27M Non-spread and DOT_96 MHz Output Enable 0 = Disable (Tri-state), 1 = Enabled
5	1	USB_48MHz	USB_48M MHz Output Enable 0 = Disabled, 1 = Enabled
4	1	REF0	REF0 Output Enable 0 = Disabled, 1 = Enabled
3	1	REF1	REF1 Output Enable 0 = Disabled, 1 = Enabled
2	1	CPU[T/C]1	CPU[T/C]1 Output Enable 0 = Disable (Tri-state), 1 = Enabled
1	1	CPU[T/C]0	CPU[T/C]0 Output Enable 0 = Disable (Tri-state), 1 = Enabled
0	0	CPU, SRC, PCI, PCIF Spread Enable	PLL1 (CPU PLL) Spread Spectrum Enable 0 = Spread off, 1 = Spread on

Byte 2: Control Register 2

Bit	@Pup	Name	Description
7	1	PCI4	PCI4 Output Enable 0 = Disabled, 1 = Enabled
6	1	PCI3	PCI3 Output Enable 0 = Disabled, 1 = Enabled
5	1	PCI2	PCI2 Output Enable 0 = Disabled, 1 = Enabled
4	1	PCI1	PCI1 Output Enable 0 = Disabled, 1 = Enabled
3	1	Reserved	Reserved, Set = 1
2	1	Reserved	Reserved, Set = 1
1	1	CPU[T/C]2	CPU[T/C]2 Output Enable 0 = Disabled (Hi-Z), 1 = Enabled
0	1	Reserved	Reserved, Set = 1

Byte 3: Control Register 3

Bit	@Pup	Name	Description
7	0	SRC7	Allow control of SRC[T/C]7 with assertion of PCI_STP# or SW PCI_STP# 0 = Free running, 1 = Stopped with PCI_STP#
6	0	SRC6	Allow control of SRC[T/C]6 with assertion of PCI_STP# or SW PCI_STP# 0 = Free running, 1 = Stopped with PCI_STP#
5	0	SRC5	Allow control of SRC[T/C]5 with assertion of PCI_STP# or SW PCI_STP# 0 = Free running, 1 = Stopped with PCI_STP#
4	0	SRC4	Allow control of SRC[T/C]4 with assertion of PCI_STP# or SW PCI_STP# 0 = Free running, 1 = Stopped with PCI_STP#
3	0	SRC3	Allow control of SRC[T/C]3 with assertion of PCI_STP# or SW PCI_STP# 0 = Free running, 1 = Stopped with PCI_STP#
2	0	SRC2	Allow control of SRC[T/C]2 with assertion of PCI_STP# or SW PCI_STP# 0 = Free running, 1 = Stopped with PCI_STP#
1	0	SRC1	Allow control of SRC[T/C]1 with assertion of PCI_STP# or SW PCI_STP# 0 = Free running, 1 = Stopped with PCI_STP#
0	0	SRC0	Allow control of SRC[T/C]0 with assertion of PCI_STP# or SW PCI_STP# 0 = Free running, 1 = Stopped with PCI_STP#

Byte 4: Control Register 4

Bit	@Pup	Name	Description
7	0	LCD_96_100M[T/C]	LCD_96_100M[T/C] PWRDWN Drive Mode 0 = Driven in PWRDWN, 1 = Tri-state
6	0	DOT96[T/C]	DOT PWRDWN Drive Mode 0 = Driven in PWRDWN, 1 = Tri-state
5	0	RESERVED	RESERVED, Set = 0
4	0	RESERVED	RESERVED, Set = 0
3	0	PCIF0	Allow control of PCIF0 with assertion of SW and HW PCI_STP# 0 = Free running, 1 = Stopped with PCI_STP#
2	1	CPU[T/C]2	Allow control of CPU[T/C]2 with assertion of CPU_STP# 0 = Free running, 1 = Stopped with CPU_STP#
1	1	CPU[T/C]1	Allow control of CPU[T/C]1 with assertion of CPU_STP# 0 = Free running, 1 = Stopped with CPU_STP#
0	1	CPU[T/C]0	Allow control of CPU[T/C]0 with assertion of CPU_STP# 0 = Free running, 1 = Stopped with CPU_STP#

Byte 5: Control Register 5

Bit	@Pup	Name	Description
7	0	SRC[T/C]	SRC[T/C] Stop Drive Mode 0 = Driven when PCI_STP# asserted, 1 = Tri-state when PCI_STP# asserted
6	0	CPU[T/C]2	CPU[T/C]2 Stop Drive Mode 0 = Driven when CPU_STP# asserted, 1 = Tri-state when CPU_STP# asserted
5	0	CPU[T/C]1	CPU[T/C]1 Stop Drive Mode 0 = Driven when CPU_STP# asserted, 1 = Tri-state when CPU_STP# asserted
4	0	CPU[T/C]0	CPU[T/C]0 Stop Drive Mode 0 = Driven when CPU_STP# asserted, 1 = Tri-state when CPU_STP# asserted
3	0	SRC[T/C][9:1]	SRC[T/C][9:1] PWRDWN Drive Mode 0 = Driven when PD asserted, 1 = Tri-state when PD asserted
2	0	CPU[T/C]2	CPU[T/C]2 PWRDWN Drive Mode 0 = Driven when PD asserted, 1 = Tri-state when PD asserted

Byte 5: Control Register 5 (continued)

Bit	@Pup	Name	Description
1	0	CPU[T/C]1	CPU[T/C]1 PWRDWN Drive Mode 0 = Driven when PD asserted, 1 = Tri-state when PD asserted
0	0	CPU[T/C]0	CPU[T/C]0 PWRDWN Drive Mode 0 = Driven when PD asserted, 1 = Tri-state when PD asserted

Byte 6: Control Register 6

Bit	@Pup	Name	Description
7	0	TEST_SEL	REF/N or Tri-state Select 0 = Tri-state, 1 = REF/N Clock
6	0	TEST_MODE	Test Clock Mode Entry Control 0 = Normal operation, 1 = REF/N or Tri-state mode,
5	1	REF1	REF1 Output Drive Strength 0 = Low, 1 = High
4	1	REF0	REF0 Output Drive Strength 0 = Low, 1 = High
3	1	PCI, PCIF and SRC clock outputs except those set to free running	SW PCI_STP Function 0=SW PCI_STP assert, 1= SW PCI_STP deassert When this bit is set to 0, all STOPPABLE PCI, PCIF and SRC outputs will be stopped in a synchronous manner with no short pulses. When this bit is set to 1, all STOPPED PCI, PCIF and SRC outputs will resume in a synchronous manner with no short pulses.
2	HW	FSC	FSC Reflects the value of the FSC pin sampled on power up 0 = FSC was low during VTT_PWRGD# assertion
1	HW	FSB	FSB Reflects the value of the FSB pin sampled on power up 0 = FSB was low during VTT_PWRGD# assertion
0	HW	FSA	FSA Reflects the value of the FSA pin sampled on power up 0 = FSA was low during VTT_PWRGD# assertion

Byte 7: Vendor ID

Bit	@Pup	Name	Description
7	0	Revision Code Bit 3	Revision Code Bit 3
6	0	Revision Code Bit 2	Revision Code Bit 2
5	0	Revision Code Bit 1	Revision Code Bit 1
4	1	Revision Code Bit 0	Revision Code Bit 0
3	1	Vendor ID Bit 3	Vendor ID Bit 3
2	0	Vendor ID Bit 2	Vendor ID Bit 2
1	0	Vendor ID Bit 1	Vendor ID Bit 1
0	0	Vendor ID Bit 0	Vendor ID Bit 0

Byte 8: Control Register 8

Bit	@Pup	Name	Description
7	0	RESERVED	RESERVED, Set = 0
6	0	RESERVED	RESERVED, Set = 0
5	0	RESERVED	RESERVED, Set = 0
4	0	RESERVED	RESERVED, Set = 0
3	0	RESERVED	RESERVED, Set = 0
2	1	USB_48M	USB_48MHz Output Drive Strength 0= Low, 1= High
1	1	RESERVED	RESERVED, Set = 1
0	1	PCIF0	PCIF0 Output Drive Strength 0 = Low, 1 = High

Byte 9: Control Register 9

Bit	@Pup	Name	Description
7	0	RESERVED	RESERVED
6	0	RESERVED	RESERVED
5	0	S1	27M_SS / LCD 96_100M SS Spread Spectrum Selection table: S[1:0] SS%
4	0	S0	'00' = -0.5%(Default value) '01' = -1.0% '10' = -1.5% '11' = -2.0%
3	1	RESERVED	RESERVED, Set = 1
2	1	27M_SS	27M Spread Output Enable 0 = Disable (Tri-state), 1 = Enabled
1	1	27M_SS Spread Enable	27M_SS Spread spectrum enable. 0 = Disable, 1 = Enable.
0	0	RESERVED	RESERVED set = 0

Byte 10: Control Register 10

Bit	@Pup	Name	Description
7	1	RESERVED	RESERVED, Set = 1
6	1	RESERVED	RESERVED, Set = 1
5	1	SRC[T/C]9	SRC[T/C]9 Output Enable 0 = Disable (Hi-Z), 1 = Enable
4	1	SRC[T/C]8	SRC[T/C]8 Output Enable 0 = Disable (Hi-Z), 1 = Enable
3	0	RESERVED	RESERVED, Set = 0
2	0	SRC[T/C]10	Allow control of SRC[T/C]10 with assertion of SW PCI_STP# 0 = Free running, 1 = Stopped with PCI_STP#
1	0	SRC[T/C]9	Allow control of SRC[T/C]9 with assertion of SW PCI_STP# 0 = Free running, 1 = Stopped with PCI_STP#
0	0	SRC[T/C]8	Allow control of SRC[T/C]8 with assertion of SW PCI_STP# 0 = Free running, 1 = Stopped with PCI_STP#

Byte 11: Control Register 11

Bit	@Pup	Name	Description
7	0	RESERVED	RESERVED
6	HW	RESERVED	RESERVED
5	HW	RESERVED	RESERVED
4	HW	RESERVED	RESERVED
3	0	27M_SS / 27M_NSS	27-MHz (spread and non-spread) Output Drive Strength 0 = Low, 1 = High
2	0	RESERVED	RESERVED
1	0	RESERVED	RESERVED Set = 0
0	HW	RESERVED	RESERVED

Byte 12: Control Register 12

Bit	@Pup	Name	Description
7	0	CLKREQ#9	CLKREQ#9 Input Enable 0 = Disable 1 = Enable
6	0	CLKREQ#8	CLKREQ#8 Input Enable 0 = Disable 1 = Enable
5	0	CLKREQ#7	CLKREQ#7 Input Enable 0 = Disable 1 = Enable
4	0	CLKREQ#6	CLKREQ#6 Input Enable 0 = Disable 1 = Enable
3	0	CLKREQ#5	CLKREQ#5 Input Enable 0 = Disable 1 = Enable
2	0	CLKREQ#4	CLKREQ#4 Input Enable 0 = Disable 1 = Enable
1	0	CLKREQ#3	CLKREQ#3 Input Enable 0 = Disable 1 = Enable
0	0	CLKREQ#2	CLKREQ#2 Input Enable 0 = Disable 1 = Enable

Byte 13: Control Register 13

Bit	@Pup	Name	Description
7	0	CLKREQ#1	CLKREQ#1 Input Enable 0 = Disable 1 = Enable
6	1	LCD 96_100M Clock Speed	LCD 96_100M Clock Speed 0 = 96 MHz 1 = 100 MHz
5	1	RESERVED	RESERVED, Set = 1
4	1	RESERVED	RESERVED, Set = 1
3	1	PCI4	PCI4 (Spread and Non-spread) Output Drive Strength 0 = Low, 1 = High
2	1	PCI3	PCI3 (Spread and Non-spread) Output Drive Strength 0 = Low, 1 = High
1	1	PCI2	PCI2 (Spread and Non-spread) Output Drive Strength 0 = Low, 1 = High
0	1	PCI1	PCI1 (Spread and Non-spread) Output Drive Strength 0 = Low, 1 = High

Table 5. Crystal Recommendations

Frequency (Fund)	Cut	Loading	Load Cap	Drive (max.)	Shunt Cap (max.)	Motional (max.)	Tolerance (max.)	Stability (max.)	Aging (max.)
14.31818 MHz	AT	Parallel	20 pF	0.1 mW	5 pF	0.016 pF	35 ppm	30 ppm	5 ppm

The CY28447 requires a Parallel Resonance Crystal. Substituting a series resonance crystal will cause the CY28447 to operate at the wrong frequency and violate the ppm specification. For most applications there is a 300-ppm frequency shift between series and parallel crystals due to incorrect loading.

Crystal Loading

Crystal loading plays a critical role in achieving low ppm performance. To realize low ppm performance, the total capacitance

the crystal will see must be considered to calculate the appropriate capacitive loading (CL).

Figure 1 shows a typical crystal configuration using the two trim capacitors. An important clarification for the following discussion is that the trim capacitors are in series with the crystal not parallel. It's a common misconception that load capacitors are in parallel with the crystal and should be approximately equal to the load capacitance of the crystal. This is not true.

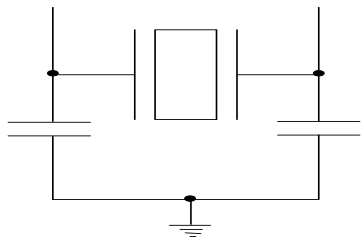


Figure 1. Crystal Capacitive Clarification

Calculating Load Capacitors

In addition to the standard external trim capacitors, trace capacitance and pin capacitance must also be considered to correctly calculate crystal loading. As mentioned previously, the capacitance on each side of the crystal is in series with the crystal. This means the total capacitance on each side of the crystal must be twice the specified crystal load capacitance (CL). While the capacitance on each side of the crystal is in series with the crystal, trim capacitors (Ce1,Ce2) should be calculated to provide equal capacitive loading on both sides.

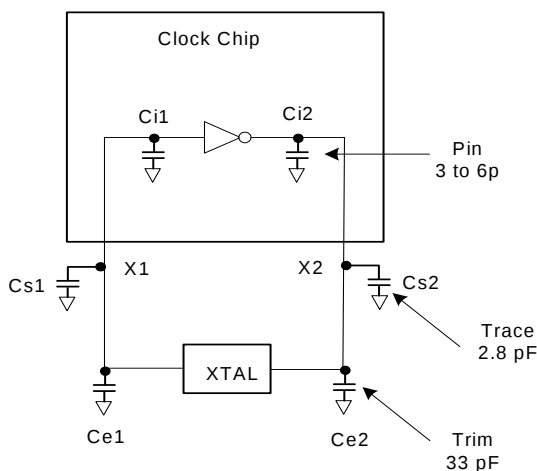


Figure 2. Crystal Loading Example

As mentioned previously, the capacitance on each side of the crystal is in series with the crystal. This means the total capacitance on each side of the crystal must be twice the specified load capacitance (CL). While the capacitance on each side of the crystal is in series with the crystal, trim capacitors

(Ce1,Ce2) should be calculated to provide equal capacitance loading on both sides.

Use the following formulas to calculate the trim capacitor values for Ce1 and Ce2.

Load Capacitance (each side)

$$C_e = 2 * CL - (C_s + C_i)$$

Total Capacitance (as seen by the crystal)

$$CL_e = \frac{1}{\left(\frac{1}{C_{e1} + C_{s1} + C_{i1}} + \frac{1}{C_{e2} + C_{s2} + C_{i2}}\right)}$$

CL.....Crystal load capacitance

CL_e.....Actual loading seen by crystal using standard value trim capacitors

C_e.....External trim capacitors

C_s.....Stray capacitance (terraced)

C_iInternal capacitance (lead frame, bond wires etc.)

CLK_REQ# Description

The CLKREQ# signals are active LOW inputs used for clean enabling and disabling selected SRC outputs. The outputs controlled by CLKREQ# are determined by the settings in register byte 8. The CLKREQ# signal is a de-bounced signal in that it's state must remain unchanged during two consecutive rising edges of SRCC to be recognized as a valid assertion or deassertion. (The assertion and deassertion of this signal is absolutely asynchronous.)

CLK_REQ[1:9]# Assertion (CLKREQ# -> LOW)

All differential outputs that were stopped are to resume normal operation in a glitch-free manner. The maximum latency from the assertion to active outputs is between 2 and 6 SRC clock periods (2 clocks are shown) with all SRC outputs resuming simultaneously. All stopped SRC outputs must be driven HIGH within 10 ns of CLKREQ# deassertion to a voltage greater than 200 mV.

CLK_REQ[1:9]# Deassertion (CLKREQ# -> HIGH)

The impact of deasserting the CLKREQ# pins is that all SRC outputs that are set in the control registers to stoppable via deassertion of CLKREQ# are to be stopped after their next transition. The final state of all stopped DIF signals is LOW, both SRCT clock and SRCC clock outputs will not be driven.

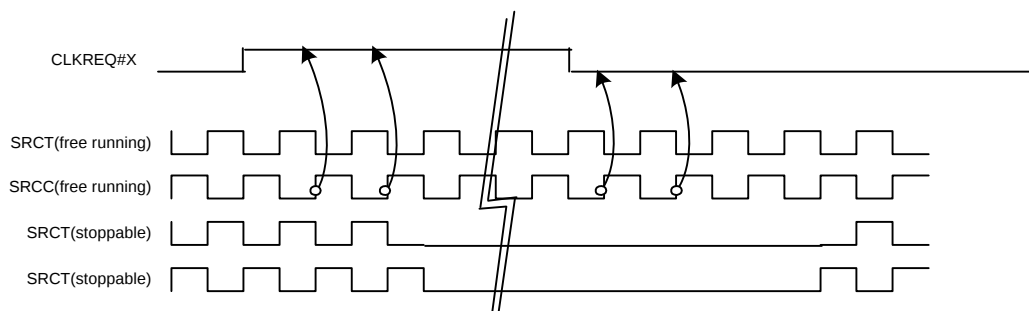


Figure 3. CLK_REQ#[1:9] Deassertion/Assertion Waveform

PD (Power-down) Clarification

The VTT_PWRGD# /PD pin is a dual-function pin. During initial power-up, the pin functions as VTT_PWRGD#. Once VTT_PWRGD# has been sampled LOW by the clock chip, the pin assumes PD functionality. The PD pin is an asynchronous active HIGH input used to shut off all clocks cleanly prior to shutting off power to the device. This signal is synchronized internal to the device prior to powering down the clock synthesizer. PD is also an asynchronous input for powering up the system. When PD is asserted HIGH, all clocks need to be driven to a LOW value and held prior to turning off the VCOs and the crystal oscillator.

PD (Power-down) Assertion

When PD is sampled HIGH by two consecutive rising edges of CPUC, all single-ended outputs will be held LOW on their next HIGH-to-LOW transition and differential clocks must be held HIGH or tri-stated (depending on the state of the control register drive mode bit) on the next diff clock# HIGH-to-LOW transition within 4 clock periods. When the SMBus PD drive mode bit corresponding to the differential (CPU, SRC, and DOT) clock output of interest is programmed to '0', the clock outputs are held with "Diff clock" pin driven HIGH at 2 x Iref, and "Diff clock#" tri-state. If the control register PD drive mode

bit corresponding to the output of interest is programmed to "1", then both the "Diff clock" and the "Diff clock#" are tri-state. Note that *Figure 4* shows CPUT = 133 MHz and PD drive mode = '1' for all differential outputs. This diagram and description is applicable to valid CPU frequencies 100, 133, 166, and 200 MHz. In the event that PD mode is desired as the initial power-on state, PD must be asserted HIGH in less than 10 μ s after asserting Vtt_PwrGd#. It should be noted that 96_100_SSC will follow the DOT waveform is selected for 96 MHz and the SRC waveform when in 100-MHz mode.

PD Deassertion

The power-up latency is less than 1.8 ms. This is the time from the deassertion of the PD pin or the ramping of the power supply until the time that stable clocks are output from the clock chip. All differential outputs stopped in a three-state condition resulting from power down will be driven high in less than 300 μ s of PD deassertion to a voltage greater than 200 mV. After the clock chip's internal PLL is powered up and locked, all outputs will be enabled within a few clock cycles of each other. *Figure 5* is an example showing the relationship of clocks coming up. It should be noted that 96_100_SSC will follow the DOT waveform is selected for 96 MHz and the SRC waveform when in 100-MHz mode.

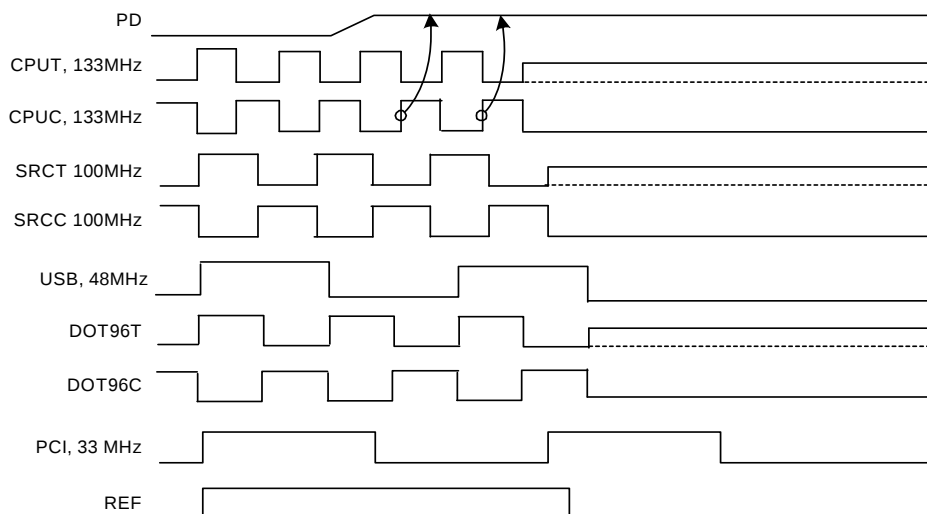


Figure 4. Power-down Assertion Timing Waveform

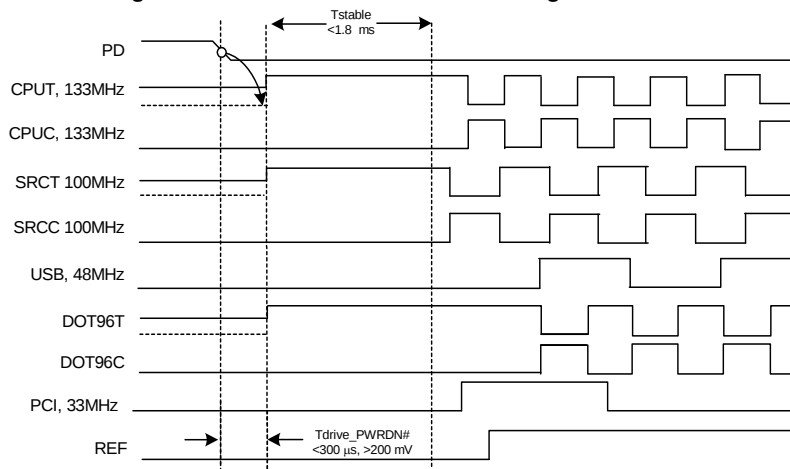


Figure 5. Power-down Deassertion Timing Waveform

CPU_STP# Assertion

The CPU_STP# signal is an active LOW input used for synchronous stopping and starting the CPU output clocks while the rest of the clock generator continues to function. When the CPU_STP# pin is asserted, all CPU outputs that are set with the SMBus configuration to be stoppable via assertion of CPU_STP# will be stopped within two–six CPU clock periods after being sampled by two rising edges of the internal CPUC clock. The final states of the stopped CPU signals are CPUT = HIGH and CPUC = LOW. There is no change to the output drive current values during the stopped state. The

CPUT is driven HIGH with a current value equal to $6 \times (I_{ref})$, and the CPUC signal will be tri-stated.

CPU_STP# Deassertion

The deassertion of the CPU_STP# signal will cause all CPU outputs that were stopped to resume normal operation in a synchronous manner, synchronous manner meaning that no short or stretched clock pulses will be produce when the clock resumes. The maximum latency from the deassertion to active outputs is no more than two CPU clock cycles.

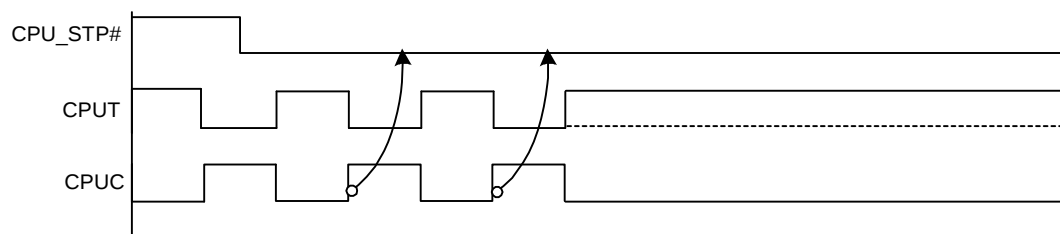


Figure 6. CPU_STP# Assertion Waveform

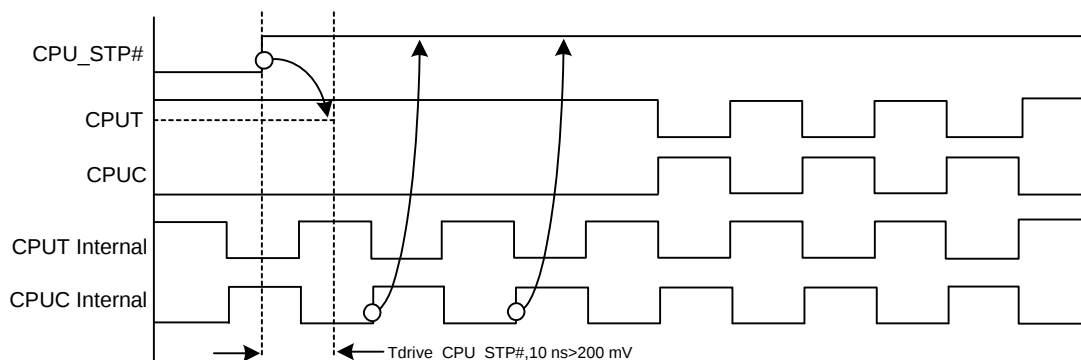


Figure 7. CPU_STP# Deassertion Waveform

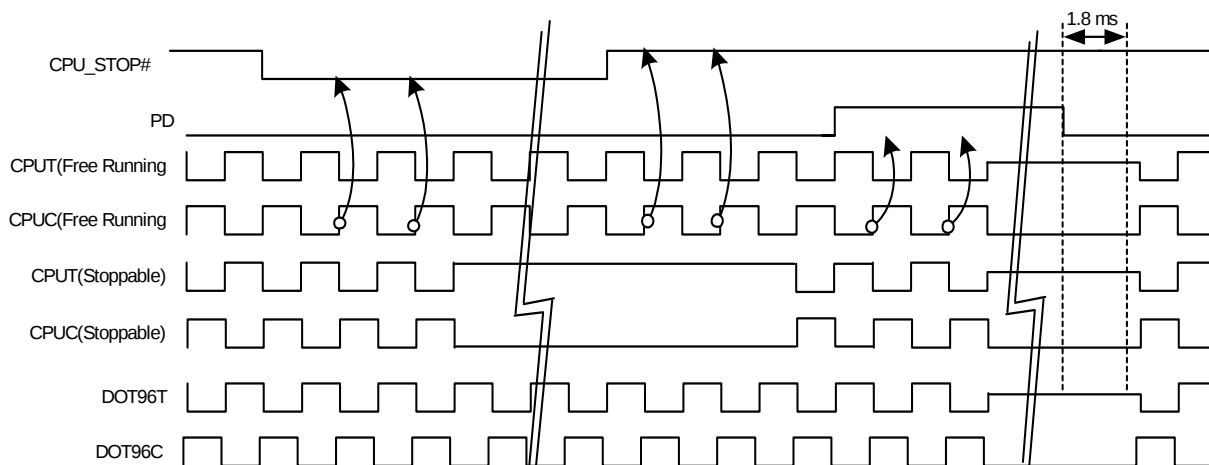


Figure 8. CPU_STP# = Driven, CPU_PD = Driven, DOT_PD = Driven

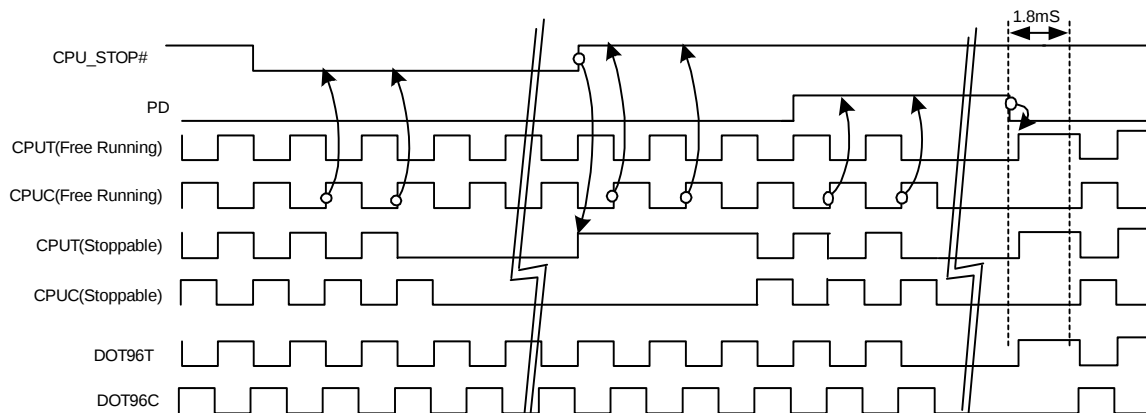


Figure 9. CPU_STP# = Tri-state, CPU_PD = Tri-state, DOT_PD = Tri-state

PCI_STP# Assertion

The PCI_STP# signal is an active LOW input used for synchronous stopping and starting the PCI outputs while the rest of the clock generator continues to function. The set-up time for capturing PCI_STP# going LOW is 10 ns (t_{su}). (See Figure 10.) The PCIF clocks will not be affected by this pin if their corresponding control bit in the SMBus register is set to allow them to be free running.

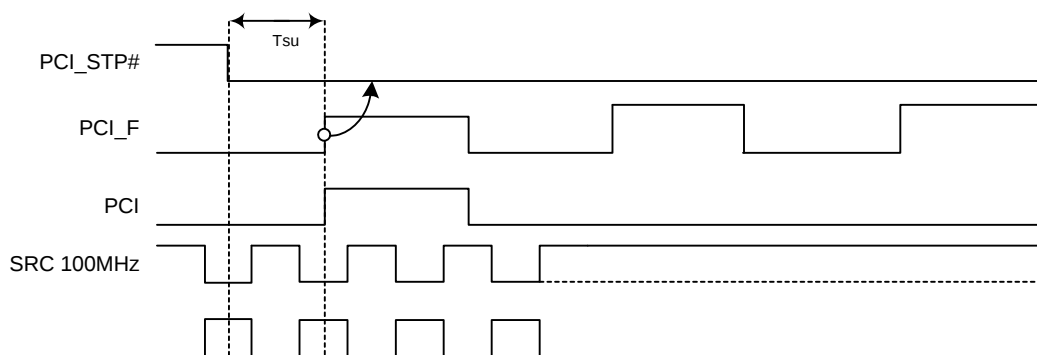


Figure 10. PCI_STP# Assertion Waveform

PCI_STP# Deassertion

The deassertion of the PCI_STP# signal will cause all PCI and stoppable PCIF clocks to resume running in a synchronous manner within two PCI clock periods after PCI_STP# transitions to a HIGH level.

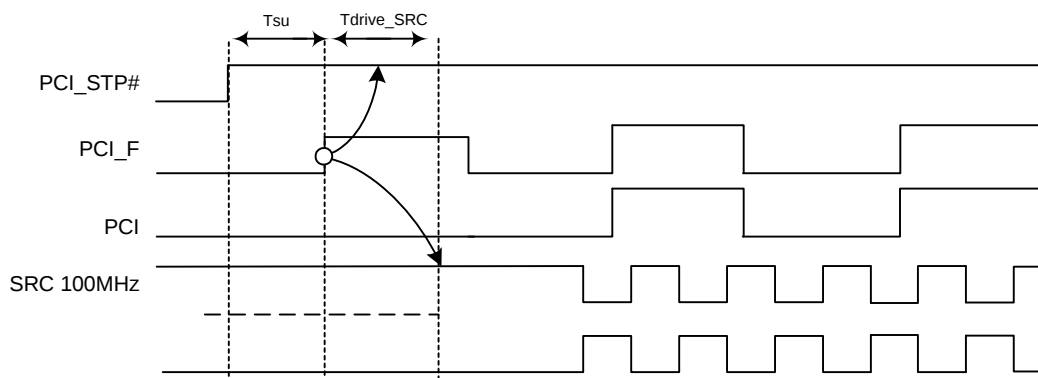


Figure 11. PCI_STP# Deassertion Waveform

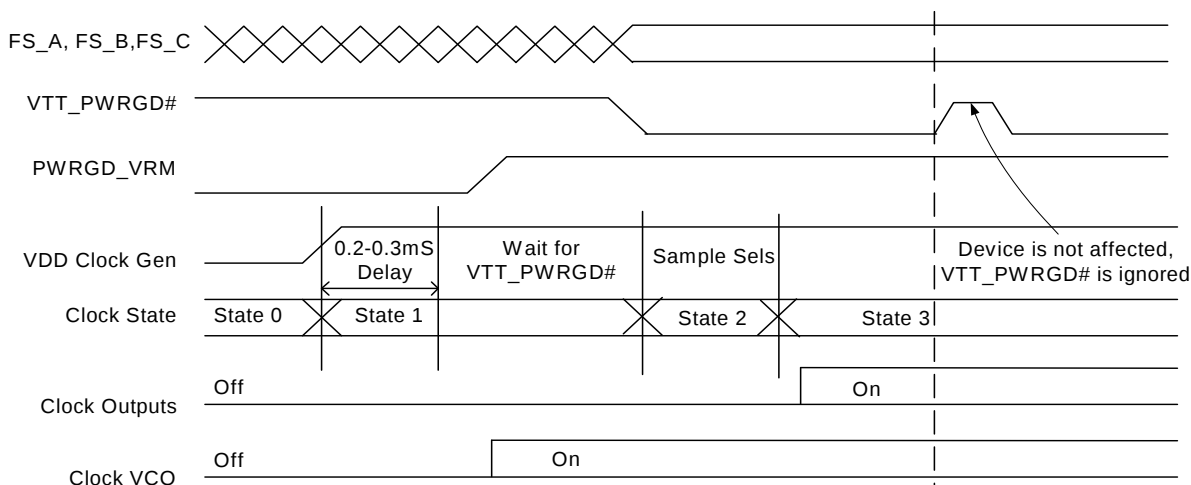


Figure 12. VTT_PWRGD# Timing Diagram

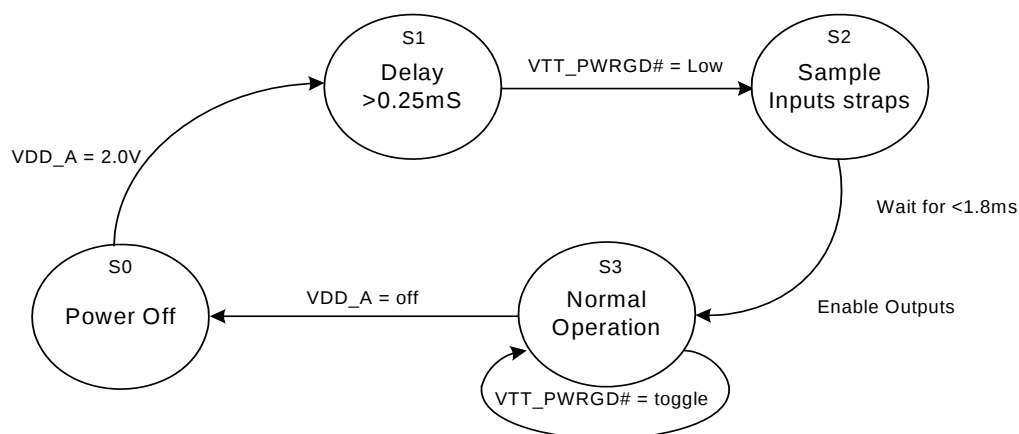


Figure 13. Single-ended Load Configuration

Absolute Maximum Conditions

Parameter	Description	Condition	Min.	Max.	Unit
V _{DD}	Core Supply Voltage		−0.5	4.6	V
V _{DD_A}	Analog Supply Voltage		−0.5	4.6	V
V _{IN}	Input Voltage	Relative to V _{SS}	−0.5	V _{DD} + 0.5	VDC
T _S	Temperature, Storage	Non-functional	−65	150	°C
T _A	Temperature, Operating Ambient	Functional	0	85	°C
T _J	Temperature, Junction	Functional	−	150	°C
Θ _{JC}	Dissipation, Junction to Case	MIL-STD-883E Method 1012.1	−	20	°C/W
Θ _{JA}	Dissipation, Junction to Ambient	JEDEC (JESD 51)	−	60	°C/W
ESD _{HBM}	ESD Protection (Human Body Model)	MIL-STD-883, Method 3015	2000	−	V
UL-94	Flammability Rating	At 1/8 in.	V-0		
MSL	Moisture Sensitivity Level		1		

Multiple Supplies: The Voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is NOT required.

DC Electrical Specifications

Parameter	Description	Condition	Min.	Max.	Unit
All VDDs	3.3V Operating Voltage	3.3 ± 5%	3.135	3.465	V
V _{ILi2C}	Input Low Voltage	SDATA, SCLK	−	1.0	V
V _{IHi2C}	Input High Voltage	SDATA, SCLK	2.2	−	V
V _{IL_FS}	FS_[A,B] Input Low Voltage		V _{SS} − 0.3	0.35	V
V _{IH_FS}	FS_[A,B] Input High Voltage		0.7	V _{DD} + 0.5	V
V _{ILFS_C}	FS_C Input Low Voltage		V _{SS} − 0.3	0.35	V
V _{IMFS_C}	FS_C Input Middle Voltage		0.7	1.7	V
V _{IHFS_C}	FS_C Input High Voltage		1.8	V _{DD} + 0.5	V
V _{IL}	3.3V Input Low Voltage		V _{SS} − 0.3	0.8	V
V _{IH}	3.3V Input High Voltage		2.0	V _{DD} + 0.3	V
I _{IL}	Input Low Leakage Current	Except internal pull-up resistors, 0 < V _{IN} < V _{DD}	−5	5	μA
I _{IH}	Input High Leakage Current	Except internal pull-down resistors, 0 < V _{IN} < V _{DD}	−	5	μA
V _{OL}	3.3V Output Low Voltage	I _{OL} = 1 mA	−	0.4	V
V _{OH}	3.3V Output High Voltage	I _{OH} = −1 mA	2.4	−	V
I _{OZ}	High-impedance Output Current		−10	10	μA
C _{IN}	Input Pin Capacitance		3	5	pF
C _{OUT}	Output Pin Capacitance		3	6	pF
L _{IN}	Pin Inductance		−	7	nH
V _{XIH}	Xin High Voltage		0.7V _{DD}	V _{DD}	V
V _{XIL}	Xin Low Voltage		0	0.3V _{DD}	V
I _{DD3.3V}	Dynamic Supply Current	At max. load in low drive mode per Figure 15 and Figure 17 @133 MHz	−	300	mA
I _{PD3.3V}	Power-down Supply Current	PD asserted, Outputs Driven	−	70	mA
I _{PD3.3V}	Power-down Supply Current	PD asserted, Outputs Tri-state	−	5	mA

AC Electrical Specifications

Parameter	Description	Condition	Min.	Max.	Unit
Crystal					
T _{DC}	XIN Duty Cycle	The device will operate reliably with input duty cycles up to 30/70 but the REF clock duty cycle will not be within specification	47.5	52.5	%
T _{PERIOD}	XIN Period	When XIN is driven from an external clock source	69.841	71.0	ns
T _R / T _F	XIN Rise and Fall Times	Measured between 0.3V _{DD} and 0.7V _{DD}	–	10.0	ns
T _{CCJ}	XIN Cycle to Cycle Jitter	As an average over 1-μs duration	–	500	ps
L _{ACC}	Long-term Accuracy	Measured at crossing point V _{OX}	–	300	ppm
CPU at 0.7V					
T _{DC}	CPUT and CPUC Duty Cycle	Measured at crossing point V _{OX}	45	55	%
T _{PERIOD}	100-MHz CPUT and CPUC Period	Measured at crossing point V _{OX}	9.997001	10.00300	ns
T _{PERIOD}	133-MHz CPUT and CPUC Period	Measured at crossing point V _{OX}	7.497751	7.502251	ns
T _{PERIOD}	166-MHz CPUT and CPUC Period	Measured at crossing point V _{OX}	5.998201	6.001801	ns
T _{PERIOD}	200-MHz CPUT and CPUC Period	Measured at crossing point V _{OX}	4.998500	5.001500	ns
T _{PERIODSS}	100-MHz CPUT and CPUC Period, SSC	Measured at crossing point V _{OX}	9.997001	10.05327	ns
T _{PERIODSS}	133-MHz CPUT and CPUC Period, SSC	Measured at crossing point V _{OX}	7.497751	7.539950	ns
T _{PERIODSS}	166-MHz CPUT and CPUC Period, SSC	Measured at crossing point V _{OX}	5.998201	6.031960	ns
T _{PERIODSS}	200-MHz CPUT and CPUC Period, SSC	Measured at crossing point V _{OX}	4.998500	5.026634	ns
T _{PERIODAbs}	100-MHz CPUT and CPUC Absolute period	Measured at crossing point V _{OX}	9.912001	10.08800	ns
T _{PERIODAbs}	133-MHz CPUT and CPUC Absolute period	Measured at crossing point V _{OX}	7.412751	7.587251	ns
T _{PERIODAbs}	166-MHz CPUT and CPUC Absolute period	Measured at crossing point V _{OX}	5.913201	6.086801	ns
T _{PERIODAbs}	200-MHz CPUT and CPUC Absolute period	Measured at crossing point V _{OX}	4.913500	5.086500	ns
T _{PERIODSSAbs}	100-MHz CPUT and CPUC Absolute period, SSC	Measured at crossing point V _{OX}	9.912001	10.13827	ns
T _{PERIODSSAbs}	133-MHz CPUT and CPUC Absolute period, SSC	Measured at crossing point V _{OX}	7.412751	7.624950	ns
T _{PERIODSSAbs}	166-MHz CPUT and CPUC Absolute period, SSC	Measured at crossing point V _{OX}	5.913201	6.116960	ns
T _{PERIODSSAbs}	200-MHz CPUT and CPUC Absolute period, SSC	Measured at crossing point V _{OX}	4.913500	5.111634	ns
T _{CCJ}	CPUT/C Cycle to Cycle Jitter	Measured at crossing point V _{OX}	–	85 ^[2]	ps
T _{CCJ2}	CPU2_ITP Cycle to Cycle Jitter	Measured at crossing point V _{OX}	–	125 ^[2]	ps
L _{ACC}	Long-term Accuracy	Measured at crossing point V _{OX}	–	300	ppm
T _{SKEW}	CPU1 to CPU0 Clock Skew	Measured at crossing point V _{OX}	–	100	ps
T _{SKEW2}	CPU2_ITP to CPU0 Clock Skew	Measured at crossing point V _{OX}	–	150	ps
T _R / T _F	CPUT and CPUC Rise and Fall Time	Measured from V _{OL} = 0.175 to V _{OH} = 0.525V	175	700	ps
T _{RFM}	Rise/Fall Matching	Determined as a fraction of 2*(T _R – T _F)/(T _R + T _F)	–	20	%
ΔT _R	Rise Time Variation		–	125	ps
ΔT _F	Fall Time Variation		–	125	ps

Note:

2. Measured with one REF on.

AC Electrical Specifications (continued)

Parameter	Description	Condition	Min.	Max.	Unit
V _{HIGH}	Voltage High	Math averages <i>Figure 17</i>	660	850	mV
V _{LOW}	Voltage Low	Math averages <i>Figure 17</i>	–150	–	mV
V _{OX}	Crossing Point Voltage at 0.7V Swing		250	550	mV
V _{OVS}	Maximum Overshoot Voltage		–	V _{HIGH} + 0.3	V
V _{UDS}	Minimum Undershoot Voltage		–0.3	–	V
V _{RB}	Ring Back Voltage	See <i>Figure 17</i> . Measure SE	–	0.2	V
SRC at 0.7V					
T _{DC}	SRCT and SRCC Duty Cycle	Measured at crossing point V _{OX}	45	55	%
T _{PERIOD}	100-MHz SRCT and SRCC Period	Measured at crossing point V _{OX}	9.997001	10.00300	ns
T _{PERIODSS}	100-MHz SRCT and SRCC Period, SSC	Measured at crossing point V _{OX}	9.997001	10.05327	ns
T _{PERIODAbs}	100-MHz SRCT and SRCC Absolute Period	Measured at crossing point V _{OX}	9.872001	10.12800	ns
T _{PERIODSSAbs}	100-MHz SRCT and SRCC Absolute Period, SSC	Measured at crossing point V _{OX}	9.872001	10.17827	ns
T _{SKEW}	Any SRCT/C to SRCT/C Clock Skew	Measured at crossing point V _{OX}	–	250	ps
T _{CCJ}	SRCT/C Cycle to Cycle Jitter	Measured at crossing point V _{OX}	–	125 ^[2]	ps
L _{ACC}	SRCT/C Long Term Accuracy	Measured at crossing point V _{OX}	–	300	ppm
T _R / T _F	SRCT and SRCC Rise and Fall Time	Measured from V _{OL} = 0.175 to V _{OH} = 0.525V	175	800	ps
T _{RFM}	Rise/Fall Matching	Determined as a fraction of 2*(T _R – T _F)/(T _R + T _F)	–	20	%
ΔT _R	Rise Time Variation		–	125	ps
ΔT _F	Fall Time Variation		–	125	ps
V _{HIGH}	Voltage High	Math averages <i>Figure 17</i>	660	850	mV
V _{LOW}	Voltage Low	Math averages <i>Figure 17</i>	–150	–	mV
V _{OX}	Crossing Point Voltage at 0.7V Swing		180	550	mV
V _{OVS}	Maximum Overshoot Voltage		–	V _{HIGH} + 0.3	V
V _{UDS}	Minimum Undershoot Voltage		–0.3	–	V
V _{RB}	Ring Back Voltage	See <i>Figure 17</i> . Measure SE	–	0.2	V
LCD 96_100M_SSC at 0.7V					
T _{DC}	SSCT and SSCC Duty Cycle	Measured at crossing point V _{OX}	45	55	%
T _{PERIOD}	100-MHz SSCT and SSCC Period	Measured at crossing point V _{OX}	9.997001	10.00300	ns
T _{PERIODSS}	100-MHz SSCT and SSCC Period, SSC	Measured at crossing point V _{OX}	9.997001	10.05327	ns
T _{PERIODAbs}	100-MHz SSCT and SSCC Absolute Period	Measured at crossing point V _{OX}	9.872001	10.12800	ns
T _{PERIODSSAbs}	100-MHz SRCT and SRCC Absolute Period, SSC	Measured at crossing point V _{OX}	9.872001	10.17827	ns
T _{PERIOD}	96-MHz SSCT and SSCC Period	Measured at crossing point V _{OX}	10.41354	10.41979	ns
T _{PERIODSS}	96-MHz SSCT and SSCC Period, SSC	Measured at crossing point V _{OX}	10.41354	10.47215	ns
T _{PERIODAbs}	96-MHz SSCT and SSCC Absolute Period	Measured at crossing point V _{OX}	10.16354	10.66979	ns
T _{PERIODSSAbs}	96-MHz SRCT and SRCC Absolute Period, SSC	Measured at crossing point V _{OX}	10.16354	10.72266	ns
T _{CCJ}	SSCT/C Cycle to Cycle Jitter	Measured at crossing point V _{OX}	–	125	ps
L _{ACC}	SSCT/C Long Term Accuracy	Measured at crossing point V _{OX}	–	300	ppm

AC Electrical Specifications (continued)

Parameter	Description	Condition	Min.	Max.	Unit
T_R / T_F	SSCT and SSCC Rise and Fall Time	Measured from $V_{OL} = 0.175$ to $V_{OH} = 0.525V$	175	700	ps
T_{RFM}	Rise/Fall Matching	Determined as a fraction of $2*(T_R - T_F)/(T_R + T_F)$	–	20	%
ΔT_R	Rise Time Variation		–	125	ps
ΔT_F	Fall Time Variation		–	125	ps
V_{HIGH}	Voltage High	Math averages <i>Figure 17</i>	660	850	mV
V_{LOW}	Voltage Low	Math averages <i>Figure 17</i>	–150	–	mV
V_{OX}	Crossing Point Voltage at 0.7V Swing		250	550	mV
V_{OVS}	Maximum Overshoot Voltage		–	$V_{HIGH} + 0.3$	V
V_{UDS}	Minimum Undershoot Voltage		–0.3	–	V
V_{RB}	Ring Back Voltage	See <i>Figure 17</i> . Measure SE	–	0.2	V
PCI/PCIF at 3.3V					
T_{DC}	PCI Duty Cycle	Measurement at 1.5V	45	55	%
T_{PERIOD}	Spread Disabled PCIF/PCI Period	Measurement at 1.5V	29.99100	30.00900	ns
$T_{PERIODSS}$	Spread Enabled PCIF/PCI Period, SSC	Measurement at 1.5V	29.9910	30.15980	ns
$T_{PERIODAbs}$	Spread Disabled PCIF/PCI Period	Measurement at 1.5V	29.49100	30.50900	ns
$T_{PERIODSSAbs}$	Spread Enabled PCIF/PCI Period, SSC	Measurement at 1.5V	29.49100	30.65980	ns
T_{HIGH}	PCIF and PCI high time	Measurement at 2.4V	12.0	–	ns
T_{LOW}	PCIF and PCI low time	Measurement at 0.4V	12.0	–	ns
T_R / T_F	PCIF/PCI rising and falling Edge Rate	Measured between 0.8V and 2.0V	1.0	4.0	V/ns
T_{SKEW}	Any PCI clock to Any PCI clock Skew	Measurement at 1.5V	–	500	ps
T_{CCJ}	PCIF and PCI Cycle to Cycle Jitter	Measurement at 1.5V	–	500	ps
L_{ACC}	PCIF/PCI Long Term Accuracy	Measured at crossing point V_{OX}	–	300	ppm
DOT96 at 0.7V					
T_{DC}	DOT96T and DOT96C Duty Cycle	Measured at crossing point V_{OX}	45	55	%
T_{PERIOD}	DOT96T and DOT96C Period	Measured at crossing point V_{OX}	10.41354	10.41979	ns
$T_{PERIODAbs}$	DOT96T and DOT96C Absolute Period	Measured at crossing point V_{OX}	10.16354	10.66979	ns
T_{CCJ}	DOT96T/C Cycle to Cycle Jitter	Measured at crossing point V_{OX}	–	250	ps
L_{ACC}	DOT96T/C Long Term Accuracy	Measured at crossing point V_{OX}	–	300	ppm
T_R / T_F	DOT96T and DOT96C Rise and Fall Time	Measured from $V_{OL} = 0.175$ to $V_{OH} = 0.525V$	175	900	ps
T_{RFM}	Rise/Fall Matching	Determined as a fraction of $2*(T_R - T_F)/(T_R + T_F)$	–	20	%
ΔT_R	Rise Time Variation		–	125	ps
ΔT_F	Fall Time Variation		–	125	ps
V_{HIGH}	Voltage High	Math averages <i>Figure 17</i>	660	850	mV
V_{LOW}	Voltage Low	Math averages <i>Figure 17</i>	–150	–	mV
V_{OX}	Crossing Point Voltage at 0.7V Swing		250	550	mV
V_{OVS}	Maximum Overshoot Voltage		–	$V_{HIGH} + 0.3$	V
V_{UDS}	Minimum Undershoot Voltage		–0.3	–	V
V_{RB}	Ring Back Voltage	See <i>Figure 17</i> . Measure SE	–	0.2	V
48_M at 3.3V					
T_{DC}	Duty Cycle	Measurement at 1.5V	45	55	%

AC Electrical Specifications (continued)

Parameter	Description	Condition	Min.	Max.	Unit
T _{PERIOD}	Period	Measurement at 1.5V	20.83125	20.83542	ns
T _{PERIODAbs}	Absolute Period	Measurement at 1.5V	20.48125	21.18542	ns
T _{HIGH}	48_M High time	Measurement at 2.4V	8.094	11.100	ns
T _{LOW}	48_M Low time	Measurement at 0.4V	7.694	11.100	ns
T _R / T _F	Rising and Falling Edge Rate	Measured between 0.8V and 2.0V	1.0	2.0	V/ns
T _{CCJ}	Cycle to Cycle Jitter	Measurement at 1.5V	–	350	ps
L _{ACC}	48M Long Term Accuracy	Measured at crossing point V _{OX}	–	100	ppm
27_M at 3.3V					
T _{DC}	Duty Cycle	Measurement at 1.5V	45	55	%
T _{PERIOD}	Spread Disabled 27M Period	Measurement at 1.5V	27.000	27.0547	ns
	Spread Enabled 27M Period	Measurement at 1.5V	27.000	27.0547	
T _{HIGH}	27_M High time	Measurement at 2.0V	10.5	–	ns
T _{LOW}	27_M Low time	Measurement at 0.8V	10.5	–	ns
T _R / T _F	Rising and Falling Edge Rate	Measured between 0.8V and 2.0V	1.0	4.0	V/ns
T _{CCJ}	Cycle to Cycle Jitter	Measurement at 1.5V	–	500	ps
L _{ACC}	27_M Long Term Accuracy	Measured at crossing point V _{OX}	–	0	ppm
REF at 3.3V					
T _{DC}	REF Duty Cycle	Measurement at 1.5V	45	55	%
T _{PERIOD}	REF Period	Measurement at 1.5V	69.8203	69.8622	ns
T _{PERIODAbs}	REF Absolute Period	Measurement at 1.5V	68.82033	70.86224	ns
T _R / T _F	REF Rising and Falling Edge Rate	Measured between 0.8V and 2.0V	1.0	4.0	V/ns
T _{SKEW}	REF Clock to REF Clock	Measurement at 1.5V	–	500	ps
T _{CCJ}	REF Cycle to Cycle Jitter	Measurement at 1.5V	–	1000	ps
L _{ACC}	Long Term Accuracy	Measurement at 1.5V	–	300	ppm
ENABLE/DISABLE and SET-UP					
T _{STABLE}	Clock Stabilization from Power-up		–	1.8	ms
T _{SS}	Stopclock Set-up Time		10.0	–	ns
T _{SH}	Stopclock Hold Time		0	–	ns

Test and Measurement Set-up

For Single-ended Signals and Reference

The following diagram shows test load configurations for the single-ended PCI, USB, and REF output signals.

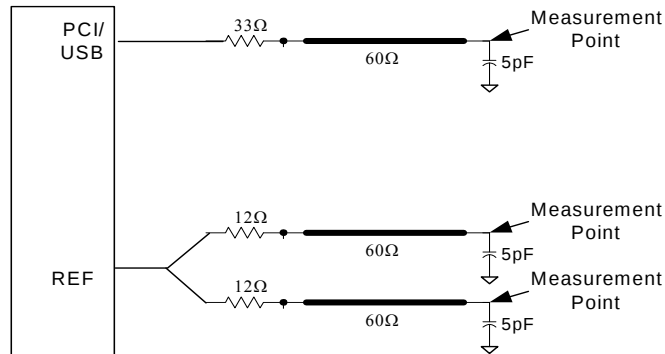


Figure 15. Single-ended Load Configuration Low Drive Option

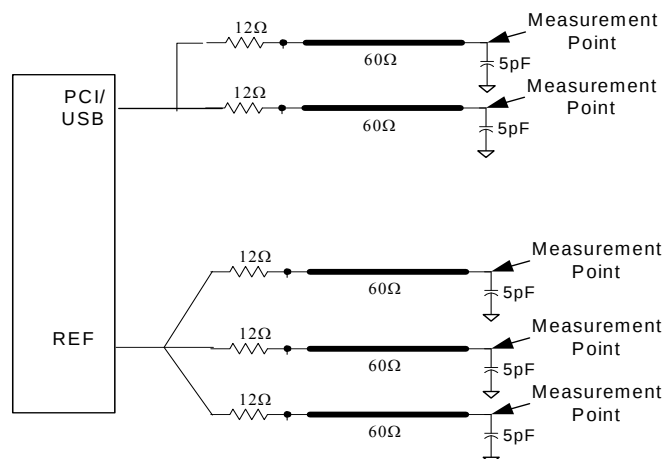


Figure 16. Single-ended Load Configuration High Drive Option

The following diagram shows the test load configuration for the differential CPU and SRC outputs.

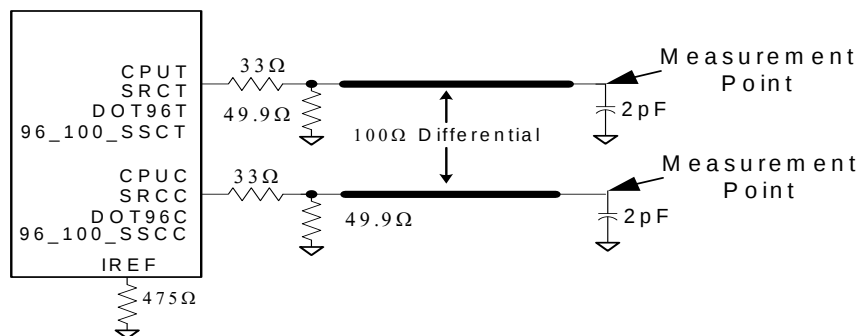


Figure 17. 0.7V Differential Load Configuration

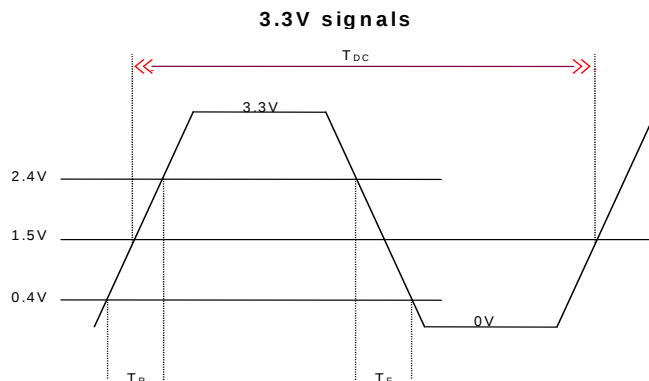


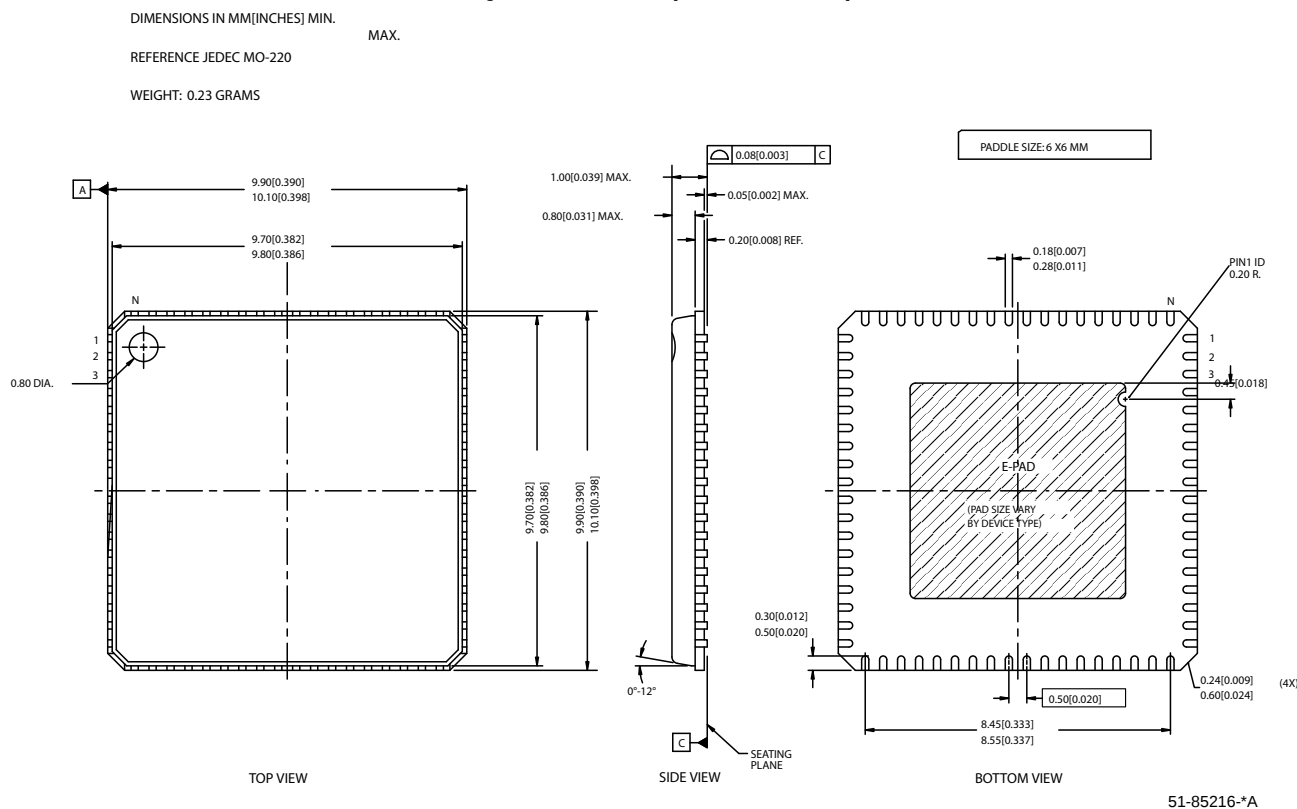
Figure 18. Single-ended Output Signals (for AC Parameters Measurement)

Ordering Information

Part Number	Package Type	Product Flow
Lead-free		
CY28447LFXC	72-pin QFN	Commercial, 0° to 85°C
CY28447LFXCT	72-pin QFN – Tape and Reel	Commercial, 0° to 85°C

Package Diagram

72-Lead QFN 10 x 10 mm (Punch Version) LF72A



Document History Page

Document Title: CY28447 Clock Generator for Intel® Calistoga Chipset Document Number: 38-07724				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	315554	See ECN	RGL	New data sheet
*A	345509	See ECN	RGL	Changed VTTWVRGD#/PD changed from PU to PD. Change Advance to Preliminary status
*B	381616	See ECN	RGL	Modify pin description table Update register table Modify AC specification of 27-MHz L _{ACC} to 0 ppm
*C	391400	See ECN	RGL	Update block diagram to show the 4th PLL Add Figure 15 and 16 for single-ended load configuration Update DC Electrical Specification table Update AC Electrical Specification table



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