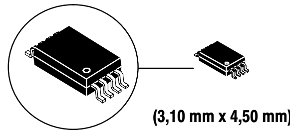


AUTOSWITCHING POWER MULTIPLEXER

FEATURES

- **Two-Input, One-Output Power Multiplexer With Low $r_{DS(on)}$ Switches:**
  - **84 mΩ Typ (TPS2115)**
  - **120 mΩ Typ (TPS2114)**
- **Reverse and Cross-Conduction Blocking**
- **Wide Operating Voltage Range: 2.8 V to 5.5 V**
- **Low Standby Current: 0.5 μA Typical**
- **Low Operating Current: 55 μA Typical**
- **Adjustable Current Limit**
- **Controlled Output Voltage Transition Times, Limits Inrush Current and Minimizes Output Voltage Hold-Up Capacitance**
- **CMOS and TTL Compatible Control Inputs**
- **Manual and Auto-Switching Operating Modes**
- **Thermal Shutdown**
- **Available in a TSSOP-8 Package**

APPLICATIONS

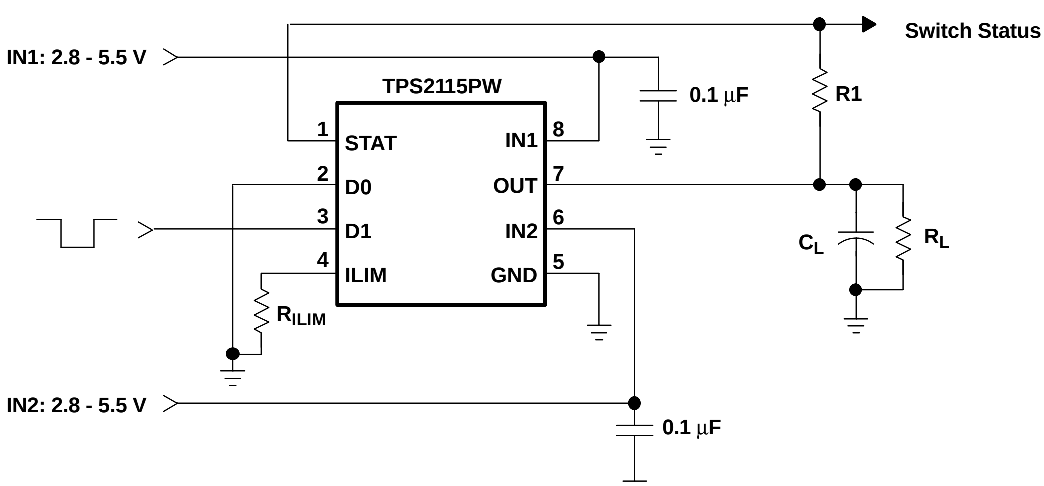
- **PCs**
- **PDAs**
- **Digital Cameras**
- **Modems**
- **Cell phones**
- **Digital Radios**
- **MP3 Players**

PW PACKAGE
(TOP VIEW)

DESCRIPTION

The TPS211x family of power multiplexers enables seamless transition between two power supplies, such as a battery and a wall adapter, each operating at 2.8-5.5 V and delivering up to 1 A. The TPS211x family includes extensive protection circuitry, including user-programmable current limiting, thermal protection, inrush current control, seamless supply transition, cross-conduction blocking, and reverse-conduction blocking. These features greatly simplify designing power multiplexer applications.

TYPICAL APPLICATION



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

AVAILABLE OPTIONS

FEATURE		TPS2110	TPS2111	TPS2112	TPS2113	TPS2114	TPS2115
Current limit adjustment range		0.31-0.75A	0.63-1.25A	0.31-0.75A	0.63-1.25A	0.31-0.75A	0.63-1.25A
Switching modes	Manual	Yes	Yes	No	No	Yes	Yes
	Automatic	Yes	Yes	Yes	Yes	Yes	Yes
Switch status output		No	No	Yes	Yes	Yes	Yes
Package		TSSOP-8	TSSOP-8	TSSOP-8	TSSOP-8	TSSOP-8	TSSOP-8

ORDERING INFORMATION

T_A	PACKAGE	ORDERING NUMBER(1)	MARKINGS
-40°C to 85°C	TSSOP-8 (PW)	TPS2114PW	2114
		TPS2115PW	2115

(1) The PW package is available taped and reeled. Add an R suffix to the device type (e.g., TPS2114PWR) to indicate tape and reel.

PACKAGE DISSIPATION RATINGS

PACKAGE	DERATING FACTOR ABOVE T_A = 25°C	$T_A \leq$ 25°C POWER RATING	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING
TSSOP-8 (PW)	3.87 mW/°C	386.84 mW	212.76 mW	154.73 mW

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

			TPS2114, TPS2115
V_I	Input voltage range	IN1, IN2, D0, D1, ILIM(2)	-0.3 V to 6 V
V_O	Output voltage range(2)	OUT, STAT	-0.3 V to 6 V
I_O	Output sink current	STAT	5 mA
I_O	Continuous output current	TPS2114	0.9 A
		TPS2115	1.5 A
	Continuous total power dissipation		See Dissipation Rating Table
T_J	Operating virtual junction temperature range		-40°C to 125°C
T_{stg}	Storage temperature range		-65°C to 150°C
	Lead temperature soldering 1,6 mm (1/16 inch) from case for 10 seconds		260°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to GND.

RECOMMENDED OPERATING CONDITIONS

			MIN	MAX	UNIT
V_I	Input voltage at IN1	$V_{I(IN2)} \geq 2.8$ V	1.5	5.5	V
		$V_{I(IN2)} < 2.8$ V	2.8	5.5	
V_I	Input voltage at IN2	$V_{I(IN1)} \geq 2.8$ V	1.5	5.5	V
		$V_{I(IN1)} < 2.8$ V	2.8	5.5	
V_I	Input voltage at D0, D1		0	5.5	V
$I_{O(OUT)}$	Current limit adjustment range	TPS2114	0.31	0.75	A
		TPS2115	0.63	1.25	
T_J	Operating virtual junction temperature		-40	125	°C

ELECTROSTATIC DISCHARGE (ESD) PROTECTION

	MIN	MAX	UNIT
Human body model		2	kV
CDM		500	V

ELECTRICAL CHARACTERISTICS

over recommended operating junction temperature range, $V_{I(IN1)} = V_{I(IN2)} = 5.5$ V, $R_{(ILIM)} = 400\ \Omega$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		TPS2114			TPS2115			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
POWER SWITCH										
$r_{DS(on)}$ [(1)]	Drain-source on-state resistance (INx-OUT)	$T_J = 25°C$, $I_L = 500$ mA	$V_{I(IN1)} = V_{I(IN2)} = 5.0$ V		120	140		84	110	mΩ
			$V_{I(IN1)} = V_{I(IN2)} = 3.3$ V		120	140		84	110	
			$V_{I(IN1)} = V_{I(IN2)} = 2.8$ V		120	140		84	110	
		$T_J = 125°C$, $I_L = 500$ mA	$V_{I(IN1)} = V_{I(IN2)} = 5.0$ V			220			150	mΩ
			$V_{I(IN1)} = V_{I(IN2)} = 3.3$ V			220			150	
			$V_{I(IN1)} = V_{I(IN2)} = 2.8$ V			220			150	

(1) The TPS211x can switch a voltage as low as 1.5 V as long as there is a minimum of 2.8 V at one of the input power pins. In this specific case, the lower supply voltge has no effect on the IN1 and IN2 switch on-resistances.

ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	TPS2115 MIN	TPS2115 TYP	TPS2115 MAX	UNIT
LOGIC INPUTS (D0 AND D1)							
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.7	V
	Input current at D0 or D1		D0 or D1 = High, sink current			1	µA
			D0 or D1 = Low, source current	0.5	1.4	5	
SUPPLY AND LEAKAGE CURRENTS							
Supply current from IN1 (operating)			D1 = High, D0 = Low (IN1 active), $V_{I(IN1)}$ = 5.5 V, $V_{I(IN2)}$ = 3.3 V, $I_{O(OUT)}$ = 0 A		55	90	µA
			D1 = High, D0 = Low (IN1 active), $V_{I(IN1)}$ = 3.3 V, $V_{I(IN2)}$ = 5.5 V, $I_{O(OUT)}$ = 0 A		1	12	
			D0 = D1 = Low (IN2 active), $V_{I(IN1)}$ = 5.5 V, $V_{I(IN2)}$ = 3.3 V, $I_{O(OUT)}$ = 0 A			75	
			D0 = D1 = Low (IN2 active), $V_{I(IN1)}$ = 3.3 V, $V_{I(IN2)}$ = 5.5 V, $I_{O(OUT)}$ = 0 A			1	
Supply current from IN2 (operating)			D1 = High, D0 = Low (IN1 active), $V_{I(IN1)}$ = 5.5 V, $V_{I(IN2)}$ = 3.3 V, $I_{O(OUT)}$ = 0 A			1	µA
			D1 = High, D0 = Low (IN1 active), $V_{I(IN1)}$ = 3.3 V, $V_{I(IN2)}$ = 5.5 V, $I_{O(OUT)}$ = 0 A			75	
			D0 = D1 = Low (IN2 active), $V_{I(IN1)}$ = 5.5 V, $V_{I(IN2)}$= 3.3 V, $I_{O(OUT)}$ = 0 A		1	12	
			D0 = D1 = Low (IN2 active), $V_{I(IN1)}$ = 3.3 V, $V_{I(IN2)}$ = 5.5 V, $I_{O(OUT)}$ = 0 A		55	90	
Quiescent current from IN1 (STANDBY)			D0 = D1 = High (inactive), $V_{I(IN1)}$ = 5.5 V, $V_{I(IN2)}$ = 3.3 V, $I_{O(OUT)}$ = 0 A		0.5	2	µA
			D0 = D1 = High (inactive), $V_{I(IN1)}$ = 3.3 V, $V_{I(IN2)}$ = 5.5 V, $I_{O(OUT)}$ = 0 A			1	
Quiescent current from IN2 (STANDBY)			D0 = D1 = High (inactive), $V_{I(IN1)}$ = 5.5 V, $V_{I(IN2)}$ = 3.3 V, $I_{O(OUT)}$ = 0 A			1	µA
			D0 = D1 = High (inactive), $V_{I(IN1)}$ = 3.3 V, $V_{I(IN2)}$ = 5.5 V, $I_{O(OUT)}$ = 0 A		0.5	2	
Forward leakage current from IN1 (measured from OUT to GND)			D0 = D1 = High (inactive), $V_{I(IN1)}$ = 5.5 V, IN2 open, $V_{O(OUT)}$ = 0 V (shorted), T_J = 25°C		0.1	5	µA
Forward leakage current from IN2 (measured from OUT to GND)			D0 = D1= High (inactive), $V_{I(IN2)}$ = 5.5 V, IN1 open, $V_{O(OUT)}$= 0 V (shorted), T_J = 25°C		0.1	5	µA
Reverse leakage current to INx (measured from INx to GND)			D0 = D1 = High (inactive), $V_{I(INx)}$ = 0 V, $V_{O(OUT)}$ = 5.5 V, T_J = 25°C		0.3	5	µA
CURRENT LIMIT CIRCUIT							
Current limit accuracy		TPS2114	$R_{(ILIM)}$ = 400 Ω	0.51	0.63	0.80	A
			$R_{(ILIM)}$ = 700 Ω	0.30	0.36	0.50	
		TPS2115	$R_{(ILIM)}$ = 400 Ω	0.95	1.25	1.56	
			$R_{(ILIM)}$ = 700 Ω	0.47	0.71	0.99	
t_d	Current limit settling time(1)		Time for short-circuit output current to settle within 10% of its steady state value.		1		ms
	Input current at ILIM		$V_{I(ILIM)}$ = 0 V, $I_{O(OUT)}$ = 0 A	-15		0	µA

(1) Not tested in production.

ELECTRICAL CHARACTERISTICS (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TPS2115			UNIT
			MIN	TYP	MAX	
UNDERVOLTAGE LOCKOUT						
IN1 and IN2 UVLO		Falling edge	1.15	1.25		V
		Rising edge		1.30	1.35	
IN1 and IN2 UVLO hysteresis(2)			30	57	65	mV
Internal V_{DD} UVLO (the higher of IN1 and IN2)		Falling edge	24	2.53		V
		Rising edge		2.58	2.8	
Internal V_{DD} UVLO hysteresis(2)			30	50	75	mV
UVLO deglitch for IN1, IN2(2)		Falling edge		110		μs
REVERSE CONDUCTION BLOCKING						
$\Delta V_{O(I\_block)}$	Minimum output-to-input voltage difference to block switching	D0 = D1 = high, $V_{I(INx)}$ = 3.3 V. Connect OUT to a 5 V supply through a series 1-kΩ resistor. Let D0 = low. Slowly decrease the supply voltage until OUT connects to IN1.	80	100	120	mV
THERMAL SHUTDOWN						
Thermal shutdown threshold(2)		TPS211x is in current limit.	135			°C
Recovery from thermal shutdown(2)		TPS211x is in current limit.	125			
Hysteresis(2)				10		
IN2-IN1 COMPARATORS						
Hysteresis of IN2-IN1 comparator			0.1		0.2	V
Deglitch of IN2-IN1 comparator, (both↑↓)(2)			90	150	220	μs
STAT OUTPUT						
Leakage current		$V_{O(STAT)}$ = 5.5 V		0.01	1	μA
Saturation voltage		$I_{I(STAT)}$ = 2 mA, IN1 switch is on		0.13	0.4	V
Deglitch time (falling edge only)				150		μs

(2) Not tested in production.

SWITCHING CHARACTERISTICS

over recommended operating junction temperature range, $V_{I(IN1)} = V_{I(IN2)} = 5.5$ V, $R_{(ILIM)} = 400\ \Omega$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		TPS2114			TPS2115			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
POWER SWITCH										
t_r	Output rise time from an enable (1)	$V_{I(IN1)} = V_{I(IN2)} = 5$ V	$T_J = 25°C$, $C_L = 1\ \mu F$, $I_L = 500$ mA, See Figure 1(a)	0.5	1.0	1.5	1	1.8	3	ms
t_f	Output fall time from a disable (1)	$V_{I(IN1)} = V_{I(IN2)} = 5$ V	$T_J = 25°C$, $C_L = 1\ \mu F$, $I_L = 500$ mA, See Figure 1(a)	0.35	0.5	0.7	0.5	1	2	ms
t_t	Transition time (1)	IN1 to IN2 transition, $V_{I(IN1)} = 3.3$ V, $V_{I(IN2)} = 5$ V	$T_J = 125°C$, $C_L = 10\ \mu F$, $I_L = 500$ mA [Measure transition time as 10-90% rise time or from 3.4 V to 4.8 V on $V_{O(OUT)}$], See Figure 1(b)		40	60		40	60	µs
		IN2 to IN1 transition, $V_{I(IN1)} = 5$ V, $V_{I(IN2)} = 3.3$ V			40	60		40	60	
t_{PLH1}	Turnon propagation delay from enable (1)	$V_{I(IN1)} = V_{I(IN2)} = 5$ V, Measured from enable to 10% of $V_{O(OUT)}$	$T_J = 25°C$, $C_L = 10\ \mu F$, $I_L = 500$ mA, SeeFigure 1(a)		0.5			1		ms
t_{PHL1}	Turnoff propagation delay from a disable (1)	$V_{I(IN1)} = V_{I(IN2)} = 5$ V, Measured from disable to 90% of $V_{O(OUT)}$	$T_J = 25°C$, $C_L = 10\ \mu F$, $I_L = 500$ mA, See Figure 1(a)		3			5		ms
t_{PLH2}	Switch-over rising propagation delay (1)	Logic 1 to Logic 0 transition on D1, $V_{I(IN1)} = 1.5$ V, $V_{I(IN2)} = 5$ V, $V_{I(D0)} = 0$ V, Measured from D1 to 10% of $V_{O(OUT)}$	$T_J = 25°C$, $C_L = 10\ \mu F$, $I_L = 500$ mA, See Figure 1(c)		0.17	1		0.17	1	ms
t_{PHL2}	Switch-over falling propagation delay (1)	Logic 0 to Logic 1 transition on D1, $V_{I(IN1)} = 1.5$ V, $V_{I(IN2)} = 5$V, $V_{I(D0)} = 0$ V, Measured from D1 to 90% of $V_{O(OUT)}$	$T_J = 25°C$, $C_L = 10\ \mu F$, $I_L = 500$ mA, See Figure 1(c)	2	3	10	2	5	10	ms

(1) Not tested in production.

TRUTH TABLE

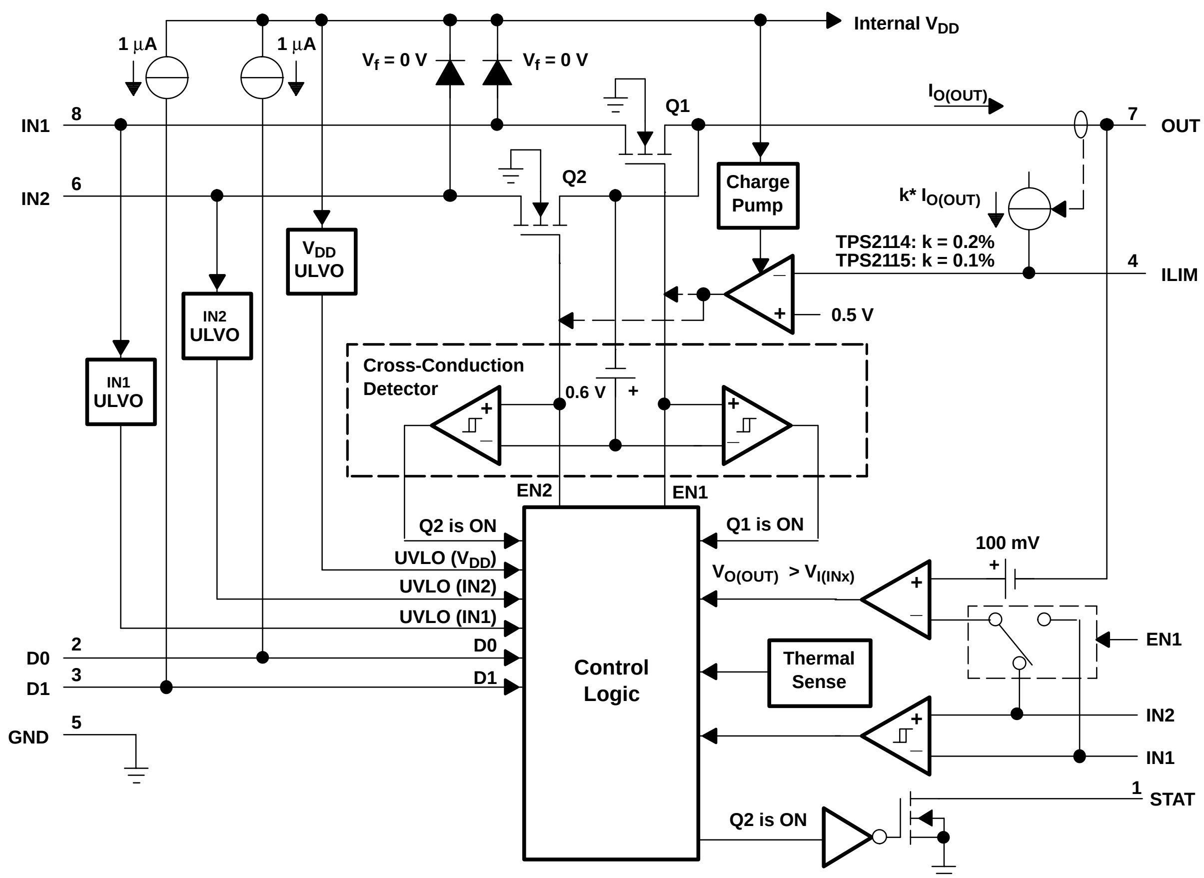
D1	D0	$V_{I(IN2)} > V_{I(IN1)}$	STAT	OUT (1)
0	0	X	Hi-Z	IN2
0	1	No	0	IN1
0	1	Yes	Hi-Z	IN2
1	0	X	0	IN1
1	1	X	0	Hi-Z

(1) The under-voltage lockout circuit causes the output OUT to go Hi-Z if the selected power supply does not exceed the IN1/IN2 UVLO, or if neither of the supplies exceeds the internal V_{DD} UVLO.

Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
D0	2	I	TTL and CMOS compatible input pins. Each pin has a 1-µA pullup resistor. The truth table shown above illustrates the functionality of D0 and D1.
D1	3	I	
GND	5	I	Ground
IN1	8	I	Primary power switch input. The IN1 switch can be enabled only if the IN1 supply is above the UVLO threshold and at least one supply exceeds the internal V_{DD} UVLO.
IN2	6	I	Secondary power switch input. The IN2 switch can be enabled only if the IN2 supply is above the UVLO threshold and at least one supply exceeds the internal V_{DD} UVLO.
ILIM	4	I	A resistor $R_{(ILIM)}$ from ILIM to GND sets the current limit I_L to $250/R_{(ILIM)}$ and $500/R_{(ILIM)}$ for the TPS2114 and TPS2115, respectively.
OUT	7	O	Power switch output
STAT	1	O	STAT is an open-drain output that is Hi-Z if the IN2 switch is ON. STAT pulls low if the IN1 switch is ON or if OUT is Hi-Z (i.e., $\overline{EN}$ is equal to logic 0).

FUNCTIONAL BLOCK DIAGRAM



PARAMETER MEASUREMENT INFORMATION

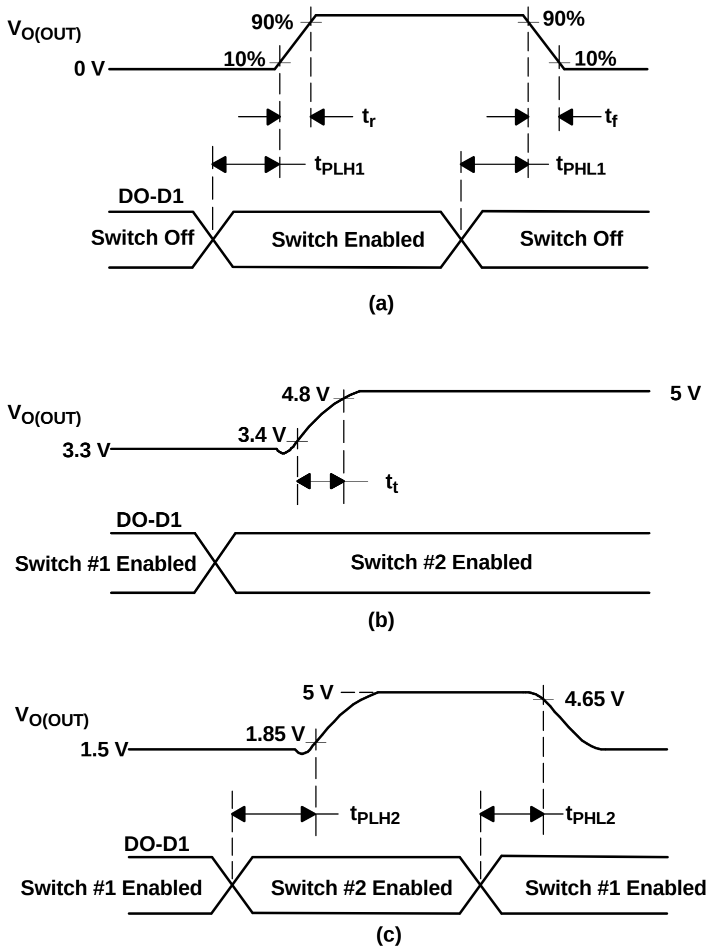
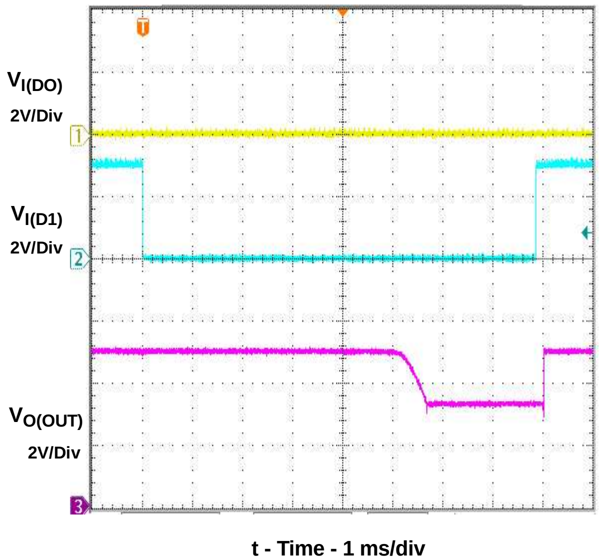
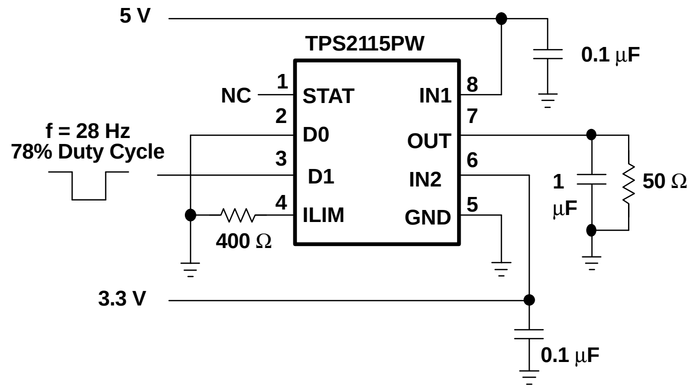


Figure 1. Propagation Delays and Transition Timing Waveforms

TYPICAL CHARACTERISTICS

OUTPUT SWITCHOVER RESPONSE

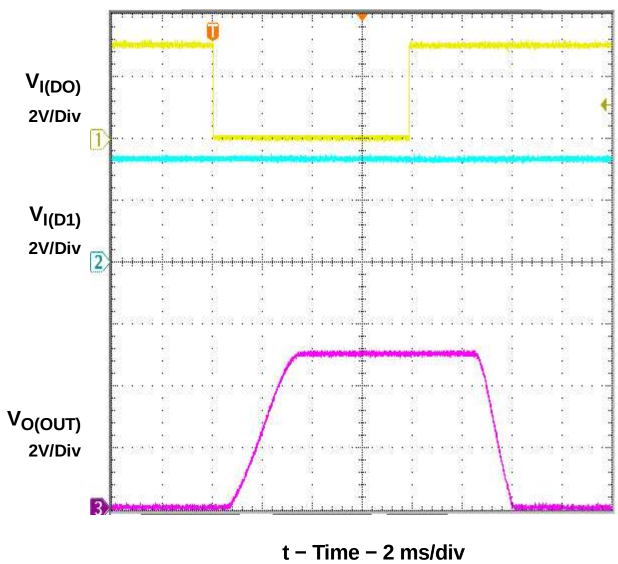


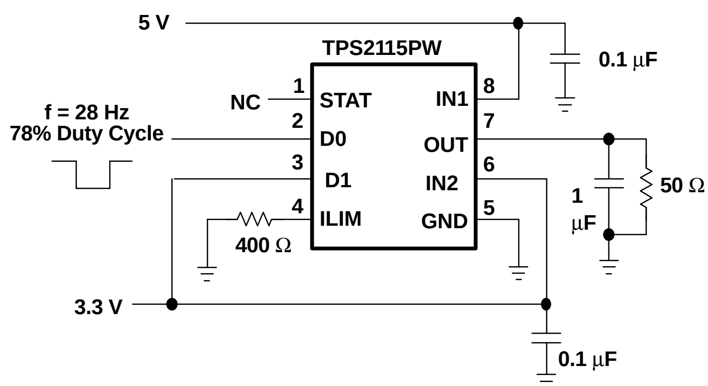


Output Switchover Response Test Circuit

Figure 2.

OUTPUT TURNON RESPONSE



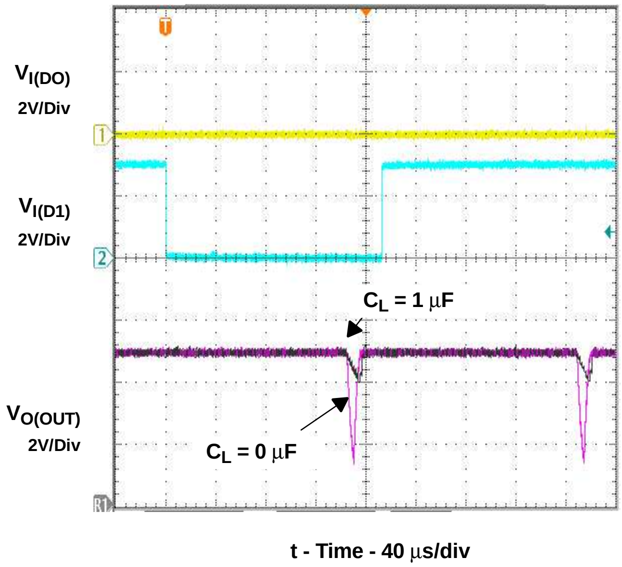


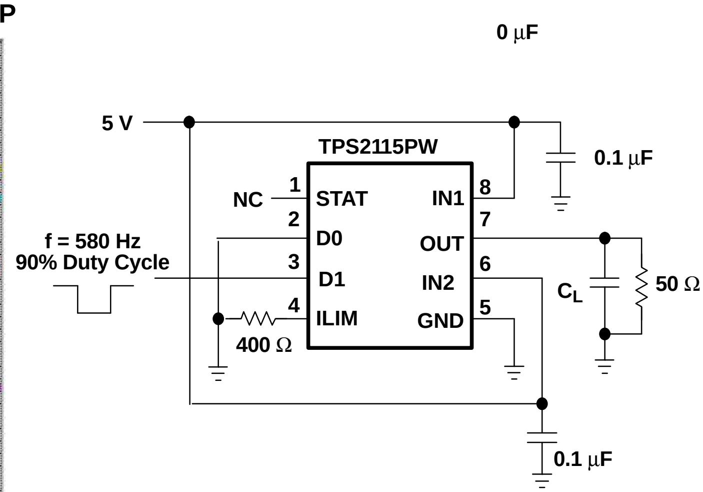
Output Turnon Response Test Circuit

Figure 3.

TYPICAL CHARACTERISTICS (continued)

OUTPUT SWITCHOVER VOLTAGE DROOP



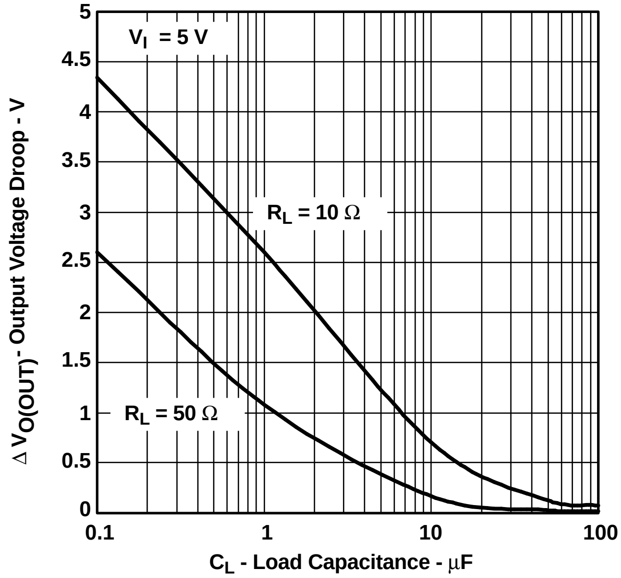


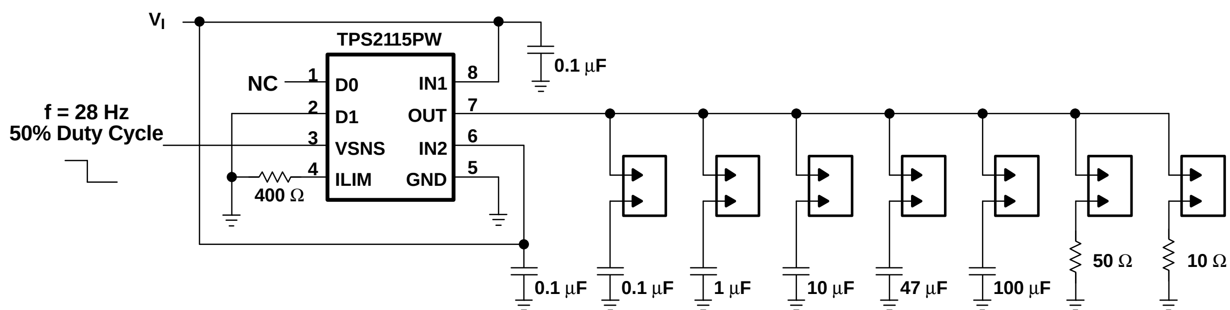
Output Switchover Voltage Droop Test Circuit

Figure 4.

TYPICAL CHARACTERISTICS (continued)

OUTPUT SWITCHOVER VOLTAGE DROOP vs LOAD CAPACITANCE

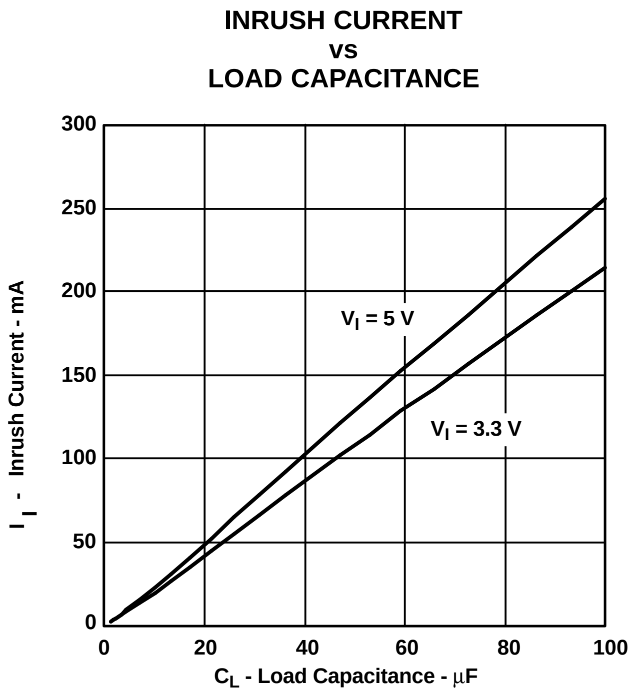


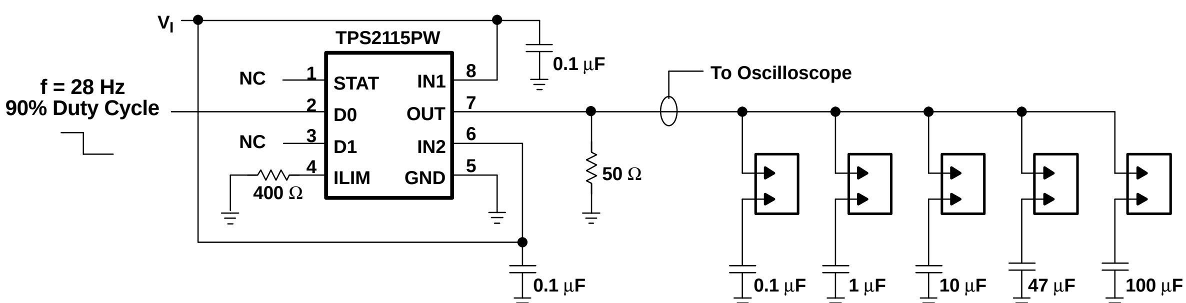


Output Switchover Voltage Droop Test Circuit

Figure 5.

TYPICAL CHARACTERISTICS (continued)





Output Capacitor Inrush Current Test Circuit

Figure 6.

TYPICAL CHARACTERISTICS (continued)

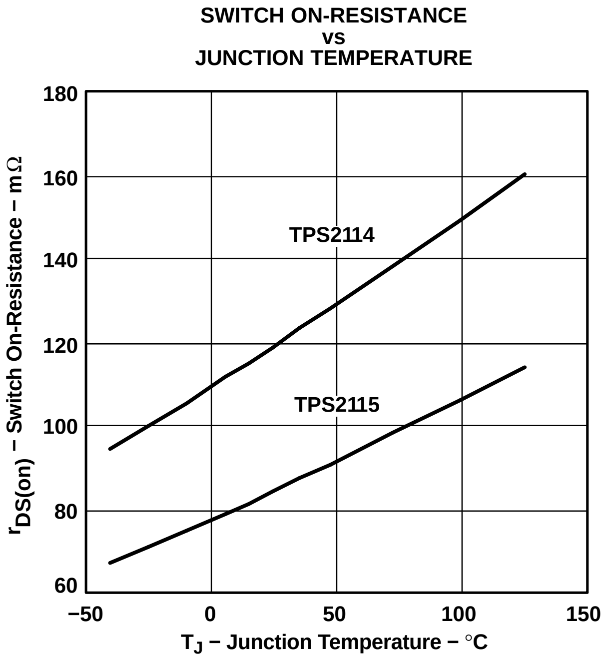


Figure 7.

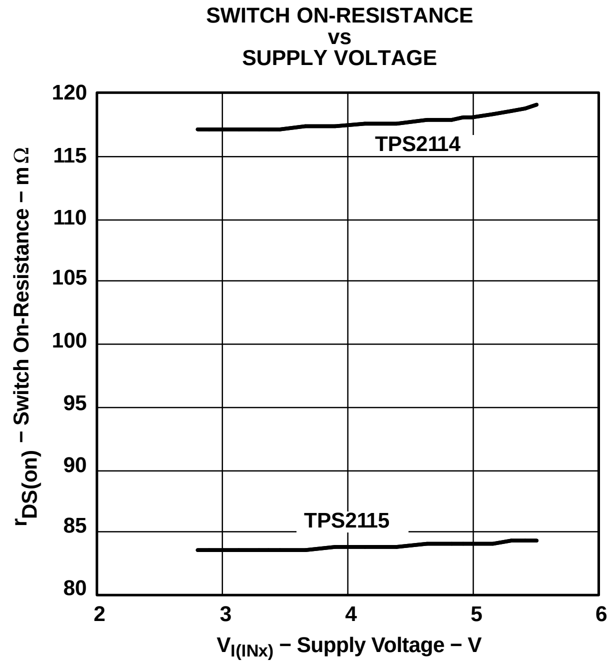


Figure 8.

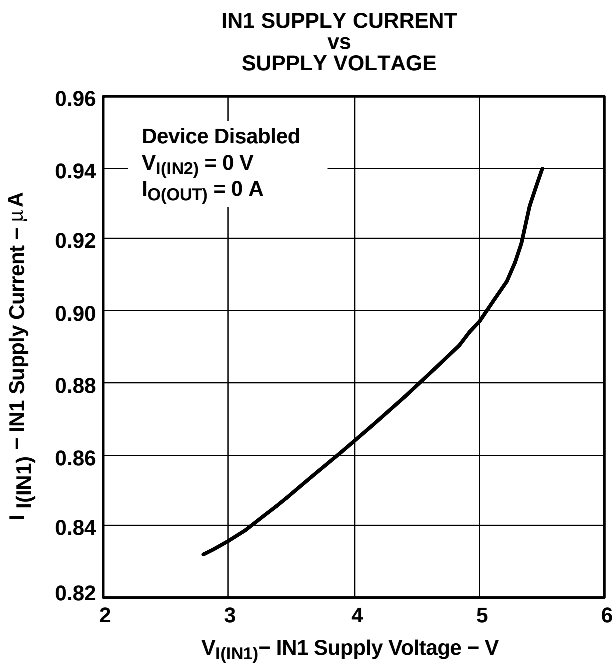


Figure 9.

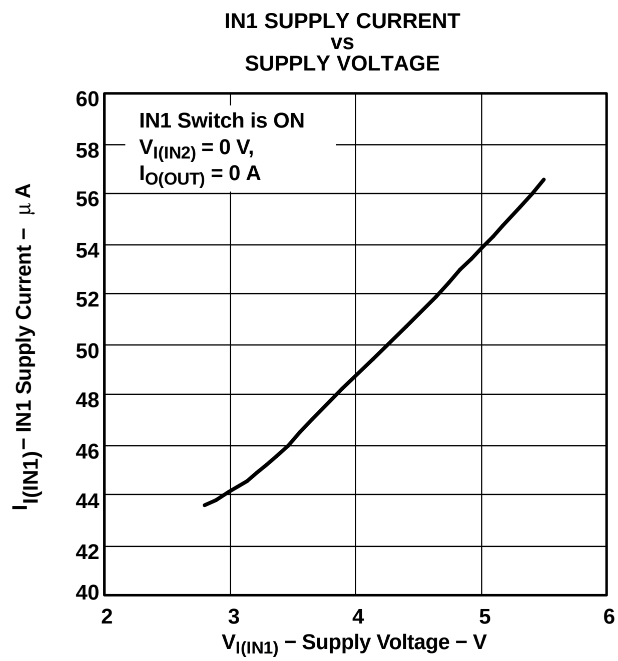


Figure 10.

TYPICAL CHARACTERISTICS (continued)

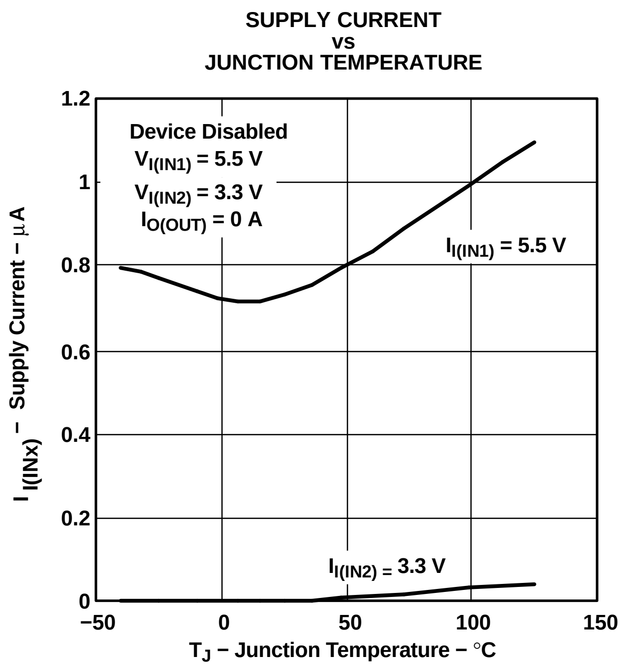


Figure 11.

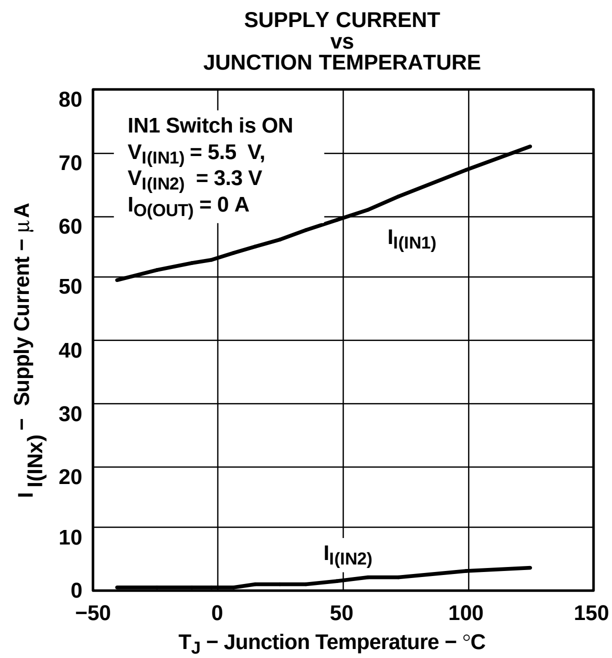


Figure 12.

APPLICATION INFORMATION

The circuit in Figure 13 allows one or two battery packs to power a system. Two battery packs allow a longer run time. The TPS2114/5 cycles between the battery packs until both packs are drained.

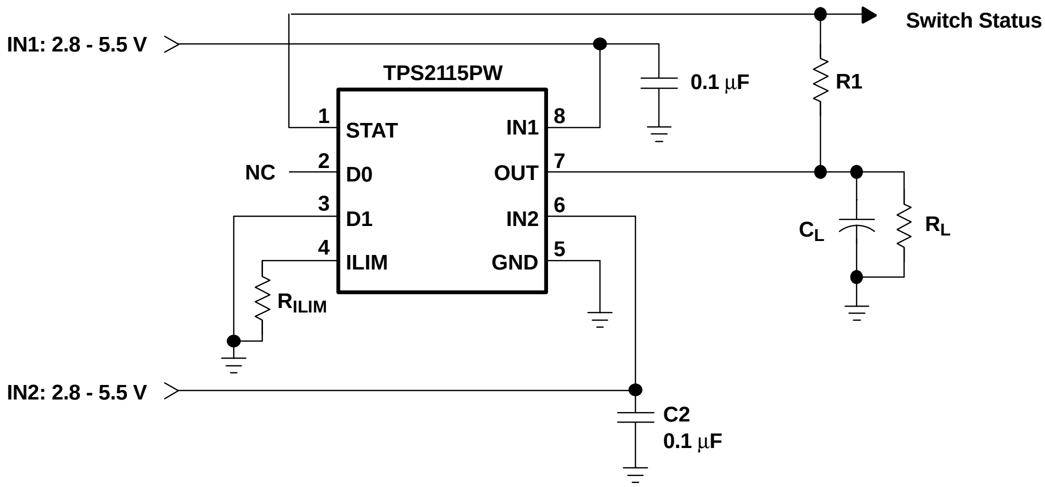


Figure 13. Running a System From Two Battery Packs

In Figure 14, the multiplexer selects between two power supplies based upon the D1 logic signal. OUT connects to IN1 if D1 is logic 1, otherwise OUT connects to IN2. The logic thresholds for the D1 terminal are compatible with both TTL and CMOS logic.

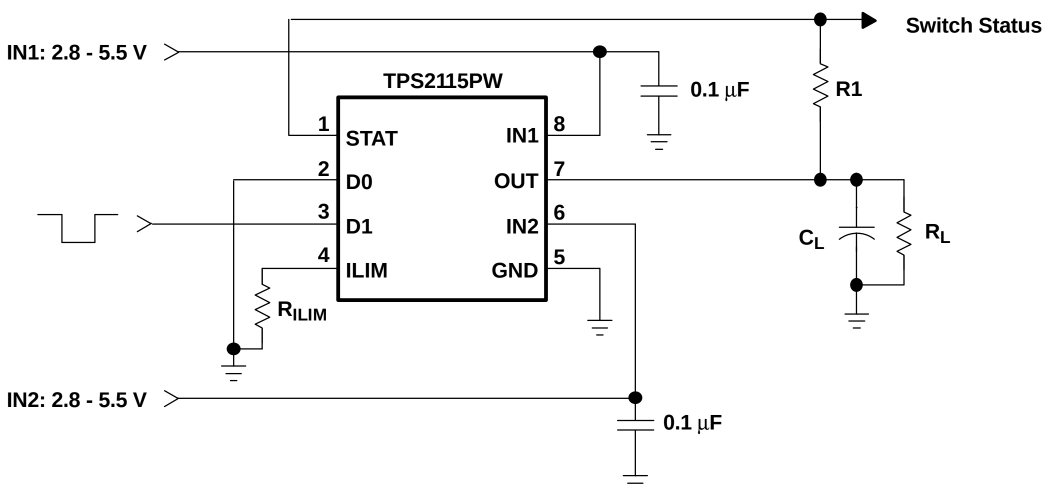


Figure 14. Manually Switching Power Sources

DETAILED DESCRIPTION

AUTO-SWITCHING MODE

D0 equal to logic 1 and D1 equal to logic 0 selects the auto-switching mode. In this mode, OUT connects to the higher of IN1 and IN2.

MANUAL SWITCHING MODE

D0 equal to logic 0 selects the manual-switching mode. In this mode, OUT connects to IN1 if D1 is equal to logic 1, otherwise OUT connects to IN2.

N-CHANNEL MOSFETs

Two internal high-side power MOSFETs implement a single-pole double-throw (SPDT) switch. Digital logic selects the IN1 switch, IN2 switch, or no switch (Hi-Z state). The MOSFETs have no parallel diodes so output-to-input current cannot flow when the FET is off. An integrated comparator prevents turnon of a FET switch if the output voltage is greater than the input voltage.

CROSS-CONDUCTION BLOCKING

The switching circuitry ensures that both power switches never conduct at the same time. A comparator monitors the gate-to-source voltage of each power FET and allows a FET to turn on only if the gate-to-source voltage of the other FET is below the turnon threshold voltage.

REVERSE-CONDUCTION BLOCKING

When the TPS211x switches from a higher-voltage supply to a lower-voltage supply, current can potentially flow back from the load capacitor into the lower-voltage supply. To minimize such reverse conduction, the TPS211x does not connect a supply to the output until the output voltage has fallen to within 100 mV of the supply voltage. Once a supply has been connected to the output, it remains connected regardless of output voltage.

CHARGE PUMP

The higher of supplies IN1 and IN2 powers the internal charge pump. The charge pump provides power to the current limit amplifier and allows the output FET gate voltage to be higher than the IN1 and IN2 supply voltages. A gate voltage that is higher than the source voltage is necessary to turn on the N-channel FET.

CURRENT LIMITING

A resistor $R_{(ILIM)}$ from ILIM to GND sets the current limit to 250/ $R_{(ILIM)}$ and 500/$R_{(ILIM)}$ for the TPS2114 and TPS2115, respectively. Setting resistor $R_{(ILIM)}$ equal to zero is not recommended as that disables current limiting.

OUTPUT VOLTAGE SLEW-RATE CONTROL

The TPS2114/5 slews the output voltage at a slow rate when OUT switches to IN1 or IN2 from the Hi-Z state (see *Truth Table*). A slow slew rate limits the inrush current into the load capacitor. High inrush currents can adversely effect the voltage bus and cause a system to hang up or reset. It can also cause reliability issues—like pit the connector power contacts, when hot plugging a load like a PCI card. The TPS2114/5 slews the output voltage at a much faster rate when OUT switches between IN1 and IN2. The fast rate minimizes the output voltage droop and reduces the output voltage hold-up capacitance requirement.

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
TPS2114PW	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS2114PWG4	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS2114PWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS2114PWRG4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS2115PW	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS2115PWG4	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS2115PWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS2115PWRG4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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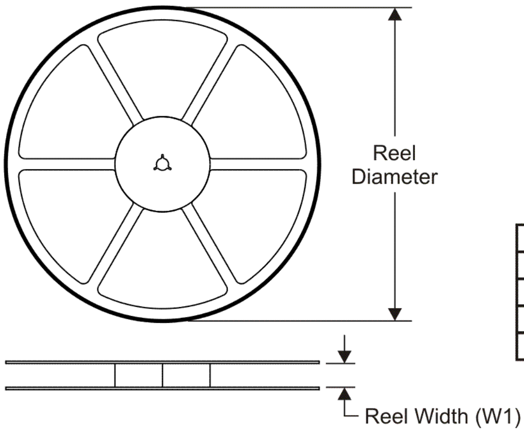
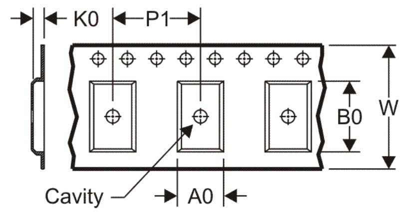
TAPE AND REEL INFORMATION

REEL DIMENSIONS

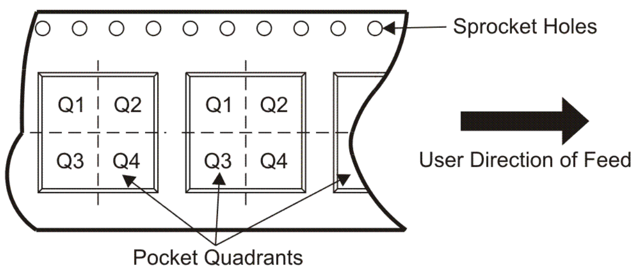


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

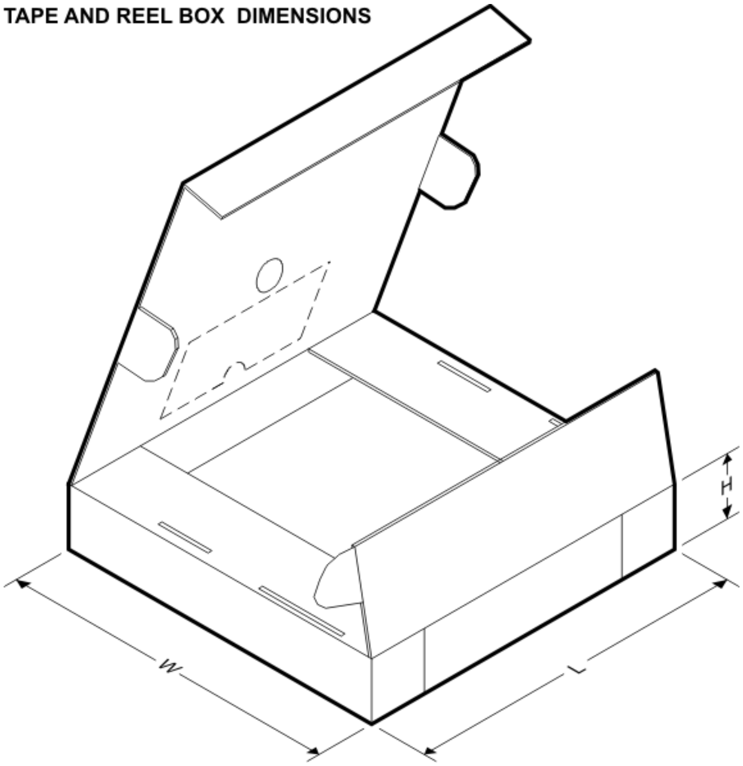
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS2114PWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TPS2115PWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

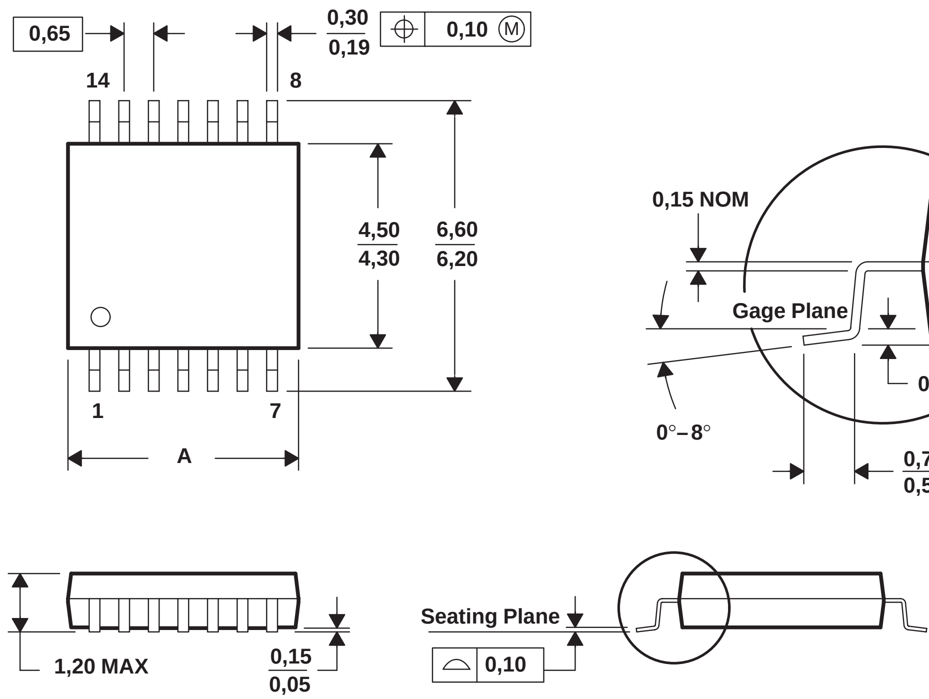


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS2114PWR	TSSOP	PW	8	2000	346.0	346.0	29.0
TPS2115PWR	TSSOP	PW	8	2000	346.0	346.0	29.0

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN



PINS ** / DIM	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

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NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153