

## **AUTOSWITCHING POWER MULTIPLEXER**

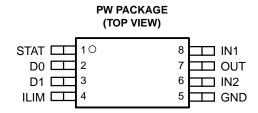
### **FEATURES**

- Two-Input, One-Output Power Multiplexer With Low r<sub>DS(on)</sub> Switches:
  - 84 m $\Omega$  Typ (TPS2115)
  - 120 mΩ Typ (TPS2114)
- Reverse and Cross-Conduction Blocking
- Wide Operating Voltage Range: 2.8 V to 5.5 V
- Low Standby Current: 0.5 μA Typical
- Low Operating Current: 55 μA Typical
- Adjustable Current Limit
- Controlled Output Voltage Transition Times, Limits Inrush Current and Minimizes Output Voltage Hold-Up Capacitance
- CMOS and TTL Compatible Control Inputs
- Manual and Auto-Switching Operating Modes
- Thermal Shutdown

### • Available in a TSSOP-8 Package

## **APPLICATIONS**

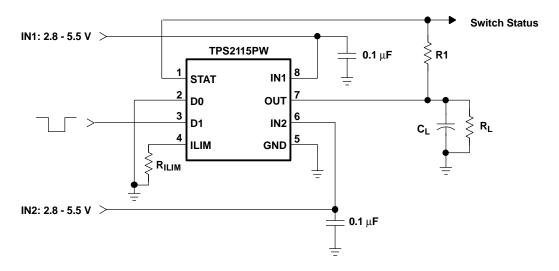
- PCs
- PDAs
- Digital Cameras
- Modems
- Cell phones
- Digital Radios
- MP3 Players



### DESCRIPTION

The TPS211x family of power multiplexers enables seamless transition between two power supplies, such as a battery and a wall adapter, each operating at 2.8-5.5 V and delivering up to 1 A. The TPS211x family includes extensive protection circuitry, including user-programmable current limiting, thermal protection, inrush current control, seamless supply transition, cross-conduction blocking, and reverse-conduction blocking. These features greatly simplify designing power multiplexer applications.

## TYPICAL APPLICATION





Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.





These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### **AVAILABLE OPTIONS**

| FEATURE                        |           | TPS2110    | TPS2111    | TPS2112    | TPS2113    | TPS2114    | TPS2115    |
|--------------------------------|-----------|------------|------------|------------|------------|------------|------------|
| Current limit adjustment range |           | 0.31-0.75A | 0.63-1.25A | 0.31-0.75A | 0.63-1.25A | 0.31-0.75A | 0.63-1.25A |
| 0 11 1                         | Manual    | Yes        | Yes        | No         | No         | Yes        | Yes        |
| Switching modes                | Automatic | Yes        | Yes        | Yes        | Yes        | Yes        | Yes        |
| Switch status output           |           | No         | No         | Yes        | Yes        | Yes        | Yes        |
| Package                        |           | TSSOP-8    | TSSOP-8    | TSSOP-8    | TSSOP-8    | TSSOP-8    | TSSOP-8    |

### **ORDERING INFORMATION**

| T <sub>A</sub> | PACKAGE       | ORDERING NUMBER (1) | MARKINGS |
|----------------|---------------|---------------------|----------|
| -40°C to 85°C  | TSSOD 8 (DM/) | TPS2114PW           | 2114     |
| -40 C to 65 C  | TSSOP-8 (PW)  | TPS2115PW           | 2115     |

<sup>(1)</sup> The PW package is available taped and reeled. Add an R suffix to the device type (e.g., TPS2114PWR) to indicate tape and reel.

### **PACKAGE DISSIPATION RATINGS**

| PACKAGE      | DERATING FACTOR             | T <sub>A</sub> ≤ 25°C | T <sub>A</sub> = 70°C | T <sub>A</sub> = 85°C |
|--------------|-----------------------------|-----------------------|-----------------------|-----------------------|
|              | ABOVE T <sub>A</sub> = 25°C | POWER RATING          | POWER RATING          | POWER RATING          |
| TSSOP-8 (PW) | 3.87 mW/°C                  | 386.84 mW             | 212.76 mW             | 154.73 mW             |

### **ABSOLUTE MAXIMUM RATINGS**

over operating free-air temperature range unless otherwise noted(1)

|                  |                                     |   | TPS2114, TPS2115             |
|------------------|-------------------------------------|---|------------------------------|
| V <sub>I</sub>   | Input voltage range                 | IN1, IN2, D0, D1, ILIM <sup>(2)</sup>       | -0.3 V to 6 V                |
| Vo               | Output voltage range <sup>(2)</sup> | OUT, STAT                                   | -0.3 V to 6 V                |
| Io               | Output sink current                 | STAT  | 5 mA                         |
|                  | Continuous sutput surrent           | TPS2114                                     | 0.9 A                        |
| 'o               | Continuous output current           | TPS2115                                     | 1.5 A                        |
|                  | Continuous total power diss         | ipation                                     | See Dissipation Rating Table |
| TJ               | Operating virtual junction ter      | mperature range                             | -40°C to 125°C               |
| T <sub>stg</sub> | Storage temperature range           |   | -65°C to 150°C               |
|                  | Lead temperature soldering          | 1,6 mm (1/16 inch) from case for 10 seconds | 260°C                        |

<sup>(1)</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltages are with respect to GND.



## **RECOMMENDED OPERATING CONDITIONS**

|                                     |   |                                | MIN   | I MAX  | UNIT |
|-------------------------------------|---|--------------------------------|-------|--------|------|
| V                                   | Input voltage of INI4                                 | $V_{I(IN2)} \ge 2.8 \text{ V}$ | 1.5   | 5.5    | V    |
| V <sub>I</sub> Input voltage at IN1 | input voitage at in i                                 | V <sub>I(IN2)</sub> < 2.8 V    | 2.8   | 3 5.5  | \ \  |
| V Input voltage et INO              | $V_{I(IN1)} \ge 2.8 \text{ V}$                        | 1.5                            | 5 5.5 | \/     |      |
| l v <sub>i</sub>                    | V <sub>I</sub> Input voltage at IN2                   | $V_{I(IN1)}$ < 2.8 V           |       | 3 5.5  | ]    |
| VI                                  | Input voltage at D0, D1                               | •                              | (     | 5.5    | V    |
|                                     | Compact limit a discrete and many                     | TPS2114                        | 0.31  | 0.75   | ^    |
| I <sub>O(OUT)</sub>                 | Current limit adjustment range TPS2115                |                                | 0.63  | 3 1.25 | A    |
| T <sub>J</sub>                      | T <sub>J</sub> Operating virtual junction temperature |                                | -4(   | ) 125  | °C   |

## **ELECTROSTATIC DISCHARGE (ESD) PROTECTION**

|                  | MIN MAX | UNIT |
|------------------|---------|------|
| Human body model | 2       | kV   |
| CDM              | 500     | V    |

## **ELECTRICAL CHARACTERISTICS**

over recommended operating junction temperature range,  $V_{I(IN1)} = V_{I(IN2)} = 5.5 \text{ V}$ ,  $R_{(ILIM)} = 400 \Omega$  (unless otherwise noted)

| PARAMETER                          |   | TEST CO   | ONDITIONS                                 | TPS2114 |     |     | TF  | 5   | UNIT      |           |
|------------------------------------|---|---|---|---------|-----|-----|-----|-----|-----------|-----------|
|                                    |   | IESI CC   | TEST CONDITIONS                           |         | TYP | MAX | MIN | TYP | MAX       | UNIT      |
| POWER S                            | SWITCH  |   |   |         |     |     |     |     |           |           |
|                                    |   |   | $V_{I(IN1)} = V_{I(IN2)} = 5.0 \text{ V}$ |         | 120 | 140 |     | 84  | 110       |           |
|                                    |   | $T_J = 25^{\circ}C$ ,<br>$I_I = 500 \text{ mA}$ | $V_{I(IN1)} = V_{I(IN2)} = 3.3 \text{ V}$ |         | 120 | 140 |     | 84  | 110       | $m\Omega$ |
| r (1)                              | Drain-source on-state                         | 1[= 000 11#1                                    | $V_{I(IN1)} = V_{I(IN2)} = 2.8 \text{ V}$ |         | 120 | 140 |     | 84  | 110       |           |
| r <sub>DS(on)</sub> <sup>(1)</sup> | resistance (INx-OUT)                          |   | $V_{I(IN1)} = V_{I(IN2)} = 5.0 \text{ V}$ |         |     | 220 |     |     | 150       |           |
|                                    | $T_J = 125^{\circ}C$ , $I_I = 500 \text{ mA}$ | $V_{I(IN1)} = V_{I(IN2)} = 3.3 \text{ V}$       |   |         | 220 |     |     | 150 | $m\Omega$ |           |
|                                    |   |   | $V_{I(IN1)} = V_{I(IN2)} = 2.8 \text{ V}$ |         |     | 220 |     |     | 150       |           |

<sup>(1)</sup> The TPS211x can switch a voltage as low as 1.5 V as long as there is a minimum of 2.8 V at one of the input power pins. In this specific case, the lower supply voltge has no effect on the IN1 and IN2 switch on-resistances.



## **ELECTRICAL CHARACTERISTICS**

over operating free-air temperature range (unless otherwise noted)

|   | PARAMETER                          | TEST CONDITIONS  | Т    | PS211 | 5    | UNIT    |  |  |
|---|------------------------------------|--|------|-------|------|---------|--|--|
|   | ANAMETER                           | TEST CONDITIONS  | MIN  | TYP   | MAX  | ONT     |  |  |
| LOGIC INPUTS (D0                            | AND D1)                            |  |      |       |      |         |  |  |
| V <sub>IH</sub> High-lev                    | vel input voltage                  |  | 2    |       |      | V       |  |  |
| V <sub>IL</sub> Low-lev                     | el input voltage                   |  |      |       | 0.7  | V       |  |  |
| Input cu                                    | irrent at D0 or D1                 | D0 or D1 = High, sink current  |      |       | 1    | μA      |  |  |
| input co                                    | inent at bo of bi                  | D0 or D1 = Low, source current   | 0.5  | 1.4   | 5    | μΛ      |  |  |
| SUPPLY AND LEAK                             | AGE CURRENTS                       |  | _    |       |      |         |  |  |
|   |                                    | D1 = High, D0 = Low (IN1 active), $V_{I(IN1)}$ = 5.5 V, $V_{I(IN2)}$ = 3.3 V, $I_{O(OUT)}$ = 0 A                     |      | 55    | 90   |         |  |  |
| Supply current from I                       | N1 (operating)                     | D1 = High, D0 = Low (IN1 active), $V_{I(IN1)}$ = 3.3 V, $V_{I(IN2)}$ = 5.5 V, $I_{O(OUT)}$ = 0 A                     |      | 1     | 12   |         |  |  |
| Supply current from t                       | ivi (operating)                    | D0 = D1 = Low (IN2 active), $V_{I(IN2)} = 5.5 \text{ V}$ , $V_{I(IN2)} = 3.3 \text{ V}$ , $I_{O(OUT)} = 0 \text{ A}$ |      |       | 75   | μA      |  |  |
|   |                                    | D0 = D1 = Low (IN2 active), $V_{I(IN2)} = 3.3 \text{ V}$ , $V_{I(IN2)} = 5.5 \text{ V}$ , $I_{O(OUT)} = 0 \text{ A}$ |      |       | 1    |         |  |  |
|   |                                    | D1 = High, D0 = Low (IN1 active), $V_{I(IN1)}$ = 5.5 V, $V_{I(IN2)}$ = 3.3 V, $I_{O(OUT)}$ = 0 A                     |      |       | 1    |         |  |  |
| Cumply asserted from I                      | N2 (operating)                     | D1 = High, D0 = Low (IN1 active), $V_{I(IN1)}$ = 3.3 V, $V_{I(IN2)}$ = 5.5 V, $I_{O(OUT)}$ = 0 A                     |      |       | 75   |         |  |  |
| Supply current from IN2 (operating)         |                                    | D0 = D1 = Low (IN2 active), $V_{I(IN1)}$ = 5.5 V, $V_{I(IN2)}$ = 3.3 V, $I_{O(OUT)}$ = 0 A                           |      | 1     | 12   | μA      |  |  |
|   |                                    | D0 = D1 = Low (IN2 active), $V_{I(IN1)}$ = 3.3 V, $V_{I(IN2)}$ = 5.5 V, $I_{O(OUT)}$ = 0 A                           |      | 55    | 90   |         |  |  |
|   |                                    | D0 = D1 = High (inactive), $V_{I(IN1)}$ = 5.5 V, $V_{I(IN2)}$ = 3.3 V, $I_{O(OUT)}$ = 0 A                            |      | 0.5   | 2    |         |  |  |
| Quiescent current fro                       | mini (STANDBY)                     | D0 = D1 = High (inactive), $V_{I(IN1)} = 3.3 \text{ V}$ , $V_{I(IN2)} = 5.5 \text{ V}$ , $I_{O(OUT)} = 0 \text{ A}$  |      |       | 1    | μA      |  |  |
| Outcoant ourrent fro                        | ~ INO (CTANDDY)                    | D0 = D1 = High (inactive), $V_{I(IN1)} = 5.5 \text{ V}$ , $V_{I(IN2)} = 3.3 \text{ V}$ , $I_{O(OUT)} = 0 \text{ A}$  |      | ,     | 1    |         |  |  |
| Quiescent current fro                       | III INZ (STANDBT)                  | D0 = D1 = High (inactive), $V_{I(IN1)}$ = 3.3 V, $V_{I(IN2)}$ = 5.5 V, $I_{O(OUT)}$ = 0 A                            |      | 0.5   | 2    | μA<br>2 |  |  |
| Forward leakage curi<br>(measured from OUT  |                                    | D0 = D1 = High (inactive), $V_{I(IN1)}$ = 5.5 V, IN2 open, $V_{O(OUT)}$ = 0 V (shorted), $T_J$ = 25°C                |      | 0.1   | 5    | μA      |  |  |
| Forward leakage curi<br>(measured from OUT  |                                    | D0 = D1= High (inactive), $V_{I(IN2)}$ = 5.5 V, IN1 open, $V_{O(OUT)}$ = 0 V (shorted), $T_J$ = 25°C                 |      | 0.1   | 5    | μA      |  |  |
| Reverse leakage cur<br>(measured from INx t |                                    | D0 = D1 = High (inactive), $V_{I(INx)} = 0 V$ , $V_{O(OUT)} = 5.5 V$ , $V_{J} = 25^{\circ}C$                         |      | 0.3   | 5    | μA      |  |  |
| CURRENT LIMIT CI                            | RCUIT                              |  |      |       |      |         |  |  |
|   | TDC0444                            | $R_{(ILIM)} = 400 \Omega$  | 0.51 | 0.63  | 0.80 |         |  |  |
| Current limit                               | TPS2114                            | $R_{\text{(ILIM)}} = 700 \ \Omega$   | 0.30 | 0.36  | 0.50 |         |  |  |
| accuracy                                    | TDCOAAF                            | $R_{(ILIM)} = 400 \Omega$  | 0.95 | 1.25  | 1.56 | A       |  |  |
|   | TPS2115                            | $R_{(ILIM)} = 700 \Omega$  | 0.47 | 0.71  | 0.99 |         |  |  |
| t <sub>d</sub> Current                      | limit settling time <sup>(1)</sup> | Time for short-circuit output current to settle within 10% of its steady state value.                                |      | 1     |      | ms      |  |  |
| Input cu                                    | irrent at ILIM                     | $V_{I(ILIM)} = 0 \text{ V}, I_{O(OUT)} = 0 \text{ A}$  | -15  |       | 0    | μA      |  |  |

<sup>(1)</sup> Not tested in production.



over operating free-air temperature range (unless otherwise noted)

| DADAMETED   | TEST CONDITIONS   | Т    | PS211 | 5    | LINUT |
|---|---|------|-------|------|-------|
| PARAMETER   | TEST CONDITIONS   | MIN  | TYP   | MAX  | UNIT  |
| UNDERVOLTAGE LOCKOUT  |   |      |       |      |       |
| IN1 and IN2 UVLO  | Falling edge  | 1.15 | 1.25  |      | V     |
|   | Rising edge   |      | 1.30  | 1.35 | V     |
| IN1 and IN2 UVLO hysteresis <sup>(2)</sup>  |   | 30   | 57    | 65   | mV    |
| Internal \/ LIVI O (the higher of INI4 and INI2)  | Falling edge  | 24   | 2.53  |      | V     |
| Internal V <sub>DD</sub> UVLO (the higher of IN1 and IN2)   | Rising edge   |      | 2.58  | 2.8  | V     |
| Internal V <sub>DD</sub> UVLO hysteresis <sup>(2)</sup>   |   | 30   | 50    | 75   | mV    |
| UVLO deglitch for IN1, IN2 <sup>(2)</sup>   | Falling edge  |      | 110   |      | μs    |
| REVERSE CONDUCTION BLOCKING   |   |      |       |      |       |
| $\Delta V_{O(I\_block)} \qquad \begin{array}{l} \text{Minimum output-to-input voltage} \\ \text{difference to block switching} \end{array}$ | D0 = D1 = high, $V_{I(INx)}$ = 3.3 V. Connect OUT to a 5 V supply through a series 1-k $\Omega$ resistor. Let D0 = low. Slowly decrease the supply voltage until OUT connects to IN1. | 80   | 100   | 120  | mV    |
| THERMAL SHUTDOWN  |   |      |       |      |       |
| Thermal shutdown threshold <sup>(2)</sup>   | TPS211x is in current limit.  | 135  |       |      |       |
| Recovery from thermal shutdown <sup>(2)</sup>   | TPS211x is in current limit.  | 125  |       |      | ∘c    |
| Hysteresis <sup>(2)</sup>   |   |      | 10    |      |       |
| IN2-IN1 COMPARATORS   |   |      |       |      |       |
| Hysteresis of IN2-IN1 comparator  |   | 0.1  |       | 0.2  | V     |
| Deglitch of IN2-IN1 comparator, (both↑↓)(2)   |   | 90   | 150   | 220  | μs    |
| STAT OUTPUT   |   |      |       |      |       |
| Leakage current   | V <sub>O(STAT)</sub> = 5.5 V  |      | 0.01  | 1    | μA    |
| Saturation voltage  | I <sub>I(STAT)</sub> = 2 mA, IN1 switch is on   |      | 0.13  | 0.4  | V     |
| Deglitch time (falling edge only)   |   |      | 150   |      | μs    |

<sup>(2)</sup> Not tested in production.



## **SWITCHING CHARACTERISTICS**

over recommended operating junction temperature range,  $V_{I(IN1)} = V_{I(IN2)} = 5.5 \text{ V}$ ,  $R_{(ILIM)} = 400 \Omega$  (unless otherwise noted)

|   | PARAMETER   | TEST COL   | CONDITIONS  |      | ΓPS211 | 4   | TPS2115 |      |     | LINIT |
|---|---|--|---|------|--------|-----|---------|------|-----|-------|
| FARAIVIETER   |   | IESI COI   | TEST CONDITIONS   |      | TYP    | MAX | MIN     | TYP  | MAX | UNIT  |
| POWE  | R SWITCH  |  |   | •    |        |     |         |      |     |       |
| t <sub>r</sub>  | Output rise time from an enable <sup>(1)</sup>          | $V_{I(IN1)} = V_{I(IN2)} = 5 \text{ V}$  | $T_J = 25^{\circ}C$ , $C_L = 1 \mu F$ , $I_L = 500 \text{ mA}$ , See Figure 1(a)        | 0.5  | 1.0    | 1.5 | 1       | 1.8  | 3   | ms    |
| t <sub>f</sub>  | Output fall time from a disable (1)                     | V <sub>I(IN1)</sub> = V <sub>I(IN2)</sub> = 5 V  | $T_J = 25^{\circ}C$ , $C_L = 1 \mu F$ , $I_L = 500 \text{ mA}$ , See Figure 1(a)        | 0.35 | 0.5    | 0.7 | 0.5     | 1    | 2   | ms    |
|   |   | IN1 to IN2 transition,<br>$V_{I(IN1)} = 3.3 \text{ V},$<br>$V_{I(IN2)} = 5 \text{ V}$  | $T_J$ = 125°C,<br>$C_L$ = 10 $\mu$ F,<br>$I_L$ = 500 mA [Measure                        |      | 40     | 60  |         | 40   | 60  |       |
| $t_t$ Transition time <sup>(1)</sup> IN2 to IN1 transition, V <sub>I(IN1)</sub> = 5 V, V <sub>I(IN2)</sub> = 3.3 V transition, on V <sub>I(IN2)</sub> |   | transition time as 10-90% rise time or from 3.4 V to 4.8 V on V <sub>O(OUT)</sub> ], See Figure 1(b)   |   | 40   | 60     |     | 40      | 60   | μs  |       |
| t <sub>PLH1</sub>   | Turnon propagation delay from enable <sup>(1)</sup>     | $V_{I(IN1)} = V_{I(IN2)} = 5 \text{ V},$<br>Measured from enable<br>to 10% of $V_{O(OUT)}$   | $T_J = 25^{\circ}C,$ $C_L = 10 \ \mu\text{F},$ $I_L = 500 \ \text{mA},$ SeeFigure 1(a)  |      | 0.5    |     |         | 1    |     | ms    |
| t <sub>PHL1</sub>   | Turnoff propagation delay from a disable <sup>(1)</sup> | $V_{I(IN1)} = V_{I(IN2)} = 5 \text{ V},$<br>Measured from disable<br>to 90% of $V_{O(OUT)}$  | $T_J = 25^{\circ}C,$ $C_L = 10 \ \mu\text{F},$ $I_L = 500 \ \text{mA},$ See Figure 1(a) |      | 3      |     |         | 5    |     | ms    |
| t <sub>PLH2</sub>   | Switch-over rising propagation delay <sup>(1)</sup>     | Logic 1 to Logic 0 transition on D1, $V_{I(IN1)} = 1.5 \text{ V}, \\ V_{I(IN2)} = 5 \text{ V}, \\ V_{I(D0)} = 0 \text{ V}, \\ \text{Measured from D1 to} \\ 10\% \text{ of } V_{O(OUT)}$ | $T_J = 25^{\circ}C,$ $C_L = 10 \ \mu\text{F},$ $I_L = 500 \ \text{mA},$ See Figure 1(c) |      | 0.17   | 1   |         | 0.17 | 1   | ms    |
| t <sub>PHL2</sub>   | Switch-over falling propagation delay <sup>(1)</sup>    | Logic 0 to Logic 1 transition on D1, $V_{I(IN1)} = 1.5 \text{ V}, \\ V_{I(IN2)} = 5 \text{ V}, \\ V_{I(D0)} = 0 \text{ V}, \text{ Measured from D1 to 90% of } \\ V_{O(OUT)}$            | $T_J = 25^{\circ}C,$ $C_L = 10 \ \mu\text{F},$ $I_L = 500 \ \text{mA},$ See Figure 1(c) | 2    | 3      | 10  | 2       | 5    | 10  | ms    |

(1) Not tested in production.

## **TRUTH TABLE**

| D1 | D0 | $V_{I(IN2)} > V_{I(IN1)}$ | $V_{I(IN2)} > V_{I(IN1)}$ STAT |      |
|----|----|---------------------------|--------------------------------|------|
| 0  | 0  | X                         | Hi-Z                           | IN2  |
| 0  | 1  | No                        | 0                              | IN1  |
| 0  | 1  | Yes                       | Hi-Z                           | IN2  |
| 1  | 0  | Х                         | 0                              | IN1  |
| 1  | 1  | X                         | 0                              | Hi-Z |

(1) The under-voltage lockout circuit causes the output OUT to go Hi-Z if the selected power supply does not exceed the IN1/IN2 UVLO, or if neither of the supplies exceeds the internal  $V_{DD}$  UVLO.

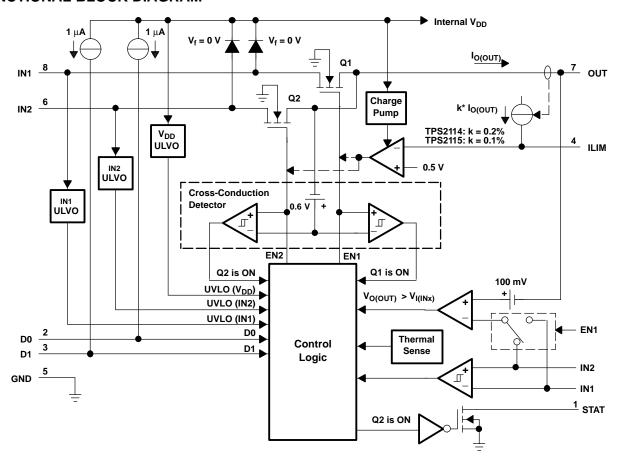
6



## **Terminal Functions**

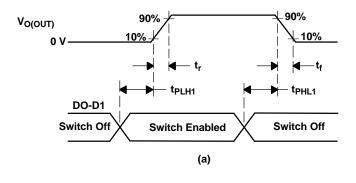
| TERM | INAL | 1/0 | DESCRIPTION   |
|------|------|-----|---|
| NAME | NO.  | 1/0 | DESCRIPTION   |
| D0   | 2    | 1   | TTL and CMOS compatible input pins. Each pin has a 1-µA pullup resistor. The truth table shown above illustrates  |
| D1   | 3    | I   | the functionality of D0 and D1.   |
| GND  | 5    | I   | Ground  |
| IN1  | 8    | I   | Primary power switch input. The IN1 switch can be enabled only if the IN1 supply is above the UVLO threshold and at least one supply exceeds the internal V <sub>DD</sub> UVLO.   |
| IN2  | 6    | I   | Secondary power switch input. The IN2 switch can be enabled only if the IN2 supply is above the UVLO threshold and at least one supply exceeds the internal V <sub>DD</sub> UVLO. |
| ILIM | 4    | I   | A resistor $R_{(ILIM)}$ from ILIM to GND sets the current limit $I_L$ to 250/ $R_{(ILIM)}$ and 500/ $R_{(ILIM)}$ for the TPS2114 and TPS2115, respectively.                       |
| OUT  | 7    | 0   | Power switch output   |
| STAT | 1    | 0   | STAT is an open-drain output that is Hi-Z if the IN2 switch is ON. STAT pulls low if the IN1 switch is ON or if OUT is Hi-Z (i.e., EN is equal to logic 0).                       |

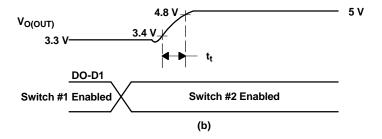
## **FUNCTIONAL BLOCK DIAGRAM**





## PARAMETER MEASUREMENT INFORMATION





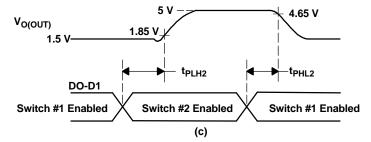


Figure 1. Propagation Delays and Transition Timing Waveforms



## TYPICAL CHARACTERISTICS

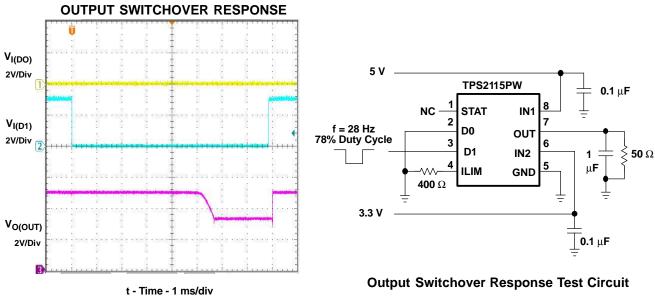


Figure 2.

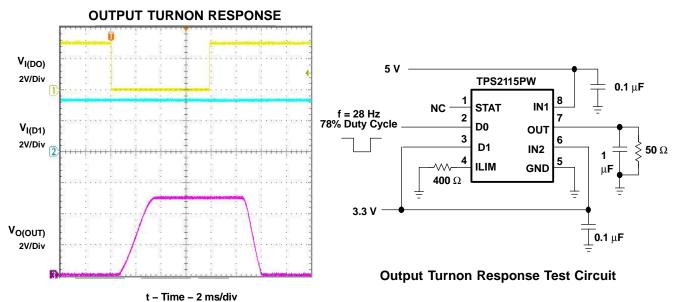


Figure 3.



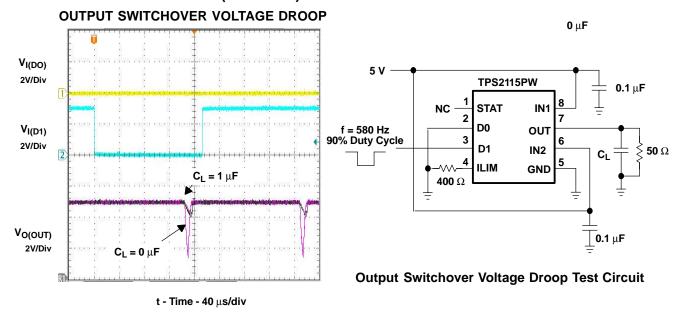
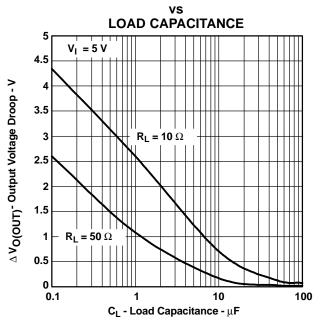
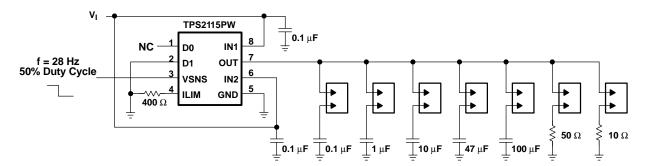


Figure 4.



## **OUTPUT SWITCHOVER VOLTAGE DROOP**



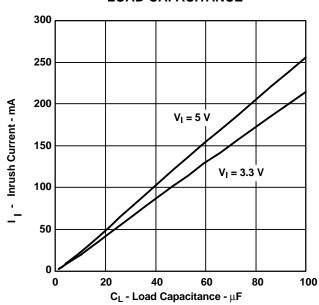


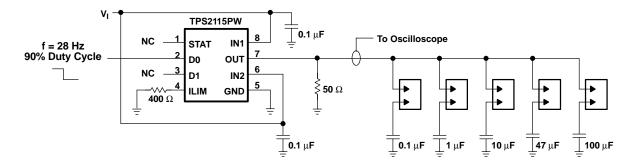
**Output Switchover Voltage Droop Test Circuit** 

Figure 5.



# INRUSH CURRENT vs LOAD CAPACITANCE





**Output Capacitor Inrush Current Test Circuit** 

Figure 6.

6



## **TYPICAL CHARACTERISTICS (continued)**

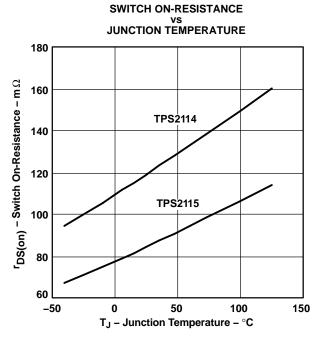
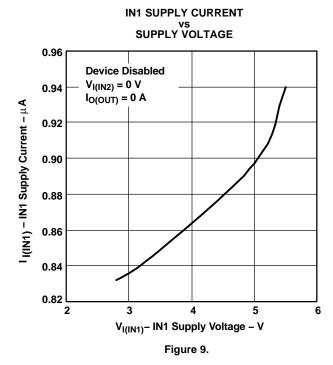
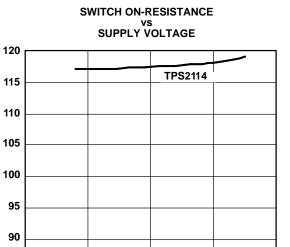


Figure 7.





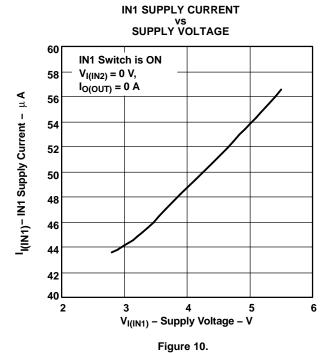
<sup>r</sup>DS(on) – Switch On-Resistance – m  $\Omega$ 

85

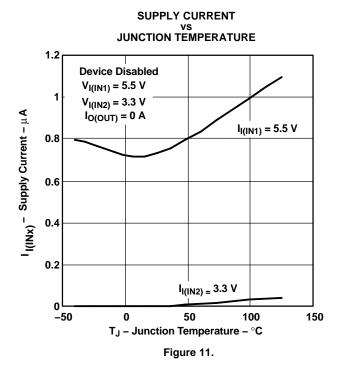
80

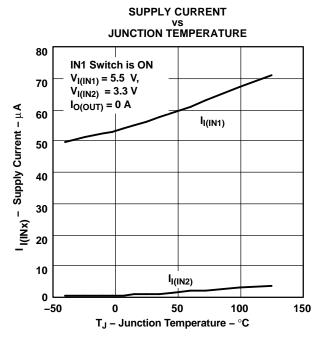
 $V_{I(INx)}$  – Supply Voltage – V Figure 8.

TPS2115











### **APPLICATION INFORMATION**

The circuit in Figure 13 allows one or two battery packs to power a system. Two battery packs allow a longer run time. The TPS2114/5 cycles between the battery packs until both packs are drained.

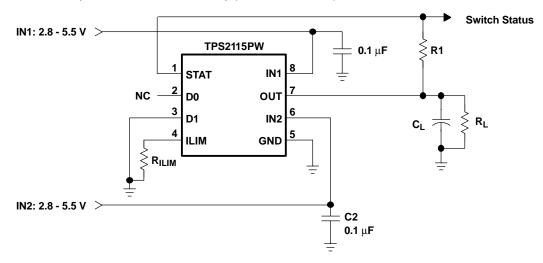


Figure 13. Running a System From Two Battery Packs

In Figure 14, the multiplexer selects between two power supplies based upon the D1 logic signal. OUT connects to IN1 if D1 is logic 1, otherwise OUT connects to IN2. The logic thresholds for the D1 terminal are compatible with both TTL and CMOS logic.

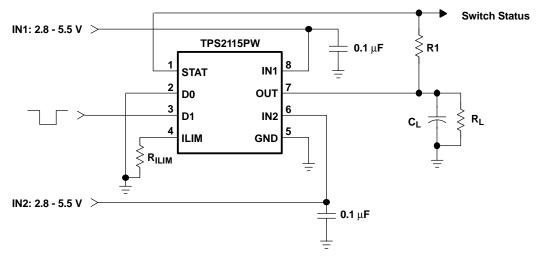


Figure 14. Manually Switching Power Sources



### **DETAILED DESCRIPTION**

### **AUTO-SWITCHING MODE**

D0 equal to logic 1 and D1 equal to logic 0 selects the auto-switching mode. In this mode, OUT connects to the higher of IN1 and IN2.

### MANUAL SWITCHING MODE

D0 equal to logic 0 selects the manual-switching mode. In this mode, OUT connects to IN1 if D1 is equal to logic 1, otherwise OUT connects to IN2.

### **N-CHANNEL MOSFETs**

Two internal high-side power MOSFETs implement a single-pole double-throw (SPDT) switch. Digital logic selects the IN1 switch, IN2 switch, or no switch (Hi-Z state). The MOSFETs have no parallel diodes so output-to-input current cannot flow when the FET is off. An integrated comparator prevents turnon of a FET switch if the output voltage is greater than the input voltage.

### **CROSS-CONDUCTION BLOCKING**

The switching circuitry ensures that both power switches never conduct at the same time. A comparator monitors the gate-to-source voltage of each power FET and allows a FET to turn on only if the gate-to-source voltage of the other FET is below the turnon threshold voltage.

### REVERSE-CONDUCTION BLOCKING

When the TPS211x switches from a higher-voltage supply to a lower-voltage supply, current can potentially flow back from the load capacitor into the lower-voltage supply. To minimize such reverse conduction, the TPS211x does not connect a supply to the output until the output voltage has fallen to within 100 mV of the supply voltage. Once a supply has been connected to the output, it remains connected regardless of output voltage.

### **CHARGE PUMP**

The higher of supplies IN1 and IN2 powers the internal charge pump. The charge pump provides power to the current limit amplifier and allows the output FET gate voltage to be higher than the IN1 and IN2 supply voltages. A gate voltage that is higher than the source voltage is necessary to turn on the N-channel FET.

## **CURRENT LIMITING**

A resistor  $R_{(ILIM)}$  from ILIM to GND sets the current limit to 250/  $R_{(ILIM)}$  and 500/ $R_{(ILIM)}$  for the TPS2114 and TPS2115, respectively. Setting resistor  $R_{(ILIM)}$  equal to zero is not recommended as that disables current limiting.

### **OUTPUT VOLTAGE SLEW-RATE CONTROL**

The TPS2114/5 slews the output voltage at a slow rate when OUT switches to IN1 or IN2 from the Hi-Z state (see *Truth Table*). A slow slew rate limits the inrush current into the load capacitor. High inrush currents can adversely effect the voltage bus and cause a system to hang up or reset. It can also cause reliability issues—like pit the connector power contacts, when hot plugging a load like a PCI card. The TPS2114/5 slews the output voltage at a much faster rate when OUT switches between IN1 and IN2. The fast rate minimizes the output voltage droop and reduces the output voltage hold-up capacitance requirement.





i.com 6-Dec-2006

### PACKAGING INFORMATION

| Orderable Device | Status <sup>(1)</sup> | Package<br>Type | Package<br>Drawing | Pins | Package<br>Qty | e Eco Plan <sup>(2)</sup> | Lead/Ball Finish | MSL Peak Temp <sup>(3)</sup> |
|------------------|-----------------------|-----------------|--------------------|------|----------------|---------------------------|------------------|------------------------------|
| TPS2114PW        | ACTIVE                | TSSOP           | PW                 | 8    | 150            | Green (RoHS & no Sb/Br)   | CU NIPDAU        | Level-1-260C-UNLIM           |
| TPS2114PWG4      | ACTIVE                | TSSOP           | PW                 | 8    | 150            | Green (RoHS & no Sb/Br)   | CU NIPDAU        | Level-1-260C-UNLIM           |
| TPS2114PWR       | ACTIVE                | TSSOP           | PW                 | 8    | 2000           | Green (RoHS & no Sb/Br)   | CU NIPDAU        | Level-1-260C-UNLIM           |
| TPS2114PWRG4     | ACTIVE                | TSSOP           | PW                 | 8    | 2000           | Green (RoHS & no Sb/Br)   | CU NIPDAU        | Level-1-260C-UNLIM           |
| TPS2115PW        | ACTIVE                | TSSOP           | PW                 | 8    | 150            | Green (RoHS & no Sb/Br)   | CU NIPDAU        | Level-1-260C-UNLIM           |
| TPS2115PWG4      | ACTIVE                | TSSOP           | PW                 | 8    | 150            | Green (RoHS & no Sb/Br)   | CU NIPDAU        | Level-1-260C-UNLIM           |
| TPS2115PWR       | ACTIVE                | TSSOP           | PW                 | 8    | 2000           | Green (RoHS & no Sb/Br)   | CU NIPDAU        | Level-1-260C-UNLIM           |
| TPS2115PWRG4     | ACTIVE                | TSSOP           | PW                 | 8    | 2000           | Green (RoHS & no Sb/Br)   | CU NIPDAU        | Level-1-260C-UNLIM           |

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

**Pb-Free** (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

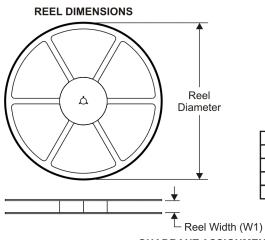
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

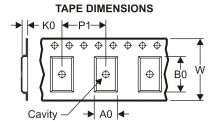
Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.



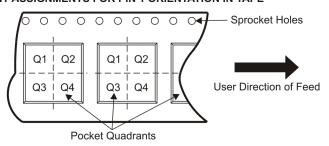
## TAPE AND REEL INFORMATION





|    | Dimension designed to accommodate the component width     |
|----|---|
| B0 | Dimension designed to accommodate the component length    |
| K0 | Dimension designed to accommodate the component thickness |
| W  | Overall width of the carrier tape                         |
| P1 | Pitch between successive cavity centers                   |

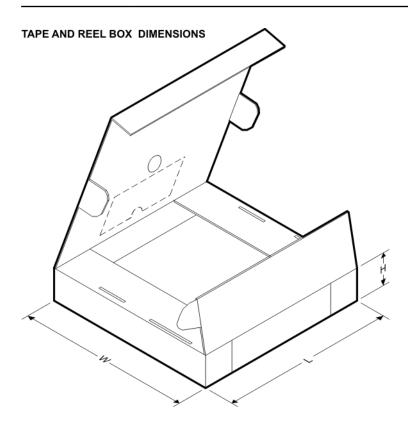
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



## \*All dimensions are nominal

| Device     | Package<br>Type | Package<br>Drawing |   |      | Reel<br>Diameter<br>(mm) | Reel<br>Width<br>W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1<br>(mm) | W<br>(mm) | Pin1<br>Quadrant |
|------------|-----------------|--------------------|---|------|--------------------------|--------------------------|---------|---------|---------|------------|-----------|------------------|
| TPS2114PWR | TSSOP           | PW                 | 8 | 2000 | 330.0                    | 12.4                     | 7.0     | 3.6     | 1.6     | 8.0        | 12.0      | Q1               |
| TPS2115PWR | TSSOP           | PW                 | 8 | 2000 | 330.0                    | 12.4                     | 7.0     | 3.6     | 1.6     | 8.0        | 12.0      | Q1               |





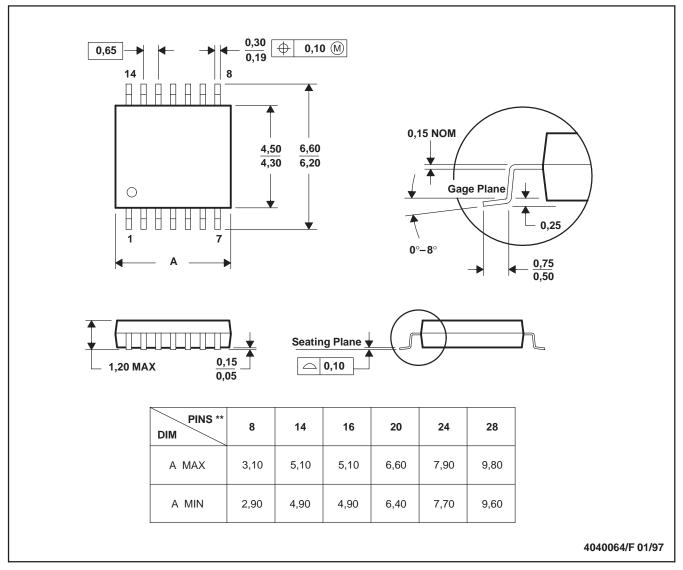
### \*All dimensions are nominal

| Device     | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TPS2114PWR | TSSOP        | PW              | 8    | 2000 | 346.0       | 346.0      | 29.0        |
| TPS2115PWR | TSSOP        | PW              | 8    | 2000 | 346.0       | 346.0      | 29.0        |

## PW (R-PDSO-G\*\*)

### 14 PINS SHOWN

## PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.

D. Falls within JEDEC MO-153

### **IMPORTANT NOTICE**

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

#### **Products Amplifiers** amplifier.ti.com Data Converters dataconverter.ti.com DSP dsp.ti.com Clocks and Timers www.ti.com/clocks Interface interface.ti.com Logic logic.ti.com Power Mgmt power.ti.com microcontroller.ti.com Microcontrollers www.ti-rfid.com RF/IF and ZigBee® Solutions www.ti.com/lprf

| Applications       |                           |
|--------------------|---------------------------|
| Audio              | www.ti.com/audio          |
| Automotive         | www.ti.com/automotive     |
| Broadband          | www.ti.com/broadband      |
| Digital Control    | www.ti.com/digitalcontrol |
| Medical            | www.ti.com/medical        |
| Military           | www.ti.com/military       |
| Optical Networking | www.ti.com/opticalnetwork |
| Security           | www.ti.com/security       |
| Telephony          | www.ti.com/telephony      |
| Video & Imaging    | www.ti.com/video          |
| Wireless           | www.ti.com/wireless       |

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265 Copyright © 2008, Texas Instruments Incorporated