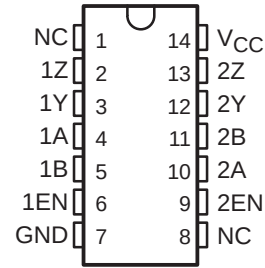


SN75159 DUAL DIFFERENTIAL LINE DRIVER WITH 3-STATE OUTPUTS

SLLS088B – JANUARY 1977 – REVISED MAY 1995

- Meets or Exceeds the Requirements of ANSI EIA/TIA-422-B and ITU Recommendation V.11
- Single 5-V Supply
- Balanced Line Operation
- TTL Compatible
- High-Impedance Output State for Party-Line Applications
- High-Current Active-Pullup Outputs
- Short-Circuit Protection
- Dual Channels
- Clamp Diodes at Inputs

D OR N PACKAGE
(TOP VIEW)



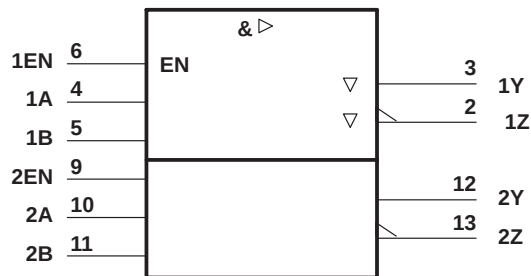
NC – No internal connection

description

The SN75159 dual differential line driver with 3-state outputs is designed to provide all the features of the SN75158 line driver with the added feature of driver output controls. There is an individual control for each driver. When the output control is low, the associated outputs are in a high-impedance state and the outputs can neither drive nor load the bus. This permits many devices to be connected together on the same transmission line for party-line applications.

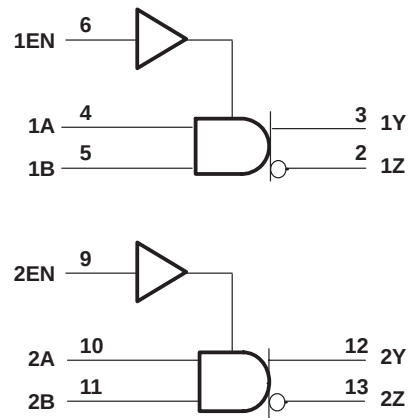
The SN75159 is characterized for operation from 0°C to 70°C.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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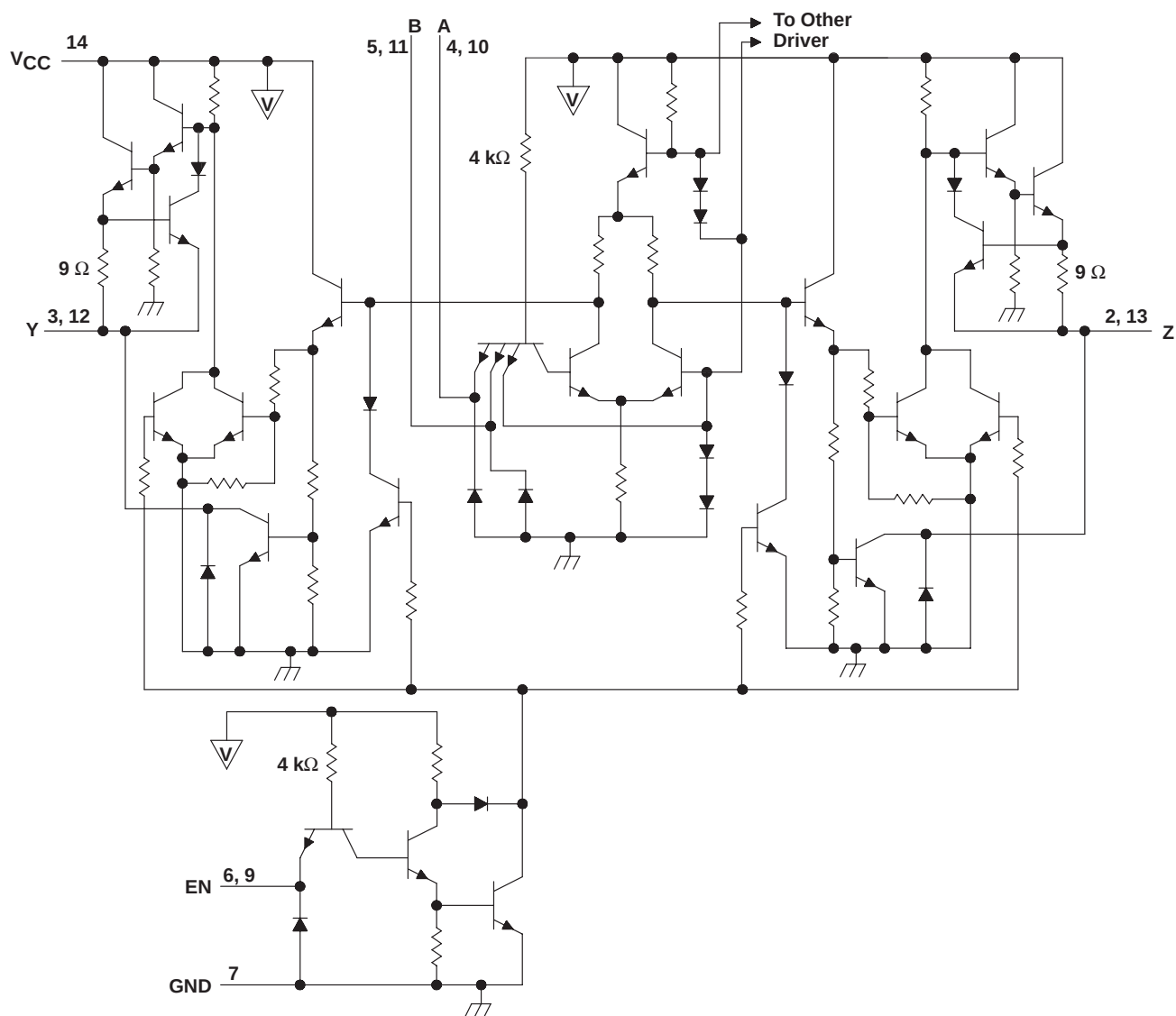
SN75159

DUAL DIFFERENTIAL LINE DRIVER

WITH 3-STATE OUTPUTS

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schematic (each driver)



△ ... VCC bus

Resistor values shown are nominal.

SN75159
DUAL DIFFERENTIAL LINE DRIVER
WITH 3-STATE OUTPUTS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage, V_I	5.5 V
Off-state voltage applied to open-collector outputs	12 V
Continuous total dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A	0°C to 70°C
Storage temperature range, T_{stg}	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values except differential output voltage V_{OD} are with respect to the network ground terminal. V_{OD} is at the Y output with respect to the Z output.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW
N	1150 mW	9.2 mW/°C	736 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
High-level output voltage, I_{OH}			–40	mA
Low-level output current, I_{OL}			40	mA
Operating free-air temperature, T_A	0		70	°C



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DUAL DIFFERENTIAL LINE DRIVER WITH 3-STATE OUTPUTS

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electrical characteristics over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP [†]	MAX	UNIT
V _{IK}	Input clamp voltage	V _{CC} = 4.75 V, I _I = −12 mA			−0.9	−1.5	V
V _{OH}	High-level output voltage	V _{CC} = 4.75 V, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OH} = −40 mA		2.4	3		V
V _{OL}	Low-level output voltage	V _{CC} = 4.75 V, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OL} = 40 mA			0.25	0.4	V
V _{OK}	Output clamp voltage	V _{CC} = 5.25 V, I _O = −40 mA			−1.1	−1.5	V
V _O	Output voltage	V _{CC} = 4.75 V to 5.25 V, I _O = 0		0		6	V
V _{OD1}	Differential output voltage	V _{CC} = 5.25 V, I _O = 0			3.5	2V _{OD2}	V
V _{OD2}	Differential output voltage	V _{CC} = 4.75 V		2	3		V
Δ V _{OD}	Change in magnitude of differential output voltage [‡]	V _{CC} = 4.75 V	R _L = 100 Ω, See Figure 1		±0.02	±0.4	V
V _{OC}	Common-mode output voltage [§]	V _{CC} = 5.25 V			1.8	3	V
		V _{CC} = 4.75 V			1.5	3	
Δ V _{OC}	Change in magnitude of common-mode output voltage [‡]	V _{CC} = 4.75 V to 5.25 V				±0.01	±0.4
I _O	Output current with power off	V _{CC} = 0	V _O = 6 V		0.1	100	μA
			V _O = −0.25 V		−0.1	−100	
			V _O = −0.25 V to 6 V			±100	
I _{OZ}	Off-state (high-impedance state) output current	V _{CC} = 5.25 V, Output controls at 0.8 V	T _A = 25°C	V _O = 0 to V _{CC}		±10	μA
			T _A = 70°C	V _O = 0		−20	
				V _O = 0.4 V		±20	
				V _O = 2.4 V		±20	
				V _O = V _{CC}		20	
I _I	Input current at maximum input voltage	V _{CC} = 5.25 V, V _I = 5.5 V				1	mA
I _{IH}	High-level input current	V _{CC} = 5.25 V, V _I = 2.4 V				40	μA
I _{IL}	Low-level input current	V _{CC} = 5.25 V, V _I = 0.4 V			−1	−1.6	mA
I _{OS}	Short-circuit output current [¶]	V _{CC} = 5.25 V		−40	−90	−150	mA
I _{CC}	Supply current (both drivers)	V _{CC} = 5.25 V, T _A = 25°C, Inputs grounded, No load			47	65	mA

[†] All typical values are at $V_{CC} = 5\text{ V}$ and $T_A = 25^\circ\text{C}$ except for V_{OC} , for which V_{CC} is as stated under test conditions.

[‡] $\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in magnitudes of V_{OD} and V_{OC} , respectively, that occur when the input is changed from a high level to a low level.

[§] In ANSI Standard EIA/TIA-422-B, V_{OC} , which is the average of the two output voltages with respect to GND, is called output offset voltage, V_{OS} .

[¶] Only one output should be shorted at a time, and duration of the short circuit should not exceed one second.

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switching characteristics over operating free-air temperature range, $V_{CC} = 5\text{ V}$

PARAMETER	TEST CONDITIONS	MIN	TYP [†]	MAX	UNIT
t_{PLH} Propagation delay time, low-to-high-level output	$C_L = 30\text{ pF}$, $R_L = 100\text{ }\Omega$, See Figure 2, Termination A		16	25	ns
t_{PHL} Propagation delay time, high-to-low-level output			11	20	ns
t_{PLH} Propagation delay time, low-to-high-level output	$C_L = 15\text{ pF}$, See Figure 2, Termination B		13	20	ns
t_{PHL} Propagation delay time, high-to-low-level output			9	15	ns
t_{TLH} Transition time, low-to-high-level output	$C_L = 30\text{ pF}$, $R_L = 100\text{ }\Omega$, See Figure 2, Termination A		4	20	ns
t_{THL} Transition time, high-to-low-level output			4	20	ns
t_{PZH} Output enable time to high level	$C_L = 30\text{ pF}$, $R_L = 180\text{ }\Omega$, See Figure 3		7	20	ns
t_{PZL} Output enable time to low level	$C_L = 30\text{ pF}$, $R_L = 250\text{ }\Omega$, See Figure 4		14	40	ns
t_{PHZ} Output disable time from high level	$C_L = 30\text{ pF}$, $R_L = 180\text{ }\Omega$, See Figure 3		10	30	ns
t_{PLZ} Output disable time from low level	$C_L = 30\text{ pF}$, $R_L = 250\text{ }\Omega$, See Figure 4		17	35	ns
Overshoot factor	$R_L = 100\text{ }\Omega$, See Figure 2, Termination C			10%	

[†] All typical values are at $T_A = 25^\circ\text{C}$.

SYMBOL EQUIVALENTS

DATA-SHEET PARAMETER	EIA/TIA-422-B
V_O	V_{Oa}, V_{Ob}
$ V_{OD1} $	V_O
$ V_{OD2} $	V_t
$\Delta V_{OD} $	$ V_t - \bar{V}_t $
V_{OC}	$ V_{os} $
$\Delta V_{OC} $	$ V_{os} - \bar{V}_{os} $
I_{OS}	$ I_{sa} , I_{sb} $
I_O	$ I_{xa} , I_{xb} $

PARAMETER MEASUREMENT INFORMATION

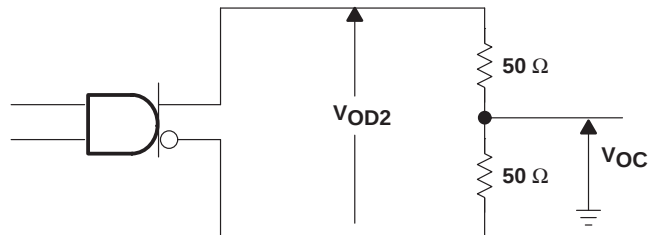
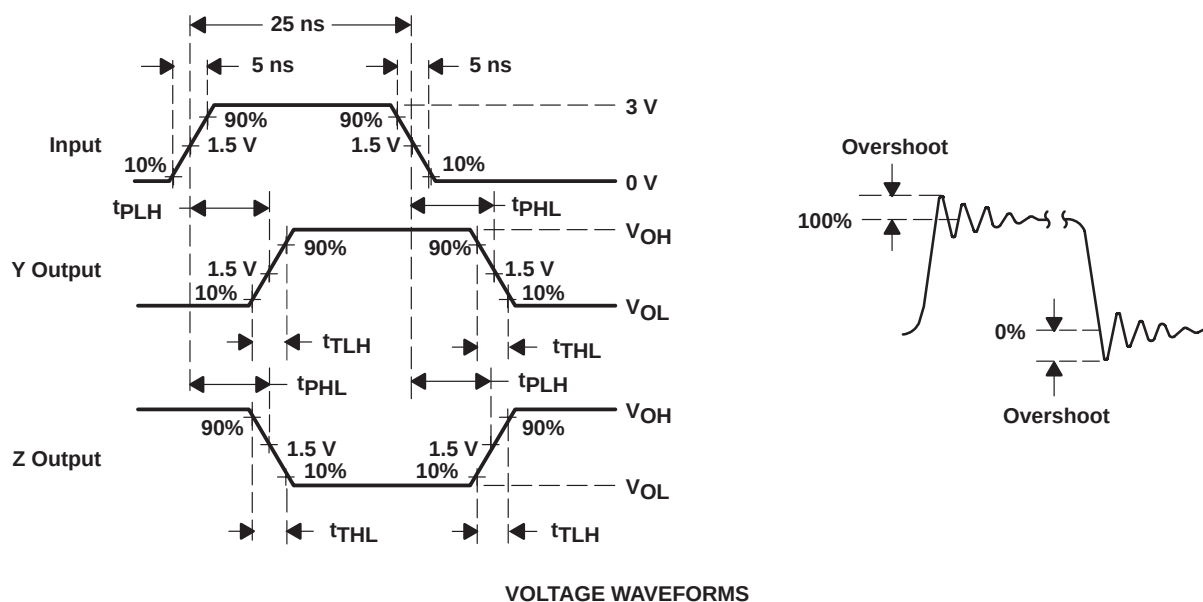
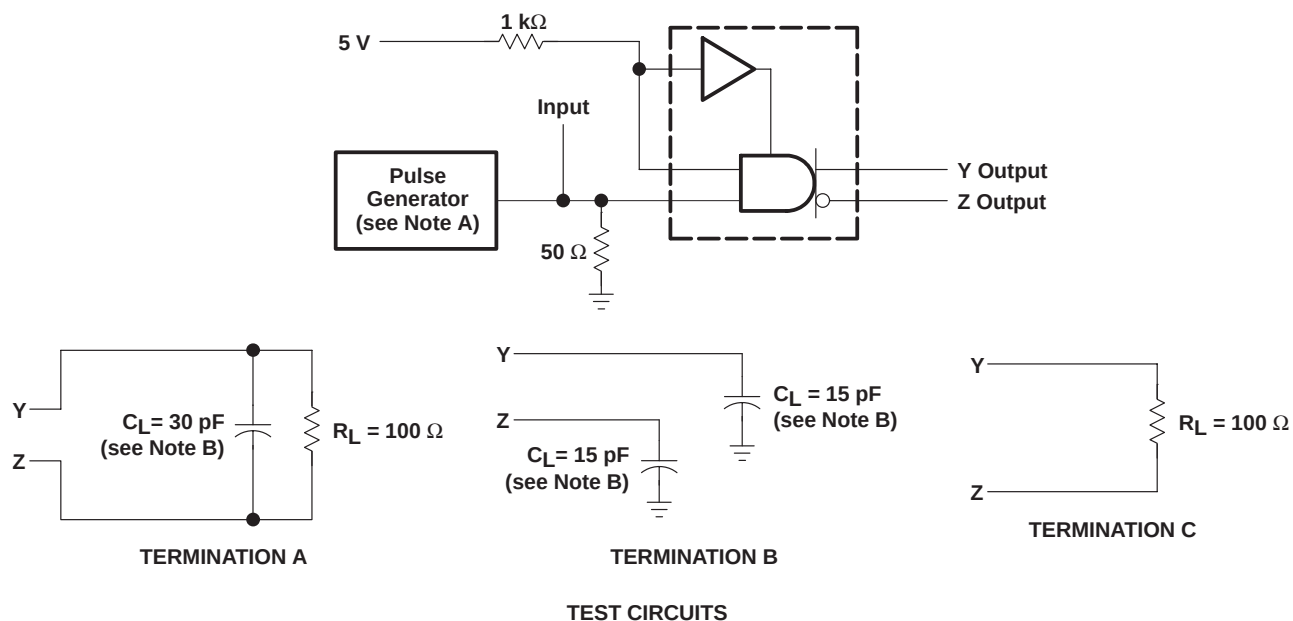


Figure 1. Differential and Common-Mode Output Voltages

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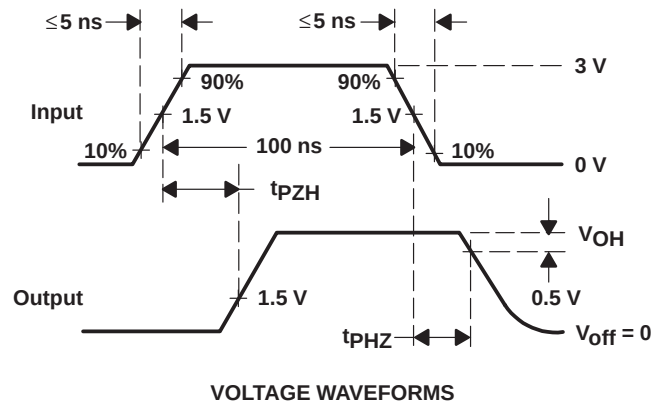
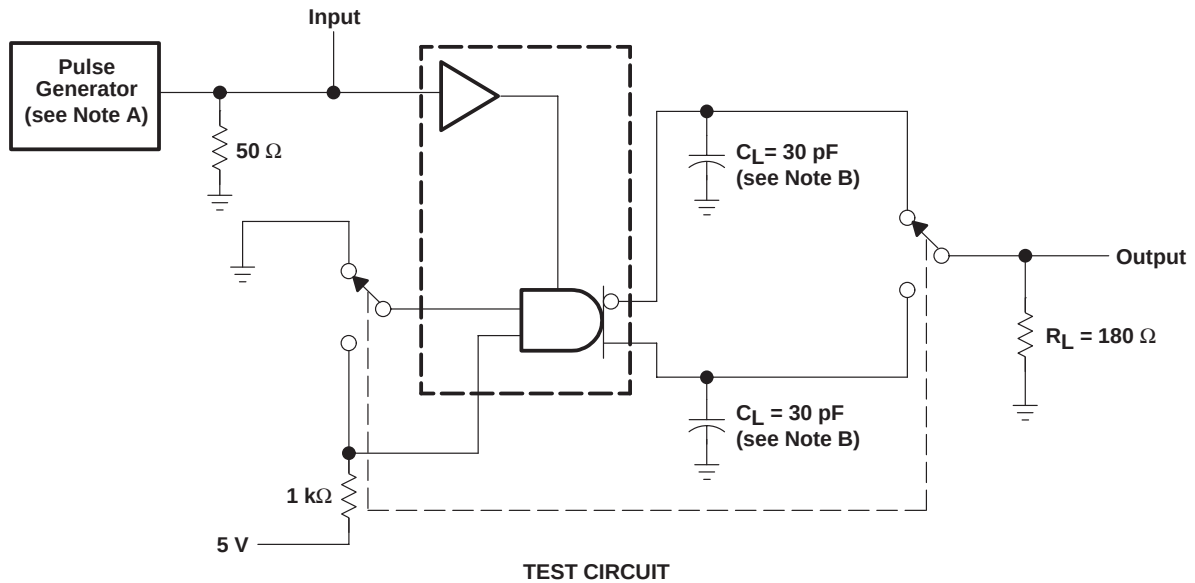
PARAMETER MEASUREMENT INFORMATION



- NOTES: A. The pulse generator has the following characteristics: $Z_O = 50$ Ω , $PRR \leq 10$ MHz.
B. C_L includes probe and jig capacitance.

Figure 2. Test Circuits, Voltage Waveforms, and Overshoot Factor

PARAMETER MEASUREMENT INFORMATION

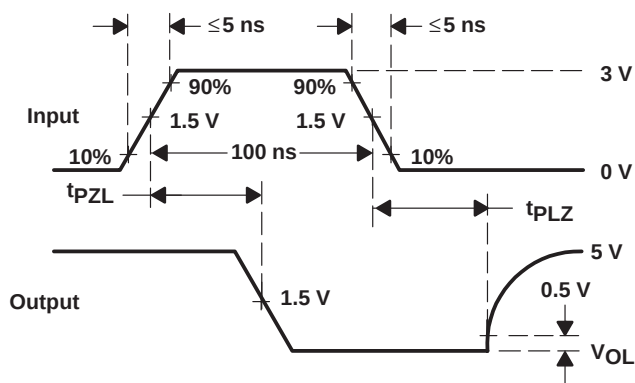


- NOTES: A. The pulse generator has the following characteristics: $Z_O = 50\ \Omega$, $PRR \leq 500\ \text{kHz}$.
B. C_L includes probe and jig capacitance.

Figure 3. Test Circuit and Voltage Waveforms

The circuit diagram shows a logic device with two inputs and two outputs. The first input is connected to a Pulse Generator (see Note A) and a 50 Ω resistor to ground. The second input is connected to a 5 V source through a 1 kΩ resistor. The first output is connected to a 5 V source through a 30 pF capacitor (see Note B). The second output is connected to a 5 V source through a 250 Ω resistor. The Output is connected to a 5 V source through a 250 Ω resistor.

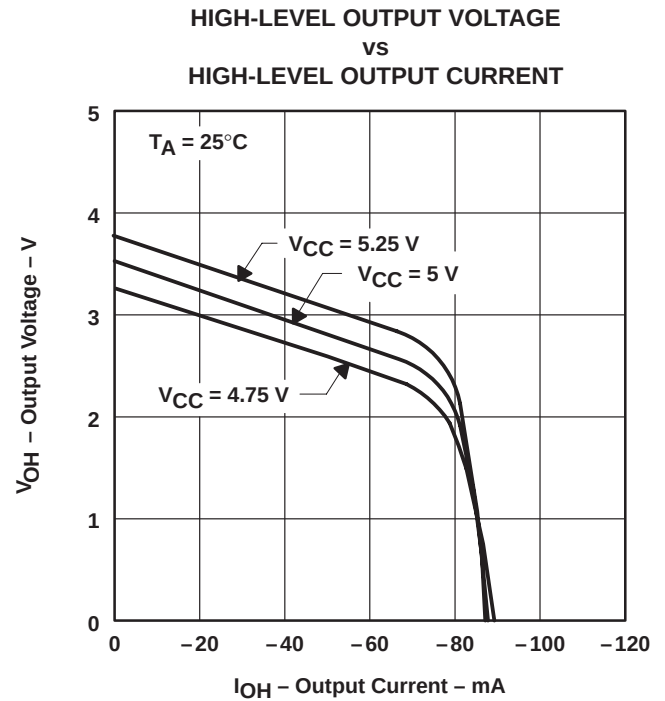
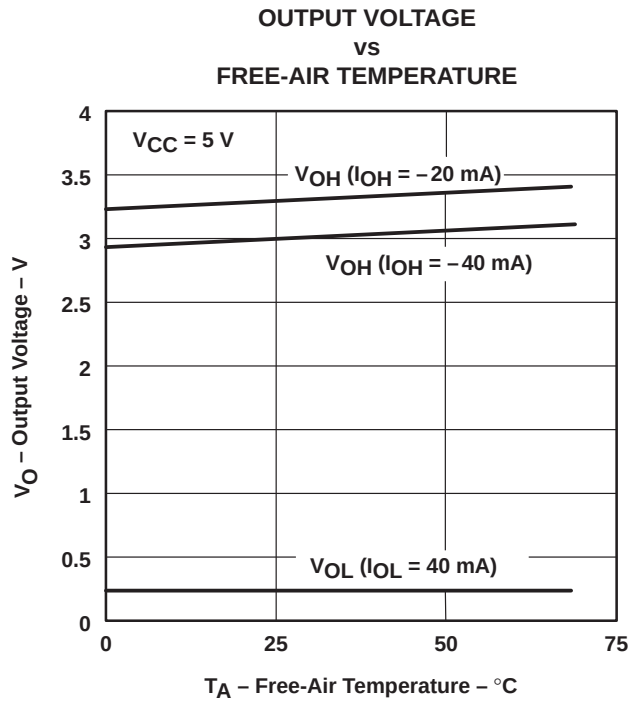
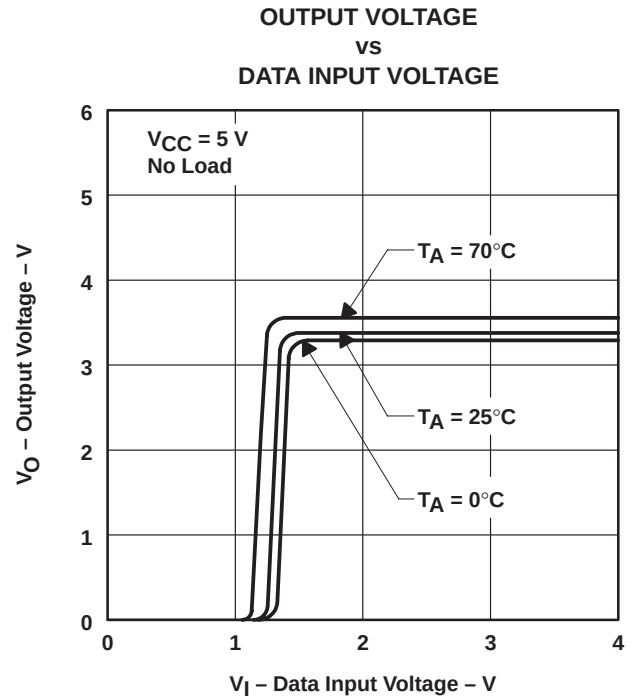
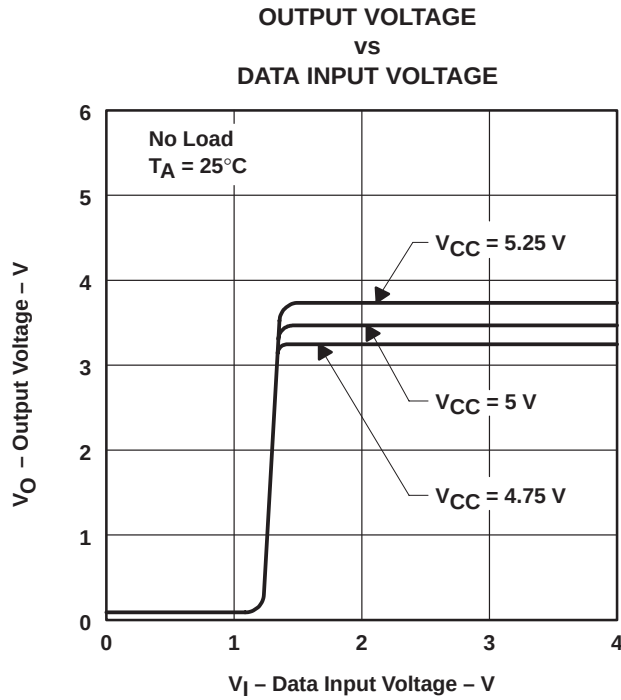
TEST CIRCUIT



VOLTAGE WAVEFORMS

Figure 4. Test Circuit and Voltage Waveform

TYPICAL CHARACTERISTICS



SN75159

DUAL DIFFERENTIAL LINE DRIVER

WITH 3-STATE OUTPUTS

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TYPICAL CHARACTERISTICS

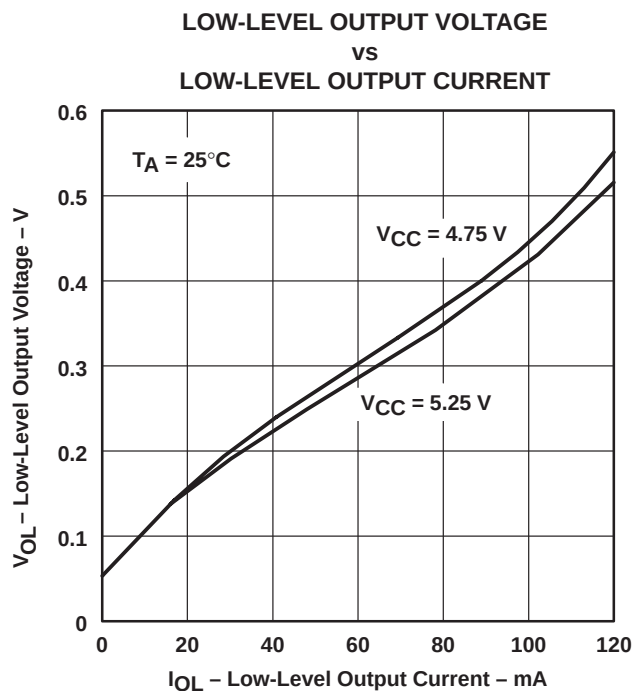


Figure 9

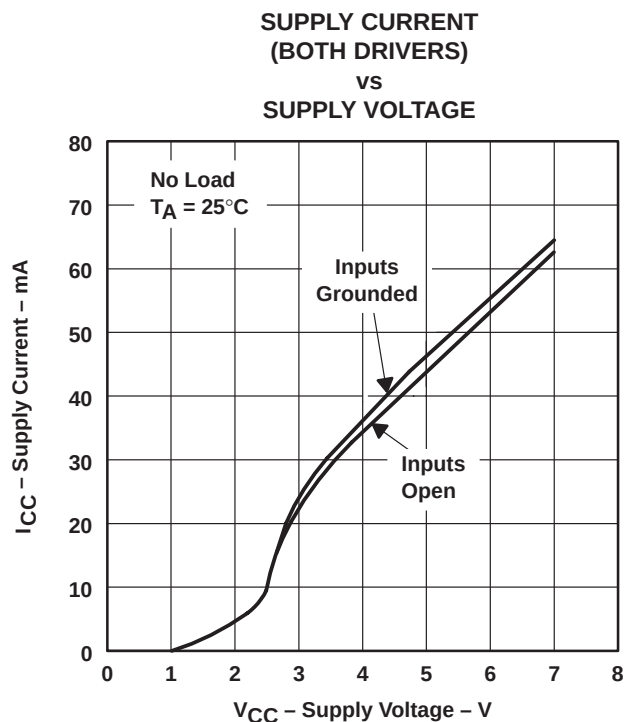


Figure 10

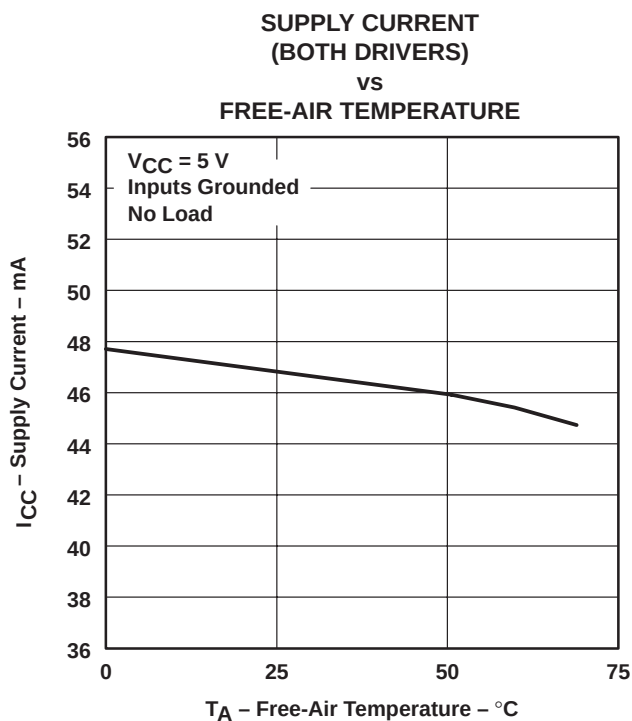


Figure 11

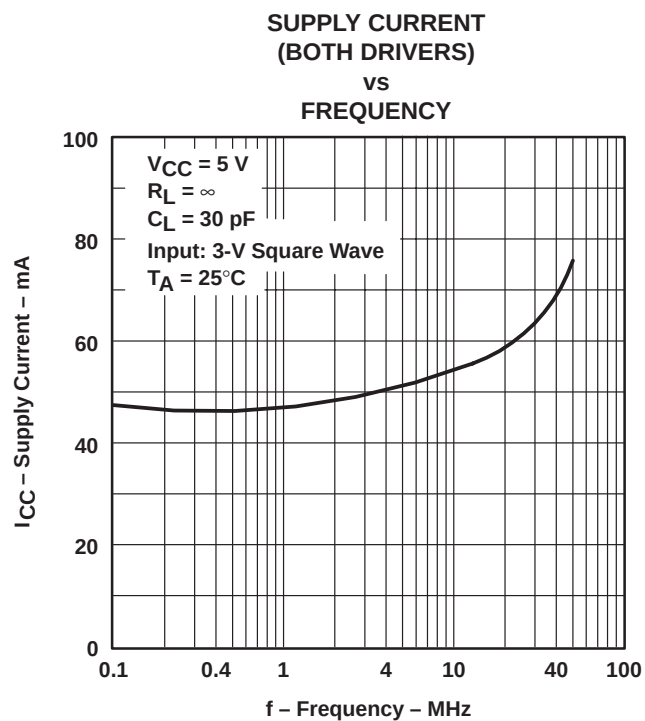
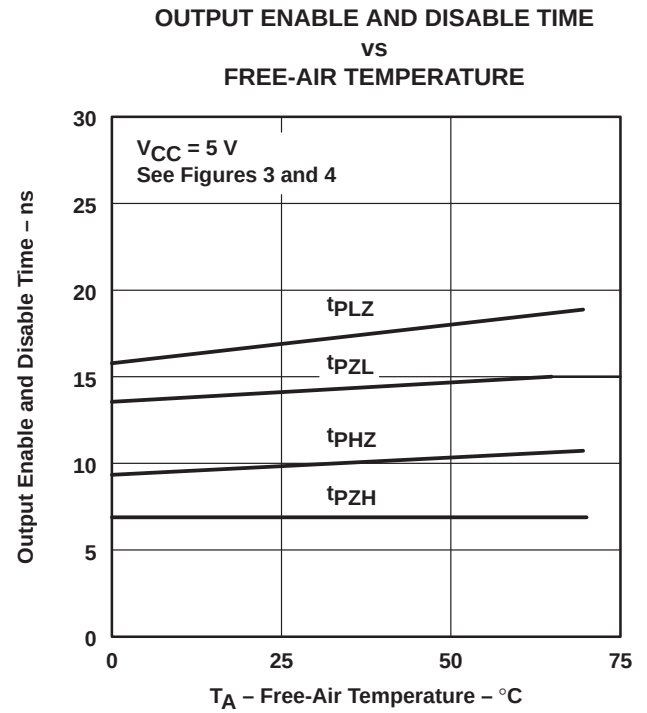
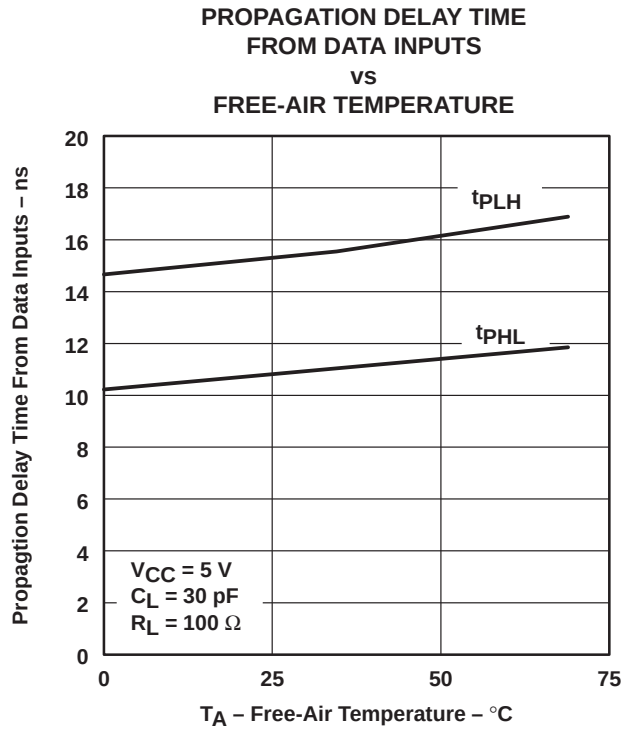


Figure 12

TYPICAL CHARACTERISTICS



PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN75159D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75159	Samples
SN75159N	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN75159N	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

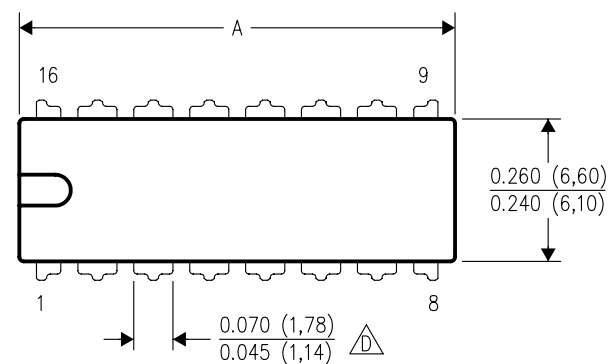
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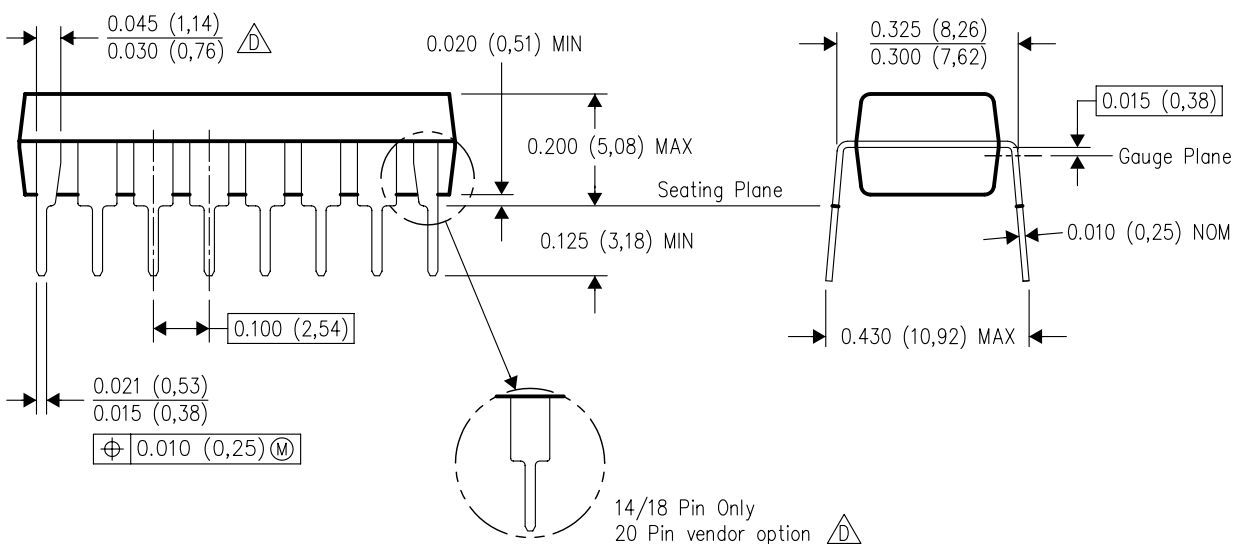
N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



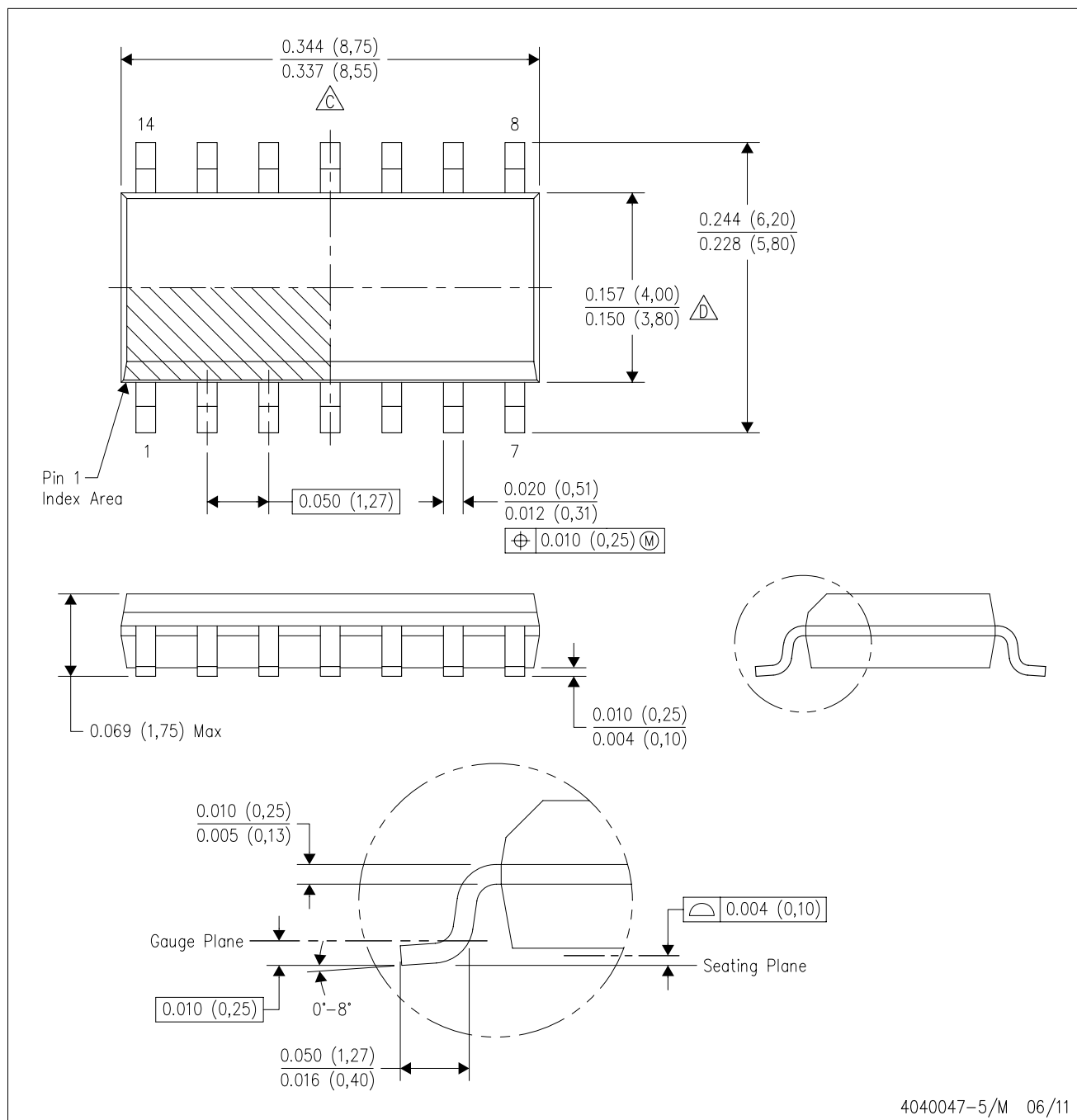
4040049/E 12/2002

NOTES:

- A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
-  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE

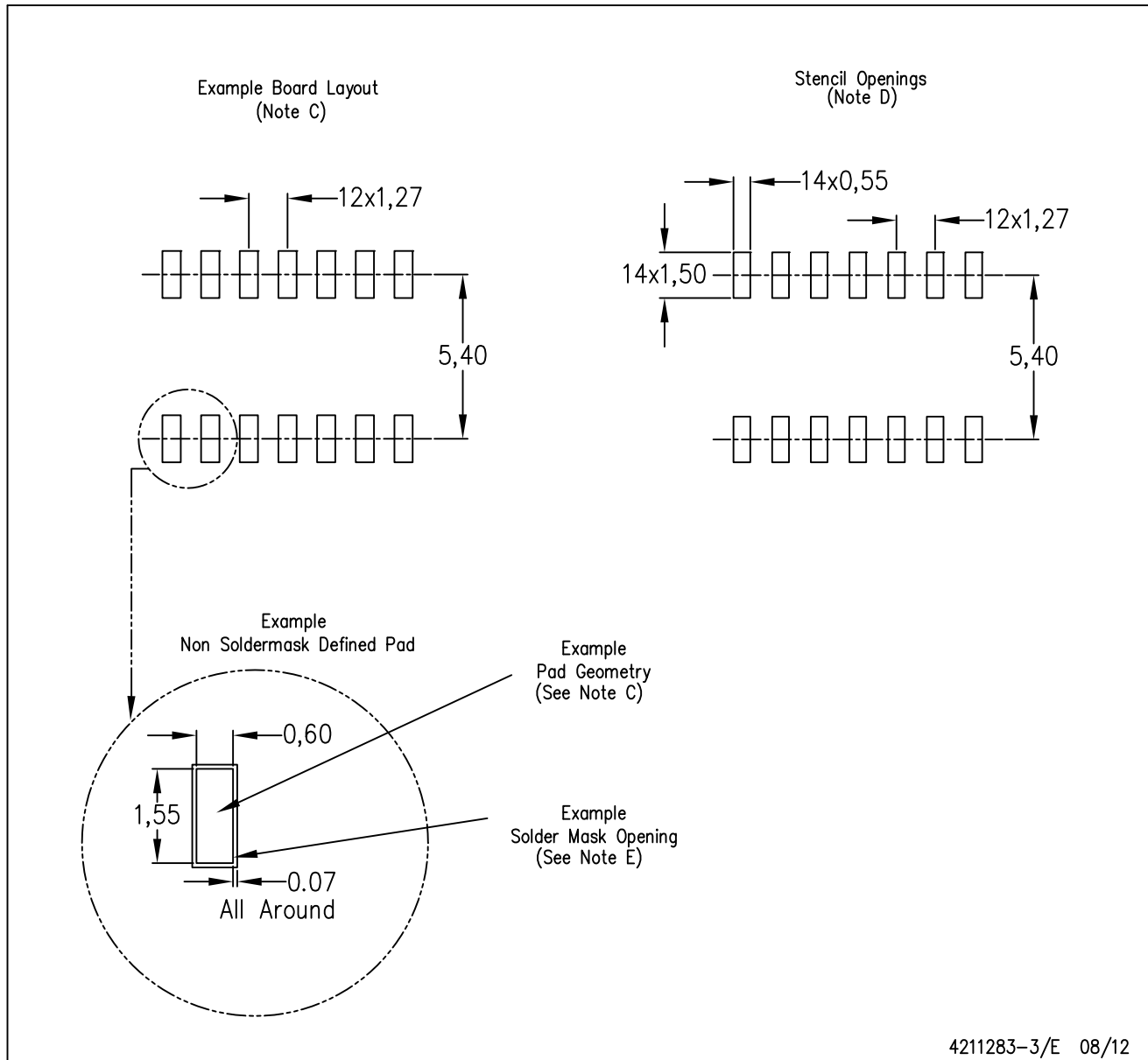


NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4211283-3/E 08/12

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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