

# DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

## 74HC/HCT109

### Dual JK flip-flop with set and reset; positive-edge trigger

Product specification

1997 Nov 25

Supersedes data of December 1990

File under Integrated Circuits, IC06

## Dual JK flip-flop with set and reset; positive-edge trigger

**74HC/HCT109**

### FEATURES

- J,  $\bar{K}$  inputs for easy D-type flip-flop
- Toggle flip-flop or “do nothing” mode
- Output capability: standard
- $I_{CC}$  category: flip-flops

### GENERAL DESCRIPTION

The 74HC/HCT109 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT109 are dual positive-edge triggered, JK flip-flops with individual J,  $\bar{K}$  inputs, clock (CP) inputs, set

( $\bar{S}_D$ ) and reset ( $\bar{R}_D$ ) inputs; also complementary Q and  $\bar{Q}$  outputs.

The set and reset are asynchronous active LOW inputs and operate independently of the clock input.

The J and  $\bar{K}$  inputs control the state changes of the flip-flops as described in the mode select function table.

The J and  $\bar{K}$  inputs must be stable one set-up time prior to the LOW-to-HIGH clock transition for predictable operation.

The JK design allows operation as a D-type flip-flop by tying the J and  $\bar{K}$  inputs together.

Schmitt-trigger action in the clock input makes the circuit highly tolerant to slower clock rise and fall times.

### QUICK REFERENCE DATA

$GND = 0 \text{ V}$ ;  $T_{amb} = 25 \text{ }^{\circ}\text{C}$ ;  $t_r = t_f = 6 \text{ ns}$

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
$t_{PHL}/t_{PLH}$	propagation delay nCP to nQ, n $\bar{Q}$	$C_L = 15 \text{ pF}$ ; $V_{CC} = 5 \text{ V}$	15	17	ns
	n $\bar{S}_D$ to nQ, n $\bar{Q}$		12	14	
	n $\bar{R}_D$ to nQ, n $\bar{Q}$		12	15	
	maximum clock frequency		75	61	
$C_I$	input capacitance		3.5	3.5	pF
$C_{PD}$	power dissipation capacitance per flip-flop	notes 1 and 2	20	22	pF

### Notes

1.  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ ):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

$f_i$  = input frequency in MHz

$f_o$  = output frequency in MHz

$\sum (C_L \times V_{CC}^2 \times f_o)$  = sum of outputs

$C_L$  = output load capacitance in pF

$V_{CC}$  = supply voltage in V

2. For HC the condition is  $V_I = GND$  to  $V_{CC}$   
For HCT the condition is  $V_I = GND$  to  $V_{CC} - 1.5 \text{ V}$ .

### ORDERING INFORMATION

See “[74HC/HCT/HCU/HCMOS Logic Package Information](#)”.

# Dual JK flip-flop with set and reset; positive-edge trigger

74HC/HCT109

## PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 15	$1\bar{R}_D, 2\bar{R}_D$	asynchronous reset-direct input (active LOW)
2, 14, 3, 13	$1J, 2J, 1\bar{K}, 2\bar{K}$	synchronous inputs; flip-flops 1 and 2
4, 12	$1CP, 2CP$	clock input (LOW-to-HIGH, edge-triggered)
5, 11	$1\bar{S}_D, 2\bar{S}_D$	asynchronous set-direct input (active LOW)
6, 10	$1Q, 2Q$	true flip-flop outputs
7, 9	$1\bar{Q}, 2\bar{Q}$	complement flip-flop outputs
8	GND	ground (0 V)
16	$V_{CC}$	positive supply voltage

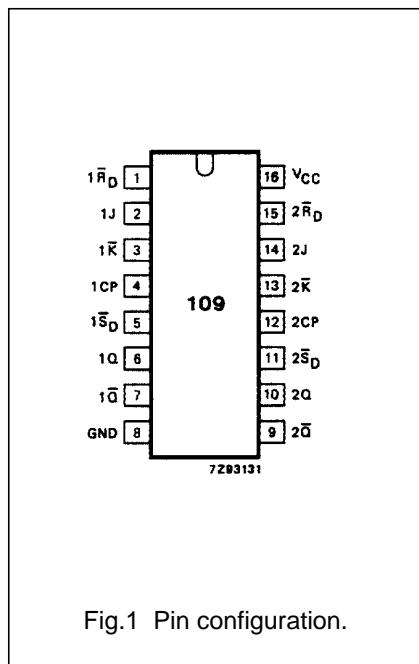


Fig.1 Pin configuration.

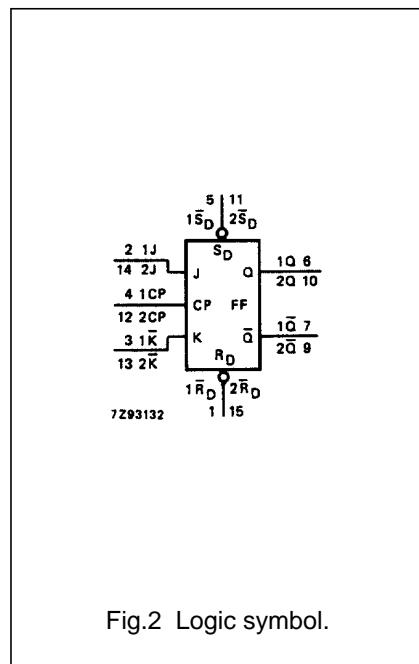


Fig.2 Logic symbol.

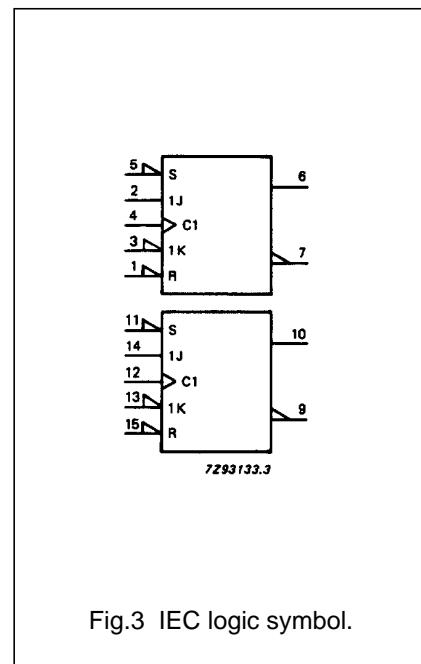


Fig.3 IEC logic symbol.

# Dual JK flip-flop with set and reset; positive-edge trigger

74HC/HCT109

## FUNCTION TABLE

OPERATING MODE	INPUTS					OUTPUTS	
	$\bar{S}_D$	$\bar{R}_D$	CP	J	$\bar{K}$	Q	$\bar{Q}$
asynchronous set	L	H	X	X	X	H	L
asynchronous reset	H	L	X	X	X	L	H
undetermined	L	L	X	X	X	H	H
toggle	H	H	↑	h	I	$\bar{q}$	q
load "0" (reset)	H	H	↑	I	I	L	H
load "1" (set)	H	H	↑	h	h	H	L
hold "no change"	H	H	↑	I	h	q	$\bar{q}$

## Notes

1. H = HIGH voltage level  
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition  
L = LOW voltage level  
I = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition  
q = lower case letters indicate the state of the referenced output one set-up time prior to the LOW-to-HIGH CP transition  
X = don't care  
↑ = LOW-to-HIGH CP transition

Fig.4 Functional diagram.

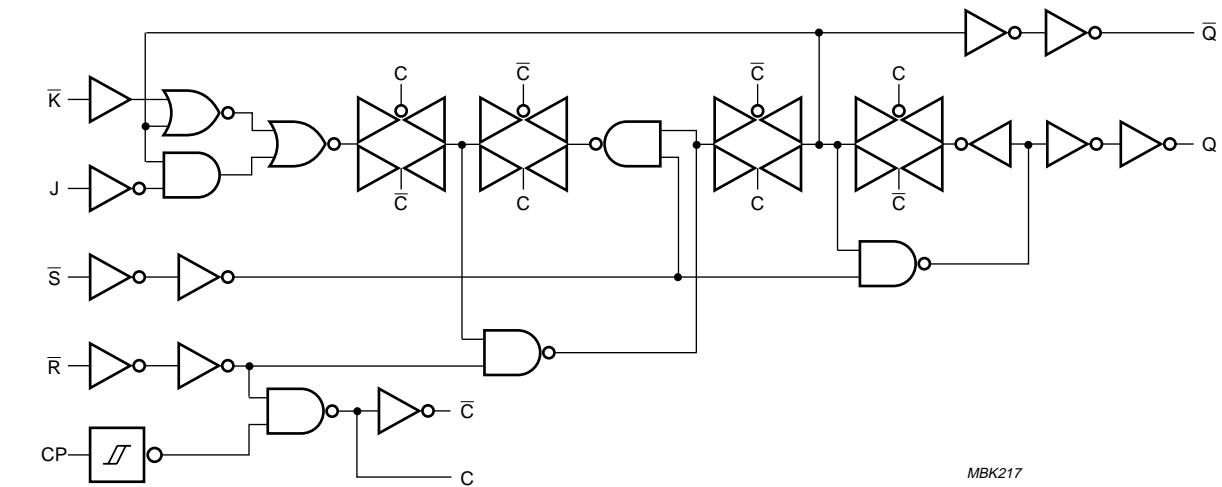


Fig.5 Logic diagram (one flip-flop).

## PACKAGE OUTLINES

See "74HC/HCT/HCU/HCMOS Logic Package Outlines".

Dual JK flip-flop with set and reset;  
positive-edge trigger

74HC/HCT109

**DC CHARACTERISTICS FOR 74HC**

For the DC characteristics see "*74HC/HCT/HCU/HCMOS Logic Family Specifications*".

Output capability: standard

I<sub>CC</sub> category: flip-flops

**AC CHARACTERISTICS FOR 74HC**

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)							UNIT	TEST CONDITIONS				
		74HC								V <sub>CC</sub> (V)	WAVEFORMS			
		+25			-40 to +85		-40 to +125							
		min.	typ.	max.	min.	max.	min.	max.						
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay nCP to nQ, n $\bar{Q}$		50 18 14	175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig.6			
t <sub>PLH</sub>	propagation delay n $\bar{S}_D$ to nQ		30 11 9	120 24 20		150 30 26		180 36 31	ns	2.0 4.5 6.0	Fig.7			
t <sub>PHL</sub>	propagation delay n $\bar{S}_D$ to n $\bar{Q}$		41 15 12	155 31 26		195 39 33		235 47 40	ns	2.0 4.5 6.0	Fig.7			
t <sub>PHL</sub>	propagation delay n $\bar{R}_D$ to nQ		41 15 12	185 37 31		230 46 39		280 56 48	ns	2.0 4.5 6.0	Fig.7			
t <sub>PLH</sub>	propagation delay n $\bar{R}_D$ to n $\bar{Q}$		39 14 11	170 34 29		215 43 37		255 51 43	ns	2.0 4.5 6.0	Fig.7			
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig.6			
t <sub>W</sub>	clock pulse width HIGH or LOW	80 16 14	19 7 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig.6			
t <sub>W</sub>	set or reset pulse width HIGH or LOW	80 16 14	14 5 4		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig.7			
t <sub>rem</sub>	removal time n $\bar{S}_D$ , n $\bar{R}_D$ to nCP	70 14 12	19 7 6		90 18 15		105 21 18		ns	2.0 4.5 6.0	Fig.7			
t <sub>su</sub>	set-up time nJ, n $\bar{K}$ to nCP	70 14 12	17 6 5		90 18 15		105 21 18		ns	2.0 4.5 6.0	Fig.6			
t <sub>h</sub>	hold time nJ, n $\bar{K}$ to nCP	5 5 5	0 0 0		5 5 5		5 5 5		ns	2.0 4.5 6.0	Fig.6			
f <sub>max</sub>	maximum clock pulse frequency	6.0 30 35	22 68 81		5.0 24 28		4.0 20 24		MHz	2.0 4.5 6.0	Fig.6			

# Dual JK flip-flop with set and reset; positive-edge trigger

74HC/HCT109

## DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see "[74HC/HCT/HCU/HCMOS Logic Family Specifications](#)".

Output capability: standard

I<sub>CC</sub> category: flip-flops

## AC CHARACTERISTICS FOR 74HCT

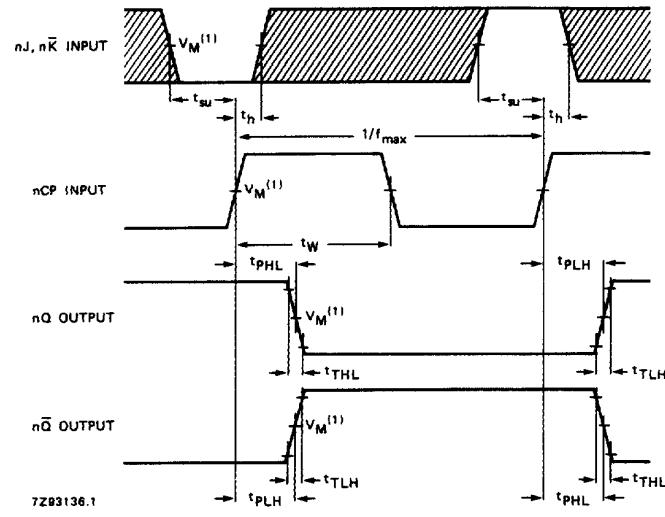
GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)							UNIT	TEST CONDITIONS				
		74HCT								V <sub>CC</sub> (V)	WAVEFORMS			
		+25			−40 to +85		−40 to +125							
		min.	typ.	max.	min.	max.	min.	max.						
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay nCP to nQ, n $\bar{Q}$		20	35		44		53	ns	4.5	Fig.6			
t <sub>PLH</sub>	propagation delay n $\bar{S}_D$ to nQ		13	26		33		39	ns	4.5	Fig.7			
t <sub>PHL</sub>	propagation delay n $\bar{S}_D$ to n $\bar{Q}$		19	35		44		53	ns	4.5	Fig.7			
t <sub>PHL</sub>	propagation delay n $\bar{R}_D$ to nQ		19	35		44		53	ns	4.5	Fig.7			
t <sub>PLH</sub>	propagation delay n $\bar{R}_D$ to n $\bar{Q}$		16	32		40		48	ns	4.5	Fig.7			
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		7	15		19		22	ns	4.5	Fig.6			
t <sub>W</sub>	clock pulse width HIGH or LOW	18	9		23		27		ns	4.5	Fig.6			
t <sub>W</sub>	set or reset pulse width HIGH or LOW	16	8		20		24		ns	4.5	Fig.7			
t <sub>rem</sub>	removal time n $\bar{S}_D$ , n $\bar{R}_D$ to nCP	16	8		20		24		ns	4.5	Fig.7			
t <sub>su</sub>	set-up time nJ, nK to nCP	18	8		23		27		ns	4.5	Fig.6			
t <sub>h</sub>	hold time nJ, n $\bar{K}$ to nCP	3	−3		3		3		ns	4.5	Fig.6			
f <sub>max</sub>	maximum clock pulse frequency	27	55		22		18		MHz	4.5	Fig.6			

# Dual JK flip-flop with set and reset; positive-edge trigger

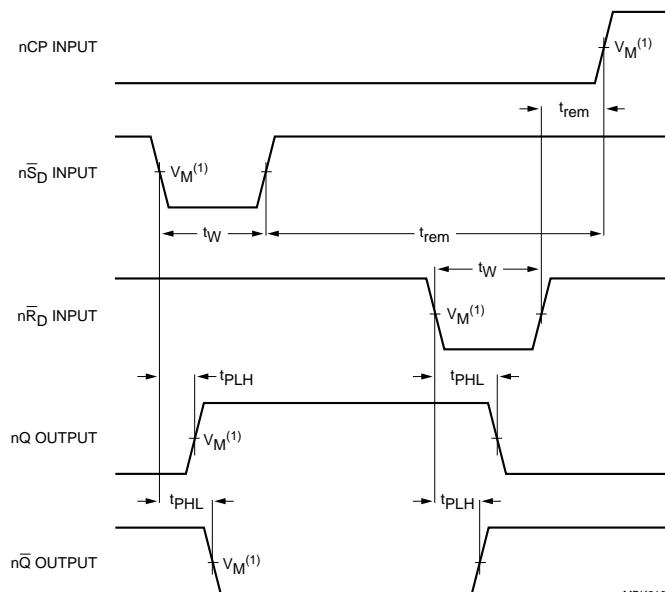
74HC/HCT109

## AC WAVEFORMS



The shaded areas indicate when the input is permitted to change for predictable output performance.

Fig.6 Waveforms showing the clock (nCP) to output (nQ, nQ̄) propagation delays, the clock pulse width, the nJ, nK̄ to nCP set-up, the nCP to nJ, nK hold times, the output transition times and the maximum clock pulse frequency.



(1) HC:  $V_M = 50\%$ ;  $V_I = \text{GND to } V_{CC}$ .  
HCT:  $V_M = 1.3 \text{ V}$ ;  $V_I = \text{GND to } 3 \text{ V}$ .

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Fig.7 Waveforms showing the set ( $n\bar{S}_D$ ) and reset ( $n\bar{R}_D$ ) input to output ( $nQ$ ,  $n\bar{Q}$ ) propagation delays, the set and reset pulse widths and the  $n\bar{R}_D$ ,  $n\bar{S}_D$  to nCP removal time.

# Dual JK flip-flop with set and reset; positive-edge trigger

74HC/HCT109

## SOLDERING

### Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our "IC Package Databook" (order code 9398 652 90011).

### DIP

#### SOLDERING BY DIPPING OR BY WAVE

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ( $T_{stg\ max}$ ). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

#### REPAIRING SOLDERED JOINTS

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

### SO, SSOP and TSSOP

#### REFLOW SOLDERING

Reflow soldering techniques are suitable for all SO, SSOP and TSSOP packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method.

Typical reflow temperatures range from 215 to 250 °C. Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

#### WAVE SOLDERING

Wave soldering can be used for all SO packages. Wave soldering is **not** recommended for SSOP and TSSOP packages, because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

If wave soldering is used - **and cannot be avoided for SSOP and TSSOP packages** - the following conditions must be observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- The longitudinal axis of the package footprint must be parallel to the solder flow and must incorporate solder thieves at the downstream end.

#### Even with these conditions:

- **Only consider wave soldering SSOP packages that have a body width of 4.4 mm, that is SSOP16 (SOT369-1) or SSOP20 (SOT266-1).**
- **Do not consider wave soldering TSSOP packages with 48 leads or more, that is TSSOP48 (SOT362-1) and TSSOP56 (SOT364-1).**

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

#### REPAIRING SOLDERED JOINTS

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

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**Dual JK flip-flop with set and reset;  
positive-edge trigger**

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**74HC/HCT109**

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**DEFINITIONS**

<b>Data sheet status</b>	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
<b>Limiting values</b>	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
<b>Application information</b>	
Where application information is given, it is advisory and does not form part of the specification.	

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