

July 1996

Features

- 14A, 60V
- $r_{DS(ON)} = 0.100\Omega$
- *Temperature Compensating* PSPICE Model
- Can be Driven Directly from CMOS, NMOS, and TTL Circuits
- Peak Current vs Pulse Width Curve
- UIS Rating Curve
- +175°C Operating Temperature

Description

The RFD14N06L, RFD14N06LSM, and RFP14N06L are N-channel power MOSFETs manufactured using the MegaFET process. This process, which uses feature sizes approaching those of LSI integrated circuits, gives optimum utilization of silicon, resulting in outstanding performance. They were designed for use in applications such as switching regulators, switching converters, motor drivers and relay drivers. This performance is accomplished through a special gate oxide design which provides full rated conductance at gate bias in the 3V - 5V range, thereby facilitating true on-off power control directly from logic level (5V) integrated circuits.

PACKAGE AVAILABILITY

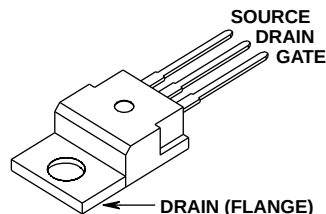
PART NUMBER	PACKAGE	BRAND
RFD14N06L	TO-251AA	14N06L
RFD14N06LSM	TO-252AA	14N06L
RFP14N06L	TO-220AB	FP14N06L

NOTE: When ordering, use the entire part number. Add the suffix 9A, to obtain the TO-252AA variant in tape and reel, i.e. RFD14N06LSM9A.

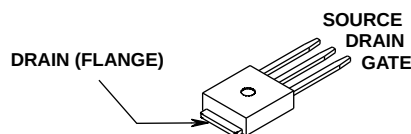
Formerly developmental type TA09870.

Packaging

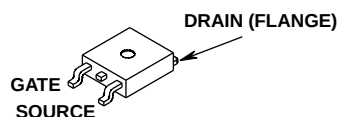
JEDEC TO-220AB



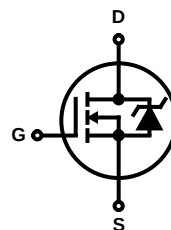
JEDEC TO-251AA



JEDEC TO-252AA



Symbol



Absolute Maximum Ratings $T_C = +25^\circ\text{C}$

	RFD14N06L, RFD14N06LSM, RFP14N06L	UNITS
Drain-Source Voltage	60	V
Drain-Gate Voltage	60	V
Gate-Source Voltage	± 10	V
Drain Current		
RMS Continuous	14	A
Pulsed Drain Current	Refer to Peak Current Curve	
Pulsed Avalanche Rating	Refer to UIS Curve	
Power Dissipation		
$T_C = +25^\circ\text{C}$	48	W
Derate above +25°C	0.32	W/°C
Operating and Storage Temperature	-55 to +175	°C
Soldering Temperature of Leads for 10s.	260	°C

Specifications RFD14N06L, RFD14N06LSM, RFP14N06L

Electrical Specifications $T_C = +25^{\circ}\text{C}$, Unless Otherwise Specified

PARAMETERS	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Drain-Source Breakdown Voltage	BV _{DSS}	I _D = 250μA, V _{GS} = 0V		60	-	-	V
Gate Threshold Voltage	V _{GS(TH)}	V _{GS} = V _{DS} , I _D = 250μA		1	-	2	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 60V, V _{GS} = 0V	T _C = +25°C	-	-	1	μA
			T _C = +150°C	-	-	50	μA
Gate-Source Leakage Current	I _{GSS}	V _{GS} = ±10V		-	-	100	nA
On Resistance	r _{DS(ON)}	I _D = 14A, V _{GS} = 5V		-	-	0.100	Ω
Turn-On Time	t _{ON}	V _{DD} = 30V, I _D = 7A, R _L = 4.28Ω, V _{GS} = 5V, R _{GS} = 0.6Ω		-	-	60	ns
Turn-On Delay Time	t _{D(ON)}			-	13	-	ns
Rise Time	t _R			-	24	-	ns
Turn-Off Delay Time	t _{D(OFF)}			-	42	-	ns
Fall Time	t _F			-	16	-	ns
Turn-Off Time	t _{OFF}			-	-	100	ns
Total Gate Charge	Q _{G(TOT)}	V _{GS} = 0V to 10V	V _{DD} = 48V, I _D = 14A, R _L = 3.43Ω	-	-	40	nC
Gate Charge at 5V	Q _{G(5)}	V _{GS} = 0V to 5V		-	-	25	nC
Threshold Gate Charge	Q _{G(TH)}	V _{GS} = 0V to 1V		-	-	1.5	nC
Input Capacitance	C _{ISS}	V _{DS} = 25V, V _{GS} = 0V, f = 1MHz		-	670	-	pF
Output Capacitance	C _{OSS}			-	185	-	pF
Reverse Transfer Capacitance	C _{RSS}			-	50	-	pF
Thermal Resistance Junction-to-Case	R _{θJC}			-	-	3.125	°C/W
Thermal Resistance Junction-to-Ambient	R _{θJA}	TO-251 and TO-252		-	-	100	°C/W
		TO-220		-	-	80	°C/W

Source-Drain Diode Ratings and Specifications

PARAMETERS	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Forward Voltage	V_{SD}	$I_{SD} = 14\text{A}$	-	-	1.5	V
Reverse Recovery Time	t_{RR}	$I_{SD} = 14\text{A}$, $dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	-	125	ns

Typical Performance Curves

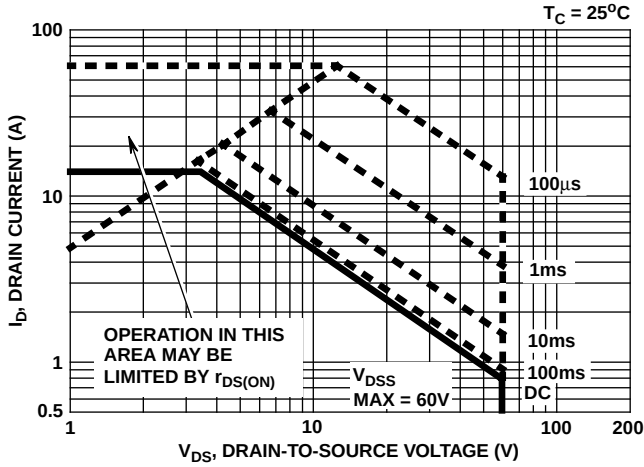


FIGURE 1. SAFE OPERATING AREA CURVE

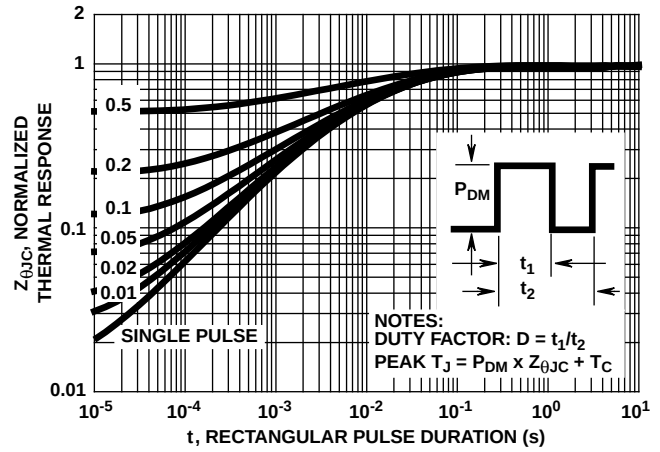


FIGURE 2. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

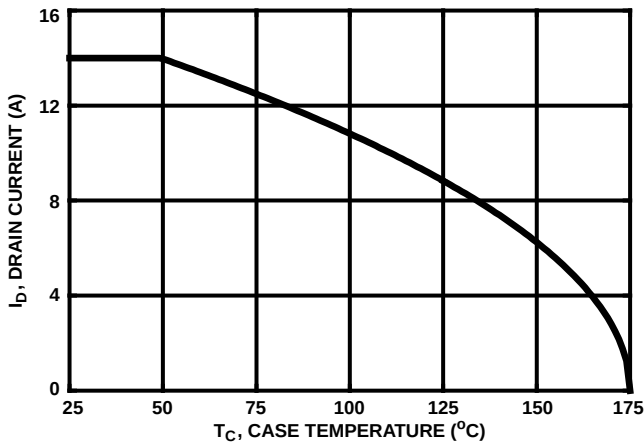


FIGURE 3. MAXIMUM CONTINUOUS DRAIN CURRENT vs TEMPERATURE

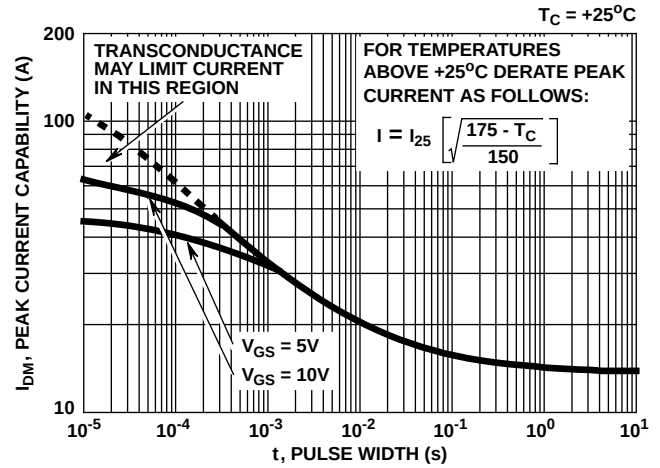


FIGURE 4. PEAK CURRENT CAPABILITY

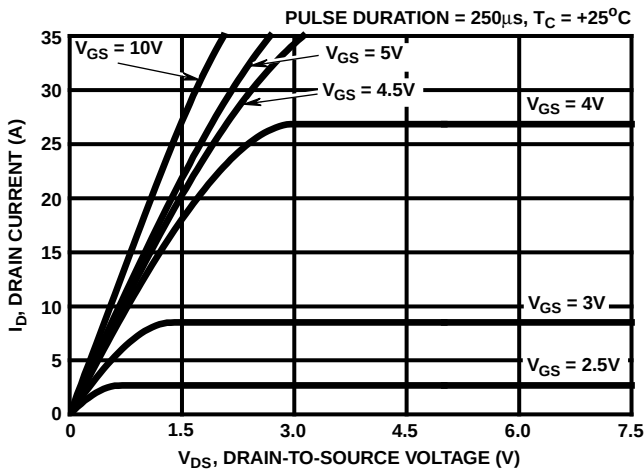


FIGURE 5. TYPICAL SATURATION CHARACTERISTICS

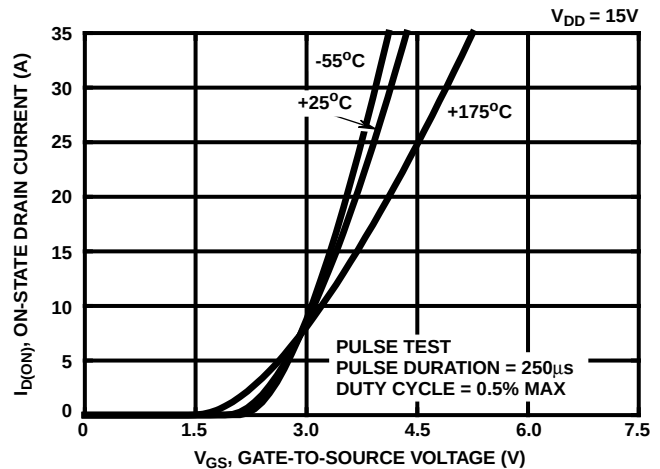


FIGURE 6. TYPICAL TRANSFER CHARACTERISTICS

Typical Performance Curves (Continued)

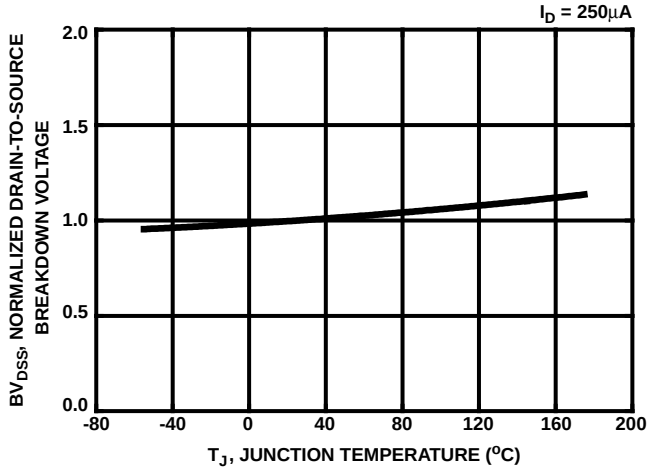


FIGURE 7. NORMALIZED DRAIN-SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

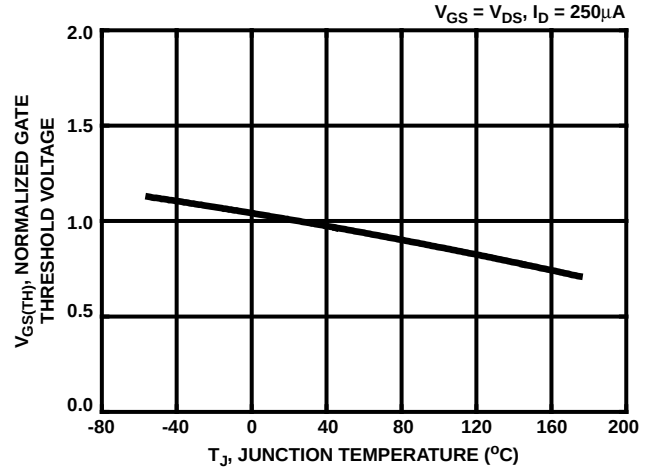


FIGURE 8. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

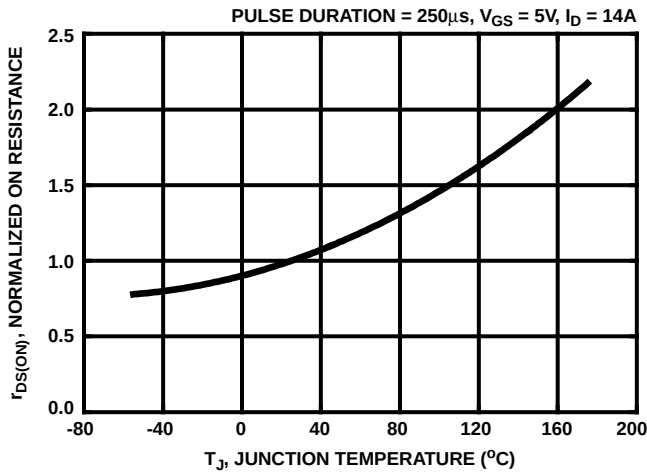


FIGURE 9. NORMALIZED $r_{DS(ON)}$ vs JUNCTION TEMPERATURE

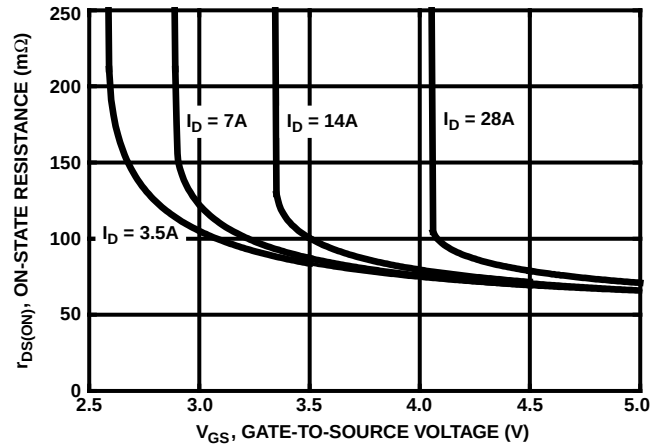


FIGURE 10. $r_{DS(ON)}$ FOR VARYING CONDITIONS OF GATE VOLTAGE AND DRAIN CURRENT

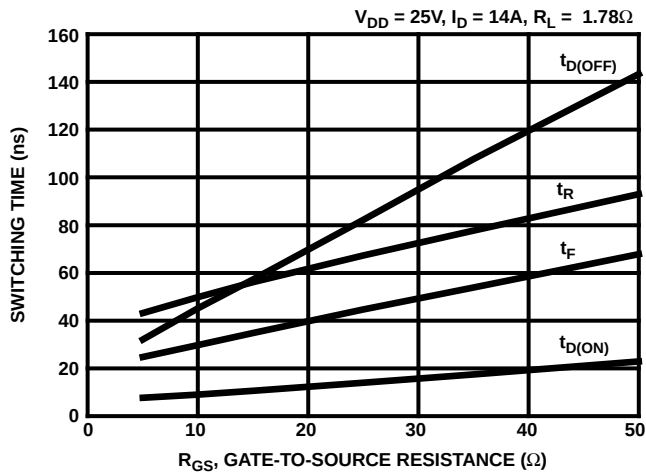


FIGURE 11. SWITCHING TIME AS A FUNCTION OF GATE RESISTANCE

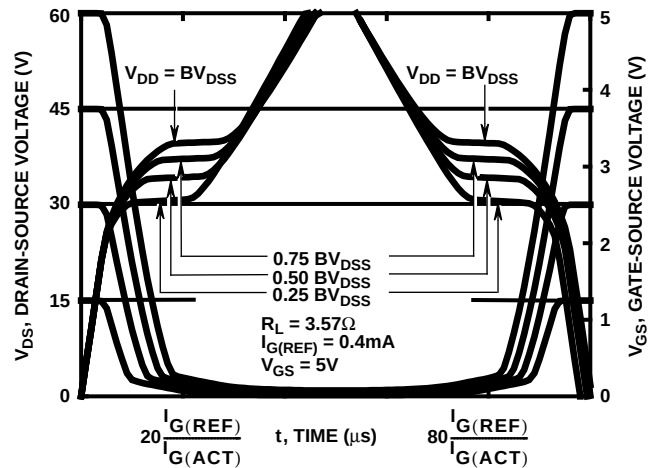


FIGURE 12. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT. REFER TO HARRIS APPLICATION NOTES AN7254 AND AN7260

Typical Performance Curves (Continued)

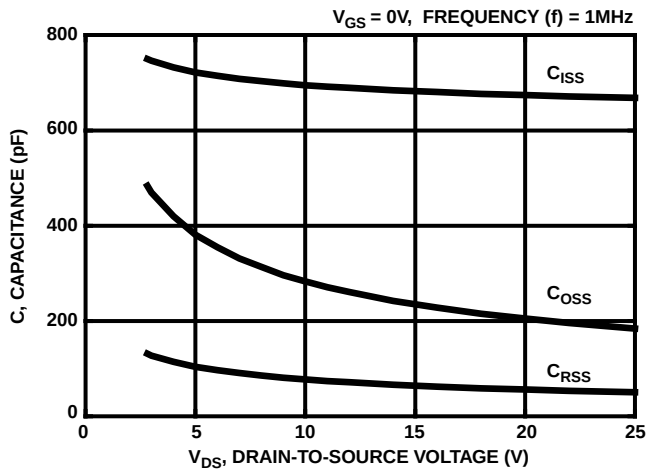


FIGURE 13. TYPICAL CAPACITANCE vs VOLTAGE

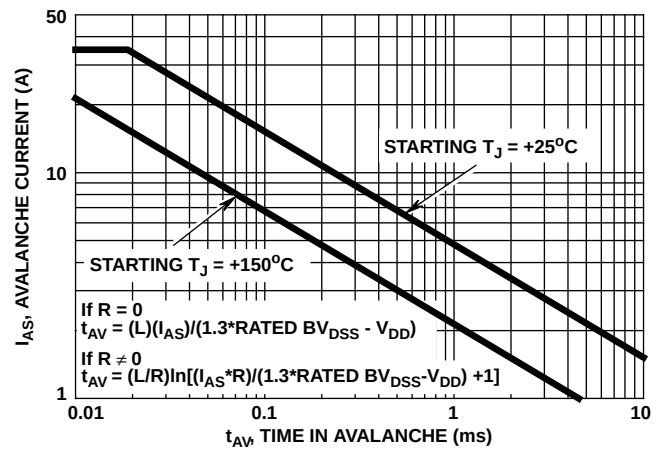


FIGURE 14. UNCLAMPED INDUCTIVE SWITCHING. REFER TO HARRIS APPLICATION NOTES AN9321 AND AN9322

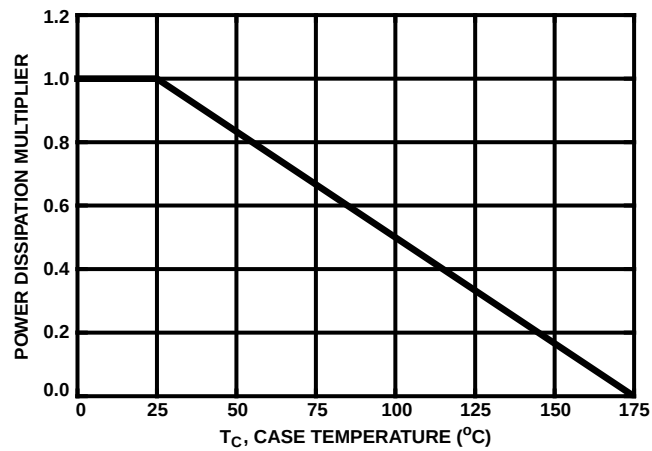


FIGURE 15. NORMALIZED POWER DISSIPATION vs TEMPERATURE DERATING CURVE

Test Circuits and Waveforms

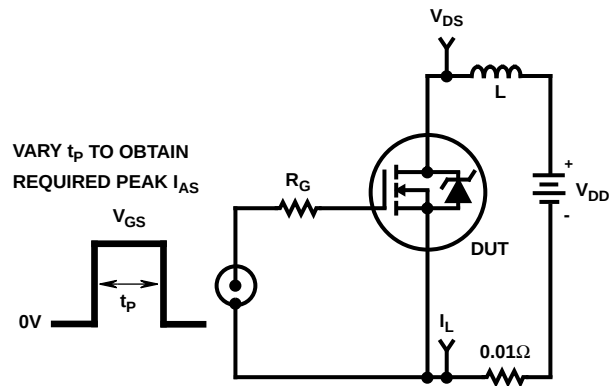


FIGURE 16. UNCLAMPED ENERGY TEST CIRCUIT

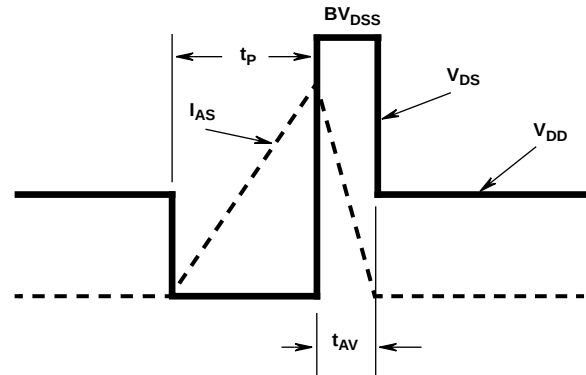


FIGURE 17. UNCLAMPED ENERGY WAVEFORMS

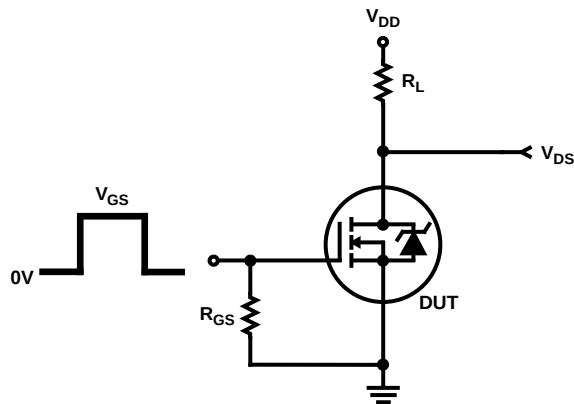


FIGURE 18. RESISTIVE SWITCHING TEST CIRCUIT

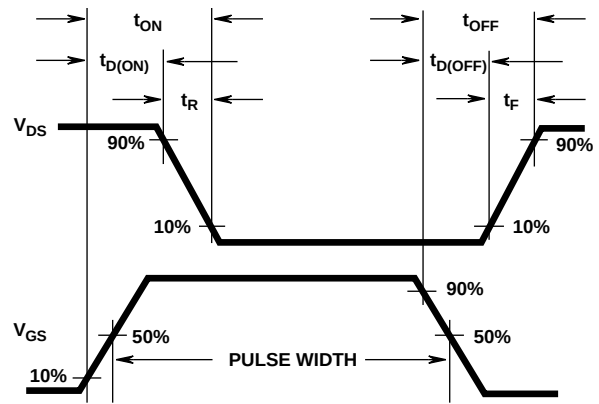


FIGURE 19. RESISTIVE SWITCHING WAVEFORMS

Temperature Compensated PSPICE Model for the RFD14N06L, RFD14N06LSM, RFP14N06L

```
.SUBCKT RFP14N06L 2 1 3 ; rev 9/15/94
CA 12 8 1.464e-9
CB 15 14 1.64e-9
CIN 6 8 6.17e-10
```

```
DBODY 7 5 DBDMOD
DBREAK 5 11 DBKMOD
DPLCAP 10 5 DPLCAPMOD
```

```
EBREAK 11 7 17 18 65.35
EDS 14 8 5 8 1
EGS 13 8 6 8 1
ESG 6 10 6 8 1
EVTO 20 6 18 8 1
```

```
IT 8 17 1
```

```
LDRAIN 2 5 1e-9
LGATE 1 9 5.68e-9
LSOURCE 3 7 5.35e-9
```

```
MOS1 16 6 8 8 MOSMOD M = 0.99
MOS2 16 21 8 8 MOSMOD M = 0.01
```

```
RBREAK 17 18 RBKMOD 1
RDRAIN 50 16 RDSMOD 33.1e-3
RGATE 9 20 5.85
RIN 6 8 1e9
RSCL1 5 51 RSCLMOD 1e-6
RSCL2 5 50 1e3
RSOURCE 8 7 RDSMOD 14.3e-3
RVTO 18 19 RVTOMOD 1
```

```
S1A 6 12 13 8 S1AMOD
S1B 13 12 13 8 S1BMOD
S2A 6 15 14 13 S2AMOD
S2B 13 15 14 13 S2BMOD
```

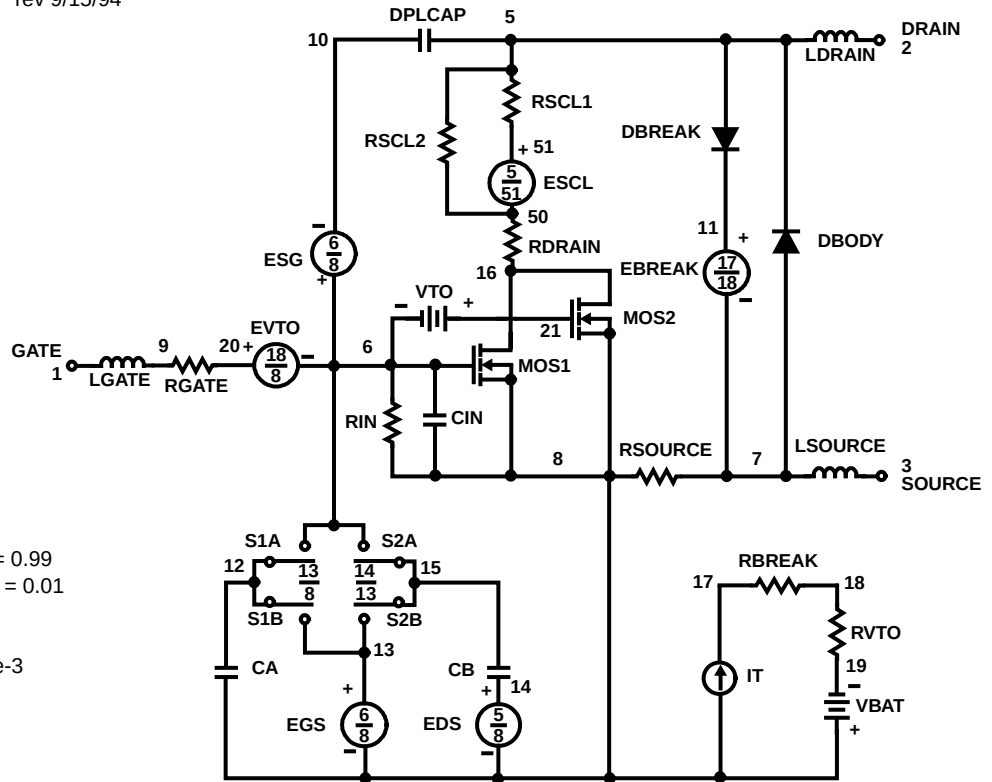
```
VBAT 8 19 DC 1
VTO 21 6 0.485
```

```
ESCL 51 50 VALUE = {(V(5,51)/ABS(V(5,51)))*(PWR(V(5,51)*1e6/46,7))}
```

```
.MODEL DBDMOD D (IS = 2.23e-13 RS = 1.15e-2 TRS1 = 1.64e-3 TRS2 = 7.89e-6 CJO = 6.83e-10 TT = 3.68e-8)
.MODEL DBKMOD D (RS = 3.8e-1 TRS1 = 1.89e-3 TRS2 = 1.13e-5)
.MODEL DPLCAPMOD D (CJO = 25.7e-11 IS = 1e-30 N = 10)
.MODEL MOSMOD NMOS (VTO = 1.935 KP = 18.89 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u)
.MODEL RBKMOD RES (TC1 = 7.18e-4 TC2 = 1.53e-6)
.MODEL RDSMOD RES (TC1 = 4.45e-3 TC2 = 2.9e-5)
.MODEL RSCLMOD RES (TC1 = 2.8e-3 TC2 = 6.0e-6)
.MODEL RVTOMOD RES (TC1 = -1.7e-3 TC2 = -2.0e-6)
.MODEL S1AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -3.55 VOFF = -1.55)
.MODEL S1BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -1.55 VOFF = -3.55)
.MODEL S2AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -2.55 VOFF = 2.45)
.MODEL S2BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = 2.45 VOFF = -2.55)
```

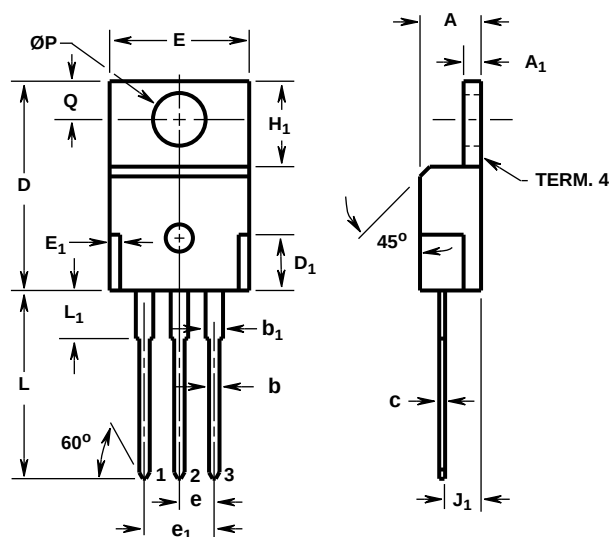
```
.ENDS
```

For further discussion of the PSPICE model, consult **A New PSPICE Sub-circuit for the Power MOSFET Featuring Global Temperature Options**; authored by William J. Hepp and C. Frank Wheatley.



TO-220AB

3 LEAD JEDEC TO-220AB PLASTIC PACKAGE



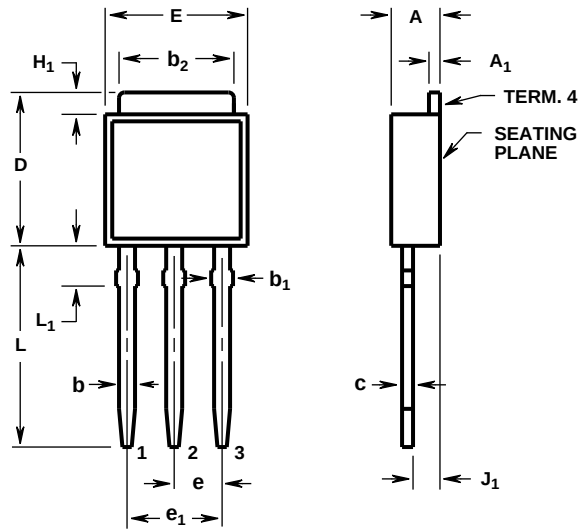
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.170	0.180	4.32	4.57	-
A ₁	0.048	0.052	1.22	1.32	-
b	0.030	0.034	0.77	0.86	3, 4
b ₁	0.045	0.055	1.15	1.39	2, 3
c	0.014	0.019	0.36	0.48	2, 3, 4
D	0.590	0.610	14.99	15.49	-
D ₁	-	0.160	-	4.06	-
E	0.395	0.410	10.04	10.41	-
E ₁	-	0.030	-	0.76	-
e	0.100 TYP		2.54 TYP		5
e ₁	0.200 BSC		5.08 BSC		5
H ₁	0.235	0.255	5.97	6.47	-
J ₁	0.100	0.110	2.54	2.79	6
L	0.530	0.550	13.47	13.97	-
L ₁	0.130	0.150	3.31	3.81	2
ØP	0.149	0.153	3.79	3.88	-
Q	0.102	0.112	2.60	2.84	-

NOTES:

1. These dimensions are within allowable dimensions of Rev. J of JEDEC TO-220AB outline dated 3-24-87.
2. Lead dimension and finish uncontrolled in L₁.
3. Lead dimension (without solder).
4. Add typically 0.002 inches (0.05mm) for solder coating.
5. Position of lead to be measured 0.250 inches (6.35mm) from bottom of dimension D.
6. Position of lead to be measured 0.100 inches (2.54mm) from bottom of dimension D.
7. Controlling dimension: Inch.
8. Revision 1 dated 1-93.

TO-251AA

3 LEAD JEDEC TO-251AA PLASTIC PACKAGE



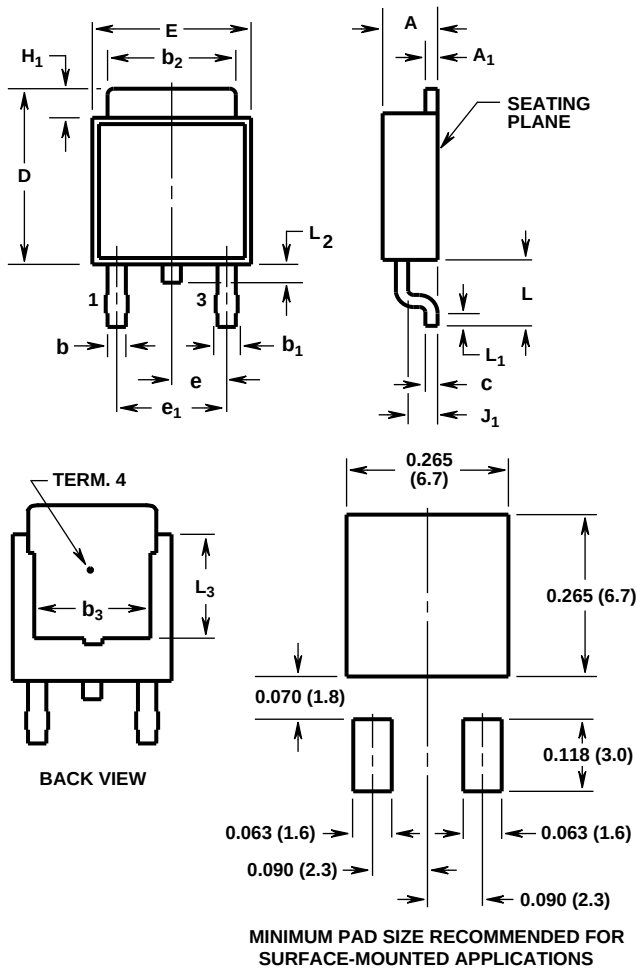
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.086	0.094	2.19	2.38	-
A ₁	0.018	0.022	0.46	0.55	3, 4
b	0.028	0.032	0.72	0.81	3, 4
b ₁	0.033	0.040	0.84	1.01	3
b ₂	0.205	0.215	5.21	5.46	3, 4
c	0.018	0.022	0.46	0.55	3, 4
D	0.270	0.290	6.86	7.36	-
E	0.250	0.265	6.35	6.73	-
e	0.090 TYP		2.28 TYP		5
e ₁	0.180 BSC		4.57 BSC		5
H ₁	0.035	0.045	0.89	1.14	-
J ₁	0.040	0.045	1.02	1.14	6
L	0.355	0.375	9.02	9.52	-
L ₁	0.075	0.090	1.91	2.28	2

NOTES:

1. These dimensions are within allowable dimensions of Rev. C of JEDEC TO-251AA outline dated 9-88.
2. Solder finish uncontrolled in this area.
3. Dimension (without solder).
4. Add typically 0.002 inches (0.05mm) for solder plating.
5. Position of lead to be measured 0.250 inches (6.35mm) from bottom of dimension D.
6. Position of lead to be measured 0.100 inches (2.54mm) from bottom of dimension D.
7. Controlling dimension: Inch.
8. Revision 2 dated 10-95.

TO-252AA

SURFACE MOUNT JEDEC TO-252AA PLASTIC PACKAGE



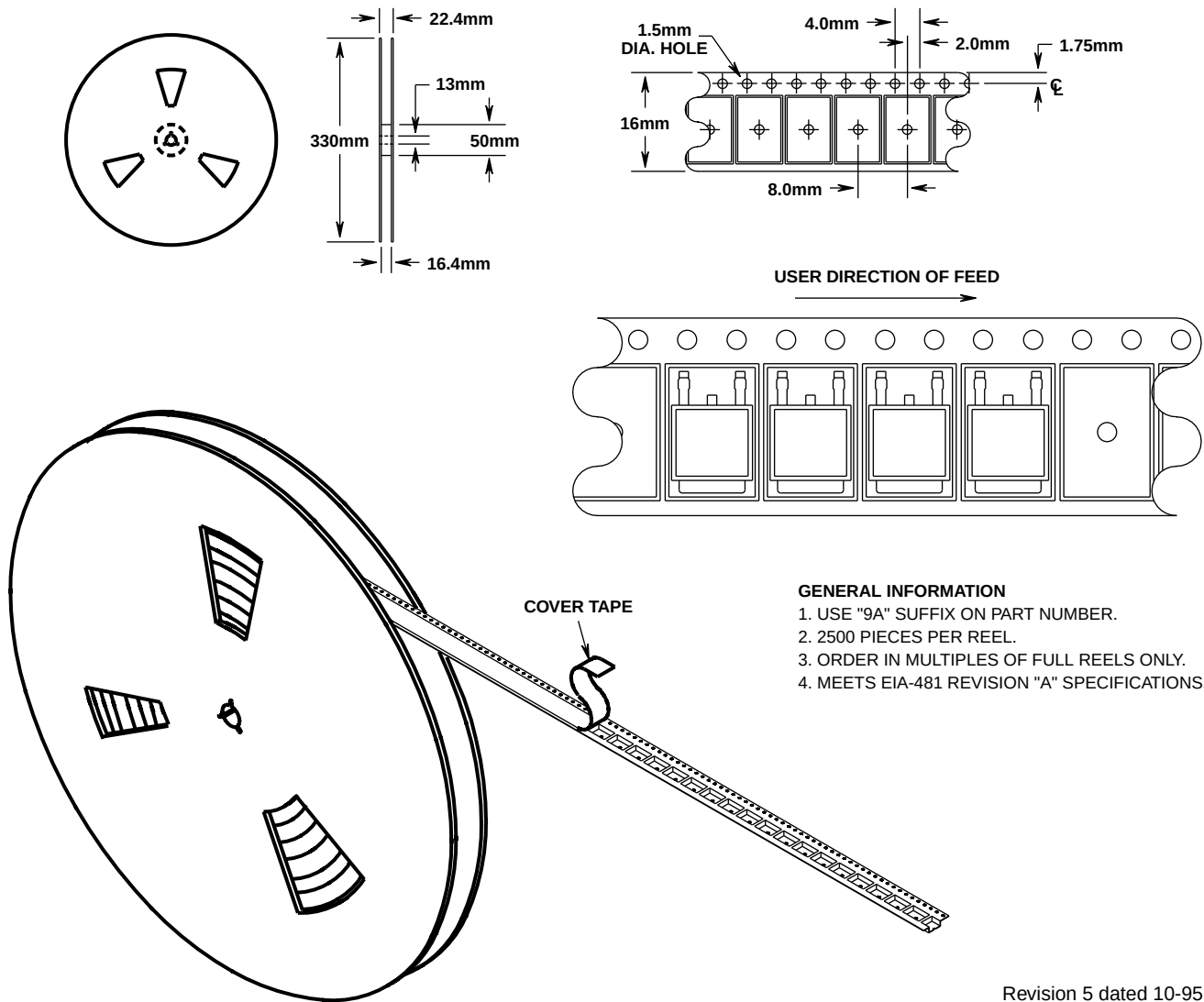
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.086	0.094	2.19	2.38	-
A ₁	0.018	0.022	0.46	0.55	4, 5
b	0.028	0.032	0.72	0.81	4, 5
b ₁	0.033	0.040	0.84	1.01	4
b ₂	0.205	0.215	5.21	5.46	4, 5
b ₃	0.190	-	4.83	-	2
c	0.018	0.022	0.46	0.55	4, 5
D	0.270	0.290	6.86	7.36	-
E	0.250	0.265	6.35	6.73	-
e	0.090 TYP		2.28 TYP		7
e ₁	0.180 BSC		4.57 BSC		7
H ₁	0.035	0.045	0.89	1.14	-
J ₁	0.040	0.045	1.02	1.14	-
L	0.100	0.115	2.54	2.92	-
L ₁	0.020	-	0.51	-	4, 6
L ₂	0.025	0.040	0.64	1.01	3
L ₃	0.170	-	4.32	-	2

NOTES:

1. These dimensions are within allowable dimensions of Rev. B of JEDEC TO-252AA outline dated 9-88.
2. L₃ and b₃ dimensions establish a minimum mounting surface for terminal 4.
3. Solder finish uncontrolled in this area.
4. Dimension (without solder).
5. Add typically 0.002 inches (0.05mm) for solder plating.
6. L₁ is the terminal length for soldering.
7. Position of lead to be measured 0.090 inches (2.28mm) from bottom of dimension D.
8. Controlling dimension: Inch.
9. Revision 5 dated 10-95.

TO-252AA

16mm TAPE AND REEL



GENERAL INFORMATION

1. USE "9A" SUFFIX ON PART NUMBER.
2. 2500 PIECES PER REEL.
3. ORDER IN MULTIPLES OF FULL REELS ONLY.
4. MEETS EIA-481 REVISION "A" SPECIFICATIONS.

Revision 5 dated 10-95

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