



74VCX16373

LOW VOLTAGE 16-BIT D-TYPE LATCH (3-STATE) WITH 3.6V TOLERANT INPUTS AND OUTPUTS

- 3.6V TOLERANT INPUTS AND OUTPUTS
- HIGH SPEED:
 - $t_{PD} = 3.0 \text{ ns (MAX.)}$ at $V_{CC} = 3.0 \text{ to } 3.6\text{V}$
 - $t_{PD} = 3.4 \text{ ns (MAX.)}$ at $V_{CC} = 2.3 \text{ to } 2.7\text{V}$
 - $t_{PD} = 6.8 \text{ ns (MAX.)}$ at $V_{CC} = 1.8\text{V}$
- POWER-DOWN PROTECTION ON INPUTS AND OUTPUTS
- SYMMETRICAL OUTPUT IMPEDANCE:
 - $|I_{OH}| = I_{OL} = 24 \text{ mA (MIN)}$ at $V_{CC} = 3.0\text{V}$
 - $|I_{OH}| = I_{OL} = 18 \text{ mA (MIN)}$ at $V_{CC} = 2.3\text{V}$
 - $|I_{OH}| = I_{OL} = 6 \text{ mA (MIN)}$ at $V_{CC} = 1.8\text{V}$
- OPERATING VOLTAGE RANGE:
 - $V_{CC} \text{ (OPR)} = 1.8\text{V to } 3.6\text{V}$
- PIN AND FUNCTION COMPATIBLE WITH 74 SERIES 16373
- LATCH-UP PERFORMANCE EXCEEDS 300mA
- ESD PERFORMANCE:
 - HBM > 2000V; MM > 200V

DESCRIPTION

The VCX16373 is a low voltage CMOS 16-BIT D-TYPE LATCH with 3 STATE OUTPUTS NON INVERTING fabricated with sub-micron silicon gate and five-layer metal wiring C²MOS technology. It is ideal for low power and very high speed 1.8 to 3.6V applications; it can be interfaced to 3.6V signal enviroment for both inputs and outputs.

These 16 bit D-Type latches are byte controlled by two latch enable inputs (nLE) and two output enable inputs (OE).

While the nLE input is held at a high level, the nQ outputs will follow the data input precisely.

When the nLE is taken low, the nQ outputs will be latched precisely at the logic level of D input data.

While the (nOE) input is low, the nQ outputs will be in a normal logic state (high or low logic level) and while high level the outputs will be in a high impedance state.

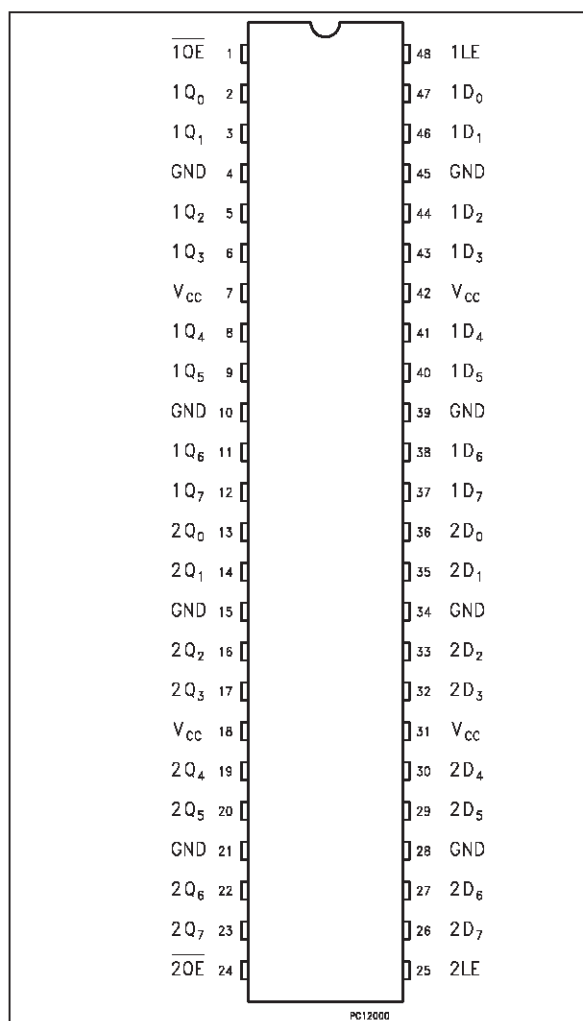
All inputs and outputs are equipped with protection circuits against static discharge, giving them 2KV ESD immunity and transient excess voltage.



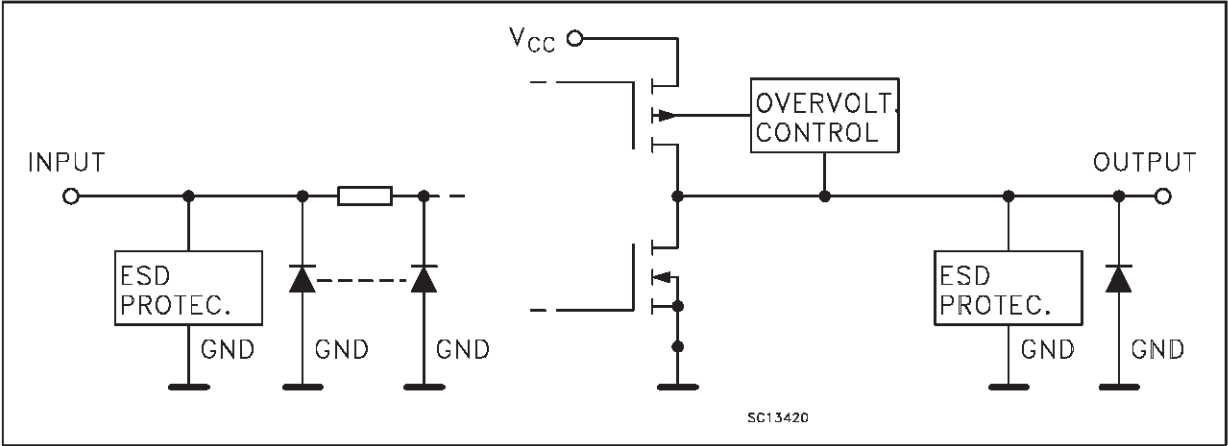
T
(TSSOP48 Package)

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74VCX16373T

PIN CONNECTION



INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

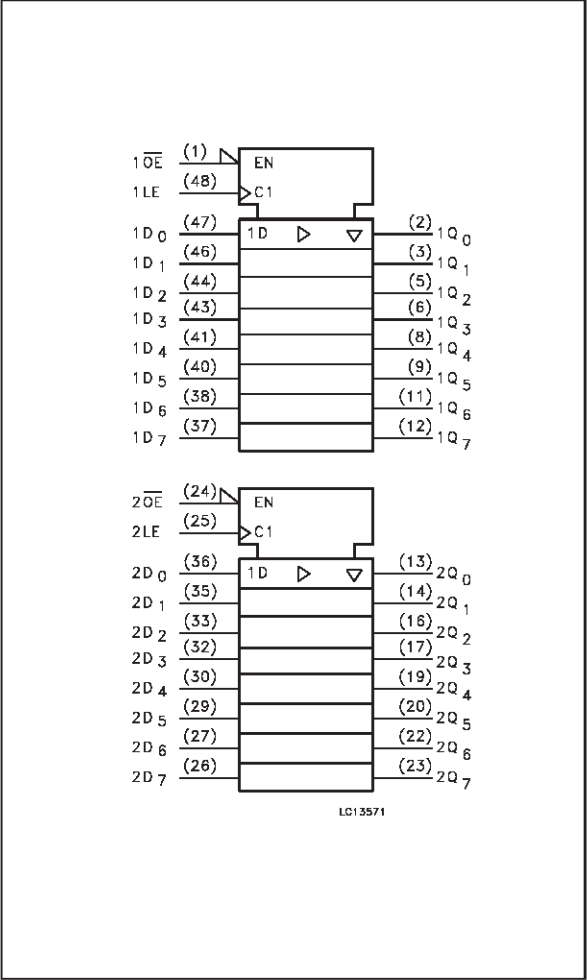
PIN No	SYMBOL	NAME AND FUNCTION
1	$\overline{1OE}$	3 State Output Enable Input (Active LOW)
2, 3, 5, 6, 8, 9, 11, 12	1Q0 to 1Q7	3 State Outputs
13, 14, 16, 17, 19, 20, 22, 23	2Q0 to 2Q7	3 State Outputs
24	$\overline{2OE}$	3 State Output Enable Input (Active LOW)
25	2LE	Latch Enable Input
36, 35, 33, 32, 30, 29, 27, 26	2D0 to 2D7	Data Inputs
47, 46, 44, 43, 41, 40, 38, 37	1D0 to 1D7	Data Inputs
48	1LE	Latch Enable Input
4, 10, 15, 21, 28, 34, 39, 45	GND	Ground (0V)
7, 18, 31, 42	V _{CC}	Positive Supply Voltage

TRUTH TABLE

INPUTS			OUTPUTS
$\overline{OE}$	LE	D	Q
H	X	X	Z
L	L	X	NO CHANGE*
L	H	L	L
L	H	H	H

X: Don't care
Z: High impedance
* Q output are latched at the timewhen the LE input is taken low level.

IEC LOGIC SYMBOLS



DC SPECIFICATIONS ($2.7V < V_{CC} \leq 3.6V$ unless otherwise specified)

Symbol	Parameter	Test Conditions			Value		Unit
		V _{CC} (V)		-40 to 85 °C			
				Min.	Max.		
V _{IH}	High Level Input Voltage	2.7 to 3.6		2.0		V	
V _{IL}	Low Level Input Voltage				0.8	V	
V _{OH}	High Level Output Voltage	2.7 to 3.6	V _I = V _{IH} or V _{IL}	I _O =-100 μA	V _{CC} -0.2	V	
		2.7		I _O =-12 mA	2.2		
		3.0		I _O =-18 mA	2.4		
		3.0		I _O =-24 mA	2.2		
V _{OL}	Low Level Output Voltage	2.7 to 3.6	V _I = V _{IH} or V _{IL}	I _O =100 μA		0.2	V
		2.7		I _O =12 mA		0.4	
		3.0		I _O =18 mA		0.4	
		3.0		I _O =24 mA		0.55	
I _I	Input Leakage Current	2.7 to 3.6	V _I = 0 to 3.6 V			±5	μA
I _{OZ}	3 State Output Leakage Current	2.7 to 3.6	V _I = V _{IH} or V _{IL} V _O = 0 to 3.6V			±10	μA
I _{off}	Power Off Leakage Current	0	V _I or V _O = 0 to 3.6V			10	μA
I _{CC}	Quiescent Supply Current	2.7 to 3.6	V _I = V _{CC} or GND			20	μA
			V _I or V _O = V _{CC} to 3.6 V			±20	
ΔI _{CC}	ICC incr. per input	2.7 to 3.6	V _{IH} = V _{CC} -0.6V			750	μA

DC SPECIFICATIONS ($2.3V < V_{CC} \leq 2.7V$ unless otherwise specified)

Symbol	Parameter	Test Conditions			Value		Unit
		V _{CC} (V)		-40 to 85 °C			
				Min.	Max.		
V _{IH}	High Level Input Voltage	2.3to 2.7			1.6		V
V _{IL}	Low Level Input Voltage					0.7	V
V _{OH}	High Level Output Voltage	2.3to 2.7	V _I = V _{IH} or V _{IL}	I _O =-100 μA	V _{CC} -0.2		V
		2.3		I _O =-6 mA	2.0		
		2.3		I _O =-12 mA	1.8		
		2.3		I _O =-18 mA	1.7		
V _{OL}	Low Level Output Voltage	2.3to 2.7	V _I = V _{IH} or V _{IL}	I _O =100 μA		0.2	V
		2.3		I _O =12 mA		0.4	
		2.3		I _O =18 mA		0.6	
I _I	Input Leakage Current	2.3to 2.7	V _I = 0 to 3.6 V			±5	μA
I _{OZ}	3 State Output Leakage Current	2.3to 2.7	V _I = V _{IH} or V _{IL} V _O = 0 to 3.6V			±10	μA
I _{off}	Power Off Leakage Current	0	V _I or V _O = 0 to 3.6V			10	μA
I _{CC}	Quiescent Supply Current	2.3to 2.7	V _I = V _{CC} or GND			20	μA
			V _I or V _O = V _{CC} to 3.6 V			±20	

DC SPECIFICATIONS ($1.8V \leq V_{CC} \leq 2.3V$ unless otherwise specified)

Symbol	Parameter	Test Conditions			Value		Unit
		V _{CC} (V)			-40 to 85 °C		
					Min.	Max.	
V _{IH}	High Level Input Voltage	1.8to 2.3			0.7V _{CC}		V
V _{IL}	Low Level Input Voltage					0.2V _{CC}	V
V _{OH}	High Level Output Voltage	1.8	V _I = V _{IH} or V _{IL}	I _O =-100 μA	V _{CC} -0.2		V
		1.8		I _O =-6mA	1.4		
V _{OL}	Low Level Output Voltage	1.8	V _I = V _{IH} or V _{IL}	I _O =100 μA		0.2	V
		1.8		I _O =6mA		0.3	
I _I	Input Leakage Current	1.8	V _I = 0 to 3.6 V			±5	μA
I _{OZ}	3 State Output Leakage Current	1.8	V _I = V _{IH} or V _{IL} V _O = 0 to 3.6V			±10	μA
I _{off}	Power Off Leakage Current	0	V _I or V _O = 0 to 3.6V			10	μA
I _{CC}	Quiescent Supply Current	1.8	V _I = V _{CC} or GND			20	μA
			V _I or V _O = V _{CC} to 3.6 V			±20	

DYNAMIC SWITCHING CHARACTERISTICS (T_a = 25°C, Input t_r = t_f = 2.0 ns, C_L = 30 pF, R_L = 500 Ω)

Symbol	Parameter	Test Conditions		Value			Unit
		V _{CC} (V)		T _A = 25 °C			
				Min.	Typ.	Max.	
V _{OLP}	Dynamic Low Voltage Quiet Output (note 1, 3)	1.8	V _{IL} = 0 V V _{IH} = V _{CC}		0.25		V
		2.5			0.6		
		3.3			0.8		
V _{OLV}	Dynamic Low Voltage Quiet Output (note 1, 3)	1.8	V _{IL} = 0 V V _{IH} = V _{CC}		-0.25		V
		2.5			-0.6		
		3.3			-0.8		
V _{OHV}	Dynamic High Voltage Quiet Output (note 2, 3)	1.8	V _{IL} = 0 V V _{IH} = V _{CC}		1.5		V
		2.5			1.9		
		3.3			2.2		

1) Number of outputs defined as "n". Measured with "n-1" outputs switching from HIGH to LOW or LOW to HIGH. The remaining output is measured in the LOW state.

2) Number of outputs defined as "n". Measured with "n-1" outputs switching from HIGH to LOW or LOW to HIGH. The remaining output is measured in the HIGH state.

3) Parameters guaranteed by design.

AC ELECTRICAL CHARACTERISTICS ($C_L = 30 \text{ pF}$, $R_L = 500 \Omega$, Input $t_r = t_f = 2.0 \text{ ns}$)

Symbol	Parameter	Test Condition		Value		Unit		
		V _{CC} (V)	Waveform	-40 to 85 °C				
				Min.	Max.			
t _{PLH} t _{PHL}	Propagation Delay Time Dn to Qn	1.8 2.3 to 2.7 3.0 to 3.6	3	1.5 1.0 0.8	6.8 3.4 3.0	ns		
t _{PLH} t _{PHL}	Propagation Delay Time LE to Qn	1.8 2.3 to 2.7 3.0 to 3.6		1	1.5 1.0 0.8		7.8 3.9 3.0	ns
t _{PZL} t _{PZH}	Output Enable Time	1.8 2.3 to 2.7 3.0 to 3.6			2		1.5 1.0 0.8	
t _{PLZ} t _{PHZ}	Output Disable Time	1.8 2.3 to 2.7 3.0 to 3.6	2			1.5 1.0 0.8	6.8 3.8 3.5	
t _s	Setup Time, HIGH or LOW level Dn to LE	1.8 2.3 to 2.7 3.0 to 3.6		1		2.5 1.5 1.5		ns
t _h	Hold Time, HIGH or LOW level Dn to LE	1.8 2.3 to 2.7 3.0 to 3.6			1	1.0 1.0 1.0		
t _w	LE Pulse Width, HIGH	1.8 2.3 to 2.7 3.0 to 3.6	1			4.0 1.5 1.5		
t _{OSLH} t _{OSHL}	Output to Output Skew Time (note 1, 2)	1.8 2.3 to 2.7 3.0 to 3.6					0.75 0.5 0.5	ns

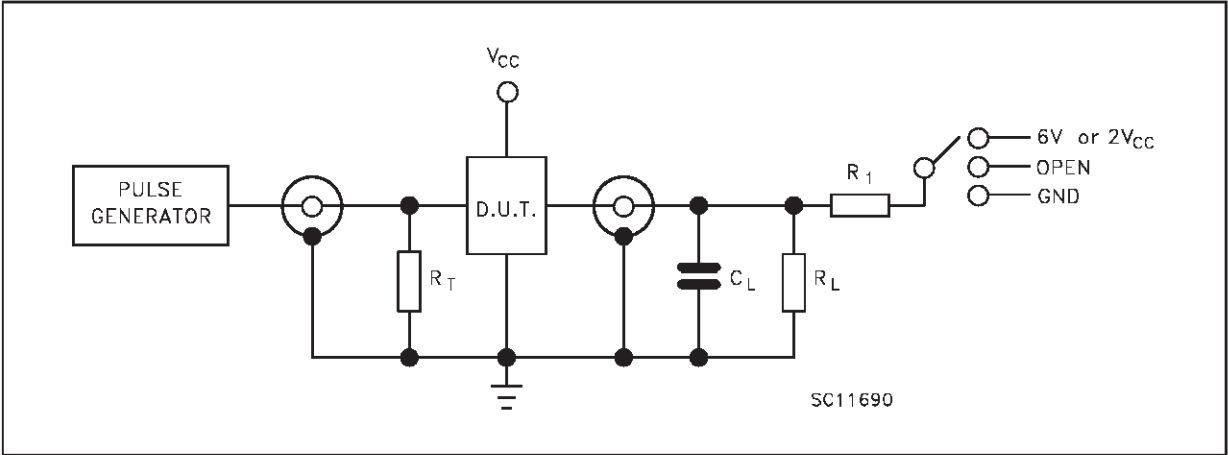
1) Skew is defined as the absolute value of the difference between the actual propagation delay for any two outputs of the same device switching in the same direction, either HIGH or LOW ($t_{OSLH} = |t_{PLHm} - t_{PLHl}|$, $t_{OSHL} = |t_{PHLm} - t_{PHLl}|$)

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions		Value			Unit
		V _{CC} (V)		T _A = 25 °C			
				Min.	Typ.	Max.	
C _{IN}	Input Capacitance	1.8, 2.5 or 3.3	V _{IN} = 0V or V _{CC}		6		pF
C _{OUT}	Output Capacitance	1.8, 2.5 or 3.3	V _{IN} = 0V or V _{CC}		7		pF
C _{PD}	Power Dissipation Capacitance (note 1)	1.8, 2.5 or 3.3	f _{IN} = 10MHz V _{IN} = 0V or V _{CC}		20		pF

1) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the following equation. $I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CD}/16$ (per circuit)

TEST CIRCUIT



TEST	SWITCH
t_{PLH} , t_{PHL}	Open
t_{PZL} , t_{PLZ} ($V_{CC} = 3.0$ to $3.6V$)	6V
t_{PZL} , t_{PLZ} ($V_{CC} = 2.3$ to $2.7V$ or $1.8V$)	$2V_{CC}$
t_{PZH} , t_{PHZ}	GND

$C_L = 30$ pF or equivalent (includes jig and probe capacitance)

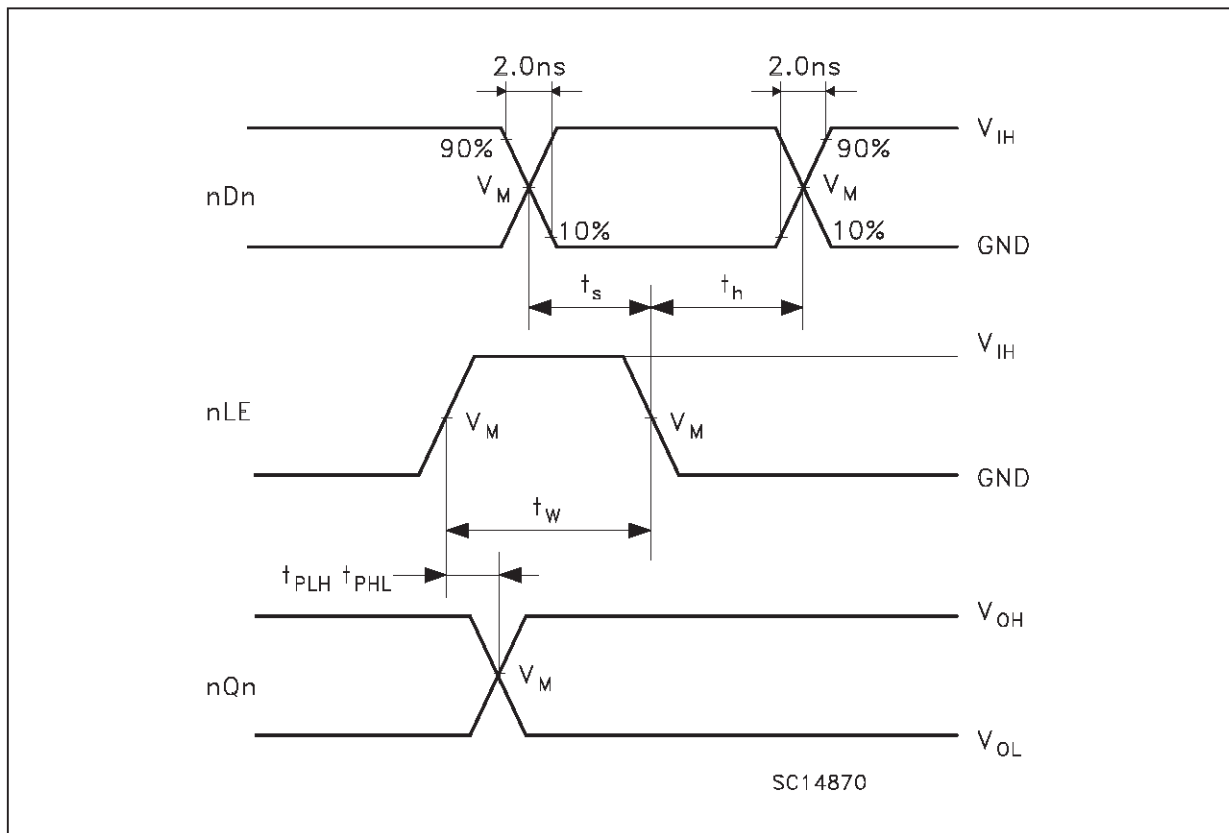
$R_L = R_1 = 500\Omega$ or equivalent

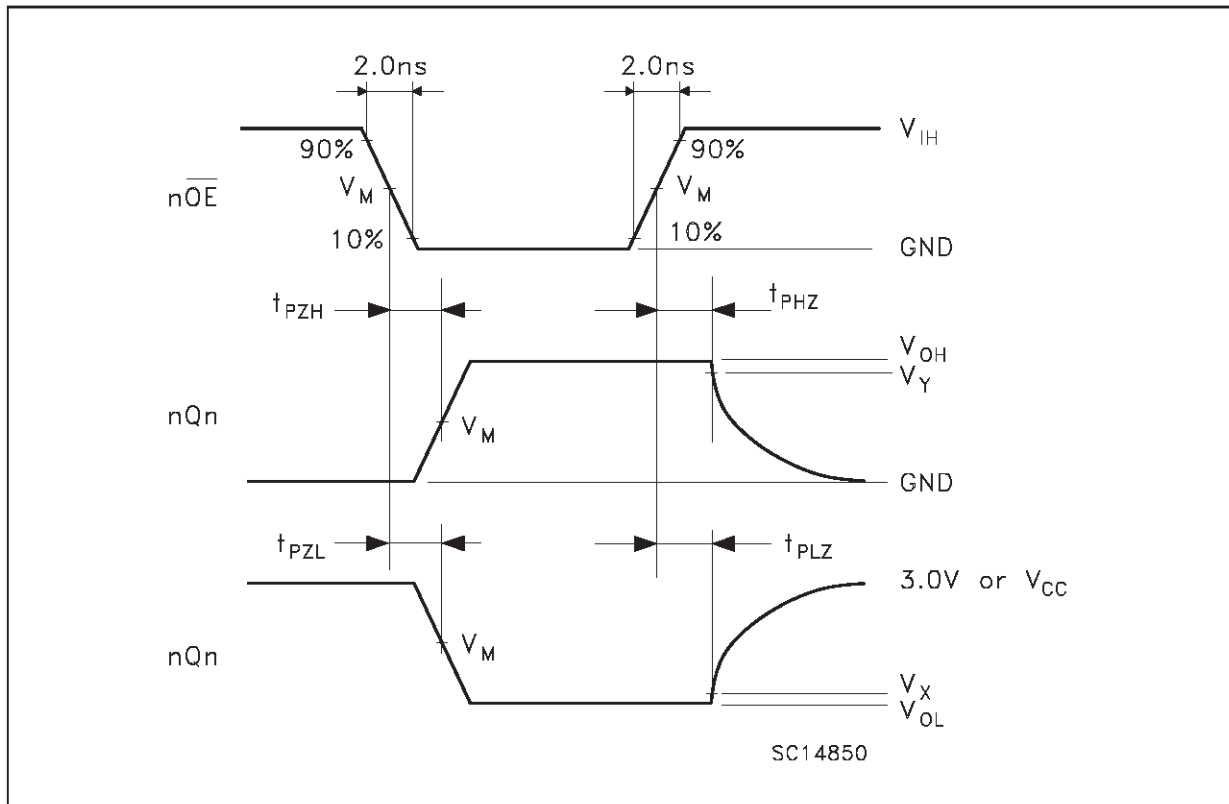
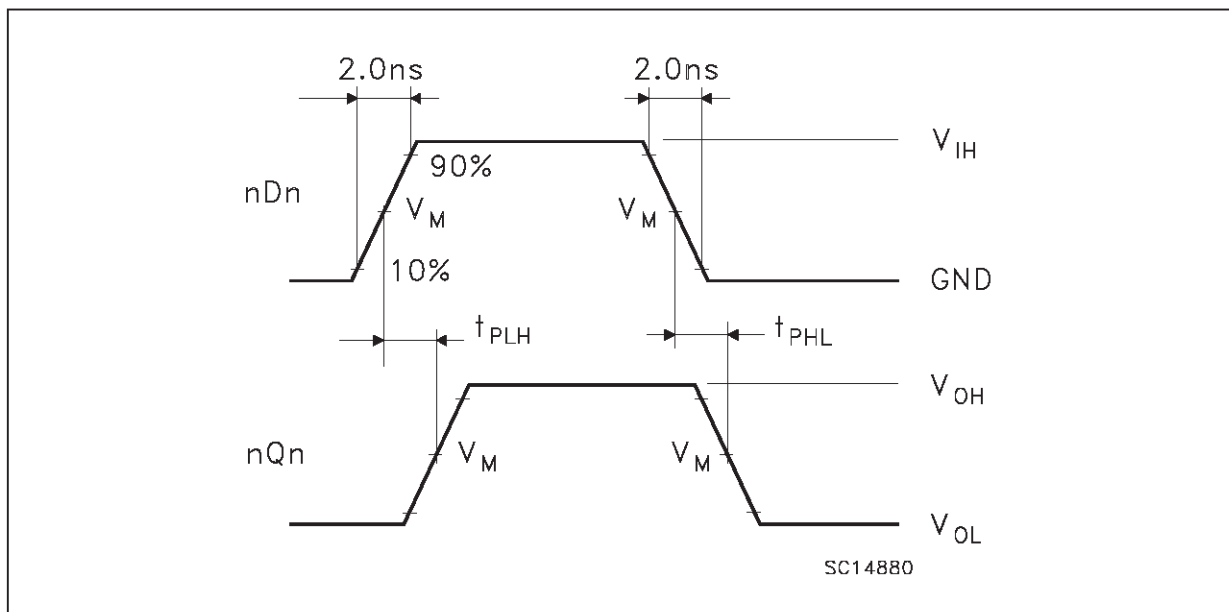
$R_T = Z_{out}$ of pulse generator (typically 50Ω)

WAVEFORM SYMBOL VALUES

Symbol	V_{CC}		
	3.0 to 3.6V	2.3 to 2.7V	1.8V
V_{IH}	2.7V	V_{CC}	V_{CC}
V_M	1.5V	$V_{CC}/2$	$V_{CC}/2$
V_X	$V_{OL} + 0.3V$	$V_{OL} + 0.15V$	$V_{OL} + 0.15V$
V_Y	$V_{OH} - 0.3V$	$V_{OH} - 0.15V$	$V_{OH} - 0.15V$

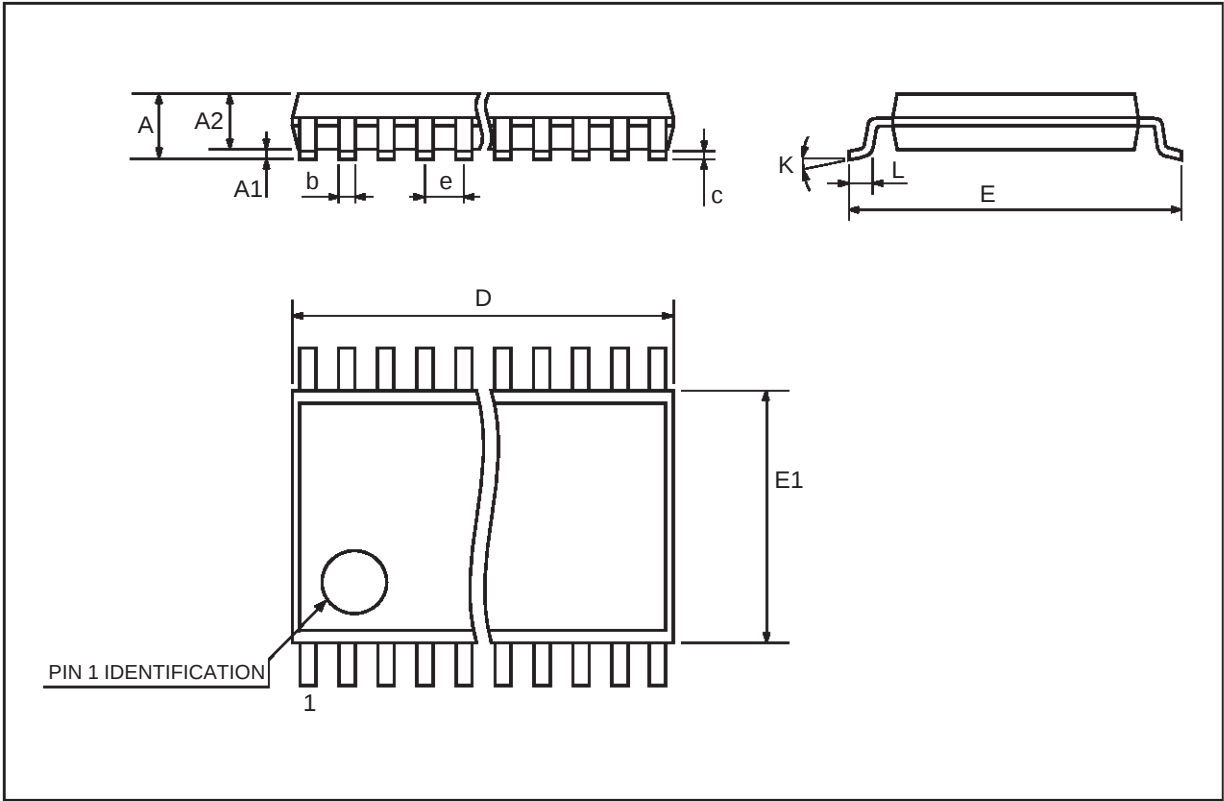
WAVEFORM 1: LE TO Qn PROPAGATION DELAYS, LE MINIMUM PULSE WIDTH, Dn TO LE SETUP AND HOLD TIMES ($f=1\text{MHz}$; 50% duty cycle)



WAVEFORM 2: OUTPUT ENABLE AND DISABLE TIMES ($f=1\text{MHz}$; 50% duty cycle)**WAVEFORM 3: PROPAGATION DELAY TIME** ($f=1\text{MHz}$; 50% duty cycle)

TSSOP48 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.1			0.433
A1	0.05	0.10	0.15	0.002	0.004	0.006
A2	0.85	0.9	0.95	0.335	0.354	0.374
b	0.17		0.27	0.0067		0.011
c	0.09		0.20	0.0035		0.0079
D	12.4	12.5	12.6	0.408	0.492	0.496
E	7.95	8.1	8.25	0.313	0.319	0.325
E1	6.0	6.1	6.2	0.236	0.240	0.244
e		0.5 BSC			0.0197 BSC	
K	0°	4°	8°	0°	4°	8°
L	0.50	0.60	0.70	0.020	0.024	0.028



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