SIEMENS

ICs for Communications

Audio Ringing Codec Filter
Featuring Speakerphone Function
ARCOFI®-SP
PSB 2163

User's Manual

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User's Manual 06.95

PSB 2163 Revision History:	Current Version 06.95
Previous Version:	02.94
Page	Subjects (changes since last revision)
108	Absolute Maximum Ratings
108	DC Characteristics
110	Analog Front End Characteristics
111	Transmission Characteristics Test Conditions corrected Addition of Overall Programming Range
112	IOM®-2 Bus Timing Specification of Jitter Timing

Data Classification

Maximum Ratings

Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

Characteristics

The listed characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specify mean values expected over the production spread. If not otherwise specified, typical characteristics apply at T_A = 25 °C and the given supply voltage.

Operating Range

In the operating range the functions given in the circuit description are fulfilled.

For detailed technical information about **“Processing Guidelines”** and **“Quality Assurance”** for ICs, see our **“Product Overview”**.

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Introduction

The PSB 2163 ARCOFI®-SP provides the subscriber with an optimized Audio, Ringing, Codec, Filter processor solution for a digital telephone. It fulfills all the necessary requirements for the completion of a low-cost digital telephone.

Please note: Throughout this whole document "ARCOFI®" refers to ARCOFI®-SP PSB 2163.

The ARCOFI performs all coding, decoding and filtering functions according to the CCITT and ETSI (NET33) norms.

Full featured applications are possible without any external elements. All the necessary hardware and software is implemented. In addition the ARCOFI offers a speakerphone and monitoring function. This feature is completely digitally implemented in the chip.

Two transducer correction filters (one for each direction) can be programmed to correct the analog transducer frequency characteristics.

The ARCOFI provides a universal DTMF, tone and ringing generator for the receive direction. The signal forms available are DTMF, square, trapezoid and sine wave. Complex signal sequences are made possible by a control generator (e.g. pulsed three tone call in conjunction with the beat generator).

A DTMF-generator for the transmit direction is also available. If the transmit DTMF-generator is active, only a part of the receive tone generator function is possible.

This flexible tone generator concept fulfills a wide range of applications.

The interfacing to a handset mouth and earpiece is facilitated by a flexible analog front end. A loudspeaker output has also been integrated on the chip as well as a secondary input for a handsfree microphone. All analog inputs and outputs are gain programmable through software.

At the digital side an ISDN-Oriented Modular (IOM®-2) interface for terminal (TE) and non-terminal (non-TE) applications or a Serial Control/Data Interface (SCI & SDI) is realized to connect layer-1/2 devices to the ARCOFI.

The ARCOFI is a BICMOS-device, available in a P-DIP-28, P-LCC-28-R or P-DSO-28 package. It operates from a single + 5 V supply and features a power-down state with very low power consumption.

Comparison between PSB 2163 and PSB 2165

Table of main differences:

PSB 2163	PSB 2165	Comment
1-µ BICMOS technology	2-µ CMOS technology	
P-DSO-28		
	SLD-interface	
Non-TE IOM-2 interface		
Serial Control/Data Interface		
One receive channel	Two receive channels	
Digital high-pass in receive direction		
AGC in receive direction	LGA (programmable gain stage) in receive direction	
Sidetone gain stage GZ with higher resolution (two byte coefficient)	GZ with one byte coefficient	
Optimized speakerphone function		Extended coefficient space is necessary
Microphone amplifier with additional 36-dB and 42-dB gain stages		
Controlled monitoring with fixed attenuation	Controlled monitoring with programmable attenuation	
Ringing directly via loudspeaker with square-wave in 3-dB steps	Ringing via loudspeaker over the second receive path	
Tone generation unit can be switched to transmit path and added to transmit speech signals		
Additional test loops	CCITT G.714	
ETSI (NET33) & CCITT G.714		

Table of Symbols

AD	Address of the ARCOFI (IOM-2 mode)
A/D	Analog to Digital converter
ADI	ARCOFI Digital Interface
AFE	Analog Front End
AGCX	Automatic Gain Control Transmit
AGCR	Automatic Gain Control Receive
AHO	Handset Output Amplifier
AIMX	Analog Input Multiplexer control bits (ATCR)
ALC	Analog Loop via Converter (TFCR)
ALF	Analog Loop via Front End (TFCR)
ALI	Analog Loop via Interface (TFCR)
ALN	Analog Loop via Noise Shaper (TFCR)
ALS	Loudspeaker Amplifier
ALTF	Analog Loop & Test Function bits (TFCR)
ALZ	Analog Loop via Z-side tone gain stage
AMI	Microphone Amplifier
ARCOFI	Audio Ringing Codec Filter
ASP	ARCOFI Signal Processor
BM	Beat Mode bit (TGCR)
BT	Beat Tone bit (TGCR)
CAM	Chip Address Mode bit (IOM-2 two chip mode; GCR)
CCITT	International Telegraph and Telephone Consultative Committee
CG	Control Generator bit (TGCR)
CMDR	Command Register
COP	Coefficient Operation (CMDR)
CR	Configuration Register
CRAM	Coefficient RAM
$\overline{\text{CS}}$	Chip Select active low (serial control interface)
D/A	Digital to Analog converter
DCE	Double Clock Enable at DCLK pin (SDICR)
DCL	IOM-2 interface clock
DCLK	Data Clock pin (serial data interface)
DD	IOM-2 Data Downstream pin
DEC	Decimation filter
DHON	Disable pin HON (XCR)
DHOP	Disable pin HOP (XCR)
DHPR	Disable High Pass Receive bit (PFCR)
DHPX	Disable High Pass Transmit bit (PFCR)
DLN	Digital Loop via Noise Shaper (TFCR)
DLP	Digital Loop via PCM-register (TFCR)

Table of Symbols (cont'd)

DLS	Digital Loop via Signal processor (TFCR)
DLSN	Disable pin LSN (XCR)
DLSP	Disable pin LSP (XCR)
DLTF	Digital Loop & Test Function bits (TFCR)
DR	Data Receive pin (serial data interface)
DRAM	Data RAM
DSP	Digital Signal Processor
DT	Dual Tone bit (TGCR)
DTMF	Dual Tone Multi Frequency bit (TGSR)
DU	IOM-2 Data Upstream pin
DX	Data Transmit pin (serial data interface)
EP0	Earpiece
EPP0	Enable Push-Pull at pin DU/DX (SDICR)
EPP1	Enable Push-Pull at pin SA/SDX (SDICR)
EPZST	Enable PZ1/PZ2 to output internal Status conditions (TFCR)
ETF	Enable Tone Filter bit (TGCR)
ETSI	European Telecommunications Standards Institute
EVX	Enable Voice Transmit bit (GCR)
EVREF	Enable VREF buffer bit (ATCR)
EWDF	Electrical Wave Digital Filter
FR	Frequency correction Receive bit (PFCR)
FSC	IOM-2 and SDI-Frame Synchronization pin (8 kHz)
FX	Frequency correction Transmit bit (PFCR)
GR	Receive Gain bit (PFCR); Receive gain stage
GX	Transmit Gain bit (PFCR); Transmit gain stage
GZ	Z-side tone Gain bit (PFCR); Z-side tone Gain stage
HO	Handset Output
HOC	Handset Output Control bits (ARCR)
HON	Handset earpiece Output – pin
HOP	Handset earpiece Output + pin
IDENT	Identification Code
IDR	Initialize Data RAM (TFCR)
INT	Interpolation filter
IOM	ISDN-Oriented Modular
ISDN	Integrated Services Digital Network

Table of Symbols (cont'd)

LAW	A-Law/μ-Law bit (GCR)
LIN	Linear data mode (VDM; DFICR)
LS	Loudspeaker
LSC	Loudspeaker Control bits (ARCR)
LSN	Loudspeaker output – pin
LSP	Loudspeaker output + pin
MCLK	Master Clock pin (synchronized system clock)
MCLKR	Master Clock Rate (SDICR)
MI3	Microphone input
MIC	Microphone Control bits (ATCR)
MIN1/2	Microphone inputs – pins
MIP1/2	Microphone inputs + pins
NOP	No Operation (CMDR)
NOT	No Test mode (TFCR)
PABX	Private Automatic Branch Exchange
PCI	Peripheral Control Interface
PCM	Pulse Code Modulation
PM	Piezo Mode; output to digital pins PZ1/PZ2 (TGSR)
POR	Power-On Reset
PU	Power-Up bit (GCR)
RAAR	Read Automatic Attenuation Receive
RCM	Reverse Channel Mode (CMDR)
RS	Reset pin
R/W	Read/Write operation bit (CMDR)
RX	Receive path
SA-SD	PCI I/O pins; I/O-control bits (SDICR)
SCAE	Speech Comparator at the Acoustic Side
SCI	Serial Control Interface
SCLE	Speech Comparator at the Line Side
SCLK	Serial Clock pin (serial control interface)
SDI	Serial Data Interface
SDR	Serial Data Receive pin (serial control interface)
SDX	Serial Data Transmit pin (serial control interface)
SLOT	IOM-2 Slot select for TE mode (GCR)
SM	Stop Mode bit (TGCR)
SOP	Status Operation (CMDR)
SP	Speakerphone enable bit (GCR)

Table of Symbols (cont'd)

SQTR	Square/Trapezoid mode bit (TGCR)
S/T	Square/Trapezoid Generator
TE	Terminal Equipment
TG	Tone Generator bit (TGCR)
TR	Three party conferencing (VDM; DFICR)
TRL	Tone Ringing via Loudspeaker (TGSR)
TRR	Tone Ringing Receive bit (TGSR)
TRX	Tone Ringing Transmit bit (TGSR)
TS	Time-Slot Selection in SDI-mode (TSCR)
TX	Transmit path
V_{DD}	Voltage supply (+ 5 V)
V_{DDP}	Analog Voltage supply for Power amplifiers (+ 5 V)
VDM	Voice Data Manipulation bits (DFICR)
V_{REF}	Reference Voltage output pin
V_{SSA}	Analog ground (0 V)
V_{SSD}	Digital ground (0 V)
V_{SSP}	Analog ground for Power amplifiers (0 V)
WDF	Wave Digital Filter
XOP	Extended Operation (CMDR)

SIEMENS

Audio Ringing Codec Filter Featuring Speakerphone Function (ARCOFI®-SP)

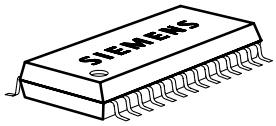
PSB 2163

Preliminary Data

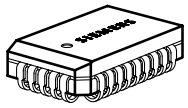
BICMOS-IC

1 Features

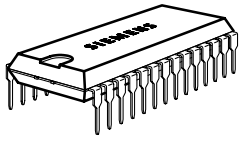
- Applications in digital terminal equipment featuring voice functions
- Digital signal processing performs all CODEC functions
- Fully compatible to the G. 714 CCITT and ETSI (NET33) specification
- PCM A-Law/μ-Law (G. 711 CCITT) and 16-bit linear data
- Flexible configuration of all internal functions
- IOM-2 interface (TE- and non-TE-mode), Serial Control Interface (SCI) and Serial Data Interface (SDI)
- Three analog inputs for the microphone in the handset, the speakerphone and the headset
- Two differential outputs for a handset earpiece (200 Ω) and a loudspeaker (50 Ω)
- 100-mW sine wave and 200-mW square wave loudspeaker driver capability
- Separate digital output for a piezo ringer
- Flexible Peripheral Control Interface (PCI) in IOM-2 TE-mode
- Flexible test and maintenance loopbacks in the analog front end and the digital signal processor
- Independent gain programmable amplifiers for all analog inputs and outputs
- Full digital speakerphone and monitoring support without any external components (speakerphone test and optimization function is available)
- Two transducer correction filters
- Side tone gain adjustment
- Flexible DTMF, tone and ringing generator
- Single 5-V power supply
- Low power consumption: standby 1 mW, operating consumption is dependent on the selected operating mode
- Advanced 1-μ BICMOS technology



P-DSO-28



P-LCC-28-R



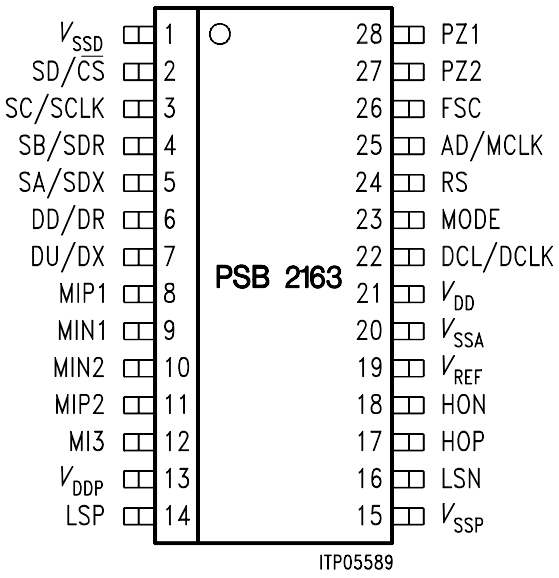
P-DIP-28

Type	Ordering Code	Package
PSB 2163-T	Q67100-H6458	P-DSO-28 (SMD)
PSB 2163-N	Q67100-H6348	P-LCC-28-R (SMD)
PSB 2163-P	Q67100-H6460	P-DIP-28

Pin Configurations

(top view)

P-DSO-28



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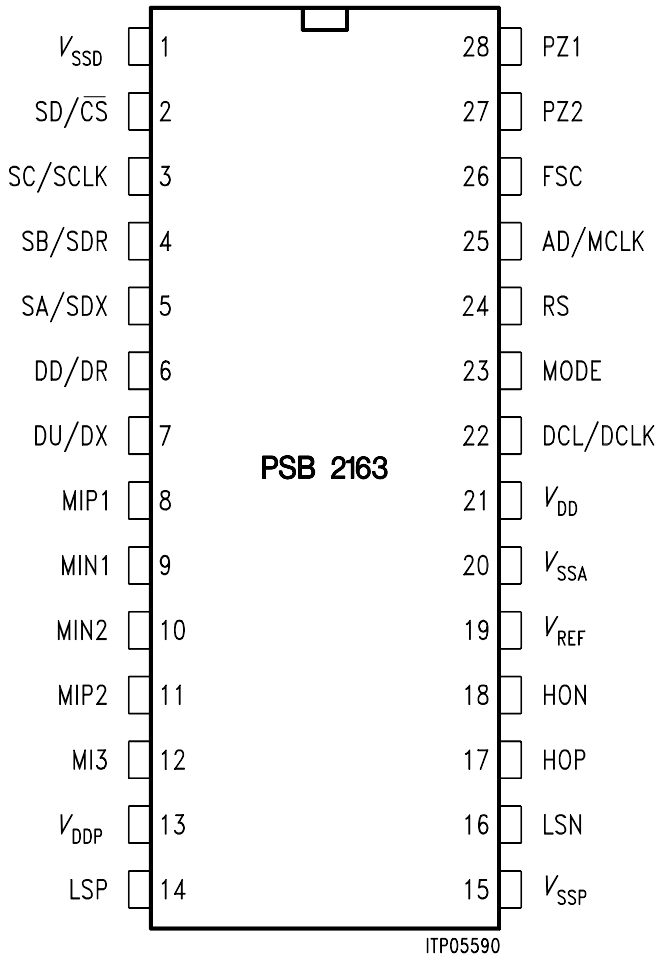
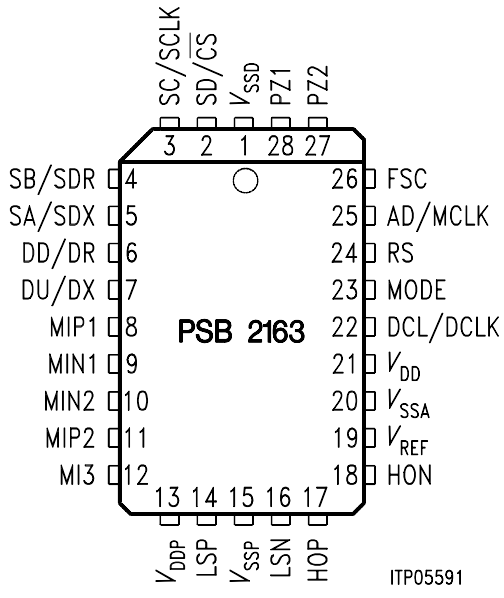


P-LCC-28-R



1.1 Pin Definitions and Functions

Pin No. P-DSO P-LCC P-DIP	Symbol	Input (I) Output (O) Open Drain (OD)	Function
21	V_{DD}	—	Power supply (5 V ± 5 %)
13	V_{DDP}	—	Power supply (5 V ± 5 %)
1	V_{SSD}	—	Digital Ground (0 V)
20	V_{SSA}	—	Analog Ground (0 V)
15	V_{SSP}	—	Analog Ground (0 V)
23	MODE	I	**Mode Selection:** IOM-2 or serial control/data interface
25	AD MCLK	I I	**IOM Address:** Chip address in IOM-2 two chip mode **Master Clock:** Synchronous system clock when serial control/data interface is selected
24	RS	I	**Reset:** A high signal on this pin forces the ARCOFI into reset state
26	FSC	I	**Frame Sync:** 8-kHz frame synchronization signal (IOM-2 and SDI-mode)
22	DCL DCLK	I I	**DCL-System Clock:** 1.536 MHz supplied by the application system clock when IOM-2 mode is selected **DCLK Data Clock:** Data clock of the serial data interface (SDI)
6	DD DR	I/(OD) [1] I	**Data Downstream:** Receive data from layer-1 IOM-2 controlling device **Data Receive:** Receive data of the serial data interface (SDI)
28 27	PZ1 PZ2	O O	**Digital Piezo Ringer Output:** When selected the tone ringer is routed to this output (PZ1 & PZ2 are in opposite phases)

[1] see DD/DU-voice channel swapping (XOP_D)

1.1 Pin Definitions and Functions (cont'd)

Pin No. P-DSO P-LCC P-DIP	Symbol	Input (I) Output (O) Open Drain (OD)	Function
7	DU	OD/I [1]	**Data Upstream:** Transmit data to the layer-1 IOM-2 controlling device
	DX	OD/O [2]	**Data Transmit:** Transmit data of the serial data interface (SDI)
2	SD	IO	**Programmable I/O PCI Pin SD:** This port pin is only available in IOM-2 TE-mode
	$\overline{CS}$	I	**Chip Select:** A low level indicates a microprocessor access to the ARCOFI-serial control interface (SCI)
3	SC	IO	**Programmable I/O PCI Pin SC:** This port pin is only available in IOM-2 TE-mode
	SCLK	I	**Serial Clock:** Clock signal of the serial control interface (SCI)
4	SB	IO	**Programmable I/O PCI Pin SB:** This port pin is only available in IOM-2 TE-mode
	SDR	I	**Serial Data Receive:** Receive data line of the serial control interface (SCI)
5	SA	IO	**Programmable I/O PCI Pin SA:** This port pin is only available in IOM-2 TE-mode
	SDX	OD/O [3]	**Serial Data Transmit:** Transmit data line of the serial control interface (SCI)
19	V_{REF}	O	**2.4 V Output:** Output for biasing analog single ended inputs
8	MIP1	I	**Microphone Input 1:** This highly symmetrical differential input has been designed for commonly used telephone microphones
9	MIN1	I	

[1] see DD/DU-voice channel swapping (XOP_D)
[2] programmable via bit SDICR.EPP0
[3] programmable via bit SDICR.EPP1

1.1 Pin Definitions and Functions (cont'd)

Pin No. P-DSO P-LCC P-DIP	Symbol	Input (I) Output (O) Open Drain (OD)	Function
11 10	MIP2 MIN2	I I	**Microphone Input 2:** This highly symmetrical differential input has been designed for commonly used telephone microphones
12	MI3	I	**Microphone Input 3:** This single-ended input has been designed for commonly used telephone microphones
14 16	LSP LSN	O O	**Loudspeaker Output:** LSP & LSN are differential output pins which can drive a 50-Ω loudspeaker directly; a piezo transducer can also be used for ringing signal instead of the loudspeaker
17 18	HOP HON	O O	**Handset Earpiece Output:** HOP & HON are differential output pins which can drive handset earpiece transducers directly

1.2 Logic Symbol

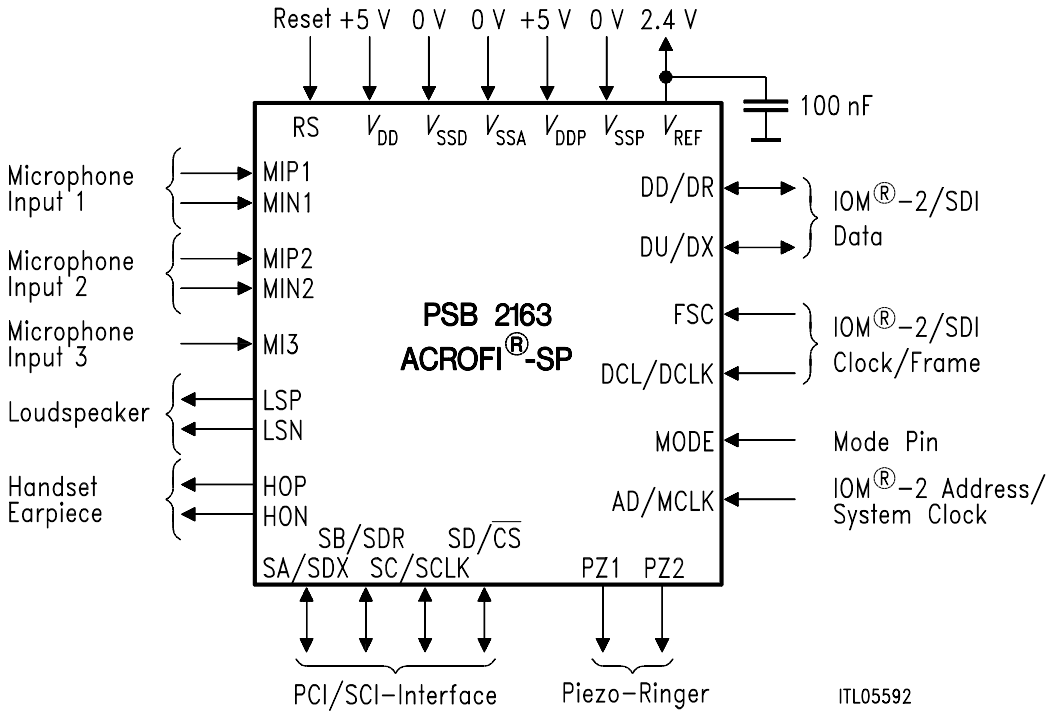


Figure 1
Logic Symbol of the ARCOFI®

1.3 Functional Block Diagram

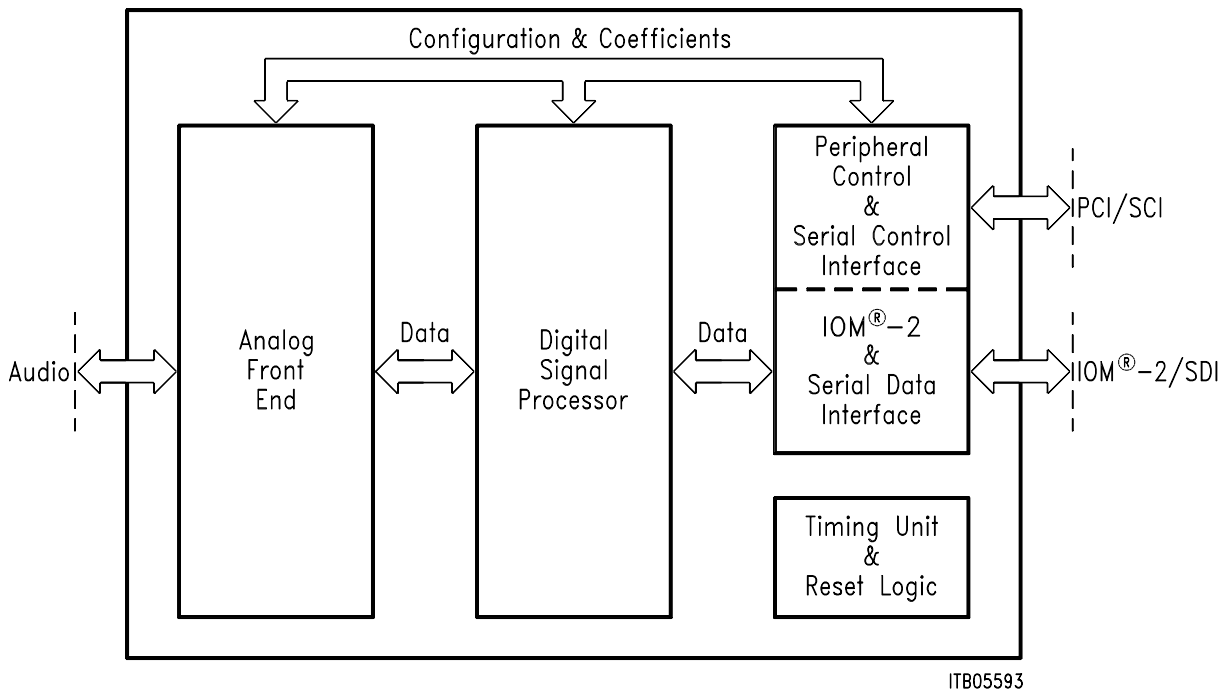


Figure 2
Block Diagram of the ARCOFI®

1.4 System Integration

The complete family of ICs for digital terminals offered by Siemens simplifies the development of these devices and gives a cost-effective solution to the design engineer. The architecture of these terminals is based on a modular interface especially conceived for ISDN and named IOM-2.

Figure 3 shows an example of an integrated multifunctional ISDN-S terminal using the ISAC®-S TE. The ISAC-S TE (ISAC-S: ISDN S-Access controller PSB 2186) provides the S interface and separates the B and D channels.

In this example one ICC (ICC: ISDN Communication Controller PEB 2070) is used to handle data packets on the D-channel. A voice processor is connected to a programmable digital signal processing codec filter (ARCOFI) via IC1 and a data encryption module to a data device via IC2. B1 is used for voice communication and B2 for data communication.

Typical terminal applications are described in the next sections.

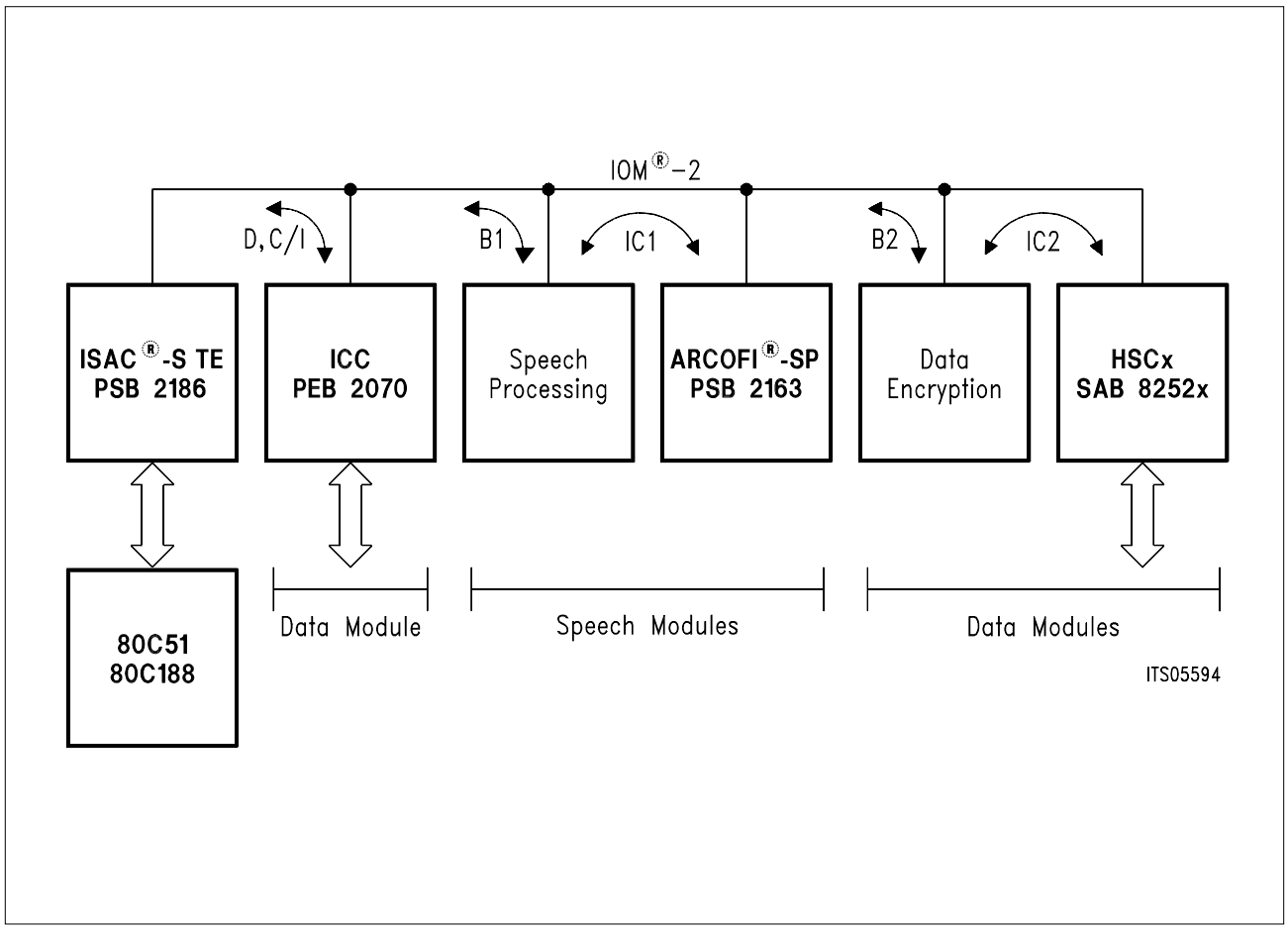


Figure 3
Example of ISDN-S Voice/Data Terminal

1.4.1 ISDN-Voice Terminal

Figure 4 shows a typical solution for a voice terminal for S interface.

The ARCOFI offers the functions of CODEC, filtering and speakerphone. It also carries out the functions of tone ringing, DTMF, and A/D- and D/A-conversions. The ARCOFI permits the direct connection of a handset and a speakerphone/loudspeaker.

The ARCOFI can be programmed and read out by the µC via the lOM-2-interface and the ISAC-S TE. The same µC supervises the keyboard functions and the function hook-on/off.

The S-interface functions such as activation/deactivation, clock recovery, clock resynchronization as well as the layer-2 functions like LAPD-protocol handling are executed by the ISDN-Subscriber Access Controller, also called ISAC-S TE PSB 2186.

A U_{K0}-interface telephone can easily be derived from the voice terminal shown on **figure 4** by replacing the ISAC-S with the ISDN-Communication Controller ICC PEB 2070 and the ISDN-Echo Cancellation Unit IEC PEB 2091.

A U_{P0}-interface telephone is obtained by interchanging the IEC with the ISDN-Burst Controller IBC PEB 2095. In this configuration the ICC PEB 2070 and the IBC PEB 2095 can be replaced by the ISAC-P TE PSB 2196.

Figure 5 shows a typical solution for a voice terminal for U_{K0}- or U_{P0}-interface.

In any case the whole terminal is power supplied either by the ISDN-Remote Power Controller IRPC PSB 2120 or by the General Purpose Power Controller GPPC PSB 2121.

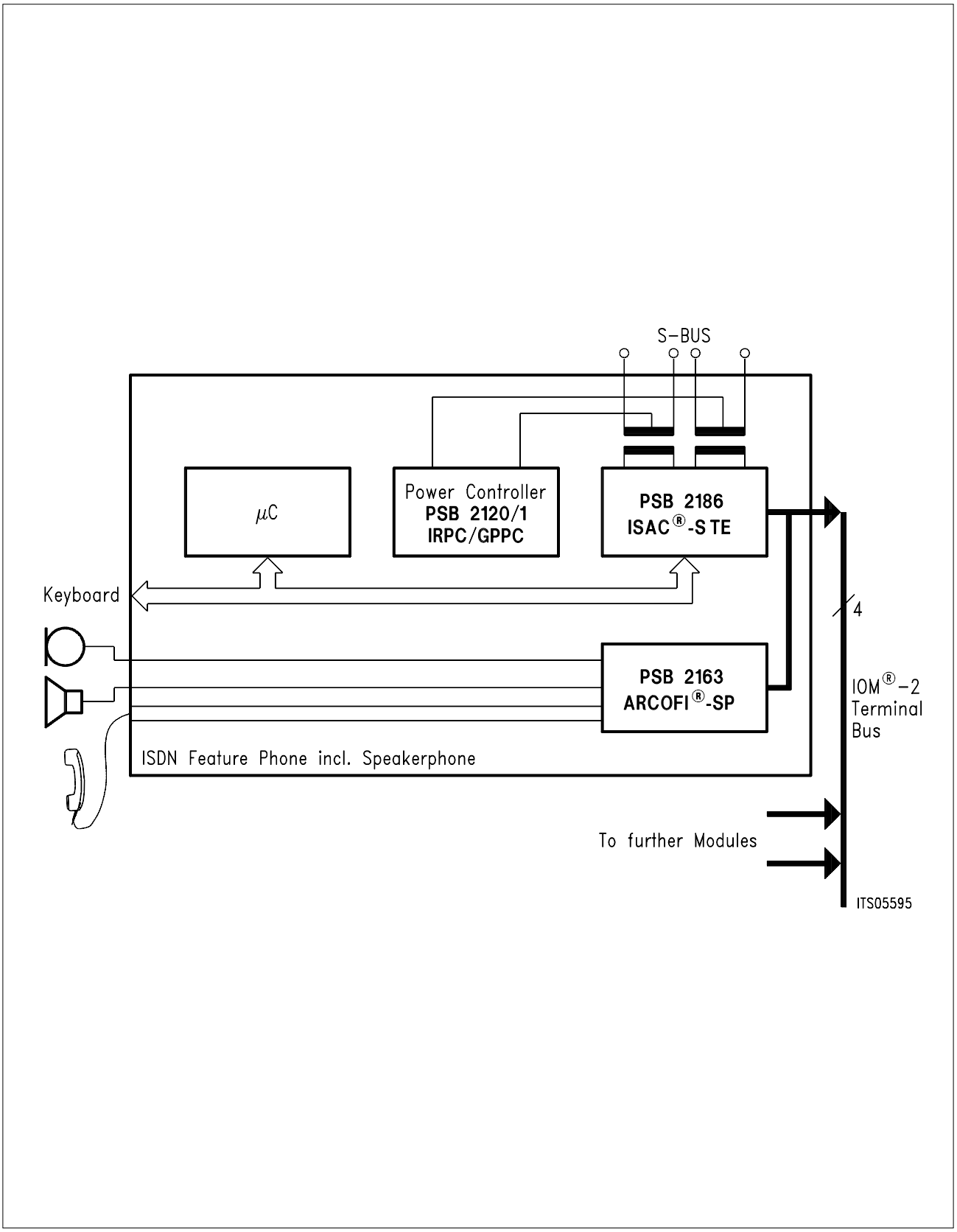
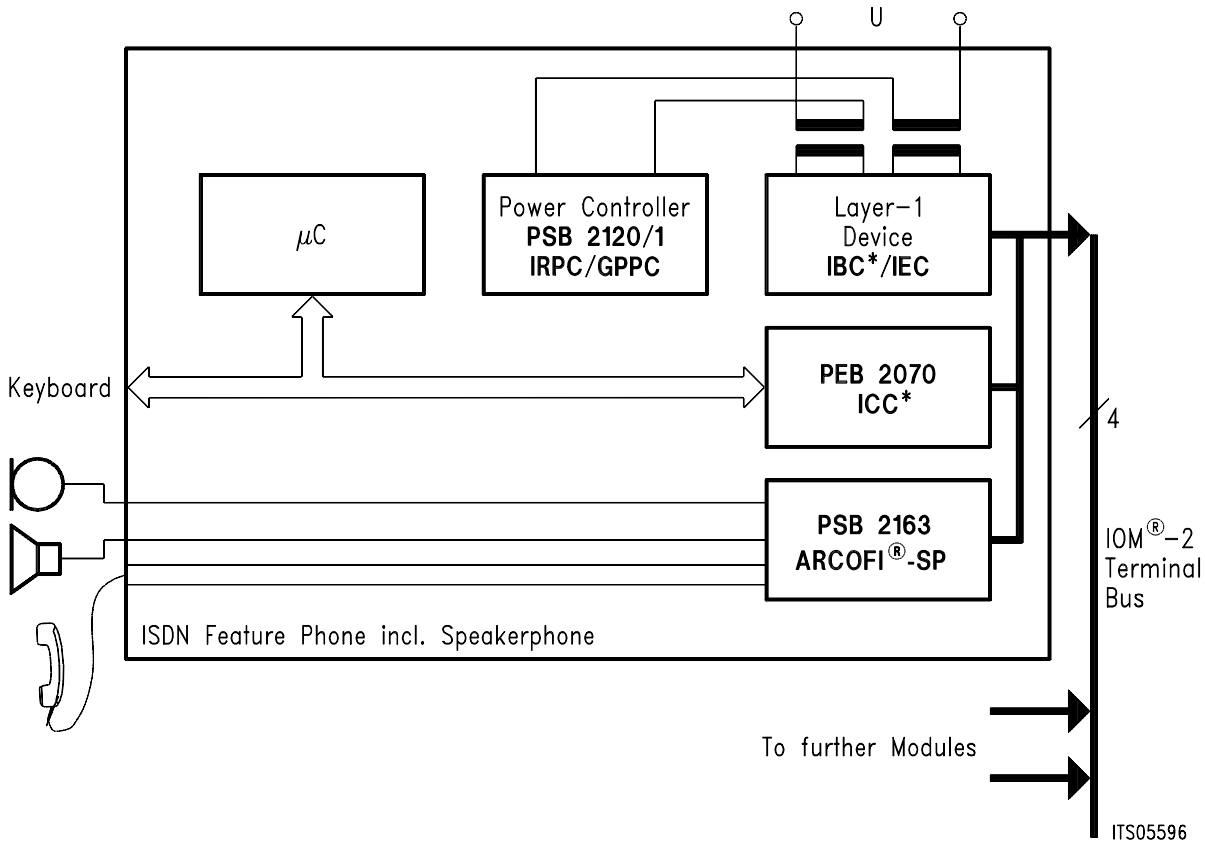


Figure 4
Basic ISDN S-Voice Terminal



*** ICC and IBC can be replaced by the ISAC®-P TE PSB 2196**

Figure 5
Basic ISDN U-Voice Terminal

1.4.2 Terminal Adapter a, b for Analog Telephones

Figure 6 shows how to implement a terminal adapter (a, b) connecting analog telephones to the ISDN-world. A SLIC can be connected to the ARCOFI.

The tip and ring information is transmitted transparently through the ARCOFI via the C/I-channel of the IOM-channel 1, through the ISAC-S TE to the µC.

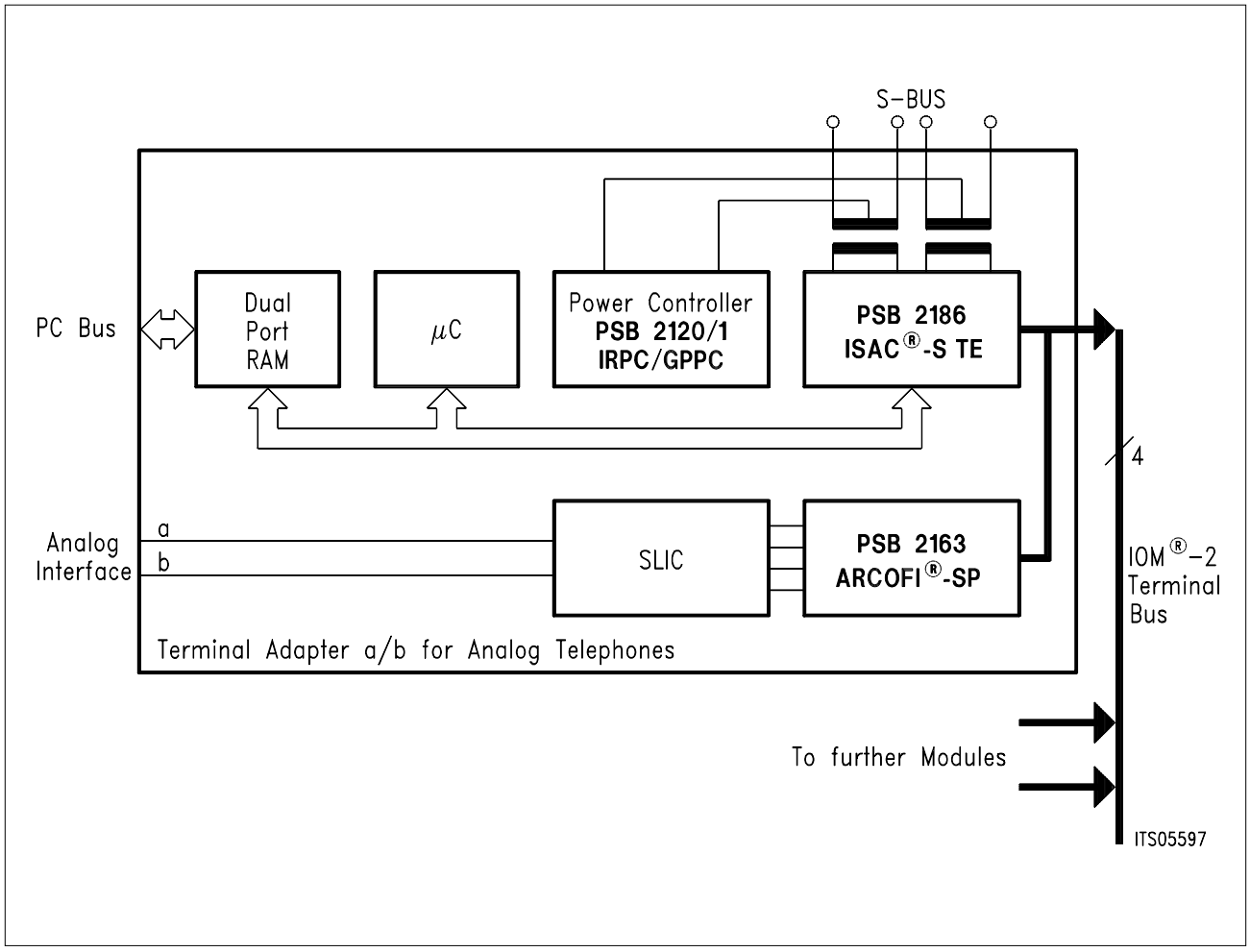


Figure 6
Terminal Adapter a, b for Analog Telephones

1.4.3 Voice/Data Terminal (PC-Card)

Figure 7 shows a voice/data terminal developed on a PC-card. The ITAC PSB 2110 (ITAC: ISDN-Terminal Adapter Circuit) ensures the bit rate adaptation necessary to connect a non ISDN-terminal (V.24) to the ISDN-world.

The COM-IC is an UART (type: 8250 or 16450) which is necessary for modem applications.

The Dual Port RAM is used for data transfer between the terminal processor and the PC.

The card is powered by the PC, and thus no power controller is necessary.

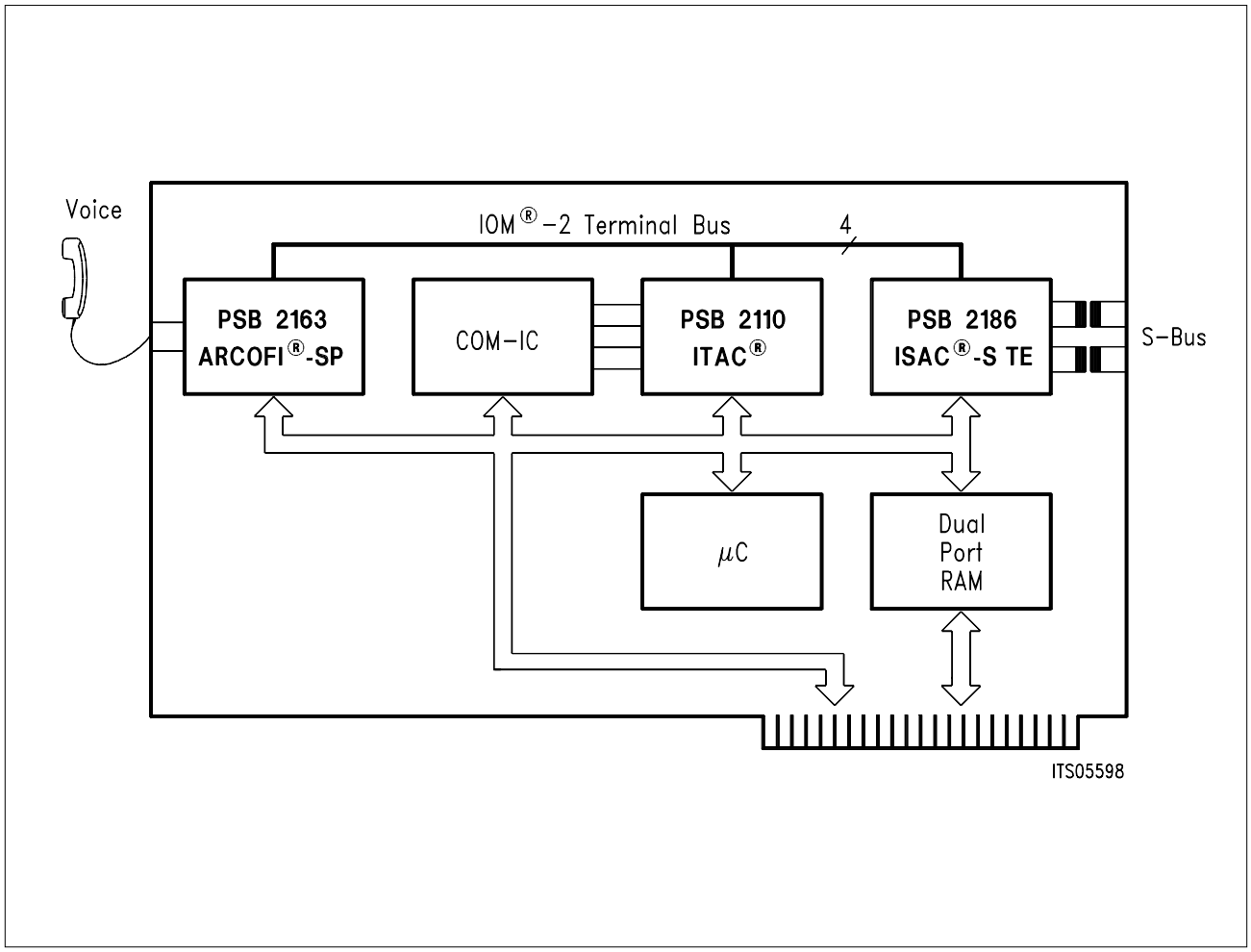


Figure 7
PC-Card as an ISDN-Voice/Data Terminal

1.4.4 Multifunctional ISDN-Terminal

Figure 8 gives an example of a multifunctional terminal. The HSCX SAB 82525 (HSCX: High-Level Serial Communications Controller Extended) simplifies the realization of an intelligent X.25 terminal adapter module whereas the ITAC PSB 2110 offers X.21, V.24, V.110 or V.120 interfaces for non ISDN-terminals.

The µC connected to the ISAC-S TE PSB 2186 is the system master. The two other µCs are the slaves. When a slave µC wants to intervene, it informs the master via the C/I-channel of IOM-2 channel 1.

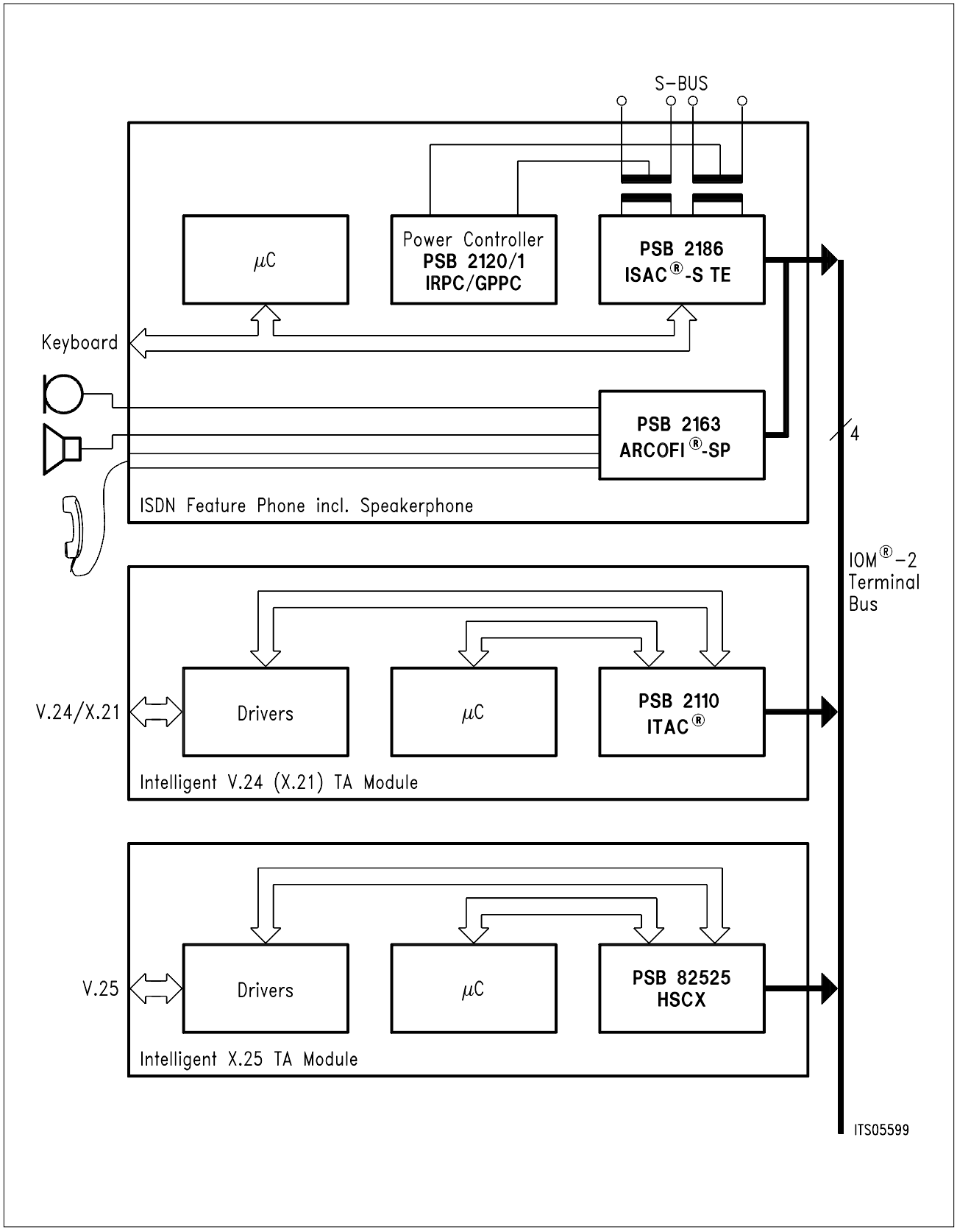


Figure 8
Multifunctional ISDN-Terminal

1.4.5 Digital Voice Terminal

The Serial Control Interface allows the ARCOFI to be programmed directly from a serial port of a microcontroller.

The voice data may be transmitted via the IOM-2 interface or on a PCM-interface provided from other transceiver devices. If the Serial Data Interface (SDI) is selected the PCM-data rate can vary from 64 kbit/s up to 4096 kbit/s.

Figure 9 shows a PABX-voice terminal using the ISAC-P TE PSB 2196 together with a Motorola type microcontroller. **Figure 10** shows a PABX-voice terminal using a transceiver device without IOM-2 interface.

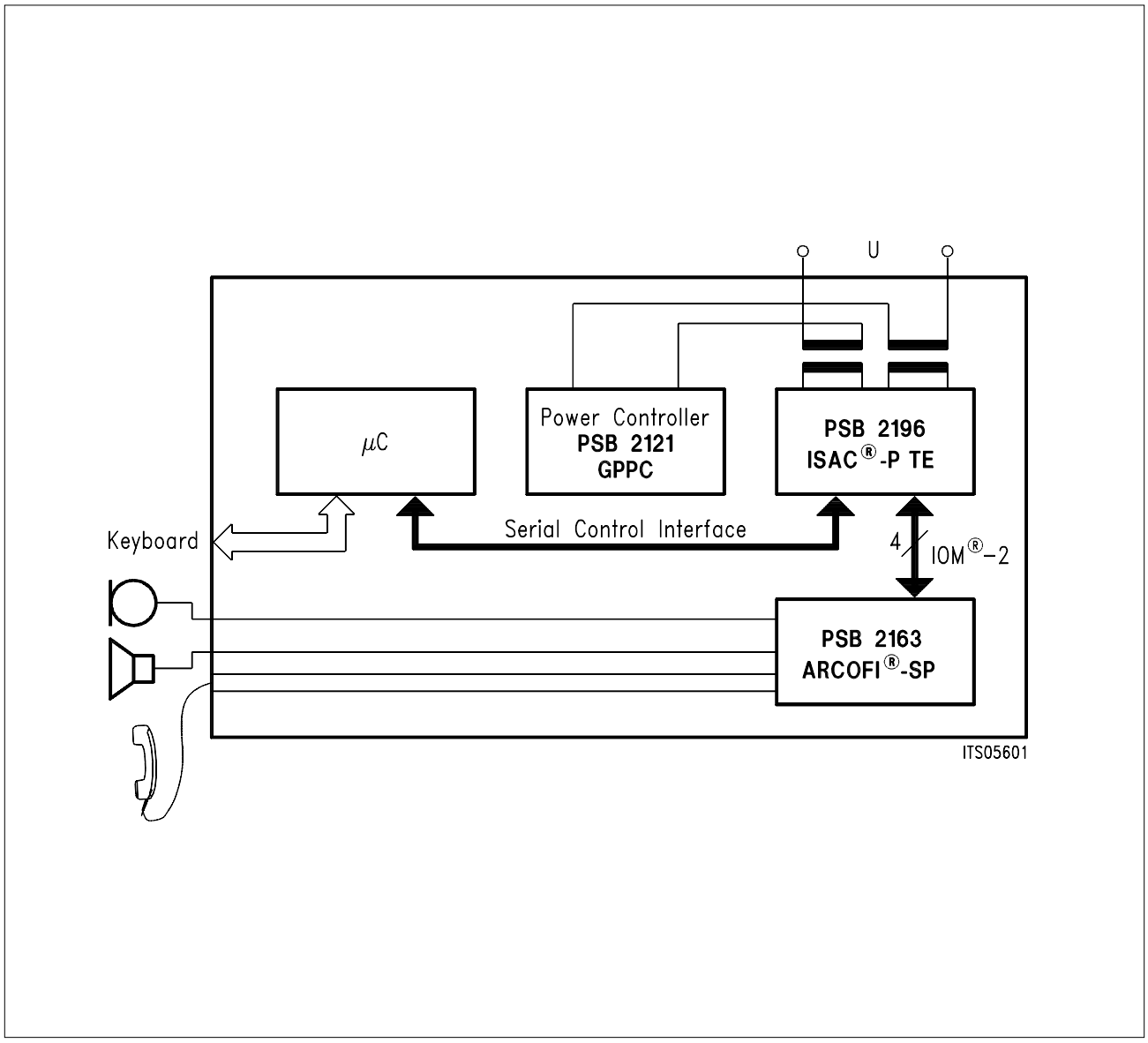


Figure 9
U_{P0} PABX-Voice Terminal

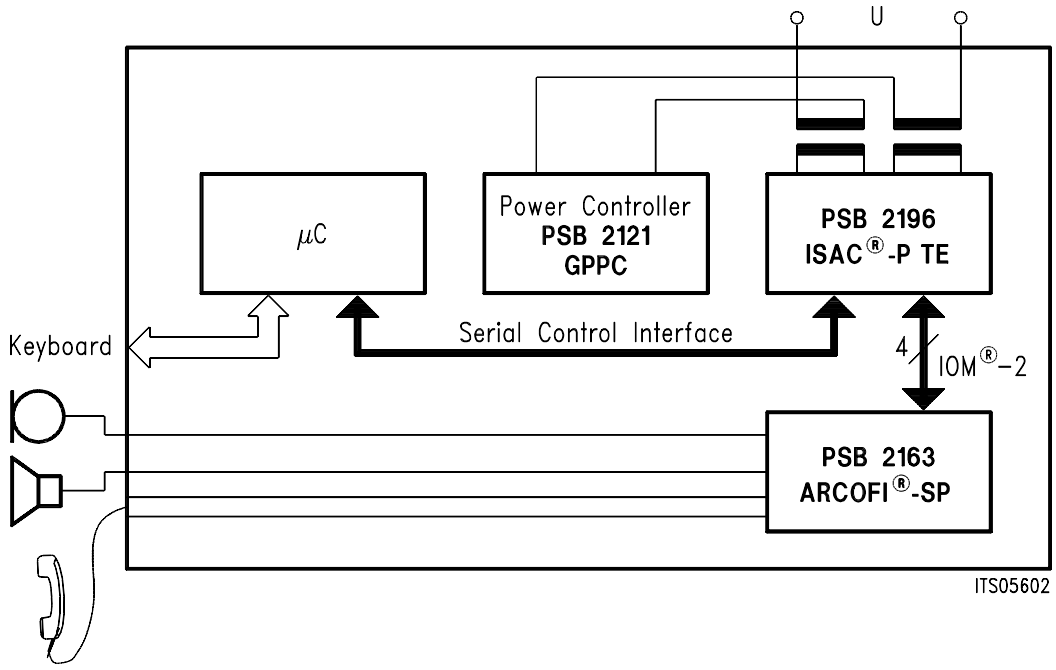


Figure 10
PABX-Voice Terminal in Non-IOM®-2 Architecture

1.4.6 IOM®-2 Line Card Application

Some applications require the ARCOFI to connect directly to the IOM-2 interface of a line card. The lOM-channel is selected via pin-strapping. The ARCOFI is programmed via the MONITOR channel of the selected lOM-channel. Up to two ARCOFIs can be distinguished via AD input on the same IOM-channel.

This configuration allows control of up to 16 ARCOFIs on one IOM-2 interface of a line card controller.

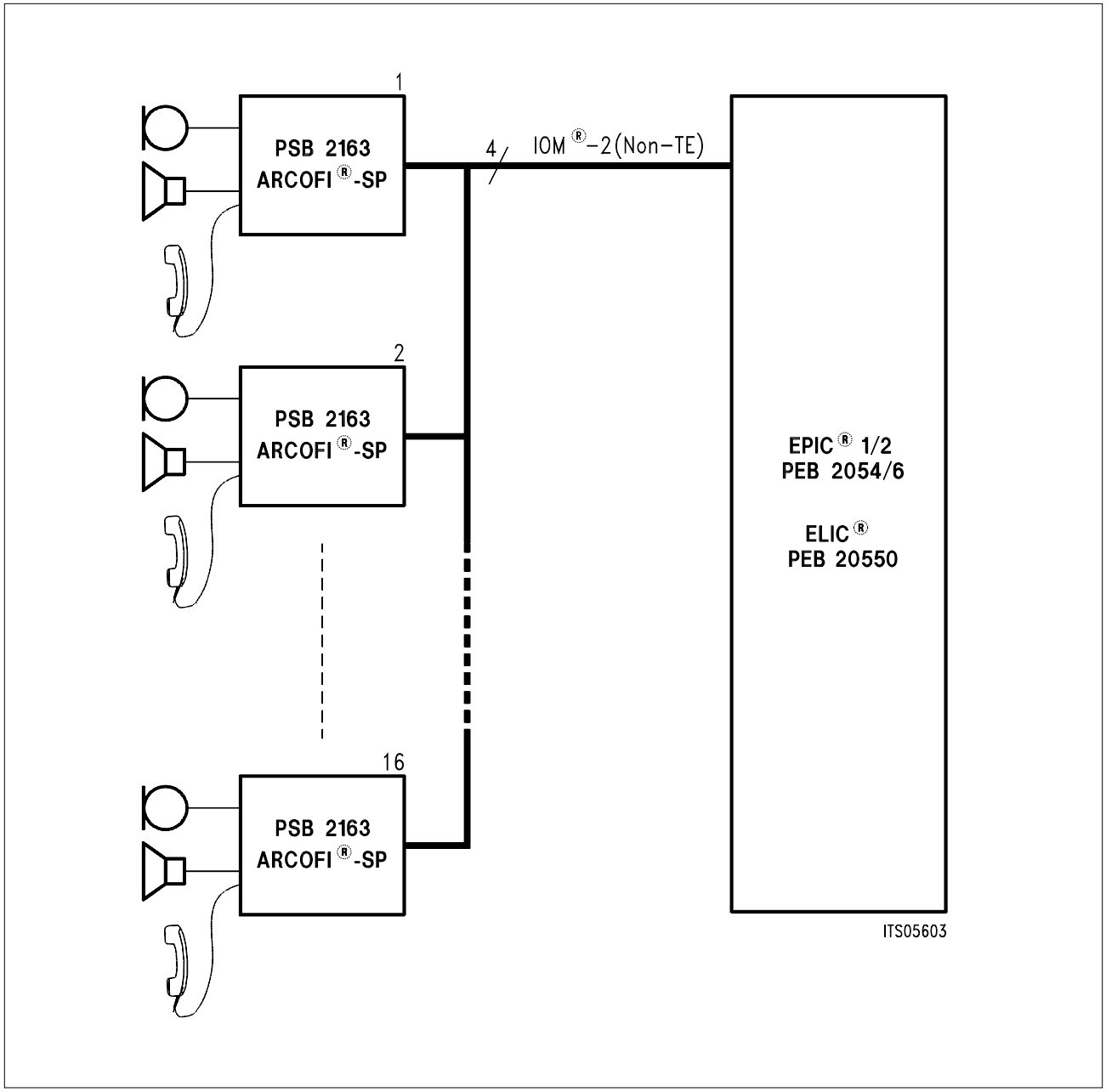


Figure 11
ARCOFI® Line-Card Application

1.4.7 Primary Rate Application

The ARCOFI is designed to be connected to a 24 or 32 time-slot PCM-interface used e.g. on primary rate equipment. The PCM-data is transmitted via the serial data interface while programming of the ARCOFI is done on the serial control interface.

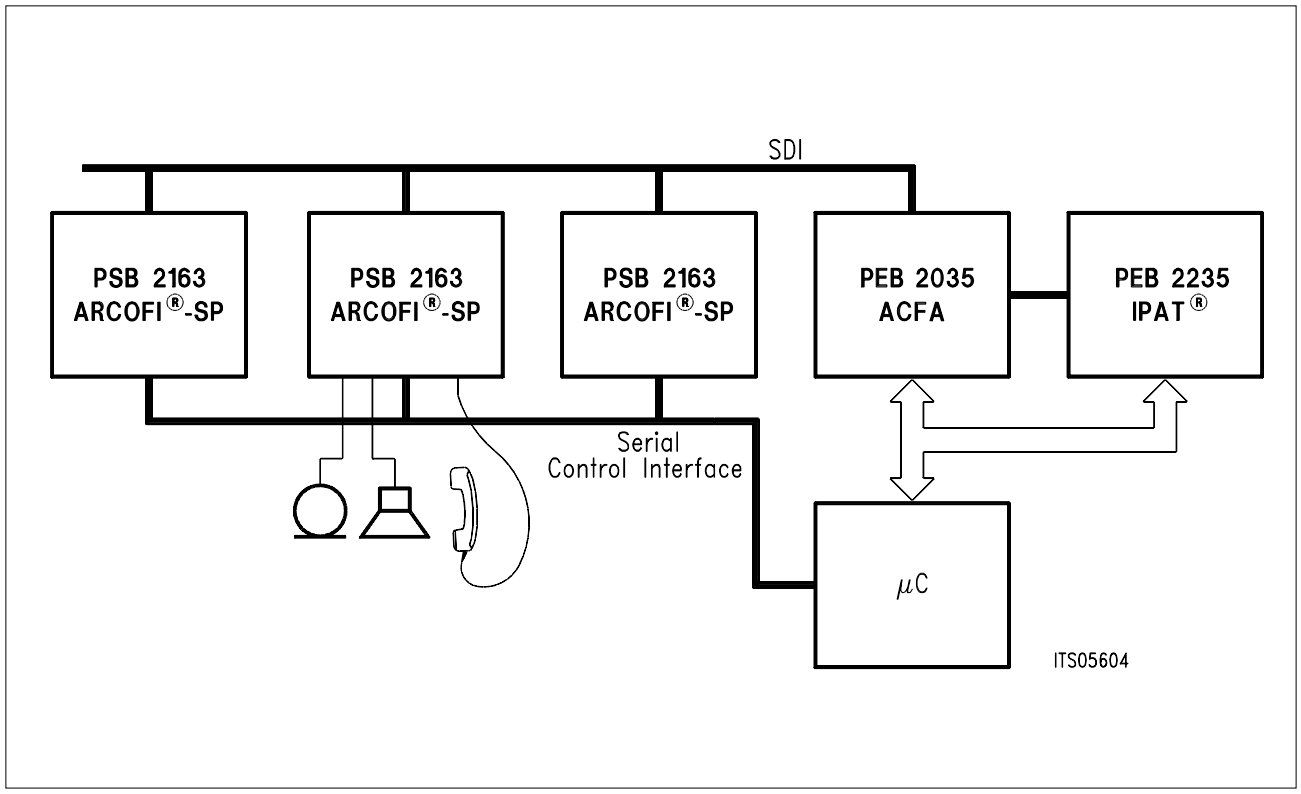


Figure 12
Primary Rate Application

1.4.8 Group 3 Fax / Modem Adapter

The ARCOFI can be connected to a standard fax or modem chip set designed for analog networks. The ARCOFI converts the analog signal to PCM-data which are transmitted over the digital network.

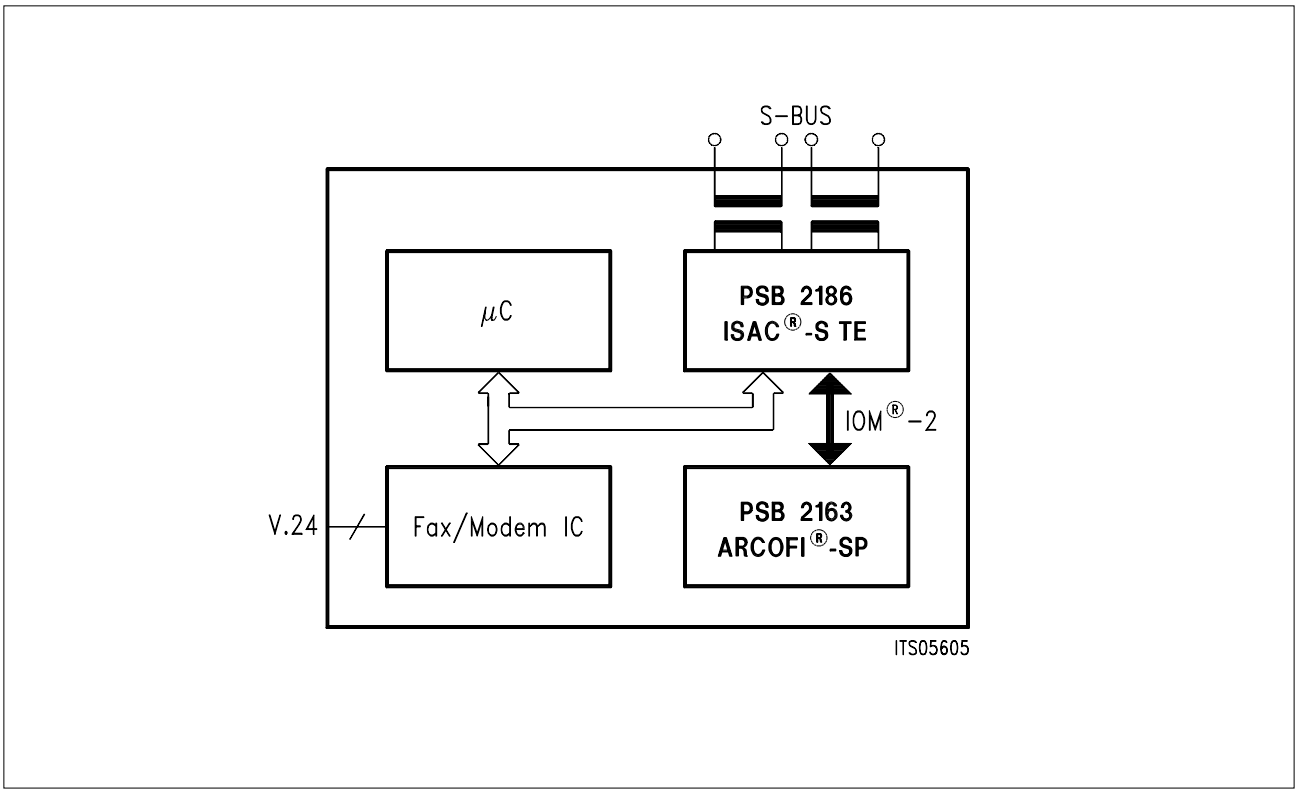


Figure 13
Group 3 Fax/Modem Adapter

2 Functional Description

The ARCOFI bridges the gap between the audio world of microphones, earphones, loudspeakers and the PCM-digital world by providing a full PCM-CODEC with all the necessary transmit and receive filters. A block diagram of the ARCOFI is shown in **figure 14**.

The ARCOFI can be subdivided in three main blocks:

- The ARCOFI Analog Front End (AFE)
- The ARCOFI Signal Processor (ASP)
- The ARCOFI Digital Interface (ADI)

A detailed description can be found in the following chapters.

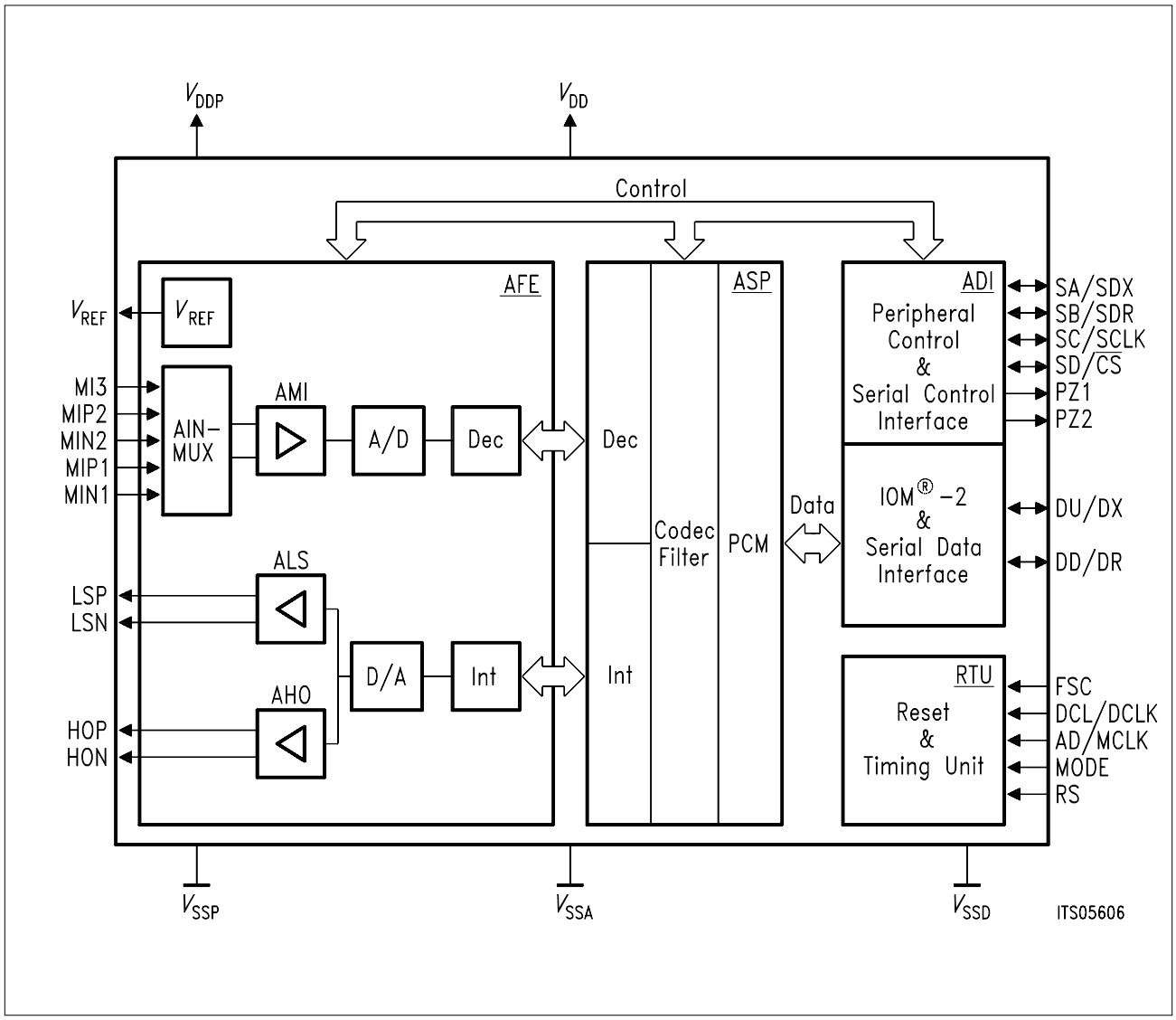


Figure 14
Architecture of the ARCOFI®

2.1 Analog Front End (AFE) Description

The Analog Front End section of the ARCOFI is the interface between the analog transducers and the digital signal processor. In the transmit direction, the AFE-function is to amplify the transducer input signals (microphones) and to convert them into digital signals. In the AFE-receive section, the incoming digital signal is converted to an analog signal which is output to an earpiece and/or a loudspeaker.

A block diagram of the AFE is shown in **figure 15**.

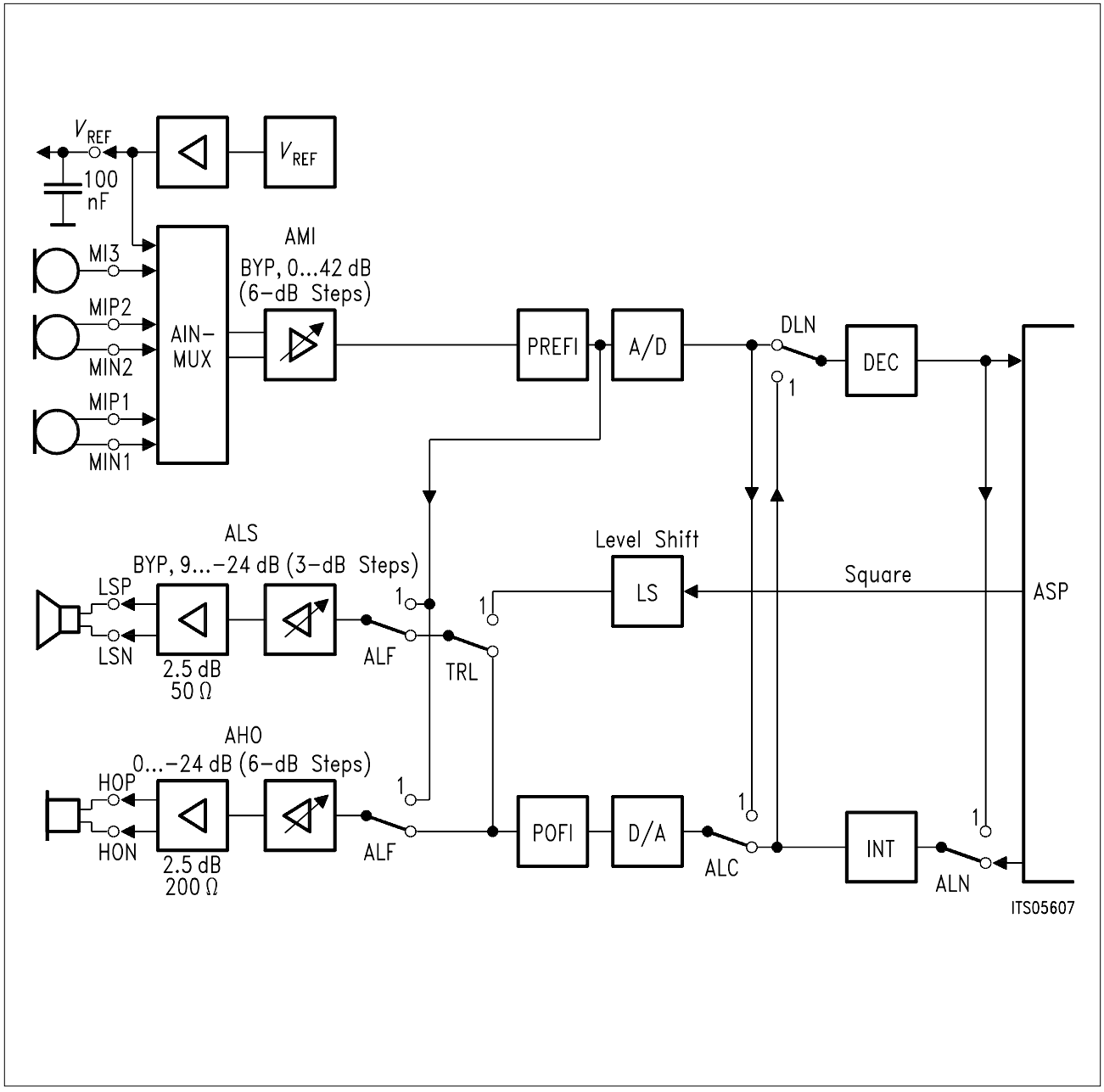


Figure 15
Signal Flow Graph of the AFE

2.1.1 Description of the Analog I/O

Two differential inputs (MIP1/MIN1 and MIP2/MIN2) and one single-ended input (MI3) are connected to the amplifier AMI via an analog input multiplexer. The programmable amplifier AMI provides a coarse gain adjustment range. Fine gain adjustment is performed in the digital domain via the programmable gain adjustment stage GX (see signal processor section). This allows a perfect level adaptation to various types of microphone transducers without loss in the signal to noise performance.

Fully differential output HOP/HON connects the amplifier AHO to a handset earpiece. Differential output LSP/LSN is provided for use with a 50-Ω loudspeaker. Up to 100 mW (sine wave) of power can be delivered to the loudspeaker via the amplifier ALS. The programmable amplifiers AHO and ALS provide a coarse gain adjustment range. Fine gain adjustment is performed in the digital domain via the programmable adjustment stage GR.

Two implemented AFE-configuration registers (ATCR & ARCR) provide a high flexibility to accommodate an extensive set of user procedures and terminal attributes.

2.1.2 AFE-Attenuation Plan

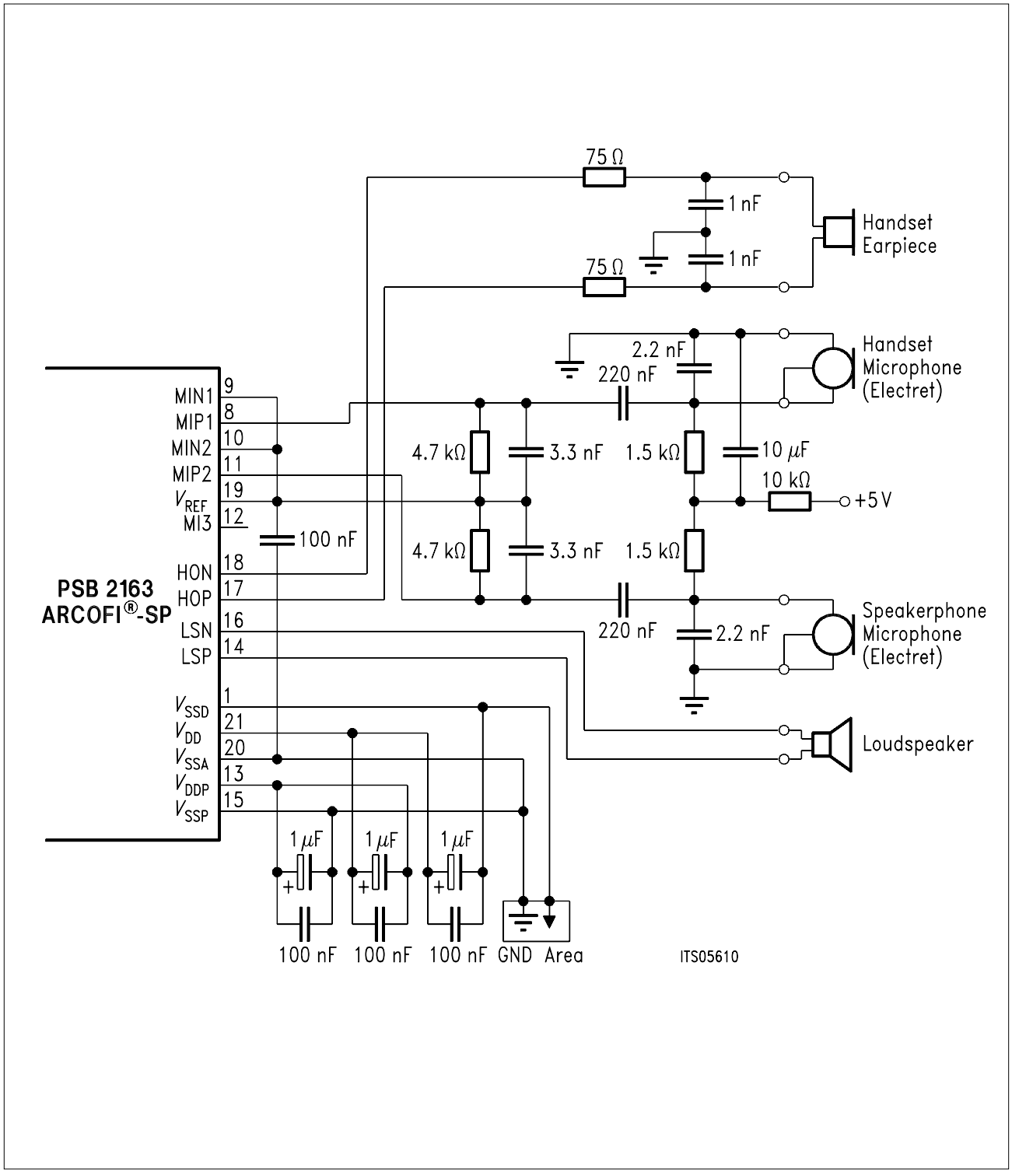
Transmit Direction

Parameter Transmit	Limit Values		Unit	Reference
	0dBm0	max.		
MIP1/MIN1 MIP2/MIN2 Microphone input level at max gain AMI = 42 dB	1.33E-02 9.38E-03 – 42 – 38.33	1.91E-02 1.35E-02 – 38.86 – 35.19	Vp Vrms dBm0 dBm	V V 1.2 V 0.775 V
MIP1/MIN1 MIP2/MIN2 Microphone input level at min gain AMI = 0 dB	1.67E-00 1.18E-00 0 3.67	2.40E-00 1.70E-00 3.14 6.81	Vp Vrms dBm0 dBm	V V 1.2 V 0.775 V
MI3 Input level at max gain AMI = 24 dB	1.06E-01 7.46E-02 – 24 – 20.37	1.51E-01 1.07E-01 – 20.86 – 17.19	Vp Vrms dBm0 dBm	V V 1.2 V 0.775 V
MI3 Input level at min gain AMI = 0 dB	8.36E-01 5.91E-01 – 6 – 2.33	1.20E-00 8.49E-01 – 2.86 0.81	Vp Vrms dBm0 dBm	V V 1.2 V 0.775 V

Receive Direction

Parameter Receive	Limit Values		Unit	Reference
	0dBm0	max.		
LSP/LSN Output level symmetrical in a 50-Ω load ALS = 2.5 dB	2.23E-00 1.58E-00 2.5 6.17	3.20E-00 2.26E-00 5.64 9.31	Vp Vrms dBm0 dBm	V V 1.2 V 0.775 V
LSP/LSN Output level symmetrical in a 50-Ω load ALS = – 21.5 dB	1.41E-01 9.95E-02 – 21.5 – 17.83	2.02E-01 1.43E-01 – 18.36 – 14.69	Vp Vrms dBm0 dBm	V V 1.2 V 0.775 V
HOP/HON Output level symmetrical in a 200-Ω load AHO = 2.5 dB	2.23E-00 1.58E-00 2.5 6.17	3.20E-00 2.26E-00 5.64 9.31	Vp Vrms dBm0 dBm	V V 1.2 V 0.775 V
HOP/HON Output level symmetrical in a 200-Ω load AHO = – 15.5 dB	2.81E-01 1.99E-01 – 15.5 – 11.83	4.03E-01 2.85E-01 – 12.36 – 8.69	Vp Vrms dBm0 dBm	V V 1.2 V 0.775 V

2.1.3 Interface to Acoustic Transducers



Note: ESD and EMV requirements are not included.

Figure 16
Example to Connect the AFE to Acoustic Transducers

2.2 ARCOFI® Signal Processor (ASP) Description

The ARCOFI signal processor (ASP) has been conceived to perform all CCITT and ETSI (NET33) recommended filtering in transmit and receive paths and is therefore fully compatible to the G.714 CCITT and ETSI (NET33) specifications. The data processed by the ASP is provided in the transmit direction by an oversampling A/D-converter situated in the analog front end (AFE). Once processed, the speech signal is converted into an 8 bit A-law or μ-law PCM-format or remains as a 16-bit linear word (2s complement) if the compander is by-passed. The by-passing of the companding depends on the bit setting in the configuration register DFICR (VDM-bits).

In the receive direction, the incoming PCM-stream is expanded into a linear format (if the linear mode is selected, the expansion logic is by-passed) and subsequently processed until it is passed to the oversampling D/A-converter.

Additionally to these standard codec functions, the ARCOFI provides a universal tone generation unit and a high quality speakerphone function.

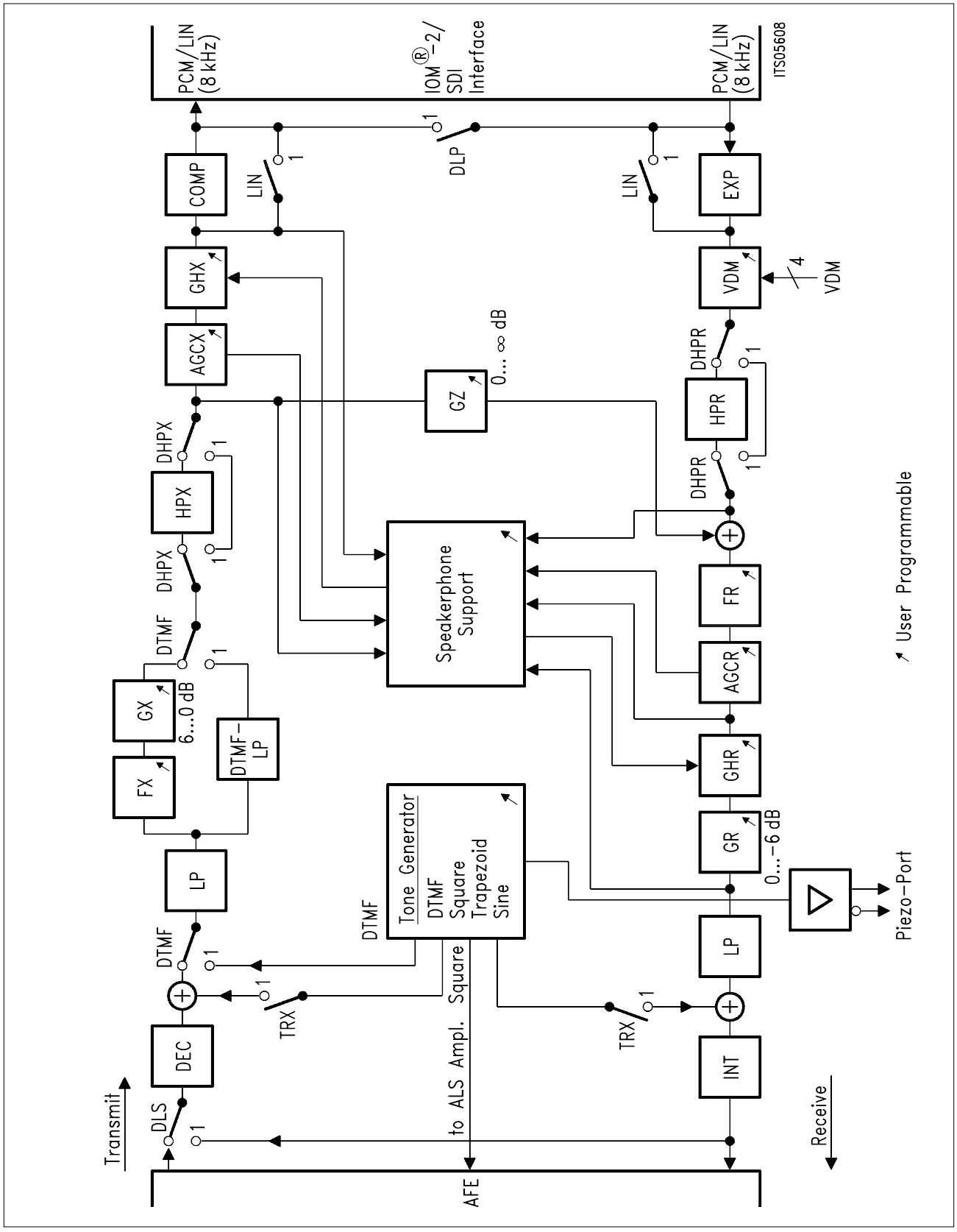


Figure 17
Processor Signal Flow Graph

2.2.1 Transmit Signal Processing

In the transmit direction a series of decimation filters reduces the sampling rate down to the 8-kHz PCM-rate. These filters attenuate the out-of-band noise by limiting the transmit signal to the voice band.

The decimation stages end with a EWDF low-pass filter which band-limits the voice signal to the CCITT G.714 and ETSI (NET33) recommendations. The ARCOFI meets or exceeds all the CCITT and ETSI (NET33) recommendations on attenuation distortion and group delay distortion.

If the tone generation unit is connected to the transmit direction (TGSR.DTMF = 1), a special 2-kHz DTMF-low-pass filter is placed in the transmit path. This filter guarantees an attenuation of all unwanted frequency components, if DTMF-signals are transmitted. Additionally, it is possible to add a programmable tone signal to the transmit voice signal (TGSR.TRX = 1).

The GX-gain adjustment stage is digitally programmable allowing the gain to be programmed from + 6 to 0 dB in steps of ≤ 0.25 dB (– ∞ dB and others are also possible). Two bytes are necessary to set GX to the desired value. On reset, the GX-gain stage is by-passed.

The transmit path contains a programmable high performance frequency response correction filter FX allowing an optimum adaptation to different types of microphones (dynamic, piezoelectric or electret). Twelve bytes are necessary to set FX to the desired frequency correction function. On reset, the FX-frequency correction filter is by-passed. **Figure 18** shows the architecture of the FX/FR-filter.

A high-pass filter (HPX) is also provided to remove power line frequencies.

The voice signal, after being linearly processed, can be output as an 8-bit PCM-word according to the CCITT G.711 A-law or the North-American μ-law format. If desired the companding stage can be by-passed, a 16-bit linear word (2s complement) is then output to the IOM-2 or SDI-interface.

2.2.2 Receive Signal Processing

In the receive path the incoming PCM-signal is expanded into a linear code according to the selected A-law or μ-law. If the linear mode is chosen, the PCM-expander circuit is by-passed and a 16-bit linear word (2s complement) has to be provided to the processor.

The block VDM offers several possibilities of voice/data manipulation for special applications.

A programmable sidetone gain stage GZ adds a sidetone signal to the incoming voice signal. The sidetone gain can be programmed from – 54 to 0 dB within a ± 1 dB tolerance

range (– ∞ dB and others are also possible). Respectively two bytes are coded in the CRAM to set GZ to the desired value. On reset, the GZ-gain stage is disabled (– ∞ dB).

A high-pass filter (HPR) is also provided to remove disturbances from 0 to 50/60 Hz due to the telecommunication network.

The FR-frequency correction response filter is similar to the FX-filter allowing an optimum adaptation to different types of loudspeakers or earpieces. Twelve bytes are necessary to set FR to the desired frequency correction function. On reset, the FR-frequency correction filter is by-passed.

The GR-gain adjustment stage is digitally programmable from – 6 to 0 dB in steps ≤ 0.25 dB (– ∞ dB and others are also possible). Respectively two bytes are coded in the CRAM to set GR to the desired value. On reset, the GR-gain stage is by-passed.

A low-pass EWDF-filter limits the signal bandwidth in the receive direction according to CCITT and ETSI (NET33) recommendations.

A series of low-pass interpolation filters increases the sampling frequency up to the desired value.The last interpolator feeds the D/A-converter.

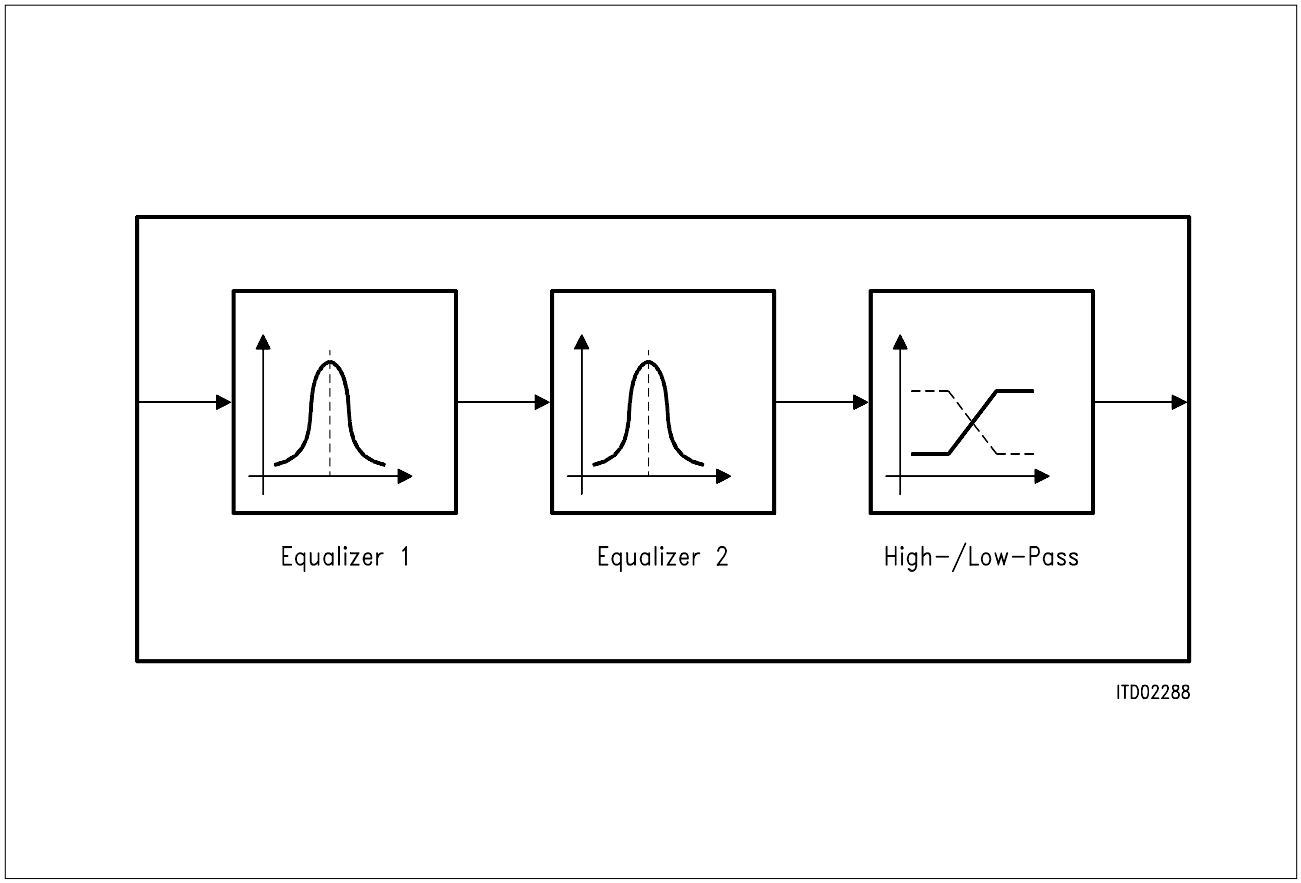


Figure 18
Architecture of the FX- and FR-Correction Filter

2.2.3 Programmable Coefficients

This section gives a short overview of important programmable coefficients. For more detailed information and about special applications, a special coefficient software package is available (ARCOS-SP PLUS SIPO 2163).

Description of the programmable level adjustment parameters:

Parameter	# of CRAM Bytes	Range	Comment
GX	2	12 to – ∞ dB **6 to 0 dB**	Transmit gain adjustment Transmission characteristics guaranteed
GR	2	12 to – ∞ dB **0 to – 6 dB**	Receive gain adjustment Transmission characteristics guaranteed
GZ	2	12 to – ∞ dB	Sidetone gain adjustment

Coefficients for GX, GR and GZ:

Gain [dB]	MSB	LSB	Gain [dB]	MSB	LSB	Gain [dB]	MSB	LSB
12.0	10_H	01_H	0	$A0_H$	01_H	– 12.0	$A9_H$	01_H
11.0	10_H	31_H	– 0.5	$B3_H$	42_H	– 13.0	$9C_H$	51_H
10.0	10_H	13_H	– 1.0	$A3_H$	$2B_H$	– 14.0	99_H	13_H
9.0	01_H	$4B_H$	– 1.5	$A2_H$	32_H	– 15.0	$8C_H$	$1B_H$
8.0	20_H	94_H	– 2.0	BB_H	$4A_H$	– 16.0	82_H	$7B_H$
7.0	30_H	94_H	– 2.5	BB_H	13_H	– 17.0	84_H	$4B_H$
6.0	13_H	51_H	– 3.0	BA_H	29_H	– 18.0	89_H	$6A_H$
5.5	$B0_H$	39_H	– 3.5	BA_H	$5B_H$	– 19.0	$8B_H$	$0C_H$
5.0	$A0_H$	49_H	– 4.0	$A2_H$	01_H	– 20.0	84_H	$1C_H$
4.5	23_H	01_H	– 4.5	AA_H	$1B_H$	– 21.0	$8C_H$	$1C_H$
4.0	22_H	$B4_H$	– 5.0	$9B_H$	$3A_H$	– 22.0	82_H	$7C_H$
3.5	23_H	12_H	– 5.5	AA_H	33_H	– 23.0	84_H	$4C_H$
3.0	32_H	$A4_H$	– 6.0	AA_H	22_H	– 24.0	89_H	$6B_H$
2.5	$B1_H$	BC_H	– 7.0	$B9_H$	$2C_H$	– 25.0	$8B_H$	$0D_H$
2.0	$B1_H$	03_H	– 8.0	$9A_H$	BC_H	– 26.0	84_H	$1D_H$
1.5	33_H	39_H	– 9.0	$9B_H$	13_H	– ∞	88_H	01_H
1.0	$B2_H$	$5A_H$	– 10.0	$9B_H$	32_H			
0.5	$B3_H$	49_H	– 11.0	93_H	02_H			

2.2.4 Tone Generation

2.2.4.1 Tone Generation Architecture

The ASP contains a universal tone generator which can be used for tone alerting, call progress tones, DTMF-signals or other audible feedback tones.

For the receive channel, a universal switching to each signal path (earpiece, loudspeaker and piezo ringer) is implemented. In the earpiece and loudspeaker direction, an addition of the programmed tone sequence (sine-wave, trapezoid, square-wave and DTMF) with the incoming voice signal is possible.

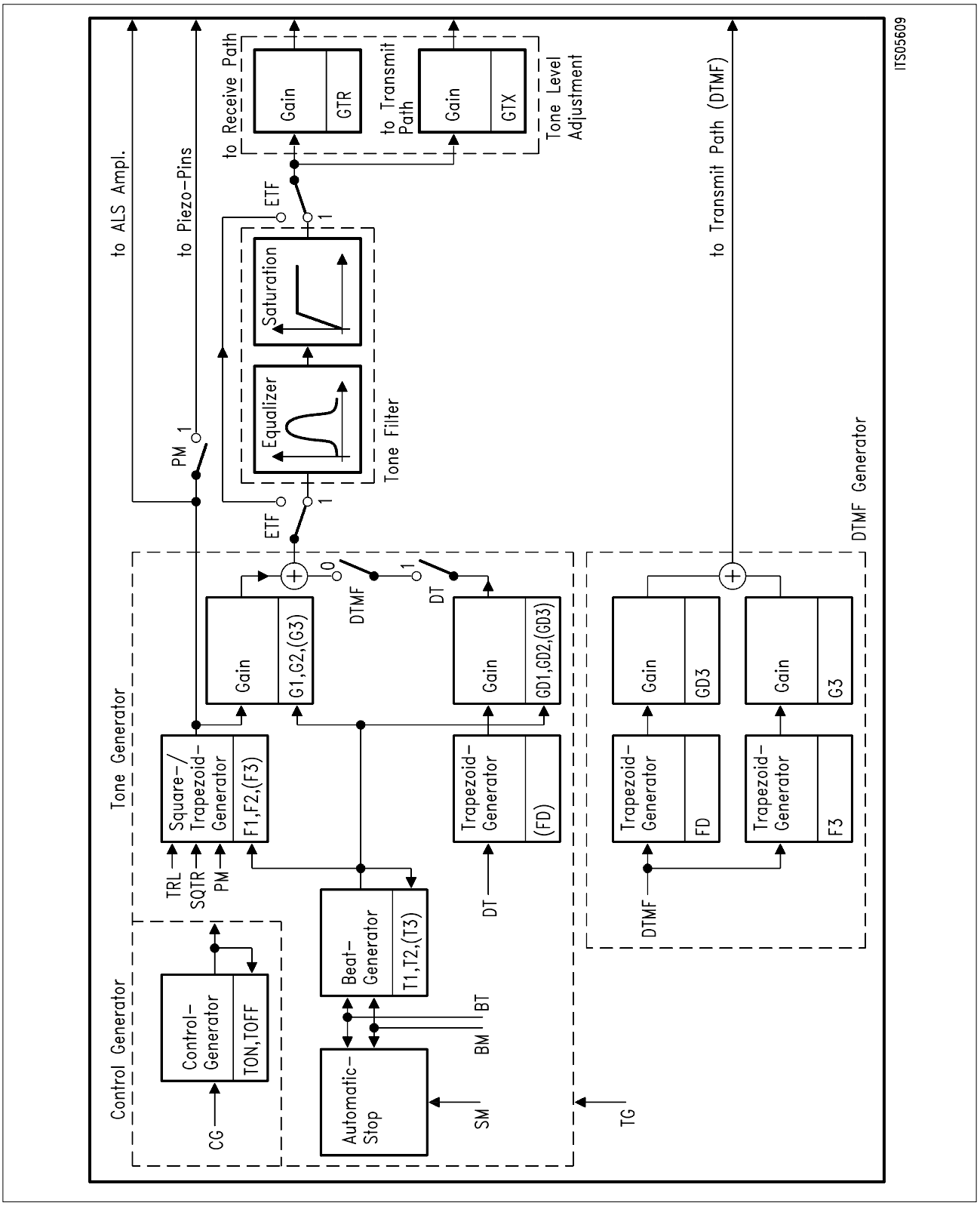
For the transmit direction, a supplementary DTMF-generator is implemented. If the DTMF-generator is active (TGSR.DTMF = 1), only a part of the tone generator (TG) is available for the receive direction (one or two tone sequences). In addition, a universal switching to the transmit path is also possible (TGSR.TRX).

All the tone generation configurations are programmable in the registers TGCR and TGSR (see description in chapter 4). A signal flow graph of the ARCOFI-tone generation unit is shown in **figure 19**.

The tone generation can be subdivided into five main blocks:

- Control Generator (CG)
- Tone Generator (TG)
- Tone Filter (TF)
- Tone Level Adjustment (TLA)
- DTMF-Generator (DTG)

A detailed description of the five main tone generation blocks follows in the next sub-sections.



Note: Adjustments in brackets are only available if the DTMF-generator is switched off (TGCR.DTMF = 0).

Figure 19
Signal Flow Graph of the Tone Generation Unit

2.2.4.2 Control Generator

In conjunction with the control generator it is possible to generate very complex signal sequences without reprogramming the necessary parameters (e.g. pulsed three tone calls). Four typical applications for the control generator programming are shown in **figure 20**.

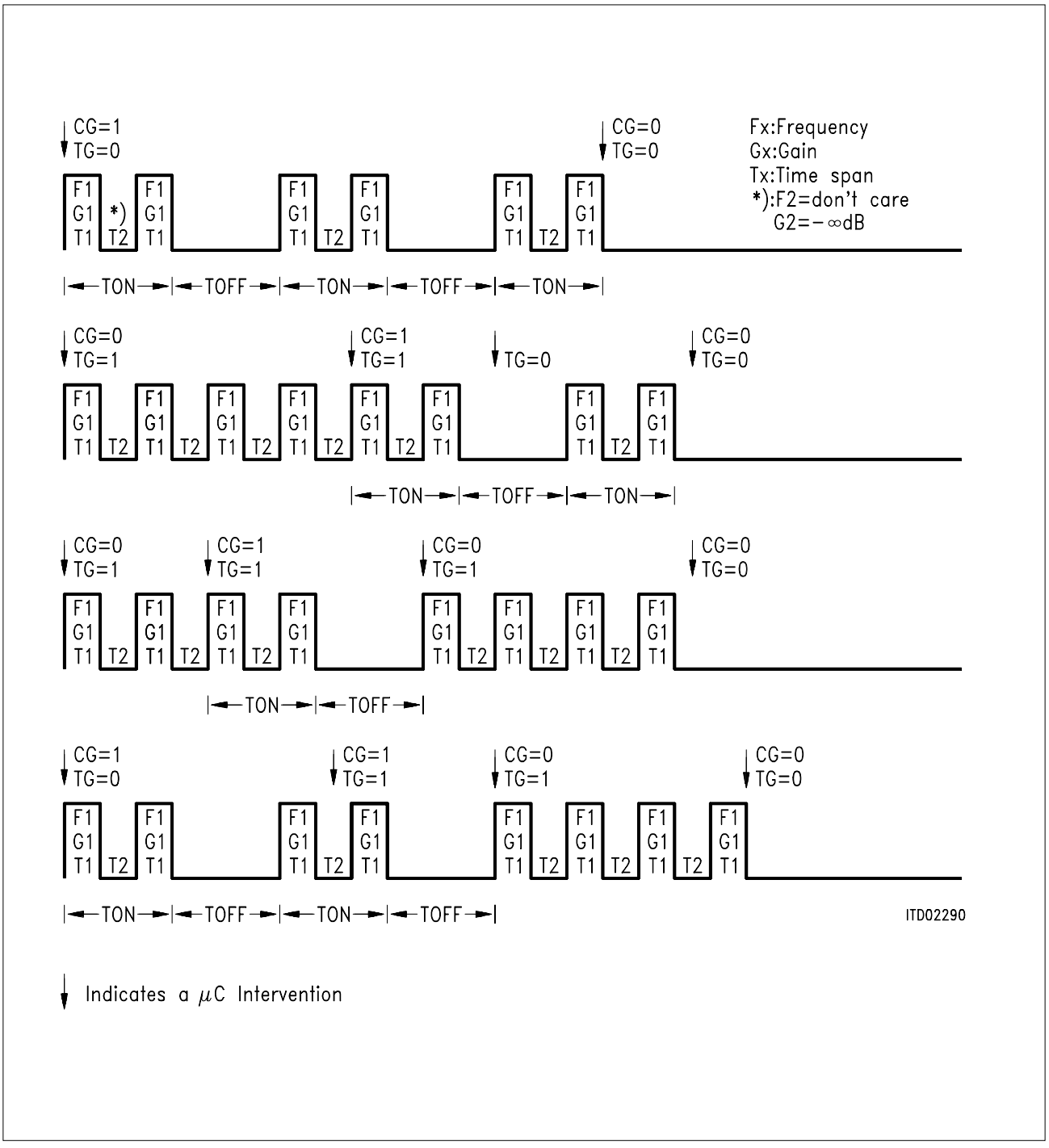


Figure 20
Typical Control Generator Application

Function table of CG/TG-bit setting in TGCR:

TON/TOFF	CG	TG	Generator Output
X	0	0	No tone
X	0	1	Ringing sequence F1, F2, F3 without break
TOFF	1	X	Break between two ringing sequences of F1, F2, F3
TON	1	X	Ringing sequence until next break

Description of the programmable parameters:

Parameter	# of CRAM Bytes	Range	Comment
TON	2	20 ms to 16 min	Period while the tone generator is turned on
TOFF	2	20 ms to 16 min	Period while the tone generator is turned off

2.2.4.3 Tone Generator

The tone generator contains a beat generator, a Square/Trapezoid generator, a second trapezoid generator and an automatic stop for two and three tone ringing signals. With the automatic stop function (SM-bit setting in TGCR) the multitone generation can be stopped after a defined frequency. This avoids unpleasant sounds when stopping the tone generator.

If the control generator is activated (TGCR.CG = 1) the bit setting of TG is insignificant. Otherwise (TGCR.CG = 0) the TG-bit setting controls the activities of the tone generator.

A functional diagram of the tone generator is shown in **figure 21**.

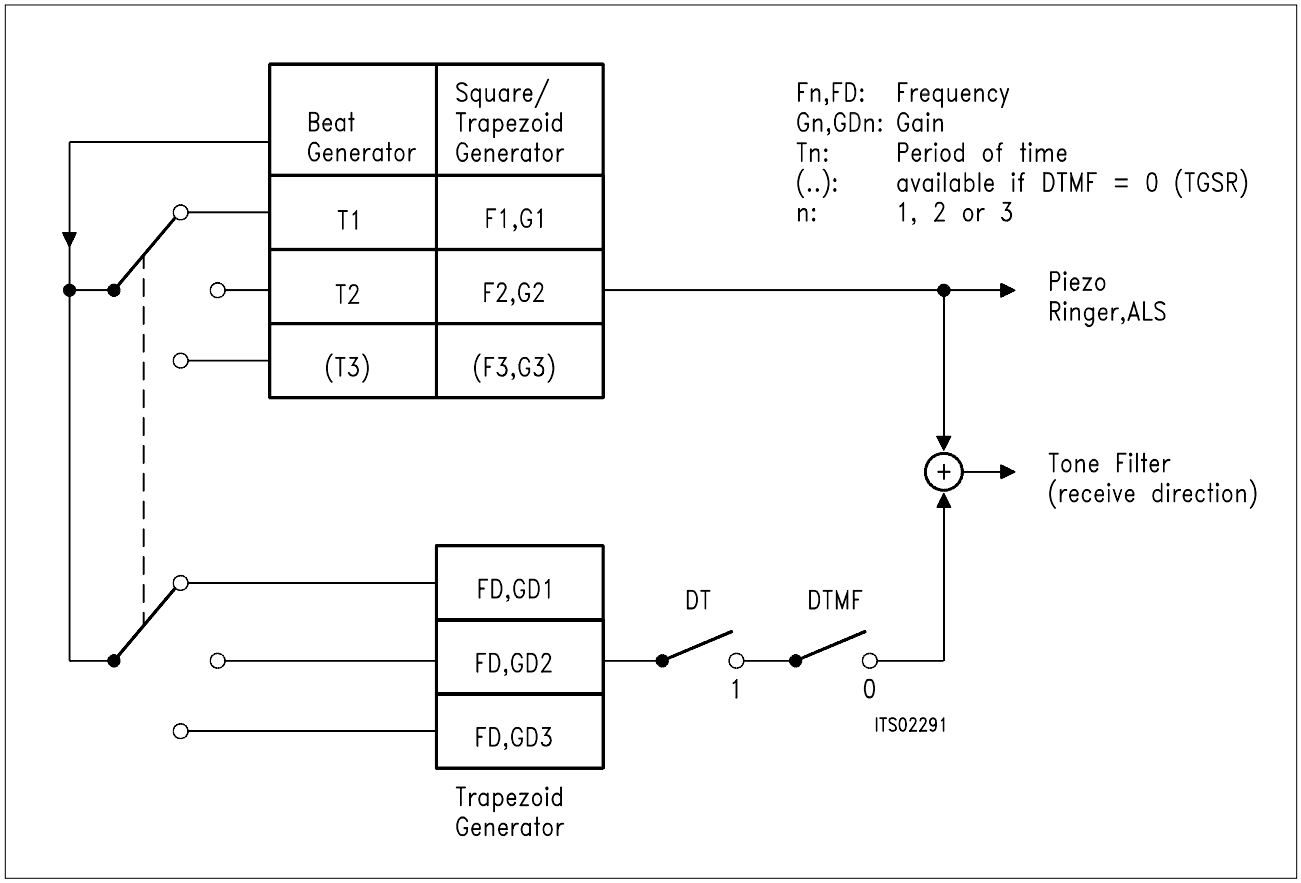


Figure 21
Functional Diagram of the Tone Generator

Distinctive alerting signals, allowing for example the use of different multitone ringing patterns, are all programmable using the beat tone generator in conjunction with the square/trapezoid generator. In the case of two or three tone ringing signals, the square/ trapezoid generator controls the output frequency pitch whilst the beat generator controls the repetition rate. Either square or trapezoid shaped tones can be generated depending on the TGCR.SQTR bit setting. If the piezo mode (PM or TRL in TGSR) is chosen, only a square-wave is available (fixed amplitude of V_{DD}). In this case the SQTR bit in TGCR has no effect.

A secondary trapezoid generator is also built into the ARCOFI. Depending on the DT-bit setting in the TGCR, the output signal of this generator is added to the output signal of the Square/Trapezoid (S/T) generator. In conjunction with the S/T generator, a wide variety of different dual tone signals can be programmed.

If the beat generator (TGCR.BT = 1) is enabled, the automatic stop function (SM-bit setting in TGCR) can be activated. This prevents an uncontrolled turn-off of the tone generator. Only when the generation of the frequency F2 or F3 (depending on the BM-bit setting in TGCR) has been completed, the tone generator will switch off.

Beat generator programming:

BT	BM	DT	Generator Output	
0	0	0	Continuous signal	F1, G1
0	0	1	Continuous signal	F1, G1 + FD, GD1
0	1	0	Continuous signal	F2, G2
0	1	1	Continuous signal	F2, G2 + FD, GD2
1	0	0	Alternating signal	F1, G1, T1; F2, G2, T2
1	0	1	Alternating signal	F1, G1, T1; F2, G2, T2 + FD, GD1, T1; FD, GD2, T2
1	1	0	Alternating signal	F1, G1, T1; F2, G2, T2; F3, G3, T3
1	1	1	Alternating signal	F1, G1, T1; F2, G2, T2; F3, G3, T3 + FD, GD1, T1; FD, GD2, T2; FD, GD3, T3

Description of the programmable parameters:

Parameter	# of CRAM Bytes	Range	Comment
Fn	2/2/2	50 Hz to 4 kHz	Trapezoid shaped tone
		16 kHz/m; (m ≥ 3)	Square-wave signal
Gn	1/1/1	0 dB to – 48 dB	Gain adjustment for square/trapezoid generator
Tn	2/2/2	10 ms to 8 s	Period of time for two or three tone sequences
FD	2	50 Hz to 4 kHz	Trapezoid shaped tone
GDn	1/1/1	0 dB to – 48 dB	Gain adjustment for trapezoid generator

n is either 1, 2 or 3

Note: 0-dB gain setting of G1, G2 or G3 and GD1, GD2 or GD3 corresponds to the maximum PCM-level (A-Law: + 3.14 dB)

2.2.4.4 Tone Filter

The tone filter contains a programmable equalizer and a saturation amplifier (**see figure 19**). If no filter function is necessary, a by-pass mode can be used (TGCR.ETF = 0). A brief description of the tone filter follows below.

The equalizer is realized as a band-pass filter. The filter parameters (center frequency, bandwidth, and attenuation of the stop-band) are programmable.

A generated square-wave or trapezoid signal can be converted by the equalizer into a sine-wave signal. A maximum attenuation of the first harmonic frequency of 50 dB is possible.

By programming the equalizer as a broadband filter, the quality of the DTMF-signal (receive direction) is improved. A level balancing of the two frequency components can be made with G1, G2, G3 and GD1, GD2, GD3.

The two main purposes of the programmable saturation amplification are:

- Level balancing of the filtered signal (avoidance of overload effects).
- Amplification up to + 12 dB followed by a saturation of the incoming signal. This saturation amplification converts a sine-wave signal into a square-wave or a trapezoid signal where their edges are eliminated. This method produces pleasant ringing tones.

Description of the programmable parameters:

Parameter	# of CRAM Bytes	Range	Comment
A1	1	200 Hz to 4 kHz	Center frequency
A2	1	0 to – 1	Bandwidth (strongly dependent on A1 and K)
K	1	0 to 54 dB	Attenuation of the stop-band
GE	1	+ 12 to – 12 dB	Saturation amplification

2.2.4.5 Tone Level Adjustment

The two level adjustment stages GTR and GTX determines the output levels of the tone generation (**see figure 19**).

Description of the programmable parameters:

Parameter	# of CRAM Bytes	Range	Comment
GTX	1	0 dB to – 50 dB (also – ∞ dB)	Level adjustment for the output which is connected to the transmit channel
GTR	1	0 dB to – 50 dB (also – ∞ dB)	Level adjustment for the output which is connected to the receive channel

2.2.4.6 DTMF-Generator (transmit)

The DTMF-generator contains two independent trapezoid generators which can be programmed in a wide frequency and gain range. If the DTMF-generator is active (TGSR.DTMF = 1), the output signal is automatically switched to the transmit direction. In this case the attenuation of the unwanted frequency components is executed by a special DTMF-low-pass filter to the following limits:

Frequency Band	Min. Attenuation
0 – 300 Hz	33 dB
300 – 3400 Hz	20 dB
3400 – 4000 Hz	33 dB

The pre-emphasis of 2 dB between the high and the low DTMF-frequency groups has to be set with the independent gain stages for the two trapezoid generators (G3 and GD3). All generated DTMF-frequencies are guaranteed within a ± 1 % deviation.

DTMF-frequency (F3, FD) programming:

CCITT Q.23	ARCOFI® Nominal	Relative Deviation from CCITT	Coefficients	
			high	low
Low Group				
697	697.1	+ 143 ppm	4F	16
770	770.3	+ 390 ppm	A6	18
852	852.2	+ 235 ppm	45	1B
941	941.4	+ 425 ppm	20	1E
High Group				
1209	1209.5	+ 414 ppm	B4	26
1336	1336.9	+ 674 ppm	C8	2A
1477	1477.7	+ 474 ppm	49	2F
1633	1632.8	– 122 ppm	40	34

Note: The deviations due to the inaccuracy of the incoming clock DCL/MCLK, when added to the nominal deviations tabulated above give the total absolute deviation from the CCITT-recommended frequencies.

Description of the programmable parameters:

Parameter	# of CRAM Bytes	Range	Comment
F3	2	50 Hz to 4 kHz	Trapezoid shaped tone 1
G3	1	0 dB to – 48 dB	Gain adjustment for trapezoid generator 1
FD	2	50 Hz to 4 kHz	Trapezoid shaped tone 2
GD3	1	0 dB to – 48 dB	Gain adjustment for trapezoid generator 2

2.2.5 ARCOFI® Speakerphone Support

The speakerphone option of the ARCOFI-SP PSB 2163 performs all voice switching functions without any external components, just by software. All these operational functions realized by the signal processor are completely parameterized. This technique offers a high level of flexibility and reproducibility.

There are three modes of operation: “speech mode”, “listen mode”, and “idle mode”. In the speech mode the receive path is attenuated while in listen mode the attenuation is switched to the transmit path. In the idle mode the attenuation is halved between transmit and receive paths. The switching is mainly controlled by the speech comparators while speech activity is recognized by the speech detectors.

As the signal flow graph of the speakerphone option shows (**figure 22**), the complete operational algorithm is situated between the Analog Front End/Signal Processing and the compression/expansion logic. This has the advantage that the speakerphone function is independent of any country specific transmission characteristics. Thus telephone sets can be optimized and adjusted to the particular geometrical and acoustic environment.

The main features of the speakerphone signal processing are:

- Two separate attenuation stages activated by voice, one for the transmit and one for the receive path. They are controlled by the current and past speech activities.
- Immediate mode switching mainly controlled by two comparators, one at the acoustic side and one at the line side.
- Speech detection by special speech detectors in the respective transmit and receive directions. Different time constants are separately programmable for signal and noise.
- Background noise monitoring to eliminate continuous background noise from speech control. All time constants are user programmable.

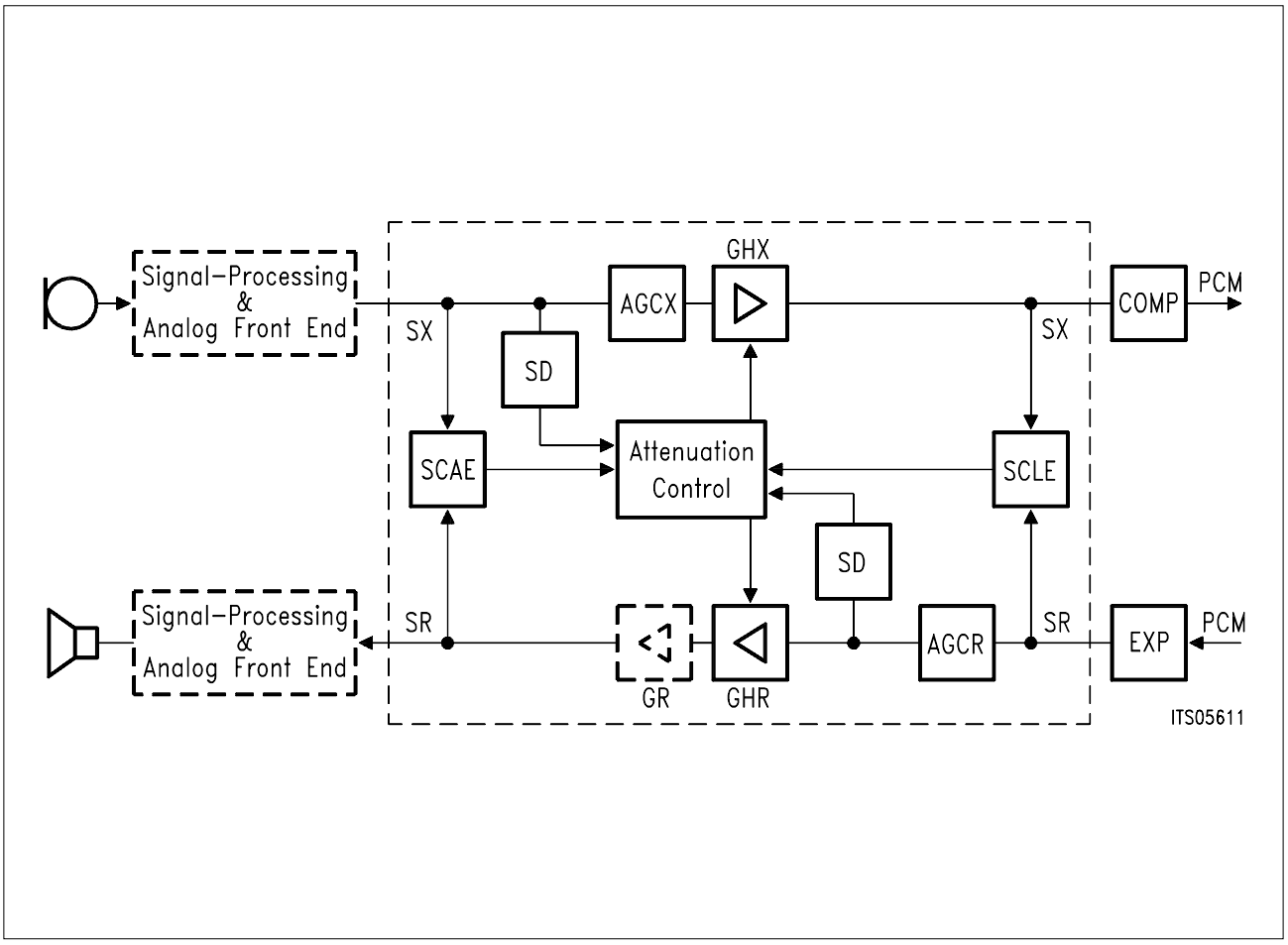


Figure 22
Speakerphone Signal Flow Graph of the ARCOFI®

2.2.5.1 Speech Detector

The speech detectors (**figure 23**) contained in both transmit and receive directions consist of two main blocks:

- Background Noise Monitor (BNM) and
- Signal Processing

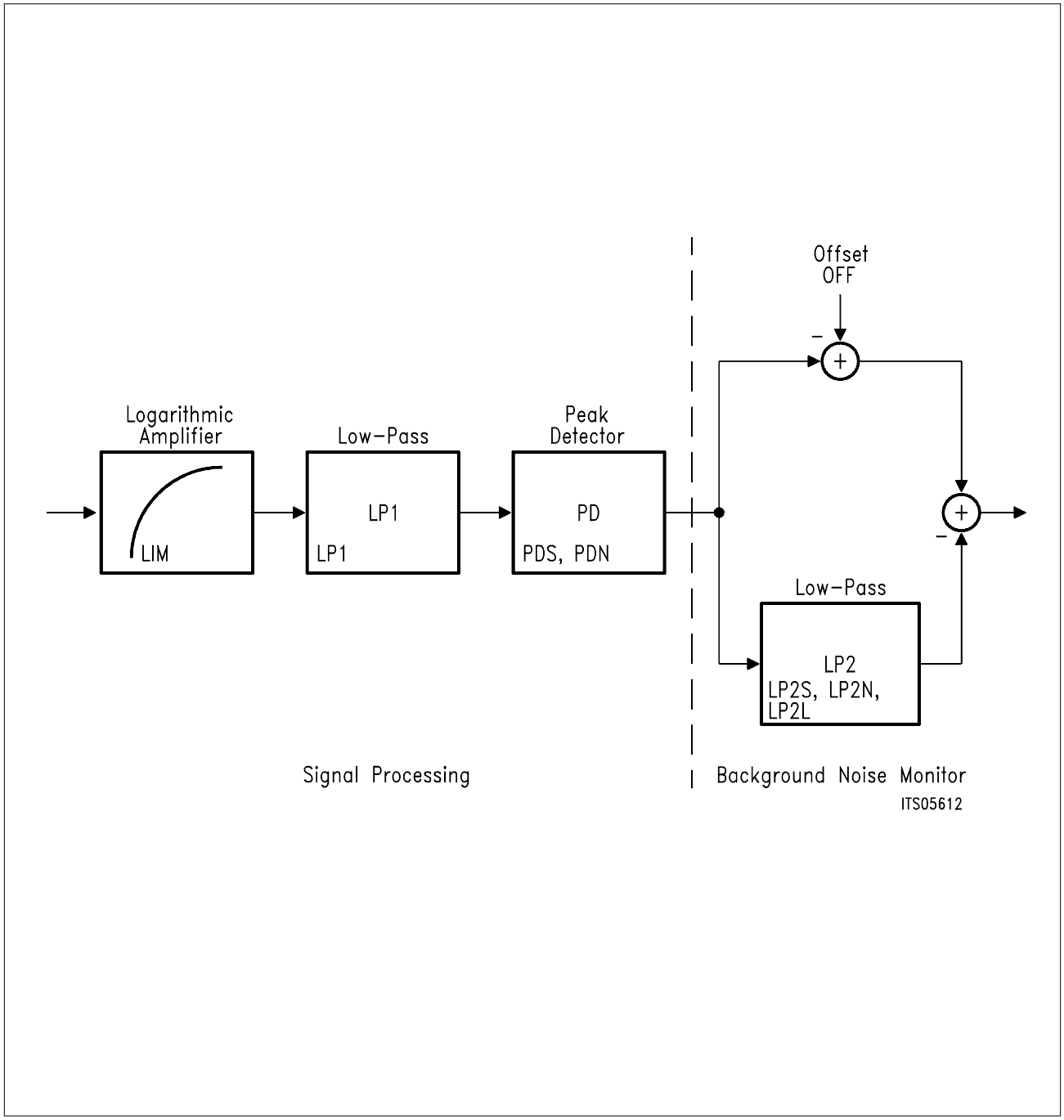


Figure 23
Speech Detector Signal Flow Graph

Background Noise Monitor

The tasks of the noise monitor are to differentiate voice signals from background noise, even if it exceeds the voice level, and to recognize voice signals without any delay. Therefore the Background Noise Monitor consists of the Low-Pass Filter 2 (LP2) and the offset in two separate branches. Basically it works on the burst-characteristic of the speech: voice signals consist of short peaks with high power (bursts). In contrast, background noise can be regarded approximately stationary from its average power.

Low-Pass Filter 2 provides different time constants for noise (non-detected speech) and speech. It determines the average of the noise reference level. In case of background noise the level at the output of LP2 is approximately the level of the input. Due to the offset OFF the comparator remains in the initial state. In case of speech at the comparator input the difference between the signal levels of the offset branch and of the LP2-branch increases and the comparator changes state. At speech bursts the digital signals arriving at the comparator via the offset branch change faster than those via the LP2-branch so that the comparator changes its polarity. Hence two logical levels are generated: one for speech and one for noise.

A small fade constant (LP2N) enables fast settling down the LP2 to the average noise level after the end of speech recognition. However, a too small time constant for LP2N can cause rapid charging to such a high level that after recognizing speech the danger of an unwanted switching back to noise exists. It is recommended to choose a large rising constant (LP2S) so that speech itself charges the LP2 very slowly. Generally, it is not recommended to choose an infinite LP2S because then approaching the noise level is disabled. During continuous speech or tones the LP2 will be charged until the limitation LP2L is reached. Then the value of LP2 is frozen until a break discharges the LP2. This limitation LP2L of this charging especially on the RX-path permits transmission of continuous tones and “music on hold”.

The offset stage represents the exact level threshold in [dB] between the speech signal and averaged noise.

Signal Processing

As described in the preceding chapter, the Background Noise Monitor is able to discriminate between speech and noise. In very short speech pauses e.g. between two words, however, it changes immediately to non-speech, which is equal to noise. Therefore a peak detection is required in front of the Noise Monitor.

The main task of the Peak Detector is to bridge the very short speech pauses during a monolog so that this time constant has to be long. Furthermore, the speech bursts are stored so that a sure speech detection is guaranteed. But if no speech is recognized the noise low-pass LP2 must be charged rapidly to the average noise level. Additionally the noise edges are to be smoothed. Therefore two time constants are necessary and are

separately programmable: PDS for speech and PDN for space (background noise) signals.

The Peak Detector is very sensitive to spikes. The LP1 filters the incoming signal containing noise in a way that main spikes are eliminated. Due to the programmable time constant it is possible to refuse high-energy sibilants and noise edges.

To compress the speech signals in their amplitudes and to ease the detection of speech, the signals have to be companded logarithmically. Hereby, the speech detector should not be influenced by the system noise which is always present but should discriminate between speech and background noise. The limitation of the logarithmic amplifier can be programmed via the parameter LIM, where the upper half-byte features LIMX and the lower half-byte LIMR. LIM is related to the maximum PCM level. A signal exceeding the limitation defined by LIM is getting amplified logarithmically, while very smooth system noise below is neglected. It should be the level of the minimum system noise which is always existing; in the transmit path the noise generated by the telephone circuitry itself and in receive direction the level of the first bit which is stable without any speech signal at the receive path.

Description of the programmable speech detector parameters:

Parameter	# of CRAM Bytes	Range	Comment
LP1	1	1 to 512 ms	Time constant LP1
OFF	1	0 to 50 dB	Level offset up to detected noise
PDS	1	1 to 512 ms	Time constant PD (signal)
PDN	1	1 to 512 ms	Time constant PD (noise)
LP2S	1	4 to 2000 s	Time constant LP2 (signal)
LP2N	1	1 to 512 ms	Time constant LP2 (noise)
LP2L	1	0 to 95 dB	Limitation of LP2, related to LIM
LIMX, LIMR	1	– 36 to – 78 dB	Limitation of logarithmic amplifier

2.2.5.2 Speech Comparators (SC)

Switching from one active mode to another one is mainly controlled by the speech comparators. There are two Speech Comparators, one at the acoustic (AE) and one at the line side (LE). This offers a different programming of the sensitivity of the speech detectors and avoids clipping due to echoes. These comparators continuously compare the signal levels of both signal paths and control the effect of the echos at the acoustic side and the line side. Once speech activity has been detected, the comparator switches at once in that direction in which the speech signal is stronger. For this purpose each signal is compared to the sum of the other and the returned echo.

Speech Comparator at the Acoustic Side (SCAE)

In principle, the SCAE works according to the following equation:

if SX > SR + VAE then TX
else RX

Being in RX-mode, the speech comparator at the acoustic side controls the switching to TX-mode. Only if the SX-signal is higher than the SR-signal plus the expected/measured acoustic level enhancement (VAE), the comparator switches immediately to TX-mode. Physically the level enhancement (VAE) is divided into two parts: GAE and GDAE.

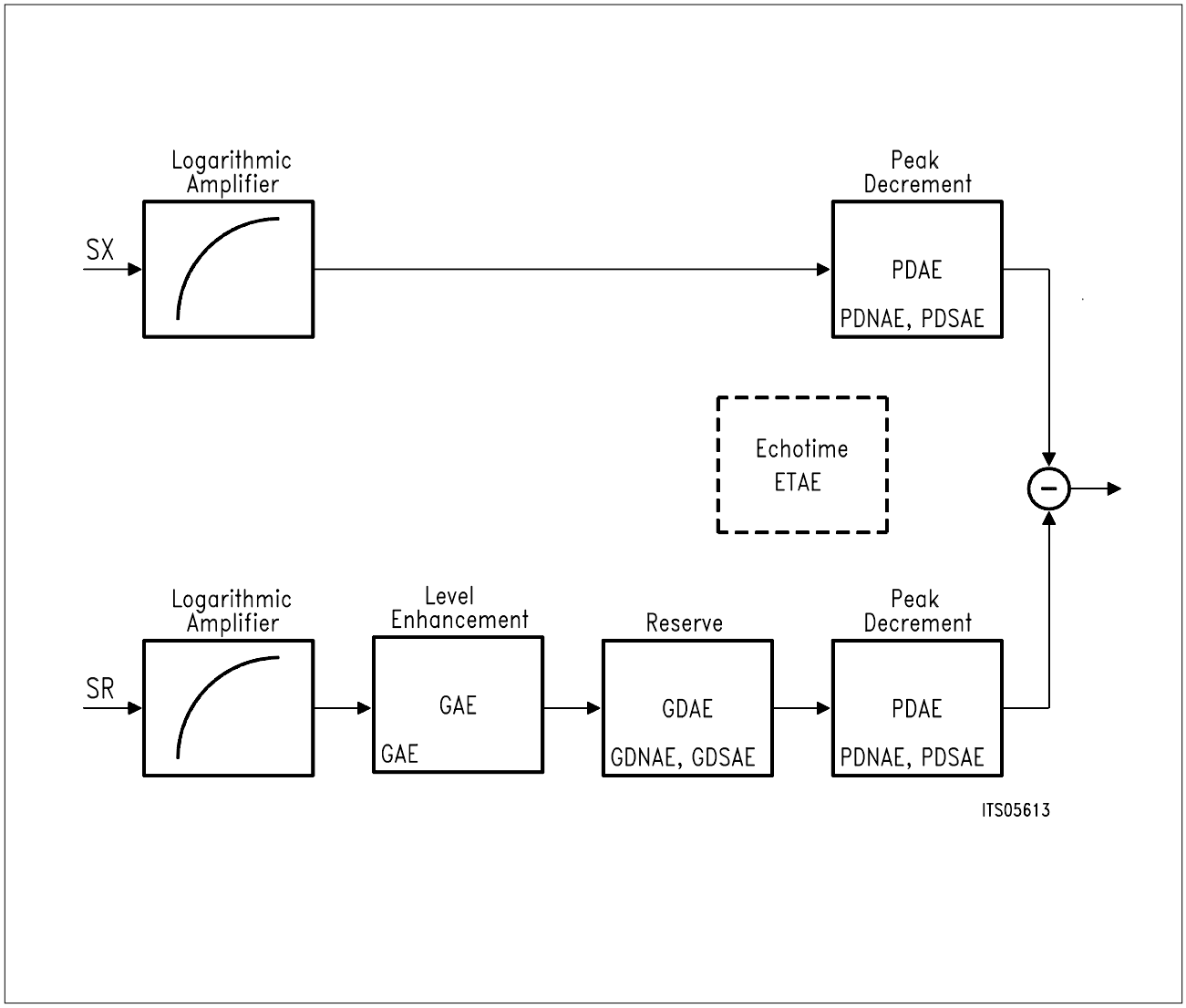


Figure 24
Speech Comparator at the Acoustic Side

At the SCAE-input, logarithmic amplifiers compress the signal range. Hence after the required signal processing for controlling the acoustic echo, pure logarithmic levels on both paths are compared.

Principally, the main task of the comparator is to control the echo. The internal coupling due to the direct sound and mechanical resonances are covered by GAE. The external coupling, mainly caused by the acoustic feedback, is controlled by GDAE/PDAE.

The Gain of the Acoustic Echo (GAE) corresponds to the terminal couplings of the complete telephone: GAE is the measured or calculated level enhancement between both receive and transmit inputs of the SCAE (**refer to figure 22**). It equals the sum of the amplification of ALS plus the gain due to the loudspeaker/microphone coupling plus the TX-amplification of AMI and GX. To succeed in a sure differentiation between original speech and echo, it must be guaranteed that the TX-signal does not run into saturation due to the loudspeaker/microphone coupling. Therefore, it is recommended to reduce the TX-gain by 10 dB in front of the SCAE at least in the loudest loudspeaker volume step. To fulfill the sending loudness rating, this gain is realized by the LGAX/ AGCX which follows the SCAE. Of course, the GAE has to be reduced by the same amount.

To control the acoustic feedback two parameters are necessary: GDAE-features the actual reserve on the measured GAE. Together with the Peak Decrement (PDAE) it simulates the echo behaviour at the acoustic side: After RX-speech has ended there is a short time during which hard couplings through the mechanics and resonances and the direct echo are present. Till the end of that time (Δt) the level enhancement VAE must be at least equal to GAE to prevent clipping caused by these internal couplings. Then, only the acoustic feedback is present. This coupling, however, is reduced by air attenuation. For this in general the longer the delay, the smaller the echo being valid. This echo behaviour is featured by the decrement PDAE.

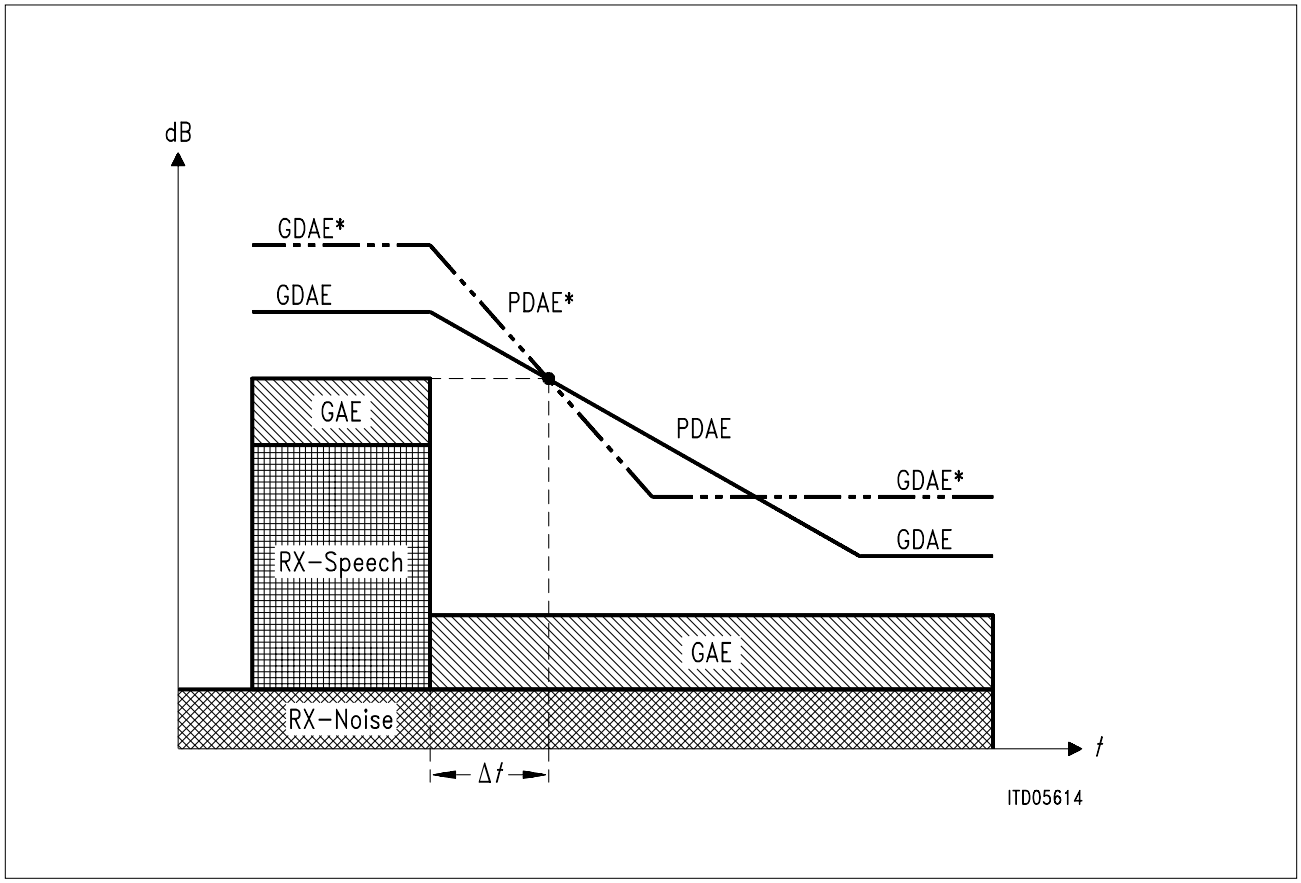


Figure 25
Interdependence of GDAE and PDAE

According to **figure 25**, a compromise between the reserve GDAE and the decrement PDAE has to be made: a smaller reserve (GDAE) above the level enhancement GAE requires a longer time to decrease (PDAE). It is easy to overshout the other side but the intercommunication is harder because after the end of the speech, the level of the estimated echo has to be exceeded. In contrary, with a higher reserve (GDAE*) it is harder to overshout continuous speech or tones, but it enables a faster intercommunication because of a stronger decrement (PDAE*).

Two pairs of coefficients, GDSAE/PDSAE when speech is detected, and GDNAE/ PDNAE in case of noise, offer a different echo handling for speech and non-speech.

With speech, even if very strong resonances are present, the performance will not be worsened by the high GDSAE needed. Only when speech is detected, a high reserve prevents clipping. A time period ETAE [ms] after speech end, the parameters of the comparator are switched to the “noise” values. If both sets of the parameters are equal, ETAE has no function.

Description of the programmable parameters:

Parameter	# of CRAM Bytes	Range	Comment
GAE	1	– 48 to + 48 dB	Gain of Acoustic Echo
GDSAE	1	0 to 48 dB	Reserve when speech is detected
PDSAE	1	0.16 to 42 ms/dB	Peak Decrement when speech is detected
GDNAE	1	0 to 48 dB	Reserve when noise is detected
PDNAE	1	0.16 to 42 ms/dB	Peak Decrement when noise is detected
ETAE	1	0 to 1020 ms	Echo time

Speech Comparator at the Line Side (SCLE)

Principally, the SCLE works similarly to the SCAE. The formula of SCLE is the following:

if SR > SX + VLE then RX
else TX

Being in TX-mode, the speech comparator at the line side controls the switching to RX-mode. When the SR-signal is higher than the SX-signal plus the expected/measured echo return loss (VLE) and if SDR has detected speech, the comparator switches immediately to RX-mode.

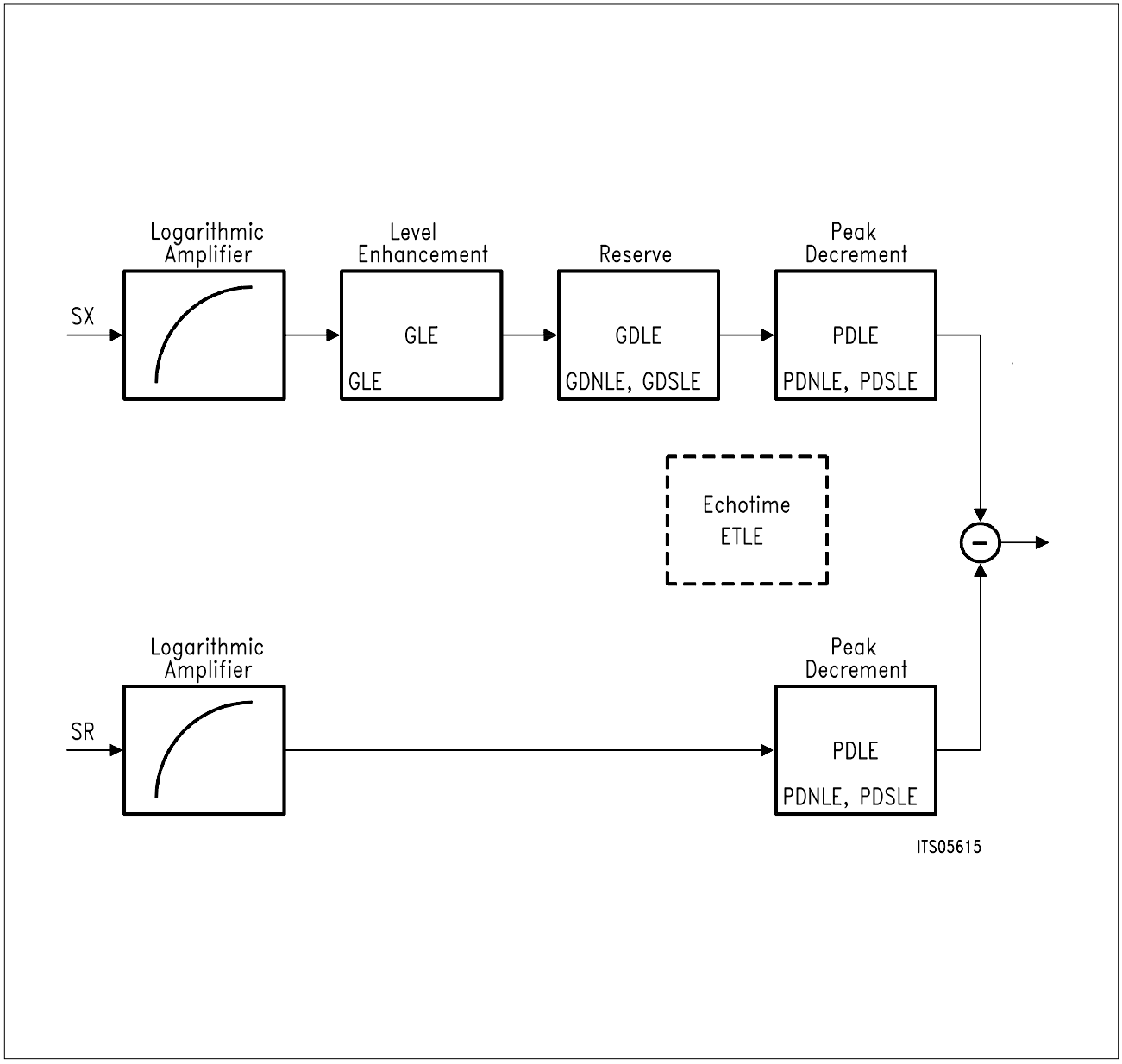


Figure 26
Speech Comparator at the Line Side

The Gain of the Line Echo (GLE) directly corresponds to the echo return loss of the link. Generally, it is specified to 27 dB. However, the worst case loss can be estimated to 10 dB. This means, the echo returns at least attenuated by 10 dB. The coefficient GLE should be programmed with an extra reserve of 2 dB so that very smooth noise is processed correctly.

Similarly to the acoustic side, GDLE at the line side features the reserve above GLE which is necessary to control the echo via the decrement PDLE. GDLE and PDLE are interdependent. Exactly Δt [ms] after the end of RX-speech the level enhancement VLE must be at least GLE to prevent clipping.

Two pairs of coefficients are available: GDSLE/PDSLE while speech is detected and GDNLE/PDNLE in case of noise. This offers the possibility to control separately the far-end echo during speech and the near-end echo while noise is detected. However, this requires an attenuation between the speech detectors SDX and SDR: If the SDX does not recognize any speech, the SDR must not detect speech due to the far-end echo. Note, that LIMX and LIMR are also influencing the sensitivity of the speech detection. ETLE [ms] after the final speech detection the parameter sets are switched. If both sets are equal, ETLE has no meaning.

Description of the programmable parameters:

Parameter	# of CRAM Bytes	Range	Comment
GLE	1	– 48 to + 48 dB	Gain of Line Echo
GDSLE	1	0 to 48 dB	Reserve when speech is detected
PDSLE	1	0.16 to 42 ms/dB	Peak Decrement when speech is detected
GDNLE	1	0 to 48 dB	Reserve when noise is detected
PDNLE	1	0.16 to 42 ms/dB	Peak Decrement when noise is detected
ETLE	1	0 to 1020 ms	Echo time

2.2.5.3 Attenuation Control Unit

The Attenuation Control unit controls the attenuation stages GHX of the transmit and GHR of the receive directions respectively. The programmable loss is switched either completely to a single path or, in the “IDLE” mode, is halved to each direction.

In addition, attenuation is also influenced by the Automatic Gain Control stages (AGCX and AGCR): For the total loop gain never to exceed 1, the sweep range (of ATT) is automatically enlarged with high-gain amplification of the AGCs while it will be accordingly reduced with low-gain.

Changing from one speakerphone mode into another one depends on the determinations of one comparator plus the corresponding speech detector. Hence attenuation is influenced by the current and past speech activities. Also rate of change varies: changing from “speech mode” or “listen mode” to “idle mode” is programmable by the rate factor DS. Direct changes from “speech mode” to “listen mode” or vice-versa and changes from “idle mode” to “speech mode” or “listen mode” can be programmed via the factor SW in a large range.

Description of the programmable parameters:

Parameter	# of CRAM Bytes	Range	Comment
TW	1	16 ms to 4 s	Wait time
ATT	1	0 dB to 95 dB	Attenuation programmed in GHR or GHX if speech activity for the other side was detected
DS	1	0.6 to 680 ms/dB	Decay Speed (Decay Time TD = DS × ATT/2)
SW	1	0.0052 to 10 ms/dB	Switching time (dependent on ATT)

2.2.5.4 Speakerphone Test Function

The ARCOFI offers a test mode to ease the optimization of the switching behaviour (TFCR.EPZST = 1). This function can also be used for signalling e.g. the speech mode during a normal telephone conversation. This mode uses the piezo pins PZ1 and PZ2.

The PZ1 pin forced to a high level indicates that neither of the speech detectors recognizes speech (refer to TW, DS, and idle state); when any speech activity is detected, this pin is at a low level. At the PZ2 pin a logical “1” indicates the speech mode (TX-mode) while a “0” signals listen mode (RX mode).

2.2.5.5 Automatic Gain Control of the Transmit Direction (AGCX)

An AGCX is inserted into the transmit path (**figure 27**) to reach nearly constant loudness ratings independent of the varying distance between the speaker and the microphone. Regulation range is between 0 dB and + 12 dB which must be enabled by setting TGSR.PM1 = 1 (Piezo-Mode).

Operation of the AGCX depends on a threshold level. Its value (via parameter COMX) corresponds to a signal level relative to the maximum PCM-value at which the microphone signal is to become amplified. Regulation follows two time constants: TMHX, which limits the signal amplitude, is shorter because the signal has to be reduced before it goes into saturation. TMLX, which amplifies the signal if it falls below the reference level, is greater because this threshold effect should hardly be perceptible.

For reasons of physiological acceptance the AGCX is automatically reduced in case of continuous background noise e.g. by ventilators. The reduction is programmed via the NOlSX-parameter. When the noise level increases the threshold determined by NOISX, the amplification AGX will be reduced by the same amount the noise level is above the threshold.

A programmable Loudness Gain Adjustment stage (LGAX) offers the possibility to amplify the TX-signal after the speech comparator SCAE and the speech detector SDX. If a lower signal range in front of the SDX is necessary to determine between speech and echo a part of the TX-amplification can be transferred to the LGAX. It is enabled together with the bit GCR.SP. Even if the AGCX is disabled in speakerphone mode the LGAX remains enabled.

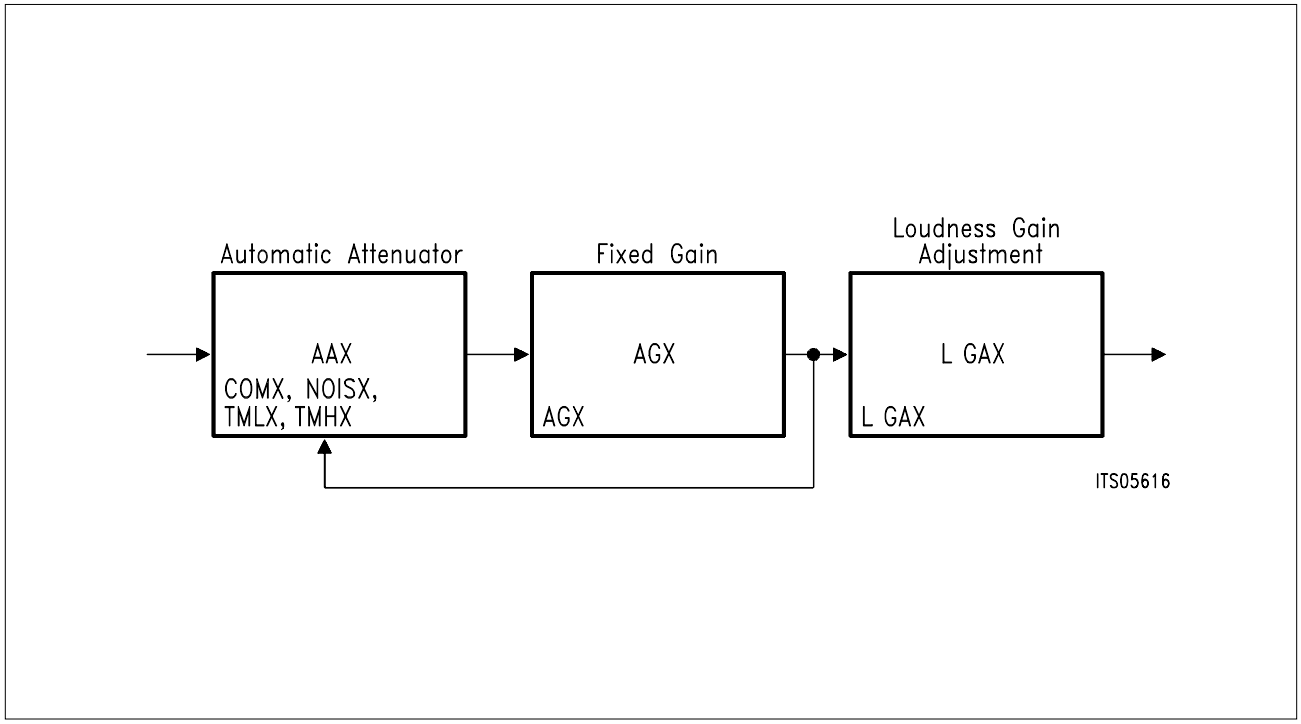


Figure 27
Function of the Transmit AGC

Description of the programmable parameters:

Parameter	# of CRAM Bytes	Range	Comment
LGAX	1	– 12 to 12 dB	Loudness Gain Adjustment
COMX	1	0 to – 73 dB	Compare level rel. to max. PCM-value
AGX	1	0 to 18 dB	Gain range of Automatic control
TMLX	1	1 to 2700 ms/dB	Settling time constant for lower levels
TMHX	1	1 to 340 ms/dB	Settling time constant for higher levels
NOISX	1	0 to – 95 dB	Threshold for AGC-reduction by background noise

2.2.5.6 Automatic Gain Control of the Receive Direction (AGCR)

The Automatic Gain Control of the receive direction AGCR (**figure 28**) is similar to the transmit AGC. One additional parameter (AAR) offers an automatic amplification. The maximum attenuation is selectable with AAR. Depending on the parameters AAR and AGR three different behaviours of the AGCR are possible:

- AGR = 0: the only task of the AGCR is to prevent clipping. If the RX-signal exceeds the compare level, the AGCR starts to attenuate it.
- AGR = AAR: the AGCR works as an automatic amplifier. The RX-signal will be amplified if it is smaller than the compare level.
- $|AAR| > AGR$: the combination of the previous tasks: If the signal is smaller than the compare level it will be amplified while if it exceeds the level it will be attenuated. The AGCR functions like a dynamic compressor. While the digital RX-signal level varies, the volume coming out of the loudspeaker remains constant.

If the AGCR is disabled in speakerphone mode, the Loudness Gain Adjustment stage (LGAR) offers a programmable amplification in front of the SDR. It is enabled together with the bit GCR.SP. It is highly recommended to program reasonable amplifications in the digital gain stages. Otherwise the ASP will run into saturation above the 3.14 dB PCM-value.

Note that the speech detector for the receive direction is supplied with the signal that comes out of the AGR-block.

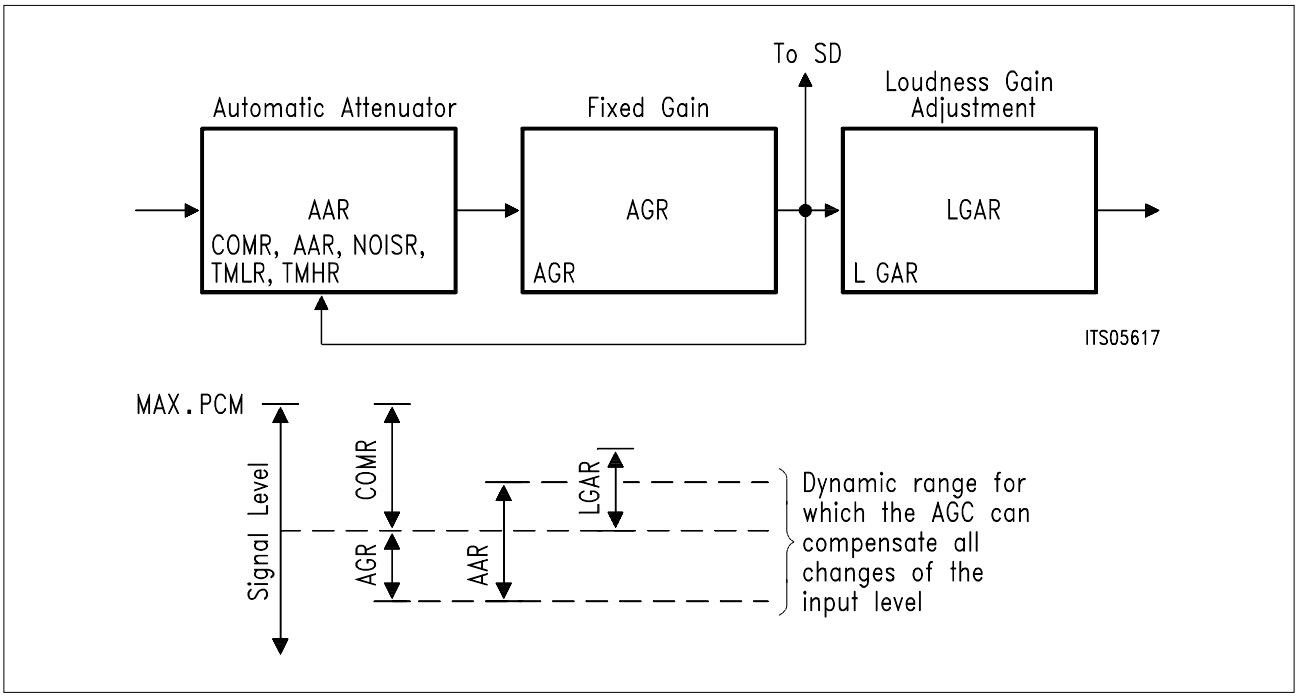


Figure 28
Function of the Receive AGC

Description of the programmable parameters:

Parameter	# of CRAM Bytes	Range	Comment
LGAR	1	– 12 to 12 dB	Loudspeaker Gain Adjustment
COM	1	0 to – 73 dB	Compare level rel. to max. PCM-value
AAR	1	0 to – 47 dB	Attenuation range of Automatic control
AGR	1	0 to 18 dB	Gain range of Automatic control
TMLR	1	1 to 2700 ms/dB	Settling time constant for lower levels
TMHR	1	1 to 340 ms/dB	Settling time constant for higher levels
NOISR	1	0 to – 95 dB	Threshold for AGC-reduction by background noise

2.2.5.7 Loudhearing

The ARCOFI-SP offers the possibility to do a so called “controlled monitoring” when the bit ARCR.CME is set. This mode can only be used together with the speakerphone mode (GCR.SP) With CME = 1 the attenuation stage GHR is fixed to a value of 0 dB but the attenuation takes place in the analog loudspeaker amplifier ALS in a way that the amplification of the ALS is set to – 9.5 dB as soon as the attenuation control unit switches to transmit mode. Therefore in transmit direction the same behaviour as in speakerphone mode occurs but in the receive direction the handset output offers a signal as in normal handset mode while the volume at the loudspeaker output will be reduced to a low level during transmit mode. If the programming for the loudspeaker output (ARCR.LSC) is already chosen for values of less or equal – 9.5 dB, no further attenuation takes place.

2.2.6 Speakerphone Coefficient Set

This example shows a possible configuration for a speakerphone application. All described coefficients can be used as a basic programming set.

CMD Sequence	Coefficient	Code	Value
COP_A	GAE	$0C_H$	4.50 dB
COP_A	GLE	$E5_H$	– 10.02 dB
COP_A	ATT	40_H	24.00 dB
COP_A	ETAE	$0C_H$	48.00 ms
COP_A	ETLE	32_H	200.00 ms
COP_A	TW	09_H	144.00 ms
COP_A	DS	25_H	– 99 ms/dB
COP_A	SW	64_H	0.6 ms/dB
COP_B	GDSAE	20_H	6.02 dB
COP_B	PDSAE	06_H	7.1 ms/dB
COP_B	GDNAE	20_H	6.02 dB
COP_B	PDNAE	06_H	7.1 ms/dB
COP_B	GDSLE	40_H	12.00 dB
COP_B	PDSLE	02_H	21.3 ms/dB
COP_B	GDNLE	40_H	12.00 dB
COP_B	PDNLE	02_H	21.3 ms/dB
COP_C	LIMX, LIMR	22_H	– 48.16 dB, – 48.16 dB
COP_C	OFFX	$0C_H$	4.50 dB
COP_C	OFFR	$0C_H$	4.50 dB
COP_C	LP2LX	20_H	12 dB
COP_C	LP2LR	20_H	12 dB
COP_C	LP1X	$E1_H$	4.00 ms
COP_C	LP1R	$E1_H$	4.00 ms
COP_C	reserved 00_H		
COP_D	PDSX	26_H	102.34 ms
COP_D	PDNX	$F4_H$	32.00 ms
COP_D	LP2SX	20_H	6.55 s
COP_D	LP2NX	44_H	30.06 ms
COP_D	PDSR	26_H	102.34 ms
COP_D	PDNR	$F4_H$	32.00 ms
COP_D	LP2SR	20_H	6.55 s
COP_D	LP2NR	44_H	30.00 ms

Speakerphone Coefficient Set (cont'd)

CMD Sequence	Coefficient	Code	Value
COP_E	LGAX	01_H	9.60 dB
COP_E	COMX	$C3_H$	– 20.43 dB
COP_E	AGX	01_H	12.04 dB
COP_E	TMHX	$0A_H$	14.00 ms/dB
COP_E	TMLX	24_H	383.00 ms/dB
COP_E	NOISX	$4F_H$	– 66.23 dB
COP_E	reserved 00_H		
COP_E	reserved 00_H		
COP_F	LGAR	$F0_H$	6.04 dB
COP_F	COMR	$B2_H$	– 15.05 dB
COP_F	AAR	55_H	– 33.16 dB
COP_F	AGR	00_H	18.06 dB
COP_F	TMHR	$0A_H$	13.95 ms/dB
COP_F	TMLR	$2F_H$	500.84 ms/dB
COP_F	NOISR	$4F_H$	– 66.23 dB
COP_F	reserved 00_H		

2.3 ARCOFI® Digital Interface (ADI)

The ADI-function consists of two interface blocks:

- The Peripheral Control Interface (PCI) or the Serial Control Interface (SCI)
- The IOM-2 interface (TE- or non-TE-timing mode) or the Serial Data Interface (SDI)

Supplementary functions are accessed by strapping the pins MODE and AD according to the following table:

Pin MODE	Pin AD	Mode	Description
0	0	IOM-2 TE	IOM-2 TE-timing mode (AD = 0)
0	1	IOM-2 TE	IOM-2 TE-timing mode (AD = 1)
0	MCLK	Test	
1	0	IOM-2 non-TE	IOM-2 Non-TE-timing mode (AD = 0)
1	1	IOM-2 non-TE	IOM-2 Non-TE-timing mode (AD = 1)
1	MCLK	SDI	Serial Data Interface

A detailed description is in the following chapter.

2.3.1 PCI-Interface

The Peripheral Control Interface (PCI) provides 4 programmable I/O-pins to control the peripheral devices (for more detailed information see section 4, DFICR). These four interface pins are only available in the IOM-2 terminal mode (TE-mode).

Otherwise these pins are used as slot select pins in the IOM-2 non-TE-timing mode or used as a Serial Control Interface (SCI).

SA-SD	Mode
PCI	IOM-2 TE
Slot Select	IOM-2 Non TE
SCI	Serial Mode

2.3.2 IOM®-2 Frame Structure and Timing Modes

This interface consists of one data line per direction (DD: Data Downstream; DU: Data Upstream). Two additional signals define the data clock (DCL) and the frame synchronization (FSC).

In terminal applications, the IOM-2 constitutes a powerful backplane bus offering intercommunication and sophisticated control capabilities for peripheral modules (e.g. ARCOFI).

The channel structure of the IOM-2 is described in **figure 29**.

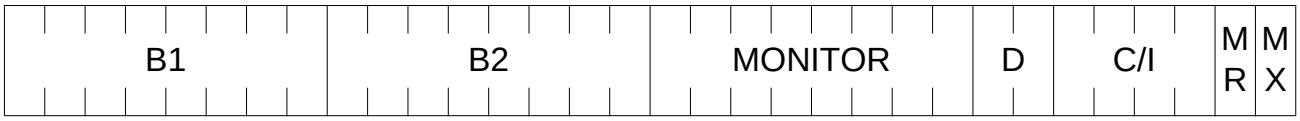


Figure 29
Channel Structure of IOM®-2

- The 64-kbit/s channels, B1 and B2, are conveyed in the first two bytes.
- The third byte (monitor channel) is used for programming and controlling devices attached to the IOM-2 interface.
- The fourth byte (control channel) contains two bits for the 16-kbit/s D-channel, four command/indication bits for controlling activation/deactivation and for additional control functions, two bits MR and MX for supporting the handling of the MONITOR channel.

In case of an IOM-2 interface the frame structure depends on whether TE- or non-TE-mode is selected.

Non-TE-Timing Mode

The frame of this mode is a multiplex of eight IOM-2 channels (**figure 30**), each channel has the structure as shown in **figure 29**.

The ARCOFI is assigned to one of eight channels (0 to 7) by strapping SB to SD according to the following table:

Pin SD	Pin SC	Pin SB	Selected IOM®-2 Channel
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

Pin SA is not used in this mode and should be connected to V_{DD} or V_{SSD}.

Thus the data rate per channel is 256 kbit/s, whereas the bit rate is 2.048 kbit/s. The IOM-2 interface signals are:

DD, DU : 2048 kbit/s
DCL : 4096 kHz (double clock rate)
FSC : 8 kHz

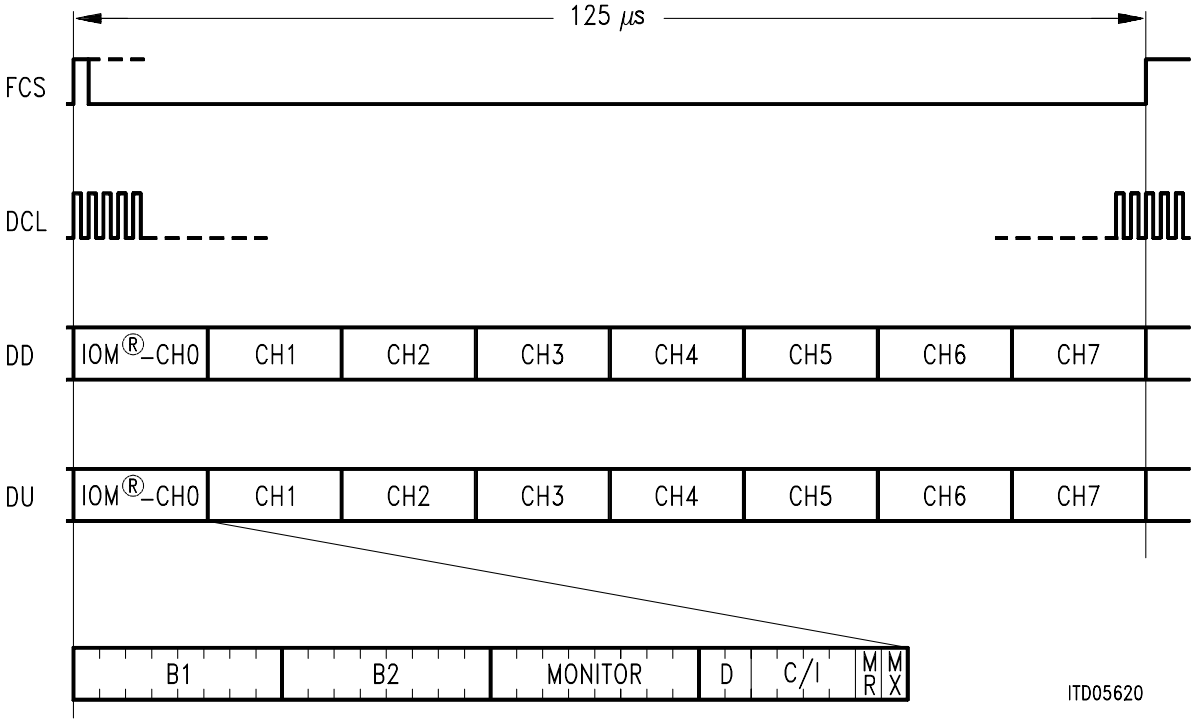


Figure 30
Multiplexed Frame Structure of the IOM®-2 Interface in Non-Terminal Timing Mode

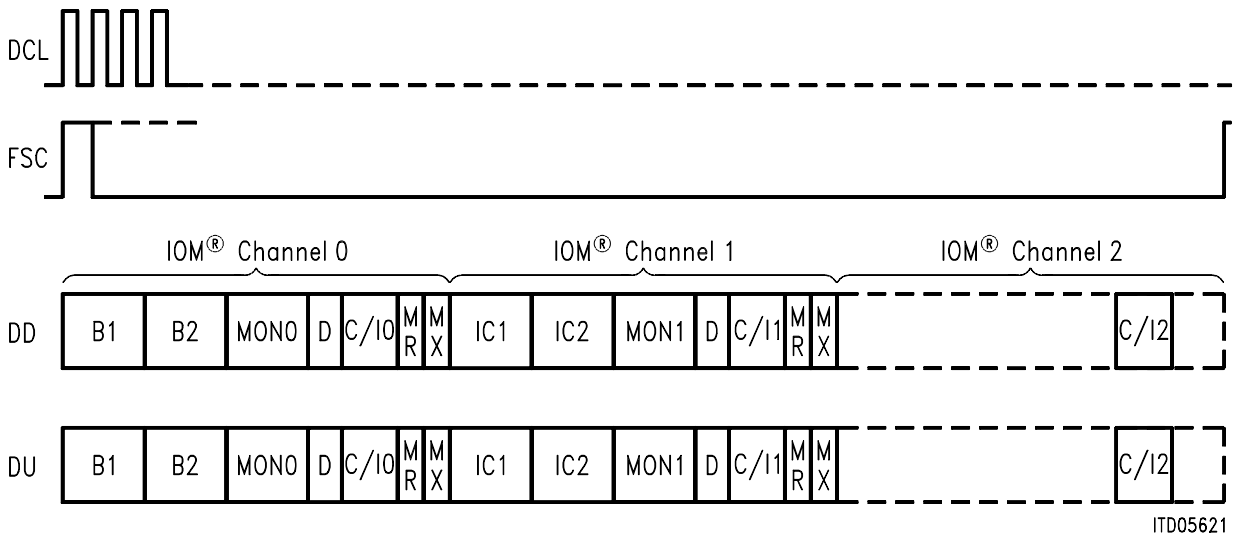
TE-Timing Mode

The IOM-2 frame provides three complete IOM channels (**figure 31**):

- Channel 0 contains 144 kbit/s (2B + D) plus monitor and command/indication channels for the layer-1 device.
- Channel 1 contains two 64-kbit/s intercommunication channels plus monitor and command/indication channels for other IOM-2 devices (e.g. ARCOFI).
- Channel 2 is used for D-channel arbitration.

The IOM-2 signals are:

DD, DU : 768 kbit/s
DCL : 1536 kHz (double clock rate)
FSC : 8 kHz



B1, B2 **Bearer voice data channel 1/2 to/from layer-1 device**
MON1 **Monitor channel 1**
C/I1 **Command/Indicate channel 1**
IC1, IC2 **Intercommunication channel 1/2**

Figure 31
IOM®-2 Interface Structure in Terminal Mode

2.3.3 Serial Control Interface

When the MODE pin is tied high and the AD/MCLK pin is used as system clock input (MCLK), the internal configuration registers and the coefficient RAM of the ARCOFI are programmable via the serial control interface. It consists of 4 lines: SCLK, SDR, SDX (open drain or push-pull) and $\overline{CS}$.

$\overline{CS}$ is used to start a serial access to the ARCOFI-registers and the coefficient RAM. Following a falling edge on $\overline{CS}$, the first eight bits transmitted on SDR specify the command. The subsequent one, two, four or eight bytes (depending on command) read(s) or write(s) the contents of the selected registers or RAM-locations until the $\overline{CS}$ line becomes inactive. If a read command is chosen, the first byte after the command is the identification code of the ARCOFI-SP PSB 2163 (**see also chapter 3.4.2.1**). After one command sequence is completed at least one NOP-command is required (**see figure 32**).

A transfer sequence can be broken by setting $\overline{CS}$ high. All bytes already sent when $\overline{CS}$ changes to high are valid.

The data transfer is synchronized by the SCLK input. SDX changes with the falling edge of SCLK while the contents of SDR is latched on the rising edge of SCLK.

Figure 32 shows the timing of a serial control interface transfer (one byte transfer).

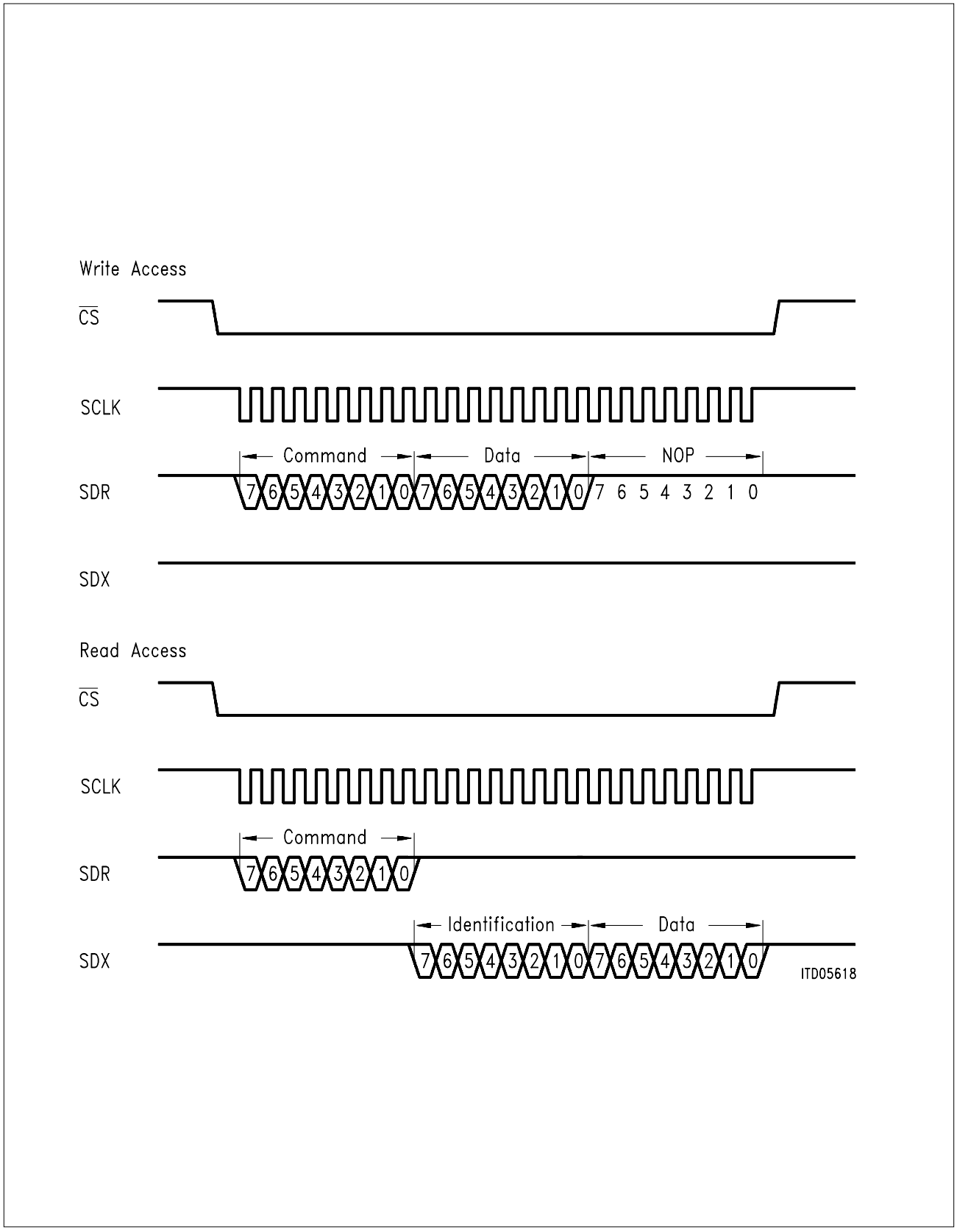


Figure 32
Serial Control Interface Timing

2.3.4 Serial Data Interface

If the serial control interface is selected, the ARCOFI supports an additional serial data interface for B-channel transfer. This control interface consists of five lines: FSC, DCLK, DX, DR and MCLK.

FSC is a 8-kHz frame synchronization signal.

The DCLK is the clock signal to synchronize the data transfer on both data lines DX and DR. The rising edge indicates the start of the bit while the falling edge is used to latch the contents of the received data line DR. If the double clock rate is chosen (twice of the transmission rate) the first rising edge indicates the start of a bit while the second falling edge is used to latch the content of the data line.

The data rate of the interface can vary from 64 kbit/s to 4.096 Mbit/s. A frame may consist of up to 64 time-slots of 8 bits each. The last 6 bits of TSCR (Time Slot Configuration Register) indicate the selected time-slot from 0 to 63. If a 16-bit mode (linear mode) is chosen, the lowest data rate is 128 kbit/s and the time-slot must be set to an even number.

The pin AD/MCLK is a system clock synchronized with FSC (necessary to synchronize internal PLL).

Figure 33 shows the timing of a serial data interface (256 kbit/s with single clock rate).

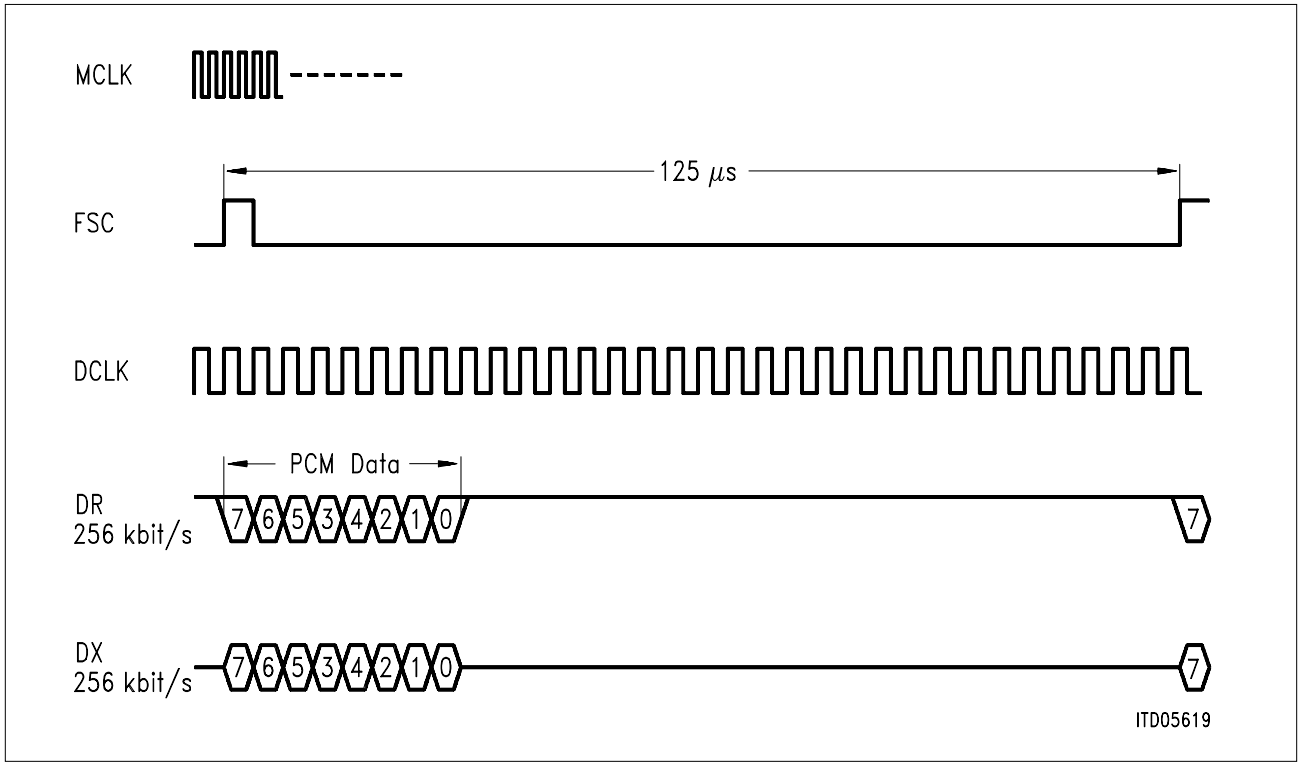


Figure 33
Serial Data Interface Timing

2.4 Test Functions

The ARCOFI provides several test and diagnostic functions which can be grouped as follows:

- All programmable configuration registers and coefficient RAM-locations are readable
- Digital loop via PCM-register (DLP)
- Digital loop via signal processor (DLS)
- Digital loop via noise shaper (DLN)
- Analog loop via analog front end (ALF)
- Analog loop via converter (ALC)
- Analog loop via noise shaper (ALN)
- Analog loop via Z-sidetone (ALZ); sidetone gain stage GZ must be enabled (PFCR.GZ = 1) and sidetone gain must be programmed with 0 dB; depending on the VDM-bit setting (DFICR) an addition to the incoming voice signal is possible
- Analog loop via digital interface (ALI).

3 Operational Description

3.1 Reset

After a RESET (internal power-on reset, hardware reset at pin RS or software reset via XOP_E) the pins SA to SD are programmed as inputs. All other output pins are in high-impedance state (HOP/HON, LSP/LSN, V_{REF}, PZ1, PZ2, DU/DX).

Note: After a Reset (only TE and Non-TE mode) the coefficient RAM-locations have defined reset values.

The defined reset values of the ARCOFI-registers are listed below:

Register	Value after RESET [hex]	Meaning
CMDR	BF	– No operation (NOP)
GCR	00	– Speakerphone disabled (incl. AGCX and AGCR) – Disable voice transmit – IOM-2 channel 0 selected (IOM-2 TE-mode) – Power-down mode – IOM-2 two chip mode (IOM-2 TE-mode) – A-Law
DFICR	F0	– SA to SD programmed as inputs – PCM-mode; receive voice blocked
PFCR	00	– Programmable digital gain disabled – Programmable sidetone gain disabled – Correction filters disabled – 50-Hz receive HP active – 50-Hz transmit HP active
TGCR	00	– Tone generator inactive – Control generator inactive
TGSR	00	– No tone generator connection to any signal path
ATCR	00	– Microphone amplifier is in power-down mode – Reference voltage buffer is in power-down mode – Pins MIP1/MIN1 are directed to the microphone amplifier AMI
ARCR	00	– Earpiece amplifier AHO is in power-down mode – Loudspeaker amplifier ALS is in power-down mode
TFCR	00	– IOM-2 handshake procedure enabled – No internal speakerphone status signals are directed to PZ1/PZ2 – Analog test mode disabled – Digital test mode disabled

Defined reset values of the ARCOFI-registers (cont'd)

Register	Value after RESET [hex]	Meaning
SDICR	00	– Single clock rate (DCLK) is enabled – DX and SDX are configured as open drain outputs – Master clock rate is 512 kHz
TSCR	00	– Time-slot 0 (SDI) is selected
XCR	00	– AHO and ALS are in the differential mode
CRAM	00	– All locations (TE and Non-TE)

3.2 Initialization

During initialization a subset of configuration registers and coefficient RAM-locations has to be programmed to set the configuration parameters according to the application and desired features.

Configuration Registers:

Register	Bit	Effect	Restricted to
GCR	SP	Speakerphone ON/OFF	
	AGCX	TX-automatic gain control (only if GCR.SP = 1)	
	AGCR	RX-automatic gain control (only if GCR.SP = 1)	
	EVX	Enable voice transmit	
	SLOT	IOM-2 slot select	IOM-2 TE
	PU	Power-up/down mode	
	CAM	IOM-2 address mode	IOM-2
	LAW	A-Law/µ-Law	
DFICR	SA-SD	PCI-port configuration	IOM-2 TE
	VDM	Voice data manipulation	
PFCR	GX	TX digital gain	
	GR	RX digital gain	
	GZ	Sidetone gain	
	FX	TX-frequency correction filter	
	FR	RX-frequency correction filter	
	DHPR	Disable high-pass (50 Hz) receive	
	DHPX	Disable high-pass (50 Hz) transmit	
TGCR	TG	Tone generator	
	DT	Dual tone mode	
	ETF	Enable tone filter	
	CG	Control generator	
	BT	Beat tone generator	
	BM	Beat mode	
	SM	Stop mode	

Configuration Registers (cont'd)

Register	Bit	Effect	Restricted to
	SQTR	Square/trapezoid shaped signal	
TGSR	PM	Piezo mode	
	TRL	Tone ringing via loudspeaker	
	TRR	Tone ringing in receive direction	
	DTMF	DTMF-signal in transmit direction	
	TRX	Tone ringing in transmit direction	
ATCR	MIC	Microphone amplifier control	
	EVREF	Enable 2.4 V reference voltage at pin V_{REF}	
	AIMX	Analog input multiplexer	
ARCR	HOC	Handset amplifier control	
	CME	Controlled monitoring	
	LSC	Loudspeaker amplifier control	
TFCR	DHS	Disable IOM-2 handshake procedure	IOM-2
	EPZST	PZ1/PZ2 as speakerphone status output	
	ALTF	Analog Loops and test functions	
	DLTF	Digital Loops and test functions	
SDICR	EPP0	Enable push/pull (DX)	SDI
	EPP1	Enable push/pull (SDX)	SDI
	DCE	Double clock enable	SDI
TSCR	MCLKR	Master clock rate	SDI
XCR	TS	Time slot select	SDI
	DHOP	Disable HOP (tristate)	
	DHON	Disable HON (tristate)	
	DLSP	Disable LSP (tristate)	
	DLSN	Disable LSN (tristate)	

Note: Before accessing the ARCOFI PCI (IOM-2 TE-mode) interface, a GCR-write command (SOP_0 or SOP_F) has to be sent.

Coefficient RAM-locations:

Mnemonic	# of Bytes	Effect
COP_0: Tone generator parameter set 1		
F1	2	Tone generator frequency
G1	1	Tone generator amplitude
GD1	1	Trapezoid generator amplitude
T1	2	Beat tone time
	2	not used

Coefficient RAM-locations (cont'd)

Mnemonic	# of Bytes	Effect
COP_1: Tone generator parameter set 2; tone generator level adjustment		
F2	2	Tone generator frequency
G2	1	Tone generator amplitude
GD2	1	Trapezoid generator amplitude
T2	2	Beat tone time span
GTR	1	Level adjustment for receive path
GTX	1	Level adjustment for transmit path
COP_2: Tone generator parameter set 3; Parameter set for the DTMF-generator (TGSR.DTMF = 1)		
F3	2	Tone generator frequency
G3	1	Tone generator amplitude
GD3	1	Trapezoid generator amplitude
T3	2	Beat tone time span
FD	2	Dual tone frequency
COP_3: Tone filter		
K	1	Attenuation of the stop-band
A1	1	Center frequency
A2	1	Bandwidth
GE	1	Saturation amplification
COP_4: Control generator		
TON	2	Turn-on period of the tone generator
TOFF	2	Turn-off period of the tone generator
COP_5: Receive and transmit gain		
GX	2	Transmit gain
GR	2	Receive gain
	4	Not used
COP_6: Sidetone gain		
GZ	2	Sidetone gain
	2	not used
COP_7/COP_8: Transmit correction filter		
FX	12	Transmit correction filter coefficients

Coefficient RAM-locations (cont'd)

Mnemonic	# of Bytes	Effect
COP_8/COP_9: Receive correction filter		
FR	12	Receive correction filter coefficients
COP_A: Parameter set for transmit and receive speech comparator Parameter set for speakerphone control unit		
GAE	1	Gain of acoustic echo
GLE	1	Gain of line echo
ATT	1	Attenuation programmed in GHR or GHX
ETAE	1	Echo time (acoustic side)
ETLE	1	Echo time (line side)
TW	1	Wait time
DS	1	Decay speed
SW	1	Switching time
COP_B: Parameter set for transmit and receive speech comparator		
GDSAE	1	Reserve when speech is detected (acoustic side)
PDSAE	1	Peak decrement when speech is detected (acoustic side)
GDNAE	1	Reserve when noise is detected (acoustic side)
PDNAE	1	Peak decrement when noise is detected (acoustic side)
GDSLE	1	Reserve when speech is detected (line side)
PDSLE	1	Peak decrement when speech is detected (line side)
GDNLE	1	Reserve when noise is detected (line side)
PDNLE	1	Peak decrement when noise is detected (line side)
COP_C: Parameter set for transmit and receive speech detector		
LIM	1	Starting level of the logarithmic amplifiers
OFFX	1	Level offset up to detected noise (transmit)
OFFR	1	Level offset up to detected noise (receive)
LP2LX	1	Limitation for LP2 (transmit)
LP2LR	1	Limitation for LP2 (receive)
LP1X	1	Time constant LP1 (transmit)
LP1R	1	Time constant LP1 (receive)
	1	not used

Coefficient RAM-locations (cont'd)

Mnemonic	# of Bytes	Effect
COP_D: Parameter set for receive and transmit speech detector		
PDSX	1	Time constant PD for signal (transmit)
PDNX	1	Time constant PD for noise (transmit)
LP2SX	1	Time constant LP2 for signal (transmit)
LP2NX	1	Time constant LP2 for noise (transmit)
PDSR	1	Time constant PD for signal (receive)
PDNR	1	Time constant PD for noise (receive)
LP2SR	1	Time constant LP2 for signal (receive)
LP2NR	1	Time constant LP2 for noise (receive)
COP_E: Parameter set for transmit AGC		
LGAX	1	Loudness gain adjustment
COMX	1	Compare level rel. to max. PCM-value
AGX	1	Gain range of automatic control
TMHX	1	Settling time constant for lower levels
TMLX	1	Settling time constant for higher levels
NOISX	1	Threshold for AGC-reduction by background noise
	1	not used
	1	not used
COP_F: Parameter set for receive AGC		
LGAR	1	Loudness gain adjustment
COMR	1	Compare level rel. to max. PCM-value
AAR	1	Attenuation range of automatic control
AGR	1	Gain range of automatic control
TIMHR	1	Settling time constant for lower levels
TIMLR	1	Settling time constant for higher levels
NOISR	1	Threshold for AGC-reduction by background noise
	1	not used

3.3 ARCOFI® Operating Modes

The most currently used ARCOFI-operating modes are documented in the following table. The 12 ARCOFI-configuration registers have enough build-in flexibility to accommodate an extensive set of user calling procedures.

The following operating mode description table is not exhaustive but should be used as an example of possible functions performed by the ARCOFI.

State	Description
POR	Power-on reset: when power is supplied to the ARCOFI an internal power-on reset is generated. In addition a hardware reset via an RC-network connected to input pin RS will force all ARCOFI internal registers to default values. The ARCOFI-registers reset state is described in section 3.1 and 4.
STAND BY	The system microprocessor can initialize the ARCOFI via the IOM-2 or the SCI-bus with a different set of filter and configuration values. Whilst remaining in power-down (GCR.PU = 0) a new set of filter coefficients and configuration bits can be loaded in the ARCOFI.
HANDSET	The system MPU detects activity from the hookswitch or from the keyboard. The ARCOFI can be placed in HANDSET state where all handset I/O are enabled (AMI & AHO activated).
RINGING	The system MPU detects an incoming call, the ARCOFI can be placed in a RINGING state by activating the tone ringer via TGCR/TGSR and configuring the ARCOFI such that either the LSP/LSN-output or the piezo output (pins PZ1/PZ2) are enabled. An emergency ringing is also implemented. In this mode, only the tone ringer and the loudspeaker amplifier are active (AMI- and AHO-amplifier are disabled by the user). The tone ringer signal is directly switched to the loudspeaker amplifier ALS.
DTMF	All audio inputs can be disabled by forcing the AMI-amplifier (ATCR) to power-down. DTMF tones are generated with the tone generator and are output to the transmit path.
PULSE DIAL	Handset audio path can be enabled by forcing a HANDSET mode. A single tone can be superimposed into the audio receive path so as to provide audible feedback when dialling.
LOUD HEARING (MONITORING)	The handset I/O and the loudspeaker outputs LSP/LSN are active (ATCR & ARCR).

Operating mode description table (cont'd)

State	Description
SPEAKERPHONE	The handset audio I/O's are disabled. The hands-free microphone input and loudspeaker outputs LSP/LSN are activated by configuring ATCR & ARCR. The ARCOFI must be set to the speakerphone mode (GCR.SP = 1).
MUTE	The ARCOFI can be placed in a MUTE state by powering down the AMI. In handset mode the outputs HOP/HON remain enabled while in speakerphone mode the outputs LSP/LSN are enabled. All other analog I/O's being disabled.
FEATURE TONE	A single tone can be superimposed to the incoming PCM-voice signal. Applications requiring system function audible feedback are therefore made possible.

3.4 IOM®-2 Interface Protocol

The following description of the IOM-2 interface comprises all ARCOFI relevant functions in the terminal and non-terminal mode (see IOM-2 interface specification for general information).

Note: Channels IC1 & IC2 are only available in the IOM-2 TE-mode. MON-channel means MON1-channel in the IOM-2 TE-mode.

3.4.1 B- and IC-Channels

The ARCOFI can receive and transmit voice data in the IOM-2 B1- & B2-channels as well as in the IC1- & IC2-intercommunication channels located in IOM-2 channels 0 and 1 respectively. The voice/data channel allocation is programmable via the ARCOFI-channel select bit SLOT in the GCR-register. B1 or B2 or respectively IC1 or IC2 can be programmed by use of the RCM-bit in the CMDR-register.

The IC1- and IC2-intercommunication channels can be used in the terminal for local data communication (e.g. answering machine). This makes post-processing of voice/data information possible (e.g. data encryption).

3.4.2 Monitor Channel

All programming data required by the ARCOFI including coefficients are transmitted exclusively in the MON-time-slot of the IOM-2 channel. The MON-channel allows a point to multi-point access where the layer-2 component acts as the master to program devices like the ARCOFI. Each programmable device is accessed by sending a specific address byte at the start of each SOP- or COP-command stream. Before executing a command, the programmable device compares the received address byte with its own address. The latter consists of 8 bits whose 4th MSB-bit must correspond to the AD-wire (AD/MCLK pin) strapped IOM-2 address.

3.4.2.1 MON-Channel Data Structure

The data to control and program the ARCOFI are transferred in the MON1-channel via the IOM-2 interface by a procedure utilizing read/write registers in the ARCOFI.

The messages transmitted in the monitor channel may have different kinds of data structures. Therefore, the first byte of the message is used to indicate the data structure (first four bits).

Identification Command

In order to be able to identify unambiguously different devices by software, the following identification command is used:

DD 1st byte value	1	0	1	X	0	0	0	0
DD 2nd byte value	0	0	0	0	0	0	0	0

The ARCOFI responds to this DD-identification sequence by sending a DU identification sequence:

DU 1st byte value	1	0	1	X	0	0	0	0
DU 2nd byte value	1	0	DESIGN					

X: logical 0 (active low): AD = 0 (A-chip)
logical 1 (passive high): AD = 1 (B-chip)

DESIGN: six bit code, specific for each device in order to identify differences in operation

e.g.	000000	ARCOFI	PSB 2160
	000010	ARCOFI-SP	PSB 2165
	000100	ARCOFI-SP	PSB 2163

This identification sequence is usually done once, when the terminal is connected for the first time.This function is used so that the software can distinguish between different possible hardware configurations. However this sequence is not compulsory.

Programming Sequence

An ARCOFI-programming sequence is characterized by a “1” being sent in the LSB-nibble of the first incoming identification code.

DD 1st byte value	1	0	1	X	0	0	0	1
DD 2nd byte value	COP_X, SOP_X, XOP_X							

All programmed configurations and coefficients can be read back when issuing an appropriate CMDR read (CMDR.R/W = 1). The ARCOFI responds by sending an IOM-2 specific address byte identifying the chip followed by the requested data.

3.4.2.2 MON-Transfer Protocol

The transfer of a stream of commands in the MON-channel is regulated by a handshake protocol mechanism implemented by two bits MX and MR in the fourth slot of the IOM-2 channel. The procedure is as follows (**figure 34**):

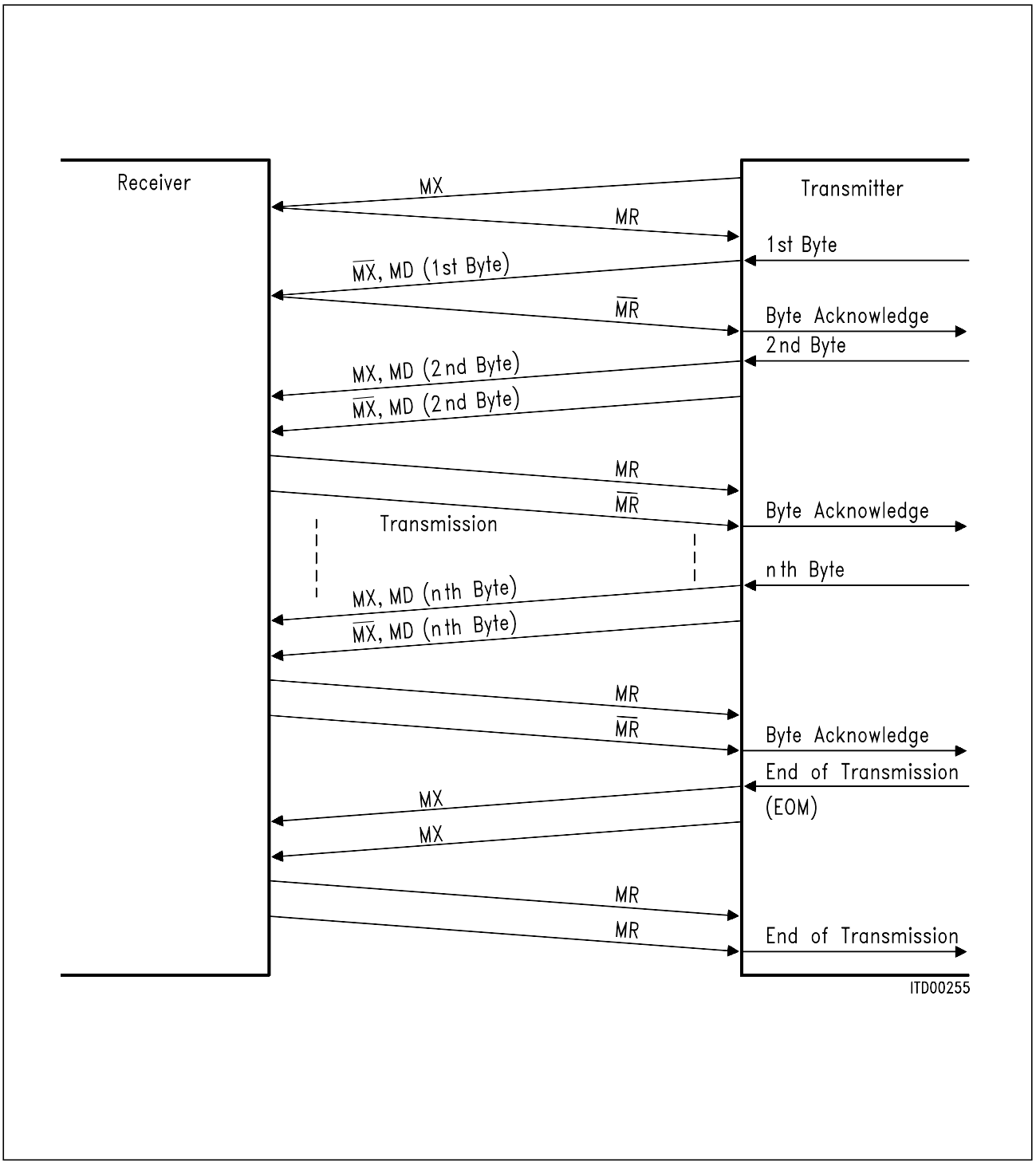


Figure 34
Monitor Channel Handshake Procedure

Monitor transfer protocol rules:

- A pair of MX and MR in the inactive state for two or more consecutive frames indicates an idle state or an end of transmission (EOM).
- A command stream initiated by a transmitter in the MON-slot is accompanied by an activated downstream MX-bit.
- The receiver acknowledges a received byte by toggling the upstream MR-bit from inactive to active in the subsequent IOM-2 frame for at least one frame.
- The transmitter indicates a new byte in the MON-slot by the transition of the MX-bit from the active to the inactive state. The MX-bit returns to the active state after one frame. Two frames with the MX-bit in the inactive state indicate the end of transmission.
- The receiver acknowledges each new byte by a similar one frame transition of the MR-bit to the inactive state. Two frames with the MR-bit set to inactive indicate a receiver request for abort.
- The transmitter can delay a transmission sequence by sending the same byte continuously. In that case the MX-bit remains active in the IOM-2 frame following the first byte occurrence.
- Delaying a transmission sequence is only possible while the receiver MR-bit and the transmitter MX-bit are active.
- Since the receiver is able to receive the MON-slot data at least twice (in two consecutive frames), the receiver waits for the reception of two successive identical bytes.
- To control this handshake procedure a collision detection mechanism is implemented in the transmitter. This is done by making a collision check per bit on the transmitted MON-data.

3.4.2.3 Implementation of the MON-Channel Protocol

The MON-receiver has the following features:

- Transparent interface between IOM-2 interface and any device internal block (sink) with respect to handshake procedure, i.e. any acknowledge, EOM, abort or request for abort is conveyed transparently through the receiver.

Figure 35 shows the state diagram of the MON-receiver. The following signals are used:

MR: MR-bit sent by the receiver
MX: MX-bit received
LL: Last two bytes were identical

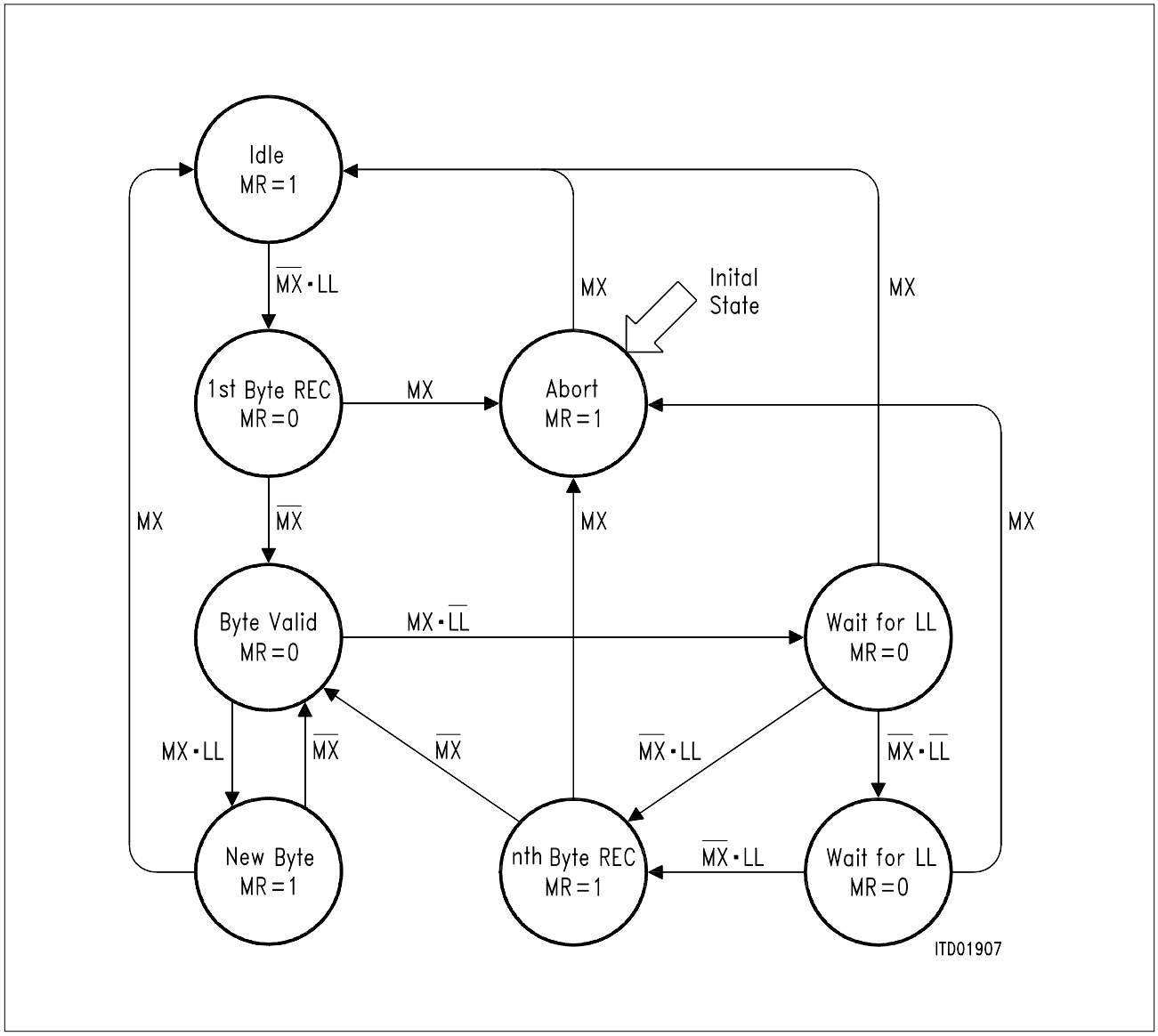


Figure 35
State Diagram of the Monitor Receiver

The MON-transmitter has the following features:

- Transparent interface between IOM-2 interface and any device internal block (source) with respect to handshake procedure, i.e. any acknowledge, abort, request for abort is conveyed transparently through the transmitter.

Figure 36 shows the state diagram of the MON-transmitter. The following signals are used:

MR: MR-bit received
MX: MX-bit transmitted
LL: Last two bytes were identical
RQT: Request transmission
EOM: End of transmission

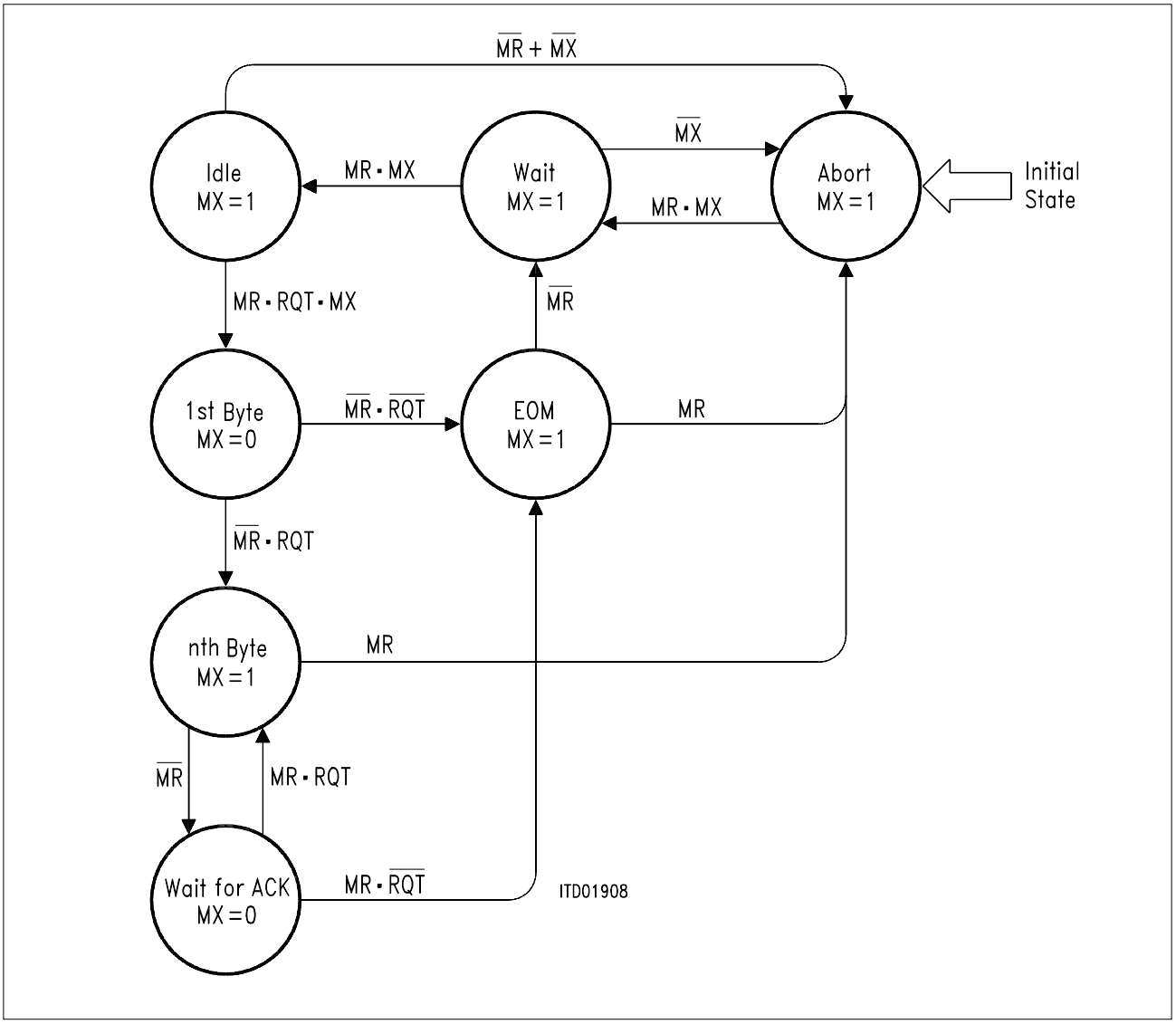


Figure 36
State Diagram of the Monitor Transmitter

3.4.3 Command/Indication Channel 1 (TE-mode)

The C/I-channel bits are represented so that the first bit transmitted/received appears on the left. The data presented to the four peripheral control interface (PCI) pins SA to SD are transparently routed to the C/I IOM-2 channel 1. Pins SA to SD can be configured individually as input or output and the information sent to the pins SA to SD or coming from them will appear respectively in the DD or DU C/I IOM-2 channel 1.

In case a reset has been asserted, the SA- to SD-pins are programmed as input, however the SA- to SD-values are not switched to the DU C/I1-channel unless a write command (except NOP) is issued.

The mapping of the peripheral control interface (PCI) pins SA to SD into the six C/I1-channel bits depends on the hardwired AD-address (see section 3.7) as follows.

AD = 1

	7					2	1	0
DD and DU	–	–	SB	SA	SD	SC	MR	MX

AD = 0 (GCR.CAM = 0; two chip mode)

DD and DU	SD	SC	–	–	–	–	MR	MX

AD = 0 (GCR.CAM = 1; one chip mode)

DD and DU	SD	SC	SB	SA	–	–	MR	MX

C/I1-Channel (Signaling) Bit Allocation Table:

CAM	AD	DD-C/I1						DU-C/I1						PCI-Configuration
		7	6	5	4	3	2	7	6	5	4	3	2	
X	X	X	X	X	X	X	X	H	H	H	H	H	H	after reset
								S	S					
0	0	X	X	X	X	X	X	D	C	H	H	H	H	PCI-pins as inputs
		S	S											
0	0	D	C	X	X	X	X	H	H	H	H	H	H	PCI-pins as outputs
		S							S					
0	0	D	X	X	X	X	X	H	C	H	H	H	H	PCI-pin SC as input PCI-pin SD as output
			S					S						
0	0	X	C	X	X	X	X	D	H	H	H	H	H	PCI-pin SD as input PCI-pin SC as output
										S	S	S	S	
X	1	X	X	X	X	X	X	H	H	B	A	D	C	PCI-pins as inputs
				S	S	S	S							
X	1	X	X	B	A	D	C	H	H	H	H	H	H	PCI-pins as outputs
					S		S			S		S		
X	1	X	X	X	A	X	C	H	H	B	H	D	H	SB and SD as inputs SA and SC as outputs
				S		S					S		S	
X	1	X	X	B	X	D	X	H	H	H	A	H	C	SA and SC as inputs SB and SD as outputs
								S	S	S	S			
1	0	X	X	X	X	X	X	D	C	B	A	H	H	PCI-pins as inputs
		S	S	S	S									
1	0	D	C	B	A	X	X	H	H	H	H	H	H	PCI-pins as outputs
		S		S					S		S			
1	0	D	X	B	X	X	X	H	C	H	A	H	H	SA and SC as inputs SB and SD as outputs
			S		S			S		S				
1	0	X	C	X	A	X	X	D	H	B	H	H	H	SB and SD as inputs SA and SC as outputs

X: don’t care
H: passive high

3.5 ARCOFI® Voice/Data Manipulation (VDM)

The ARCOFI offers several possibilities of voice/data manipulation for special applications.

According to the manipulation mode chosen, the byte B1 or B2 (or IC1 or IC2 in the IOM-2 TE-mode) can be output via the handset channel and/or the loudspeaker channel.

The following tables gives an overview of the different voice/data manipulation modes.

- **PCM-mode or normal mode (DFICR.VDM = 000X):**

DFICR.VDM	AD Pin (IOM-2) [1]	CMDR.RCM (IOM-2)	GCR.SLOT (IOM-2)	Receive Channel	Transmit Channel
0000	0	0	0	–	B1
	0	0	1	–	IC1
	0	1	0	–	B2
	0	1	1	–	IC2
	1	0	0	–	B2
	1	0	1	–	IC2
	1	1	0	–	B1
	1	1	1	–	IC1
0001	0	0	0	B1	B1
	0	0	1	IC1	IC1
	0	1	0	B2	B2
	0	1	1	IC2	IC2
	1	0	0	B2	B2
	1	0	1	IC2	IC2
	1	1	0	B1	B1
	1	1	1	IC1	IC1

- **Linear mode (DFICR.VDM = 010X):**

This mode exists only in the SDI mode (in the programmed and the following channel) or in the IOM-2 one chip mode (GCR.CAM = 1). The two voice/data channels B1 and B2 (or IC1 and IC2 in the IOM-2 TE-mode) are connected to one 16-bit linear channel (2s complement).

DFICR.VDM	AD Pin (IOM-2)	CMDR.RCM (IOM-2)	GCR.SLOT (IOM-2)	Receive Channel	Transmit Channel
0100	–	–	0	–	B1 & B2
	–	–	1	–	IC1 & IC2
0101	–	–	0	B1 & B2	B1 & B2
	–	–	1	IC1 & IC2	IC1 & IC2

[1] This table is given for the IOM-2 two chip mode (GCR.CAM = 0).

B1&B2 (IC1&IC2) means B1 (IC1) byte followed by B2 (IC2) byte (totally 16 bits).

- **Three party conferencing (DFICR.VDM = 100X):**

This mode is available only in the SDI-mode (in the programmed and the following channel) or in the IOM-2 one chip mode (GCR.CAM = 1).

DFICR.VDM	AD Pin (IOM-2)	CMDR.RCM (IOM-2)	GCR.SLOT (IOM-2)	Receive Channel	Transmit Channel
1000	– –	– –	0 1	B1 + B2 IC1 + IC2	B1, B2 IC1, IC2

B1 + B2 (IC1 + IC2) means the B1 (IC1) and the B2 (IC2) byte are added together (on 8 bits).
B1, B2 (IC1, IC2) means B1 (IC1) and B2 (IC2) byte have the same information.

- **Voice monitoring mode (DFICR.VDM = 1100):**

This mode is available only in the SDI-mode or in the IOM-2 one chip mode (GCR.CAM = 1). The monitoring chip and the transmission chip must be strapped to a different hardware address (IOM-2: AD/MCLK pin).

The active DU-voice channel of the monitoring chip must be set in the Hi Z-mode (GCR.EVX = 0).

The PCI-port of both chips must be set in the compatible configurations to avoid collision problems in the DU-C/I1 channel.

DFICR.VDM	AD Pin (IOM-2)	CMDR.RCM (IOM-2)	GCR.SLOT (IOM-2)	Receive Channel	Transmit Channel
1100	1/0 1/0 1/0 1/0	0 0 1 1	0 1 0 1	B1D + B1U IC1D + IC1U B2D + B2U IC2D + IC2U	B1 IC1 B2 IC2

Explanations:

–	no signal
B1/B2	voice channels
IC1/IC2	IOM-2 intercommunication channels
B1D/B2D	IOM-2 voice channels (downstream)
B1U/B2U	IOM-2 voice channels (upstream)
IC1D/IC2D	IOM-2 intercommunication channels (downstream)
IC1U/IC2U	IOM-2 intercommunication channels (upstream)

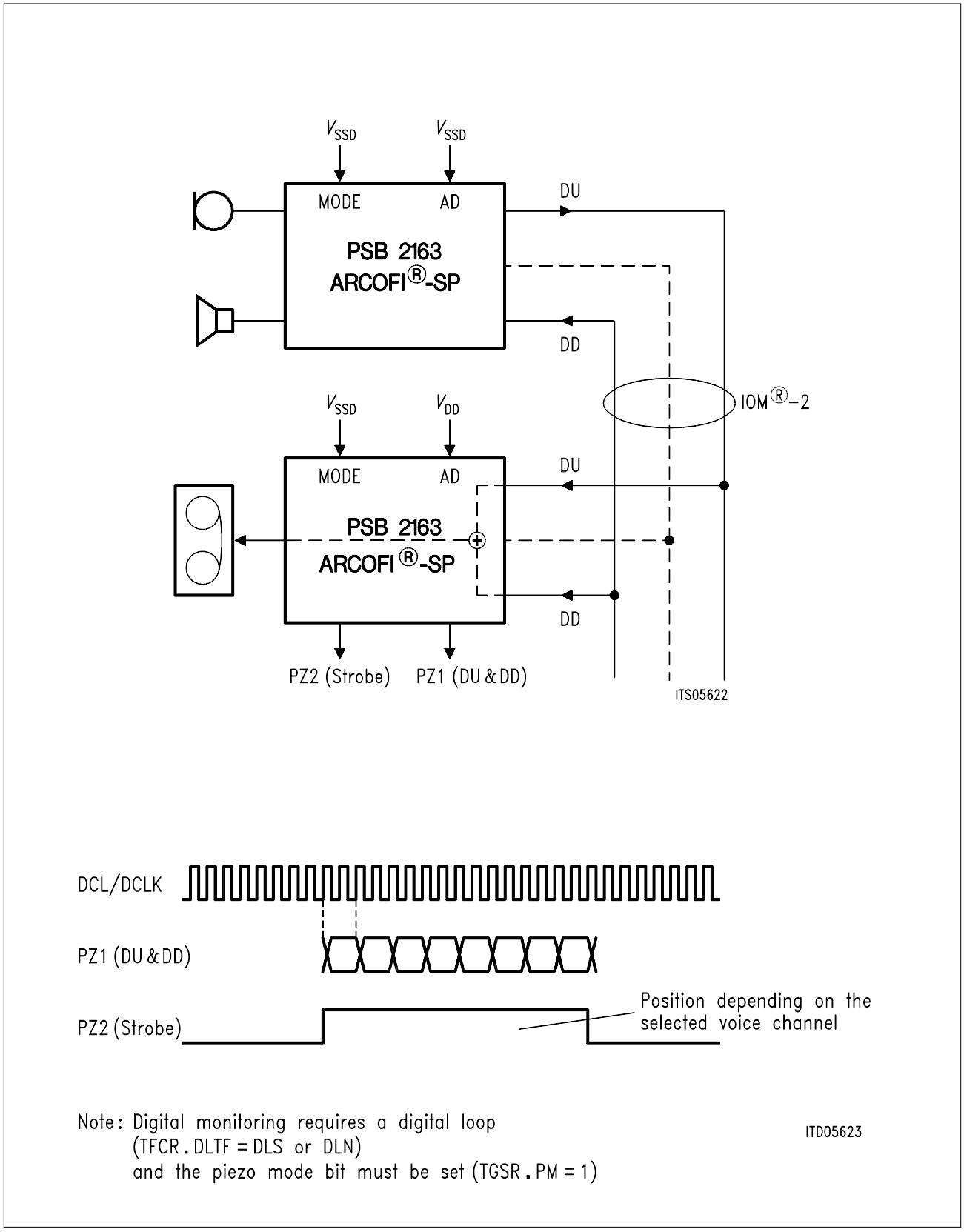


Figure 37
Configuration of the IOM®-2 TE-Monitoring Mode

4 Detailed Register Description

The following section describes the various ARCOFI-registers and coefficient RAM-locations accessible from the terminal equipment microcontroller via the IOM-2 bus or via the serial controller interface (SCI).

A summary of the 12 registers located in the ADI-block is presented below followed by a detailed description of the register content.

Command Register (CMDR)

	7							0
CMDR	R/W	RCM	CMD5	CMD4	CMD3	CMD2	CMD1	CMD0

General Configuration Register (GCR)

	7							0
GCR	SP	AGCX	AGCR	EVX	SLOT	PU	CAM	LAW

Data Format and Interface Configuration Register (DFICR)

	7					0
DFICR	SD	SC	SB	SA	VDM	

Programmable Filter Configuration Register (PFCR)

	7							0
PFCR	GX	GR	GZ	FX	0	FR	DHPR	DHPX

Tone Generator Configuration Register (TGCR)

	7							0
TGCR	TG	DT	ETF	CG	BT	BM	SM	SQTR

Tone Generator Switch Register (TGSR)

	7							0
TGSR	PM	TRL	0	TRR	DTMF	TRX	0	0

AFE Transmit Configuration Register (ATCR)

	7							0
ATCR	MIC				EVREF	0	AIMX	

AFE Receive Configuration Register (ARCR)

	7							0
ARCR	HOC				CME	LSC		

Test Function Configuration Register (TFCR)

	7							0
TFCR	0	EPZST	ALTF				DLTF	

SDI-Configuration Register (SDICR); only available in SDI-mode

	7							0
SDICR	0	0	EPP1	EPP0	DCE	MCLKR		

Time-Slot Configuration Register (TSCR); only available in SDI-mode

	7							0
TSCR	0	0	TS					

Extended Configuration Register (XCR)

	7							0
XCR	PGCR	PGCX	RAAR	OBS	DHOP	DHON	DLSP	DLSN

Test Mode Register (TMR)

	7							0
TMR	TM			0	0	0	0	0

4.1 Command Register (CMDR)

Value after reset: BF_H

	7							0
CMDR	R/W	RCM	CMD5	CMD4	CMD3	CMD2	CMD1	CMD0

R/W 0: writing to configuration registers or to coefficient RAM
1: reading from configuration registers or from coefficient RAM

RCM **Reverse Channel Mode** (if R/W = 0)
0: receive and transmit in B1 (or IC1 in TE-mode)
1: receive and transmit in B2 (or IC2 in TE-mode)

For the IOM-2 two chip mode (GCR.CAM = 0), when pin AD is strapped to V_{SS} the above applies. When pin AD is strapped to V_{DD}, RCM operates in the reverse order.

CMDx Address to internal programmable locations

CMD 5	4	3	2	1	0	
0	0	X	X	X	X	code reserved
0	1	X	X	X	X	status operation (SOP)
1	0	X	X	X	X	coefficient operation (COP)
1	1	X	X	X	X	extended operation (XOP)

Coding of status operations (SOP):

Bit 3	2	1	0	CMD Name	Status	CMD Seq. Len.	CMD Sequence Description
0	0	0	0	SOP_0	R/W	2	<GCR>
0	0	0	1	SOP_1	R/W	2	<DFICR
0	0	1	0	SOP_2	R/W	2	<PFCR>
0	0	1	1	SOP_3	R/W	2	<TGCR>
0	1	0	0	SOP_4	R/W	2	<TGSR>
0	1	0	1	SOP_5	R/W	2	<ATCR>
0	1	1	0	SOP_6	R/W	2	<ARCR>
0	1	1	1	SOP_7	R/W	2	<TFCR>
1	0	0	0	SOP_8	R/W	2	<SDICR>
1	0	0	1	SOP_9	R/W	2	<TSCR>
1	0	1	0	SOP_A	R/W	2	<XCR>
1	1	0	1	SOP_D	R	2	<IDENT>[1)]
1	1	1	0	SOP_E	R/W	2	<TMR>
1	1	1	1	SOP_F	R/W	9	<TFCR>..<GCR>

1) See also 4.12.

Coding of coefficient operations (COP):

Bit 3	2	1	0	CMD Name	Status	CMD Seq. Len.	CMD Sequence Description	Comments
0	0	0	0	COP_0	R/W	9	<F1> <F1> <G1> <GD1> <T1> <T1> <..> <..>	Tone generator 1
0	0	0	1	COP_1	R/W	9	<F2> <F2> <G2> <GD2> <T2> <T2> <GTR> <GTX>	Tone generator 2 Additional TG-gain
0	0	1	0	COP_2	R/W	9	<F3> <F3> <G3> <GD3> <T3> <T3> <FD> <FD>	Tone generator 3 Dual tone frequency
0	0	1	1	COP_3	R/W	5	<K> <A1> <A2> <GE>	Tone filter
0	1	0	0	COP_4	R/W	5	<TON> <TON> <TOFF> <TOFF>	Control generator
0	1	0	1	COP_5	R/W	9	<GX> <GX> <GR> <GR> <..> <..> <..> <..>	Transmit gain Receive gain
0	1	1	0	COP_6	R/W	5	<GZ> <GZ> <..> <..>	Sidetone gain
0	1	1	1	COP_7	R/W	9	<FX1>..<FX8>	Correction filter FX
1	0	0	0	COP_8	R/W	9	<FX9>..<FX12> <FR1>..<FR4>	Correction filter FR
1	0	0	1	COP_9	R/W	9	<FR5>..<FR12>	
1	0	1	0	COP_A	R/W	9	<SP1>..<SP8>	Coefficients for
1	0	1	1	COP_B	R/W	9	<SP9>..<SP16>	Speakerphone
1	1	0	0	COP_C	R/W	9	<SP17>..<SP24>	
1	1	0	1	COP_D	R/W	9	<SP25>..<SP32>	
1	1	1	0	COP_E	R/W	9	<AGCX1>..<AGCX8>	AGC-transmit
1	1	1	1	COP_F	R/W	9	<AGCR1>..<AGCR8>	AGC-receive

Coding of extended operations (XOP):

Bit 3	2	1	0	CMD Name	Status	CMD Seq. Len.	Comments
0	0	0	0	XOP_0	W	1	Power-down mode
0	0	0	1	XOP_1	W	1	Power-up mode
1	1	0	1	XOP_D	W	1	DD/DU-voice channel swap (toggle function)
1	1	1	0	XOP_E	W	1	Software reset
1	1	1	1	XOP_F	R/W	1	Normal operation (NOP)

4.2 General Configuration Register (GCR)

Value after reset: 00_H

	7							0
GCR	SP	AGCX	AGCR	EVX	SLOT	PU	CAM	LAW

SP **Speakerphone**
0: speakerphone support disabled
1: speakerphone support enabled

AGCX **Automatic Gain Control Transmit**
0: automatic gain control disabled
1: automatic gain control enabled; only if speakerphone support is enabled (SP = 1)

AGCR **Automatic Gain Control Receive**
0: automatic gain control disabled
1: automatic gain control enabled; only if speakerphone support is enabled (SP = 1)

EVX **Enable Voice Transmit**
0: disable transmit voice data
1: enable transmit voice data (if GCR.PU = 0, idle code is transmitted)

SLOT **IOM-2 Slot Select** (IOM-2 TE-mode only)
0: bearer channels in IOM-channel 0
1: bearer channels in IOM-channel 1

PU **Power-Up**
0: the ARCOFI is placed in standby mode (power-down); all registers and coefficient RAM contents are saved and all interface functions are available
1: the ARCOFI is in a normal operating mode (power-up)

This bit can be directly accessed by the XOP_0/XOP_1 operations.

CAM **Chip Address Mode** (IOM-2 mode only)
0: two ARCOFIs are connected to the IOM-2 bus
1: only one ARCOFI is connected to the IOM-2 bus

LAW **Coding Law**
0: A-Law enabled
1: µ-Law enabled

4.3 Data Format and Interface Configuration Register (DFICR)

Value after reset: $F0_H$

	7				0
DFICR	SD	SC	SB	SA	VDM

SD-SA **Signaling I/O** (PCI-interface; only available in IOM-2 TE-mode)
0: Sx pin programmed as output (x: D, C, B or A)
1: Sx pin programmed as input (x: D, C, B or A)

VDM **Voice Data Manipulation**

Bit 3	2	1	0	Receive Voice Channel	Transmit Voice Channel	Description
0	0	0	0	–	B1	Transmit only
0	0	0	1	B1	B1	Transfer mode
0	1	0	0	–	B1 & B2	16-bit transmit only
0	1	0	1	B1 & B2	B1 & B2	16-bit transfer mode
1	0	0	0	B1 + B2	B1, B2	Conferencing mode
1	1	0	0	B1D + B1U	B1	Monitoring mode

– no signal

Note: In this table above the voice channels indicated are only examples. Other combinations of B1 and B2 (IC1 and IC2 in IOM-2 TE-mode) are possible and a complete description is given in section 3.5.

4.4 Programmable Filter Configuration Register (PFCR)

Value after reset: 00_H

	7							0
PFCR	GX	GR	GZ	FX	0	FR	DHPR	DHPX

GX **Transmit Gain**
0: gain set to 0 dB
1: gain coefficients loaded from coefficient RAM (CRAM)

GR **Receive Gain**
0: gain set to 0 dB
1: gain coefficients loaded from CRAM

GZ **Sidetone Gain**
0: gain set to – ∞ dB
1: gain coefficients loaded from CRAM

FX **Transmit Frequency Correction Filter**
0: filter is by-passed
1: filter coefficients loaded from CRAM

FR **Receive Frequency Correction Filter**
0: filter is by-passed
1: filter coefficients loaded from CRAM

DHPR **Disable High-Pass Receive** (50/60 Hz filter)
0: filter enabled
1: filter disabled

DHPX **Disable High-Pass Transmit** (50/60 Hz filter)
0: filter enabled
1: filter disabled

4.5 Tone Generator Configuration Register (TGCR)

Value after reset: 00_H

	7							0
TGCR	TG	DT	ETF	CG	BT	BM	SM	SQTR

TG **Tone Generator**
0: tone generator is disabled (if CG = 0)
1: tone generator is enabled; frequency and gain coefficients loaded from CRAM; CG has priority over TG

DT **Dual Tone Mode** (DTMF)
0: second trapezoid generator is disabled
1: second trapezoid generator is enabled; the output signal is added to the S/T signal generator (only if TGSR.DTMF = 0)

ETF **Enable Tone Filter**
0: tone filter is by-passed
1: tone filter is enabled; filter coefficients loaded from CRAM

CG **Control Generator**
0: control generator is disabled
1: control generator is enabled; time coefficients loaded from CRAM (tone generator is activated independently of TG-bit setting)

BT **Beat Tone Generator**
0: beat tone generator is disabled
1: beat tone generator is enabled; time coefficients loaded from CRAM

BM **Beat Mode**
0: beat mode is disabled; two tone ring activated when BT-generator is enabled
1: beat mode is enabled; three tone ring activated when BT-generator is enabled (only if TGSR.DTMF = 0)

SM **Stop Mode**
0: automatic stop mode is disabled
1: automatic stop mode is enabled; two and three tone ring gets turned off after the sequence is completed

SQTR **Square/Trapezoid Waveform**
0: trapezoid shaped signal is enabled (
only if tone ringing via loudspeaker and piezo mode is disabled: TGSR.TRL = 0 & TGSR.PM = 0)
1: square-wave signal is enabled

4.6 Tone Generator Switch Register (TGSR)

Value after reset: 00_H

	7							0
TGSR	PM	TRL	0	TRR	DTMF	TRX	0	0

PM **Piezo Mode**
0: ringing signal is not output to the piezo ring pins
1: ringing signal (square) is output to the piezo ring pins PZ1/PZ2

TRL **Tone Ringing via Loudspeaker**
0: ringing signal is not output directly to the loudspeaker pins
1: ringing signal (square) is output directly to the loudspeaker pins LSP/LSN

TRR **Tone Ringing Receive**
0: tone generator for receive direction is disabled
1: tone generator for receive direction is enabled

DTMF **DTMF-Generator** (transmit)
0: DTMF-generator for transmit direction is disabled
1: DTMF-generator for transmit direction is enabled

TRX **Tone Ringing Transmit**
0: tone generator for transmit direction is disabled
1: tone generator for transmit direction is enabled

4.7 AFE-Transmit Configuration Register (ATCR)

Value after reset: 00_H

	7							0
ATCR	MIC				EVREF	0	AIMX	

MIC **Microphone Control**

Bit 7	6	5	4	Selected Mode
0	0	0	0	AMI is in **power-down** mode
0	0	0	1	0 dB amplification
0	0	1	0	6 dB amplification
0	0	1	1	12 dB amplification
0	1	0	0	18 dB amplification
0	1	0	1	24 dB amplification
0	1	1	0	30 dB amplification
0	1	1	1	36 dB amplification
1	0	0	0	42 dB amplification
1	1	1	1	AMI is in **by-pass** mode

EVREF **Enable V_{REF}** (2.4-V reference voltage)

0: V_{REF}-buffer is enabled in function of bit GCR.PU (global power-up) and ATCR/ARCR-programming

1: V_{REF}-buffer and internal reference voltage generation are enabled independently of the ARCOFI-configuration

AIMX **Analog Input Multiplexer**

Bit 1	0	Selected Input
0	0	AMI is connected to the pins MIP1/MIN1 (differential input)
0	1	AMI is connected to the pins MIP2/MIN2 (differential input)
1	0	AMI is connected to the pin MI3 (single-ended input)
1	1	not used

4.8 AFE-Receive Configuration Register (ARCR)

Value after reset: 00_H

	7			0
ARCR	HOC	CME	LSC	

HOC **Handset Output Control**

Bit 7	6	5	Selected Mode
0	0	0	AHO is in **power-down** mode
0	0	1	2.5 dB amplification
0	1	0	– 3.5 dB amplification
0	1	1	– 9.5 dB amplification
1	0	0	– 15.5 dB amplification
1	0	1	– 21.5 dB amplification
1	1	1	AHO is in **by-pass** mode

CME **Control Monitoring Enable** (GCR.SP = 1)
0: controlled monitoring disabled
1: controlled monitoring enabled (if transmit speech is detected, ALS-programming is fixed to – 9.5 dB if LSC > – 9.5 dB)

LSC **Loudspeaker Output Control**

Bit 3	2	1	0	Selected Mode
0	0	0	0	ALS is in **power-down** mode
0	0	0	1	11.5 dB amplification
0	0	1	0	8.5 dB amplification
0	0	1	1	5.5 dB amplification
0	1	0	0	2.5 dB amplification
0	1	0	1	– 0.5 dB amplification
0	1	1	0	– 3.5 dB amplification
0	1	1	1	– 6.5 dB amplification
1	0	0	0	– 9.5 dB amplification
1	0	0	1	– 12.5 dB amplification
1	0	1	0	– 15.5 dB amplification
1	0	1	1	– 18.5 dB amplification
1	1	0	0	– 21.5 dB amplification
1	1	1	1	ALS is in **by-pass** mode

4.9 Test Function Configuration Register (TFCR)

Value after Reset: 00_H

	7			0
TFCR	0	EPZST	ALTF	DLTF

EPZST **Enable PZ1/PZ2** (piezo pins) to output internal Status Information
0: PZ1/PZ2 are used as piezo port pins
1: PZ1/PZ2 are used to indicate internal speakerphone conditions (PZ1: speakerphone idle condition; PZ2: speakerphone transmit active)
Note: PM-bit must be set (TGSR.PM = 1)

ALTF **Analog Loop** and **Test Functions**

Bit 5	4	3	Test Function
0	0	0	NOT: No Test Mode
0	0	1	ALF: Analog Loop via Front End
0	1	0	ALC: Analog Loop via Converter
0	1	1	ALN: Analog Loop via Noise Shaper
1	0	0	ALI: Analog Loop via Interface

DLTF **Digital Loop** and **Test Functions**

Bit 2	1	0	Test Function
0	0	0	NOT: No Test Mode
0	0	1	IDR: Initialize DRAM
0	1	0	DLP: Digital Loop via PCM-Register
0	1	1	DLS: Digital Loop via Signal Processor
1	0	0	DLN: Digital Loop via Noise Shaper

4.10 SDI-Configuration Register (SDICR); SDI-mode only

Value after reset: 00_H

	7					0
SDICR	0	0	EPP1	EPP0	DCE	MCLKR

EPP0 **Enable Push-Pull** at pin DU/DX (SDI-mode only)
0: open drain enabled
1: push-pull enabled

EPP1 **Enable Push-Pull** at pin SDR/SDX (SDI-mode only)
0: open drain enabled
1: push-pull enabled

DCE **Double Clock Enable** for DCLK (SDI-mode only)
0: single clock rate
1: double clock rate

MCLKR **Master Clock Rate** (synchronized system clock)

Bit 2	**1**	**0**	**MCLK-Clock Rate**
0	0	0	512 kHz
0	0	1	1.536 MHz
0	1	0	2.048 MHz
0	1	1	4.096 MHz
1	X	X	16.384 MHz (test mode)

4.11 Time-Slot Configuration Register (TSCR); SDI-mode only

Value after Reset: 00_H

	7			0
TSCR	0	0	TS	

TS **Time-Slot Selection**

Bit 5	4	3	2	1	0	Time-Slot
0	0	0	0	0	0	0
0	0	0	0	0	1	1
		.				.
		.				.
1	1	1	1	1	1	63

4.12 Extended Configuration Register (XCR)

Value after reset: 00_H

	7							0
XCR	PGCR	PGCX	RAAR	OBS	DHOP	DHON	DLSP	DLSN

PGCR **Position of Gain Control Receive**
0: in front of the speech detector
1: behind the speech detector

PGCX **Position of Gain Control Transmit**
0: behind the speech detector
1: in front of the speech detector

RAAR **Read Automatic Attenuation Receive**
0: disabled
1: enabled

OBS **Observation** of internal modes (only for internal tests)
0: disabled
1: enabled

DHOP **Disable HOP**-Amplifier
0: HOP-amplifier normal mode
1: Disable HOP-amplifier (power-down, output high impedance)

DHON **Disable HON**-Amplifier
0: HON-amplifier normal mode
1: Disable HON-amplifier (power-down, output high impedance)

DLSP **Disable LSP**-Amplifier
0: LSP-amplifier normal mode
1: Disable LSP-amplifier (power-down, output high impedance)

DLSN **Disable LSN**-Amplifier
0: LSN-amplifier normal mode
1: Disable LSN-amplifier (power-down, output high impedance)

Note: XCR.RAAR = 1, SOP_D (read) monitors the magnitude of the gain-cell AGCR instead of IDENT.

4.13 Test Mode Register (TMR)

Value after reset: 00_H

	7					0
TMR	TM	0	0	0	0	0

TM **Test Mode** (only for internal tests)
000: normal mode

5 Electrical Characteristics

Absolute Maximum Ratings

Parameter	Symbol	Limit Values	Unit
Ambient temperature under bias	T_A [1)]	– 25 to 80	˚C
Storage temperature	T_{STG}	– 65 to125	˚C
Voltage on any pin with respect to ground	V_S	– 0.3 to V_{DD} + 0.3	V
Maximum voltage on any pin	V_{max}	7	V

1) Reduced performance

ESD-integrity (according MIL-Std 883D, method 3015.7): 1000 V
exception: The pins #14, #16, #17 and #18 are not protected against voltage stress > 630 V (versus VSSx, x = A, D, P). The output performance prohibits the use of adequate protective structures.

Note: Stresses above those listed here may cause permanent damage to the device. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

DC-Characteristics

V_{DD}/V_{DDP} = 5 V ± 5 %; $V_{SSD}/V_{SSA}/V_{SSP}$ = 0 V; T_A = 0 to 70 ˚C

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Input leakage current	I_{IL}	– 1.0	1.0	µA	0 V ≤ V_{IN} ≤ V_{DD}
H-input level (except pins SCLK, MCLK, DCLK)	V_{IH1}	2.0	V_{DD} + 0.3	V	
L-input level (except pins SCLK, MCLK, DCLK)	V_{IL1}	– 0.3	0.8	V	
H-input level (except pins SCLK, MCLK, DCLK)	V_{IH2}	0.7 V_{DD}	V_{DD}	V	
L-input level (except pins SCLK, MCLK, DCLK)	V_{IL2}	0	0.3 V_{DD}	V	
H-output level (except pins PZ1/PZ2)	V_{OH1}	2.4		V	I_O = 400 µA
H-output level (pins PZ1/PZ2)	V_{OH2}	V_{DD} – 0.45		V	I_O = 2 mA

DC-Characteristics (cont'd)

V_{DD}/V_{DDP} = 5 V ± 5 %; $V_{SSD}/V_{SSA}/V_{SSP}$ = 0 V; T_A = 0 to 70 °C

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
L-output level (except pin DU)	V_{OL1}		0.45	V	I_O = – 2 mA
L-output level (pins DU, DD[1])	V_{OL2}		0.45	V	I_O = – 7 mA
V_{DD} supply current standby (IOM-2 TE)	I_{DDS1}		0.9	mA	V_{DD} = 5 V; DCL = ON
	I_{DDS2}		0.2	mA	DCL = OFF
V_{DD} supply current operating (IOM-2 TE) [2]	I_{DDO1}		25	mA	V_{DD} = 5 V emergency ringing via ALS (TGSR.TRL = 1)
	I_{DDO2}		25	mA	handset mode (ARCR.HOC = 010_B)
Input capacitance	C_I		10	pF	
Output capacitance	C_O		15	pF	

1) If voice channel swap (XOP_D) is enabled.

2) Operating power dissipation is measured with all analog outputs open.
All analog inputs are set to V_{REF}.
The digital input signal (pin DD) is set to an idle code.
For the emergency ringing mode, the tone generator is set to 400-Hz single tone (square).
In this mode the loudspeaker amplifier is set to – 3.5 dB (3.2 Vpp)

Note: Power dissipation values are target values.

AC-Characteristics

Inputs are driven to 2.4 V for a logical "1" and to 0.45 V for a logical "0". Timing measurements are made at 2.0 V for a logical "1" and 0.8 V for a logical "0". The AC-testing input/output waveforms are shown below.

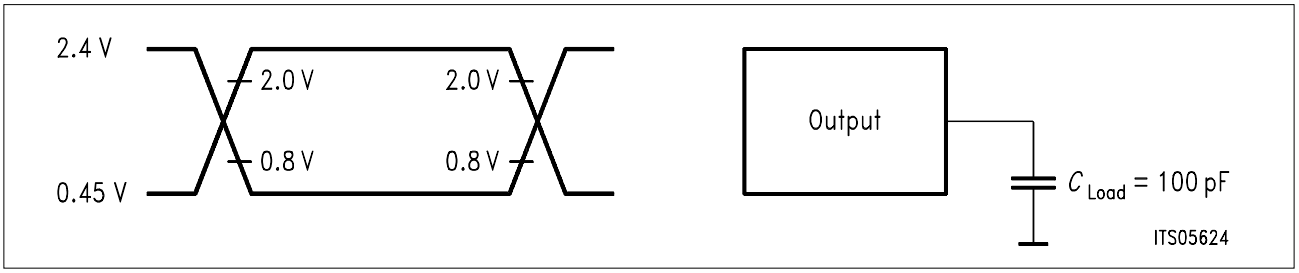


Figure 38
Input/Output Waveforms for AC-Tests

Analog Front End Input Characteristics

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
AMI-input impedance	Z_{AMI}	15			kΩ	300 – 3400 Hz
AMI-input voltage swing	V_{AMI}			19.3	mVpk	42 dB
AMI-gain	G_{AMI}			42	dB	9.55 mV at 1 kHz

Analog Front End Output Characteristics

AHO-output impedance	Z_{AHO}			2	Ω	300 – 3400 Hz
AHO-output voltage swing [1)]	V_{AHO}		3.2		Vpk	Load measured from HOP to HON
AHO-output high voltage [1)]	V_{AHOH}		3.2		Vpk	input load – 1 mA @ HOP/HON
AHO-output low voltage [1)]	V_{AHOL}		3.2		Vpk	input load + 1 mA @ HOP/HON
ALS-output impedance	Z_{ALS}			2	Ω	300 – 3400 Hz
ALS-output voltage swing [1)]	V_{ALS}		3.2		Vpk	Load measured from LSP to LSN
ALS-output high voltage [1)]	V_{ALSH}		3.08		Vpk	input load – 60 mA @ LSP/LSN
ALS-output low voltage [1)]	V_{ALSL}		3.08		Vpk	input load + 60 mA @ LSP/LSN
V_{REF} output impedance	Z_{VREF}			2	Ω	Load measured from V_{REF} to V_{SSA}
V_{REF} output voltage	V_{VREF}	2.35		2.45	V	input load – 2 mA @ V_{REF}

[1)] The maximum output voltage swing corresponds to the maximum incoming PCM-code (± 127).

Transmission Characteristics

V_{DD}/V_{DDP} = 5 V ± 5 %; $V_{SSD}/V_{SSA}/V_{SSP}$ = 0 V; T_A = 0 to 70 ˚C

Parameter	Limit Values		Unit	Test Condition
	min.	max.		
Attenuation Distortion @ 0 dBmO	0 – 0.25 – 0.25 – 0.25 – 0.25 0	 0.25 0.45 0.9 	dB dB dB dB dB dB	< 200 Hz 200 – 300 Hz 300 – 2400 Hz 2400 – 3000 Hz 3000 – 3400 Hz > 3400 Hz
Out-of-band signals		 – 35 – 45 – 35 – 40	 dB dB dB dB	receive: 4.6 kHz 8.0 kHz transmit: 4.6 kHz 8.0 kHz
Group delay distortion @ 0 dBmO [1]		750 380 130 750	µs µs µs µs	500 – 600 Hz 600 – 1000 Hz 1000 – 2600 Hz 2600 – 2800 Hz
Signal-to-total distortion (method 2)	35 29 24		dB dB dB	0 to – 30 dB – 40 dB – 45 dB
Gain tracking (method 2) @ – 10 dBmO	– 0.3 – 0.6 – 1.6	0.3 0.6 1.6	dB dB dB	3 to – 40 dB – 40 to – 50 dB – 50 to – 55 dB
Idle-channel noise		– 75 – 66	dBmO dBmO	receive (A-Law; Psoph.) transmit (A-Law; Psoph.)
Cross-talk		– 66	dB	Reference: 0 dBmO
Programmable AFE gain	– 0.5 – 1.0	0.5 1.0	dB dB	step accuracy overall accuracy
Overall programming range (with specified transmission characteristics)	 – 21.5 – 21.5 0 0	 11.5 2.5 42 24	 dB dB dB dB	Receive: loudspeaker earpiece Transmit: differential inputs single ended input

[1] Delay measurements include delays through the A/D and D/A with all features filters FX, GX, FR and GR disabled.

IOM®-2 Bus Switching Characteristics

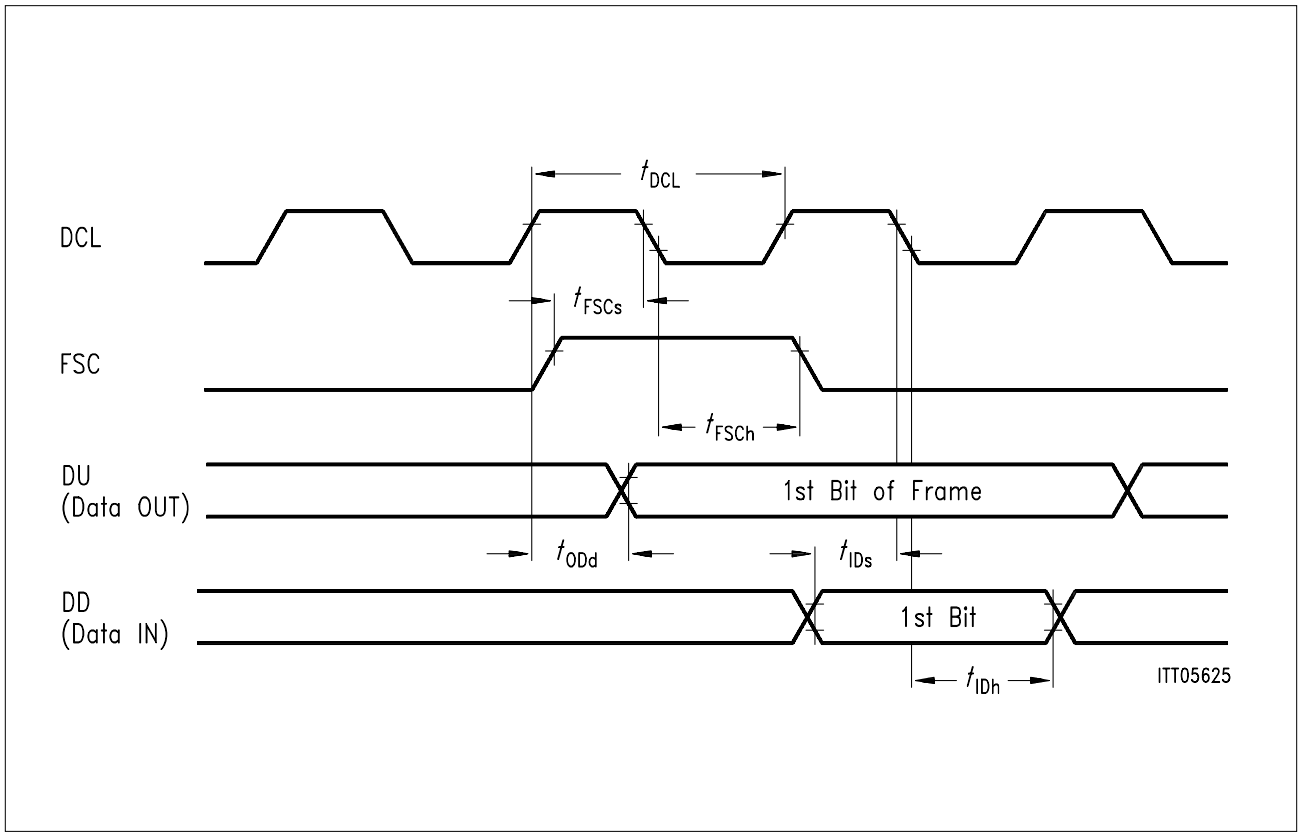


Figure 39
IOM®-2 Bus Timing Diagram

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
DCL-clock period [1]	t_{DCL}		651		ns
DCL-clock period [2]	t_{DCL}		244		ns
DCL-duty cycle		30	50	70	%
FSC-period	t_{FSC}		125		µs
FSC-setup time	t_{FSCs}	70			ns
FSC-hold time	t_{FSCh}	40			ns
DD-data-in setup time	t_{IDs}	50			ns
DD-data-in hold time	t_{IDh}	50			ns
DU-data-out delay	t_{ODd}			150	ns

1) 768 kbit/s (IOM-2 TE-Mode); max. jitter of ± 160 ns once in FSC-period.
2) 2048 kbit/s (IOM-2 Non-TE-Mode)

PCI-Switching Characteristics (IOM®-2 TE-Mode)

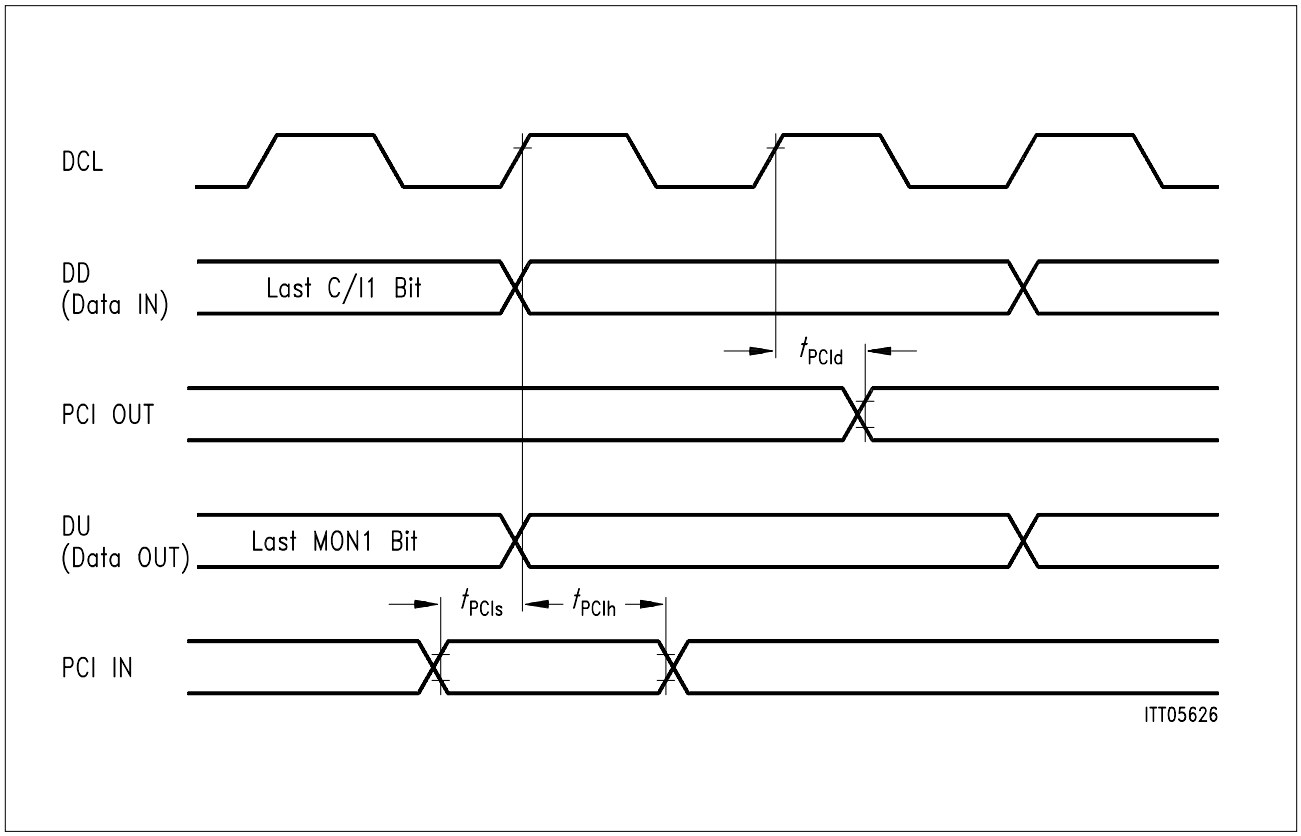


Figure 40
IOM®-2 Bus Timing Diagram (TE-Mode)

Parameter	Symbol	Limit Values		Unit
		min.	max.	
PCI-data-out delay	t_{PCld}		350	ns
PCI-data-in setup time	t_{PCIs}	50		ns
PCI-data-in hold time	t_{PCIh}	100		ns

SCI-Switching Characteristics

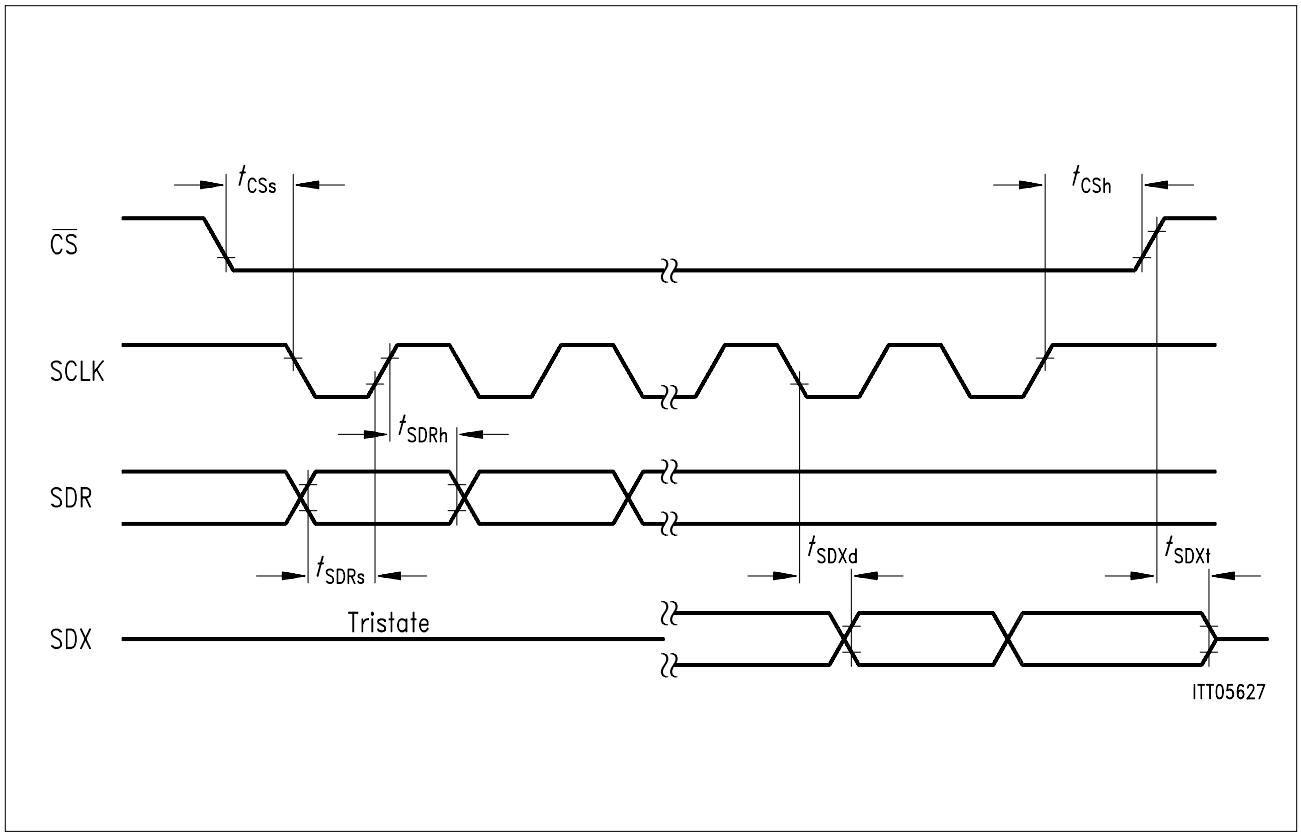


Figure 41
SCI-Switching Timing Diagram

Parameter	Symbol	Limit Values		Unit
		min.	max.	
SCLK-frequency	f_{SCLK}		2048	kHz
Chip Select setup time	t_{CSs}	0		ns
Chip Select hold time	t_{CSh}	0		ns
SDR-setup time	t_{SDRs}	50		ns
SDR-hold time	t_{SDRh}	50		ns
SDX-data-out delay	t_{SDXd}		150	ns
SDX $\overline{CS}$ high to tristate	t_{SDXt}		30	ns

SDI-Switching Characteristics

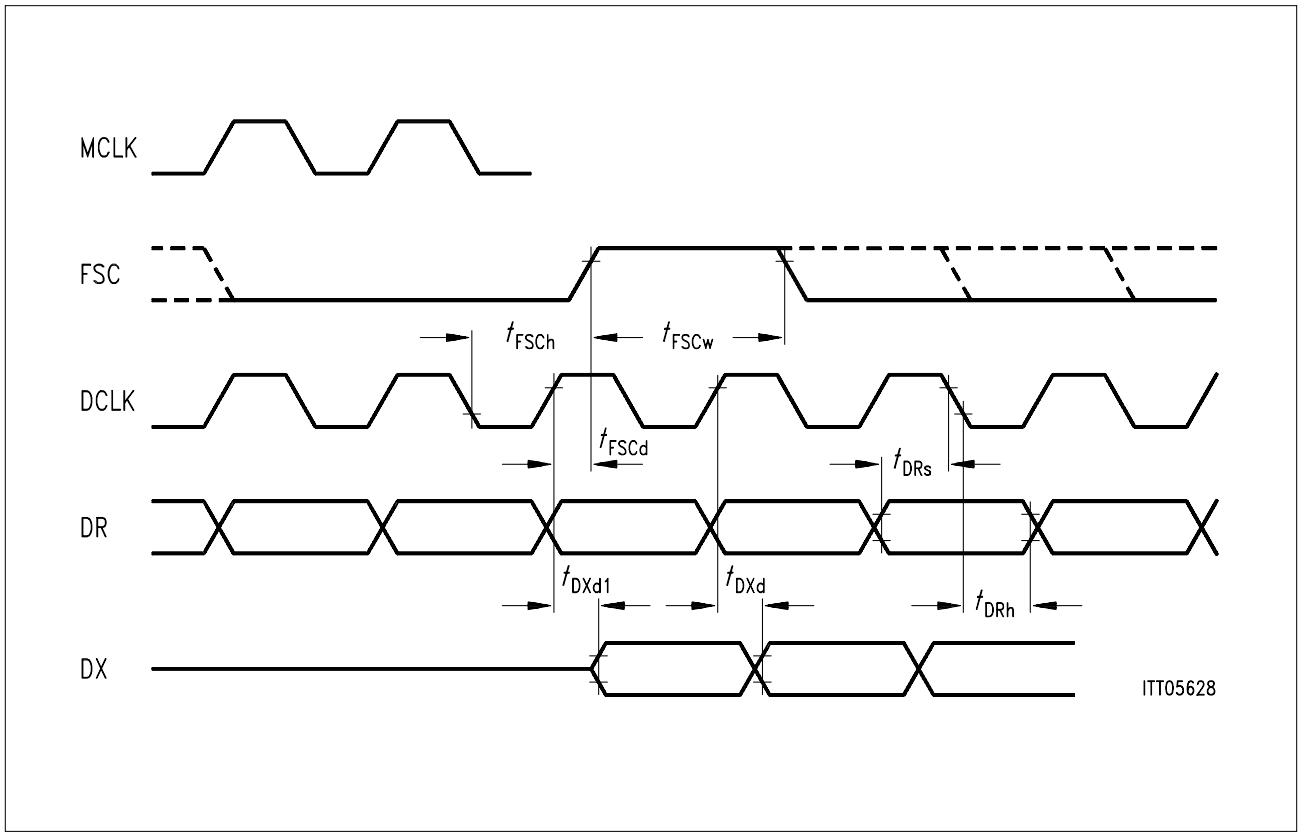


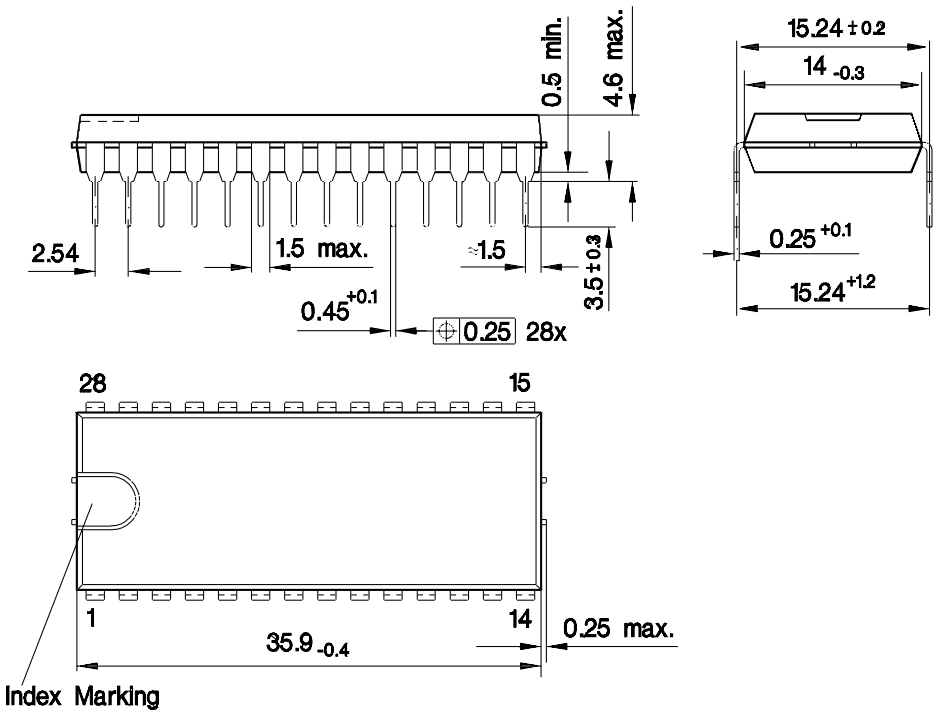
Figure 42
SDI-Switching Timing Diagram

Parameter	Symbol	Limit Values		Unit
		min.	max.	
MCLK-frequency	f_{MCLK}	512	4096	kHz
DCLK-frequency	f_{DCLK}	64	4096	kHz
FSC-pulse width	t_{FSCw}	40		ns
FSC-hold time from DCLK low	t_{FSCh}	30		ns
FSC-delay time	t_{FSCd}		30	ns
DR-setup time	t_{DRs}	50		ns
DR-hold time	t_{DRh}	50		ns
DX-data-out delay (t_{FSCd} < 0 ns)	t_{DXd1}		80	ns
DX-data-out delay ($t_{FSCd} \geq 0$ ns)	t_{DXd1}		80 + t_{FSCd}	ns
DX-data-out delay	t_{DXd}		80	ns

6 Package Outlines

Plastic Package, P-DIP-28

(Dual-in-Line)

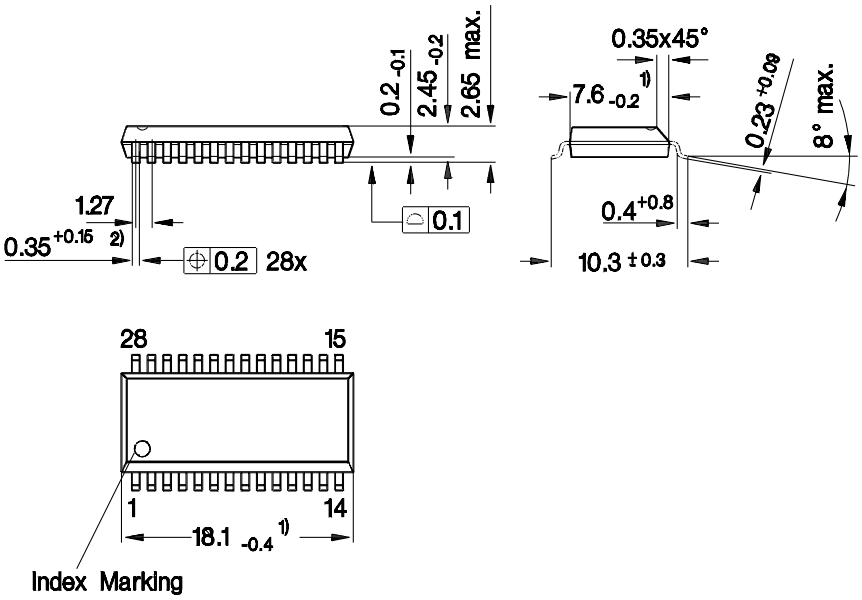


Sorts of Packing

Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”

Dimensions in mm

Plastic Package, P-DSO-28 (SMD)
(Dual Small Outline)



1) Does not include plastic or metal protrusion of 0.15 max. per side
2) Does not include dambar protrusion

GPS05123

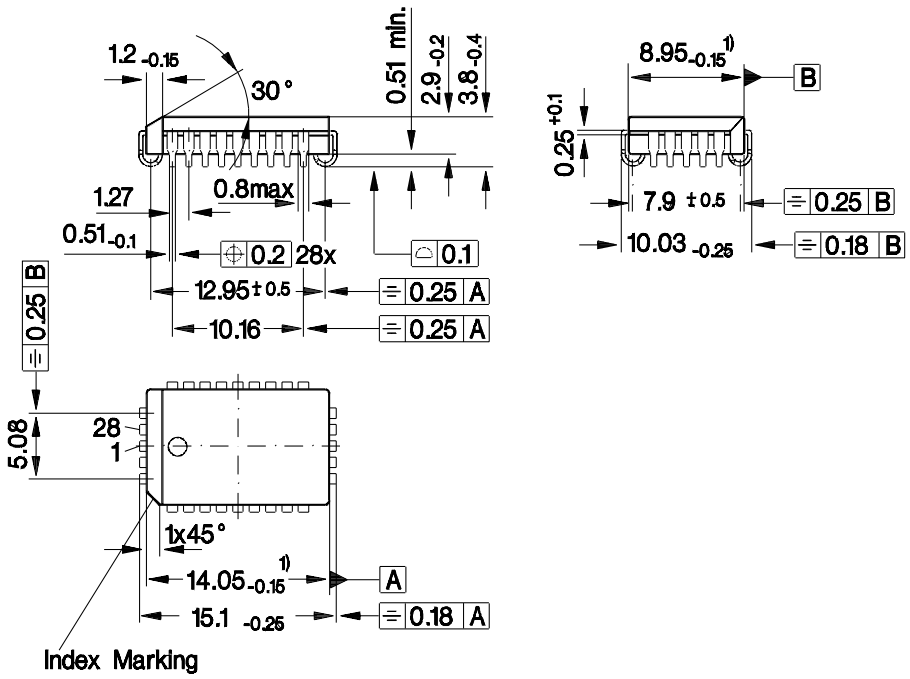
Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”

SMD = Surface Mounted Device

Dimensions in mm

Plastic Package, P-LCC-28-1 (R) (SMD)

(Plastic Leaded Chip Carrier)



1) Does not include plastic or metal protrusion of 0.15 max. per side

GPL05018

Sorts of Packing

Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”

SMD = Surface Mounted Device

Dimensions in mm

Application Notes

Vakat

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Vakat

Introduction

The Siemens ARCOFI®-SP PSB 2163 is an Audio, Ringing, CODEC, Filter like the ARCOFI® PSB 2160, but with additional integrated, enhanced speakerphone features, which has been designed to save space, development costs, and time in any application of digital terminal equipment (TE) featuring voice transmission, i.e. from the low-feature telephone to the high-comfort telephone and the multifunctional terminal.

The present document has been conceived to help the digital TE-designer to take best advantage of all the ARCOFI-SP-features.

This chapter consists of the application notes available on the ARCOFI-SP PSB 2163 as well as a short description of the hardware and software tools developed, to give the ARCOFI-SP user a good understanding of the component more quickly.

The present document does not replace the “ARCOFI-SP Technical Manual”; it is to be used together with it.

Vakat

The Speakerphone Implementation

Vakat

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About this Application Note

The intention of this application note is to give a thorough understanding of the speakerphone implementation of the ARCOFI-SP. After introducing the general aspects of speakerphones and the related problems (chapter 1) the ARCOFI-SP and all its parameters are described (**chapter 2**). In **chapter 3** practical aspects are discussed and an example set of coefficients is given.

In the application note, the term "telephone" is used to describe the particular hardware, the ARCOFI-SP is used for. Nevertheless, the ARCOFI-SP fits to a variety of applications, like intercoms, videoconferencing systems etc.

Throughout this application note, registers or CRAM coefficients are written in bold and capital letters (**See “Notation and Coefficients” on page 138**).

Some ARCOFI-SP parameters are related to the maximum PCM value. In the application note A-law coding is assumed, therefore this value is written as 3.14 dBm0. For μ-law coding 3.17 dBm0 would be correct.

1 General Aspects of Speakerphone Realizations

1.1 Introduction

Plain telephony suffers from the fact of being tied to a telephone set, and even mobile telephony requires at least a handset to be held. To move freely for e.g. fetching some documents needed during a discussion or when phoning while driving a car, the speakerphone support is an important feature of telephone terminals.

High-feature telephones are mainly to be found as terminal devices in private exchanges (PABX) and central offices (CO) to offer enhanced comfort compared to plain analog terminals. In an Integrated Services Digital Network (ISDN), which opens access to a lot of completely new services in the large list of terminal features, the speakerphone support ranges on top and may be considered as a standard feature of comfort terminals. But even high quality analog terminals take more and more advantage of digital signal processing techniques and offer speakerphone support.

In contrast to using a handset which by its construction precludes feedback from loudspeaker to microphone, the speakerphone feature opens such bypasses. It involves much technical expense to cope with these various and time-varying couplings at a reasonable performance level.

In general, today´s speakerphone realizations are based on a half-duplex transmission mode which breaks the existing acoustic coupling between the receiver loudspeaker and the speakerphone microphone by amplifying just one path (receive or transmit) while the other one is attenuated.

Former realizations required a lot of discrete components to achieve a satisfying quality, where "satisfying" is still subject to a rather personal sensation. Contemporary solutions consist of an integrated circuit with still about 40 passive external components instead. They reach an acceptable quality, but optimization is mainly empirical and tuning the circuitry to the particular preferences of the user is impossible.

Controlled loudhearing, also called monitoring, is a valuable and very comfortable feature, since it allows other people to follow a discussion running with a remote phone partner. With the ARCOFI-SP, loudhearing can be regarded as a particular speakerphone mode with reduced attenuation while using the handset microphone.

The digital realization of the speakerphone feature greatly simplifies the optimization and tuning procedure by using the efficiency of a digital signal processor. The ARCOFI-SP PSB 2163 incorporates the necessary computing capacity to realize a speakerphone of superior performance without any external components. In the following sections the typical coupling problems and technical solutions will be discussed, before in the second part of this application note the concrete realization with the PSB 2163 is described in detail.

1.2 Speakerphone Fundamentals

In a traditional telephone connection that uses handsets on both sides there is almost a full duplex conversation (both subscribers can talk and listen at one and the same time), and the gains required for the microphone and the earpiece are moderate.

As soon as people start to enjoy the handsfree telephony -moving free in the room, more people listening and talking at the same time- the problems come up. The gain required for amplifying microphone and loudspeaker signals is much higher and there are more ways for the received signal to reach the microphone again than there are in a handset. Unfortunately, any system at which an output signal can reach the input again starts to oscillate if the loop gain increases 1 (and if a certain phase angle relation is fulfilled). Especially the far-end echoes may be very annoying as they cause a delayed perception of one's own speech.

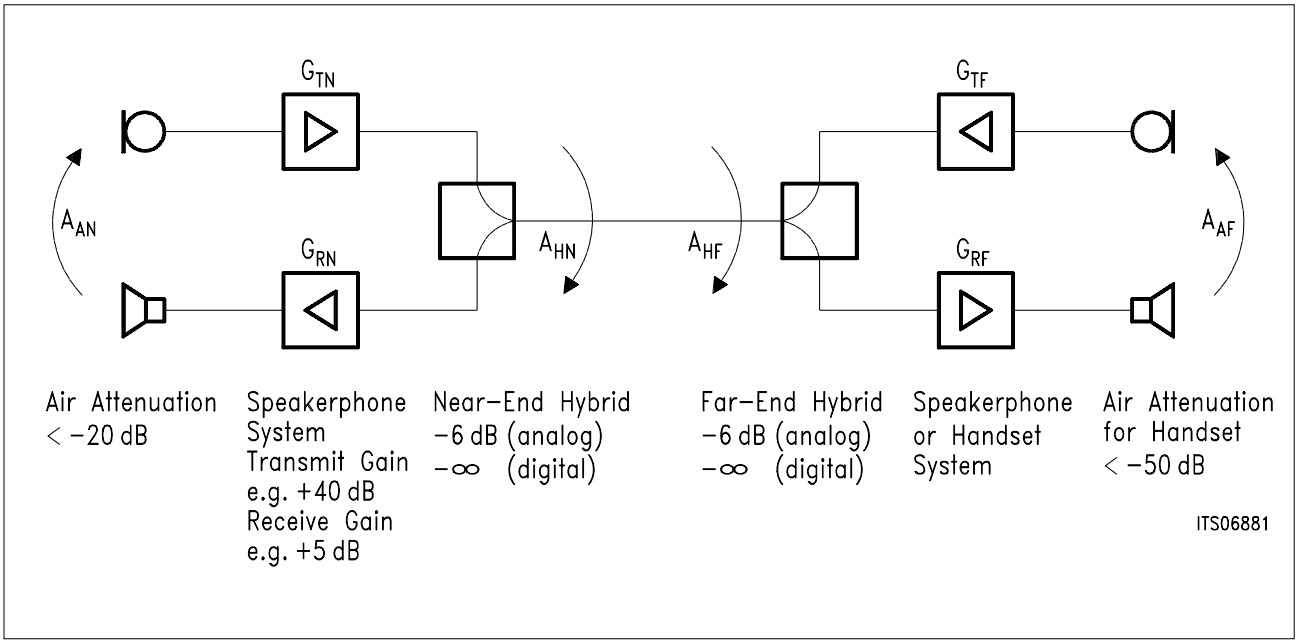

Figure 1
Coupling Problems Introduced by Speakerphones

The system shown in **figure 1** should help to understand the different sources of echo and delay. The speakerphone system on the left side is connected over a network to either a handset or a speakerphone terminal at the far end. Amplifications are given in dB with a positive sign, attenuation is marked with a negative sign. In a pure digital world there is no 2/4-wire conversation, therefore the whole system is stable if the following equation holds during conversation (not considering the delays):

$G_{TN} + G_{RN} + A_{AN} + G_{TF} + G_{RF} + A_{AF} < 0$ dB.

With reflections inside the network or with analog lines the situation becomes more difficult and A_{HN}, A_{HF} must be considered as follows:

$G_{TN} + G_{RN} + A_{AN} + [A_{HN} || A_{HF} || (G_{TF} + G_{RF} + A_{AF})] < 0$ dB.

Since there are a lot of possibilities for the signal to loop back in a speakerphone system, efforts must be taken to keep the loop gain well below 0dB and to avoid regeneration. Much technical expense is required to handle the different effects that occur in such a system.

1.3 Today’s Speakerphone Realizations

Basically, it has to be distinguished between two different speakerphone realizations, between the full-duplex and the half-duplex approach. A full-duplex system employs a two-way transmission, whereas with a half-duplex system only a one-way transmission is available at a time.

Full-Duplex

A full-duplex system is as comfortable as a round-table discussion, because the interlocutors can talk and listen at the same time. The today's realizations like the compander process or the echo cancellation cause enormous system costs and are very critical, because in case of echo variations they react in a rather unpredictable manner. Additionally, perceptible delays introduced by long calculation times due to the numeric algorithm involved are annoying.

For this application note these remarks should be sufficient; more information can be found in literature.

Half-Duplex

With a half-duplex system signal transmission is permitted only in one direction at any time thus breaking the loop. The half-duplex process is stable under all circumstances, and costs of such systems are remarkably lower than of full-duplex ones. A certain discussion discipline, however, is required. Analog and digital realizations of the half-duplex system are available in form of integrated circuits.

The ARCOFI-SP contains a powerful digital implementation of an enhanced half-duplex speakerphone system with an adjustable amount of switchable attenuation, therefore the performance is somewhere between a full- and a half-duplex realization. The value of the additional attenuation is programmable, and it is always switched into the non-active path.

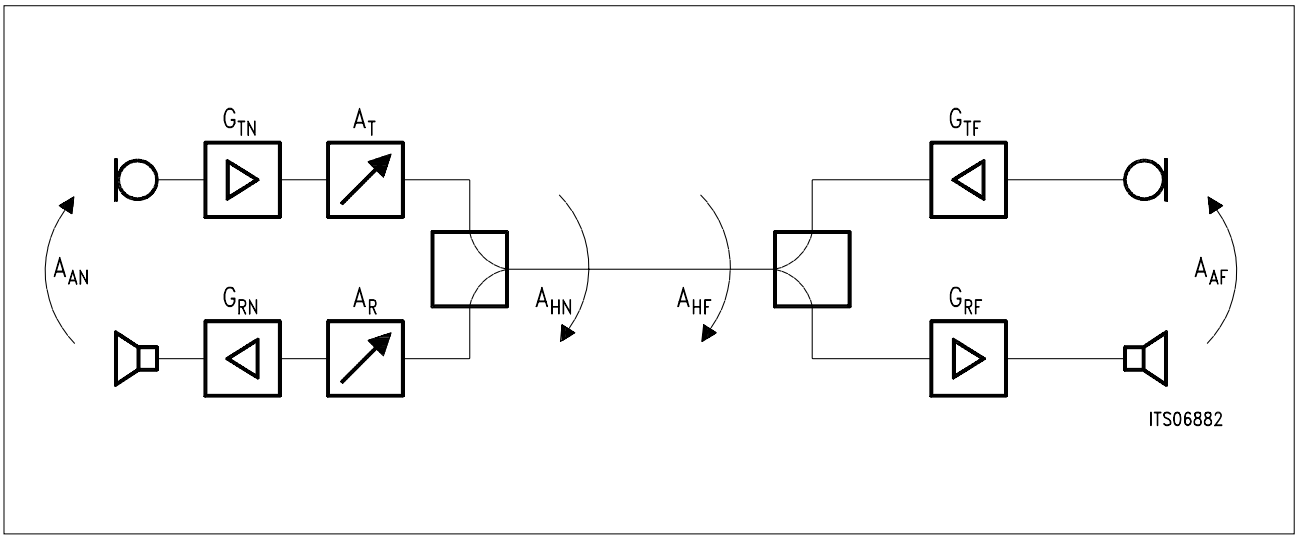

Figure 2
Half-Duplex Speakerphone with Switchable Attenuation A_R and A_T

1.4 Discussion of Practical Realizations of Half-Duplex Systems

To realize a high-quality half-duplex speakerphone, a sophisticated control mechanism is necessary to decide where and when to use additional attenuation. This paragraph explains the requirements to be fulfilled by such a control logic.

The switching between the transmit and receive direction must happen as discretely as possible. This leads to the following requirements of the switching algorithm:

- Voice signals have to be recognized doubtless even if the background noise exceeds the speech signals
- Ambient noise must not block the speakerphone switching process
- Speech direction switching must occur without any delay
- During a one-direction talk, the system must not switch prematurely
- Each speaker should be able to interrupt the other one

These specifications are partly contradictory, so that compromises have to be found. Thus judging the speakerphone switching performance is rather subjective.

Transients

To get a satisfying switching performance, experience shows, that losses of the loop should be kept as low as possible[1)]. Ideally, a loss of about 10 - 20 dB should be sufficient and in reality this loss is not perceptible very well, so that a pseudo full-duplex character can be achieved. In contrast, a switched attenuation larger than 40 dB gives the feeling of speaking into a hole, like a dead line. In general, it is a fact that the lower the volume of the speech comes out of the loudspeaker, the lower the inserted attenuation may be. Of course, to the singing threshold there should always be a certain reserve to avoid instability and annoying echoes.

For the switching control two speech detectors are necessary, one in the transmit path and one in the receive branch. Both have to distinguish completely separately between speech activity and (background) noise. The direction exhibiting a better S/N ratio should normally be blocked and the path with a poorer S/N ratio should normally be activated. Thus the path with a higher noise is normally transparent, and hence it will not be necessary to have a large level difference between noise and speech. On the other hand, in the path with a better S/N it is not difficult to discriminate between speech bursts and noise edges.

A volume control must be arranged in such a way that, when turned down, it will reduce the loss switched in both paths by the same amount. This guarantees that only the minimum of loss is switched, which yields a comfortable switching feeling.

The sum of build-up and attack times should be very short (around 10 ms), the shorter the better. The build-up time is the delay associated with the detection of a rising voice signal, and the attack time (analogous release time) is the switching time required after having detected speech. The sum of decay time (delay while detecting a decreasing voice signal) and release time must be relatively long (150 ms)[2)]. This prevents clipping and does not delay mode switching in a way that it becomes noticeable.

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1 A. Busla: "Fundamental Considerations in the Design of a Voice-Switched Speakerphone", The Bell System Technical Journal; Vol. XXXIX, March 1969, Number 2

2 A. Busla: "Fundamental Considerations in the Design of a Voice-Switched Speakerphone", The Bell System Technical Journal; Vol. XXXIX, March 1969, Number 2

1.5 Steady-State Problems and Transient Effects

Steady-state problems arise from the speakerphone system being stable either in transmit mode or in receive mode. These problems are:

- *Singing*: occurs if the loss switched within the loop is too small (refer to **figure 2**)
- *Transmit Blocking*: the system remains in receive mode when it should have switched to transmit mode; this can be due to large noise in the receive path or due to a small A_{HN} or A_{HF}
- *Receive Blocking*: due to room noise or due to a strong coupling between loudspeaker and microphone (refer to page 135) the circuit is prevented to switch from transmit to receive mode

Transient effects occur during switching from one mode to another; these are:

- *Initial Clipping*: loss of the first syllables is caused by the operational time of the speech detector and subsequent mode switching; it is influenced also by the sensitivity of the speech detectors
- *Final Clipping*: the loss of the terminating parts of words is caused by the hangover time
- The *Starting Echo* can be described as follows: speech signals are coming via the line to the speakerphone system. The receive path is not attenuated, and there is a large level enhancement due to the loudspeaker-microphone coupling. As a result, the level at the transmit speech detector input is greater than that at the receive detector. Thus when the non-speakerphone side starts speaking, the transmit speech detector can recognize speech earlier than the receive detector. This may result in switching to the transmit side (mode switching) and lead to some instability at speech onset.
- Similarly, the *end echo* can cause immediate mode switching. During a speech interruption or pause in receive direction, the speakerphone system switches to transmit mode. The reason is, that due to acoustic delays speech may still be effective at the transmit speech detector when the receive speech detector has already recognized "end of speech".

Additional problems arise from background noise and from speech collision during short breaks in the flow of words or due to low-energy syllables. Also the varying coupling of the speaker to the microphone may cause trouble at the transmit side.

1.6 Optimization of Half-Duplex Speakerphone Systems

A real speakerphone telephone set is a rather complex unit. Its performance is affected both by electrical and acoustical couplings, the latter ones are set up via the surrounding air and the telephone case itself. Arriving at a true optimum performance is only possible if all trimming resources are exhausted.

The minimization of both, the acoustical feedbacks and the electrical couplings is indispensable.

The minimization of both the acoustical feedbacks and the electrical couplings must be done by acoustical as well as by electrical means. The gains made acoustically must not be realized by programming the speakerphone hardware. It is not possible to optimize a speakerphone system just by using only one method, acoustical or electrical. Starting developing a speakerphone system is most effective in searching first for an economical partitioning between both methods: only a sufficient acoustical optimization provides a sound basis for completing the optimization electrically. Theoretically it is possible to eliminate the near-end acoustical couplings almost completely by acoustical means, so that only the hybrid couplings have to be controlled by loss switching.

Acoustical Optimizations

- Mechanical loop-back based on resonances of the telephone case (seismic coupling): shock-proof mounting of the microphone and implementing some extra mounting "towers" for obtaining a resonant-proof telephone case. Using soft materials for fixing the microphone and loudspeaker to the telephone case.
- Acoustic loop-back via air inside the case: acoustic separation of critical case parts. Insertion of additional walls inside the telephone case to block coupling via air.
- Acoustic loop-back due to the air external to the case: orienting the loudspeaker and the microphone in different directions decouples effectively. An optimum is given, if the lobe patterns of loudspeaker and microphone take an angle of 90°.
- "Hollow Barrel" effect: placing the loudspeaker on the top towards the room and the microphone near the bottom of the case. Placing the microphone into tubes, however, generates unfavorable effects like reverberation.
- Maximum effectivity of the transmit amplification: the larger the opening on the telephone case, the larger is the sound pressure at the microphone. Placing the microphone in an angle of 45° to the horizontal towards the desk makes the microphone receive the direct acoustical pressure and the indirect sound pressure reflected at the desk. This results in an additional amplification of 4 - 6 dB.
- Acoustical feedback at the far-end talker side: this feedback is very small if a handset is used. The attenuation via air due to the small amplifications in the earpiece and handset microphone paths is about 50 dB, so that it can be neglected. If the far-end

side uses also a speakerphone system, an additional loss of 3 dB is required. This loss has always to be provided because it must be admitted that a speakerphone device is connected at the far-end side.

Electrical Feedbacks

There are various electrical couplings which cause attenuated echoes with and without delays. Referring to **figure 1**, couplings exist in the hybrid where the 4/2-wire conversion is realized, and at the interfaces between analog and digital transmission lines.

External to the telephone case in pure digital connections electrical feedbacks do not exist, but large delays can result from digital processing in the exchanges. Additional delays may be introduced e.g. by an intercontinental link or by links via satellites. Though these delays are very annoying, it is not possible to eliminate them. Moreover, in every speakerphone they can generate enormous problems.

At the near-end hybrid (A_{HN}) the attenuation of the echo varies from one link to another in a range between 6 - 20 dB. In the worst case it can decrease to just 6 dB. Due to the relative small distance between the speakerphone system and the near-end hybrid, the delay is negligible.

At the far-end hybrid the attenuation (A_{HF}) of the generated echo can also reach 6 dB, but via the analog line inserted, additional loss may be introduced. The still more annoying effect is that the echo returns to the loudspeaker with some non-negligible delay.

2 Speakerphone with the PSB 2163

2.1 Introduction

From the general description of speakerphone problems it can be seen that designing and tuning a speakerphone system is a tricky task. A digital approach to solve the problems not only makes the design independent of productional variations and of environmental conditions, but also offers easy tuning to the desired response. Finally, a single chip contains the complete circuitry, therefore no additional external components are required. For the application of the speakerphone and controlled loudhearing features all these necessary hard- and software can be found inside the ARCOFI-SP PSB 2163.

A substantial feature of the ARCOFI-SP is to provide means for minimizing feedback in electrical loops and to compensate for acoustical couplings. Therefore, the ARCOFI-SP offers a lot of parameters which are set by software programming. No further external components or trimming are required.

Note: Although the ARCOFI-SP allows the control of all kinds of feedback, it is strongly recommended to have the majority of the acoustic couplings minimized by an optimal design of the telephone case. The better the acoustic design, the better the speakerphone will be.

The operational functions are realized with a signal processor where all necessary parameters are parameterized. This technique offers a high level of flexibility and reproducibility. An enormous advantage is the reduction of the optimization time. It is possible to optimize the speakerphone system using just one link. The iterated procedure of "building-up a line $\rightarrow$ testing $\rightarrow$ deactivating the link $\rightarrow$ opening the telephone case $\rightarrow$ resoldering some RC-elements $\rightarrow$ closing the case" is reduced to a comfortable computer session, focusing on the real work: the optimization of the switching behavior.

As the signal flow graph of the ARCOFI-SP shows (see **figure 3**), the complete operational algorithm is situated between the analog front end and the compression/ expansion logic. This offers the advantage that the speakerphone function is independent of any country specific transmission characteristics. Thus telephone sets can be optimized and adjusted to the particular geometrical and acoustic environment. Furthermore, it is possible to connect different microphones to the speakerphone block, so that controlled loudhearing may also be easily established.

The main features of the speakerphone signal processing are:

- Two separate attenuation stages, one for the transmit and one for the receive path, controlled by an intelligent control logic, which processes information about the current and the past speech activities;
- Two point speech detection; one speech detector for each path, with separate time constants and separately programmable for signal and noise;
- Control of the acoustic echo performed by a fully programmable speech comparator;
- Control of the far-end echo performed by a fully programmable comparator for the line echo;
- Background noise monitoring to eliminate continuous background noise from decision.

The following chapters describe how the speakerphone implementation works and give detailed hints about the values to be used for the different parameters. After discussion of the block-diagram of the speakerphone, the speech detectors and the speech comparators are described.

2.2 Notation and Coefficients

The ARCOFI-SP can be programmed with so called COP sequences ("Coefficient Operation") and SOP sequences ("Status Operation"). Throughout this application note, bold and uppercase abbreviations refer to CRAM coefficients to be programmed with COP sequences (example: parameter **ATT**). Single bits or bit combinations to be set in one of the registers are referred to as <Register>.<Bit> (example: **GCR.SP**). These bits are always programmed with SOP sequences. For a description of all ARCOFI-SP registers, please refer to the user's manual.

The ARCOFI-SP offers a lot of CRAM coefficients which can be programmed. The hex-value that corresponds to a certain physical value (e.g. $B1_H\,49_H$ representing 0dB amplification in the GX stage) can be evaluated very comfortably with the ARCOS-SP software or with the ARCOS-SP PLUS software (SIPO 2163) by pressing the right mouse button. The ARCOS-SP PLUS software offers additionally hardware access to program the ARCOFI-SP in different environments. The CRAM coefficients are not completely documented in the user's manual.

2.3 Signal Flow Graphs

Figure 3 shows the whole signal processor part of the ARCOFI-SP which interfaces to the analog front end (AFE) on the left side.

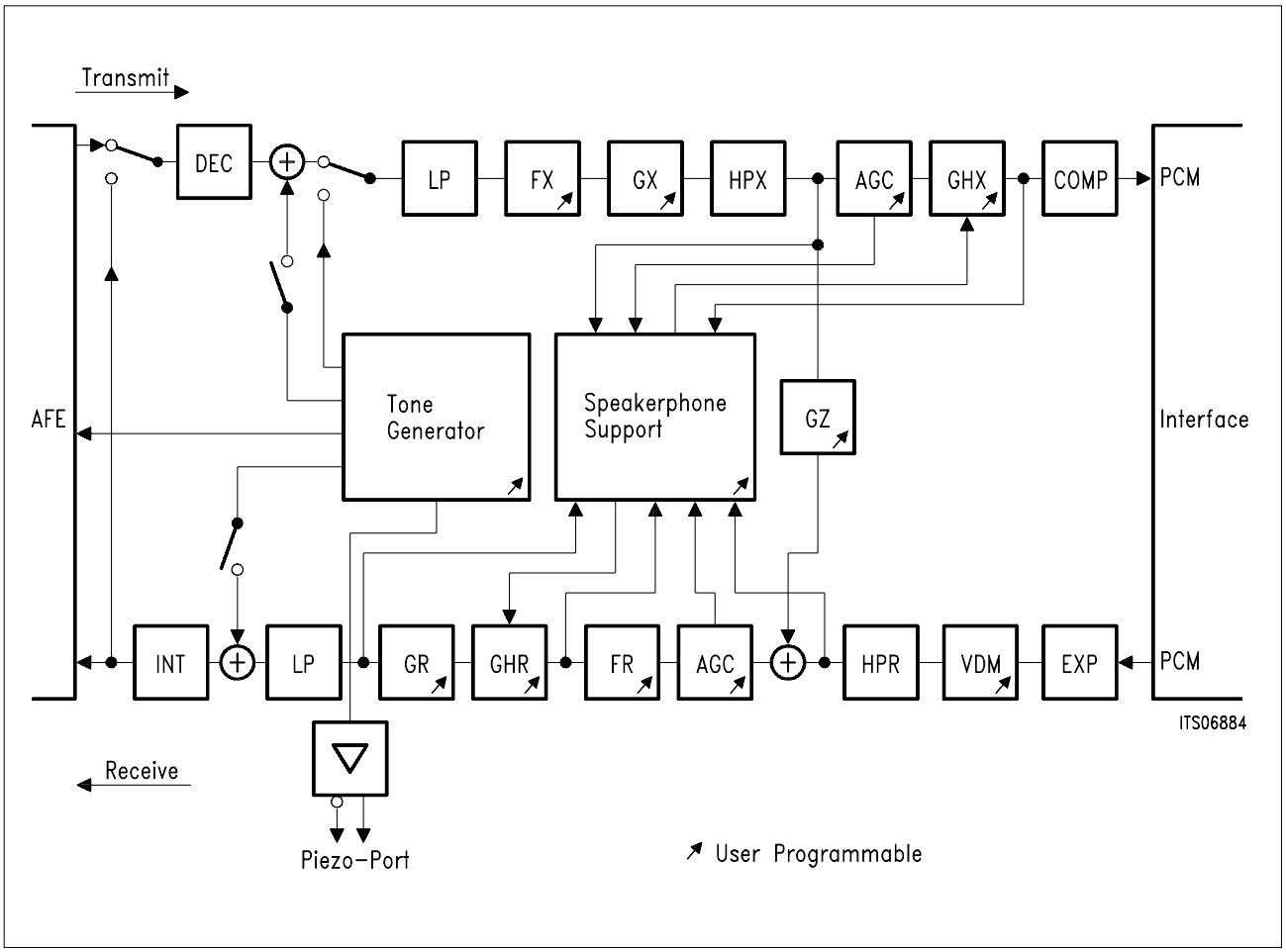

Figure 3
Signal Flow Graph of the ARCOFI-SP Signal Processor (ASP)

Figure 4 gives an general idea of all signal processing blocks important for understanding the speakerphone function. Some of the blocks like AGCX, AGCR (automatic gain stages) and the attenuation stages GHX, GHR can be found directly in the signal flow graph in **figure 3**. Others, like the two speech detectors SD and the speech comparators SCAE, SCLE are located inside the block labeled "speakerphone support" in **figure 3**.

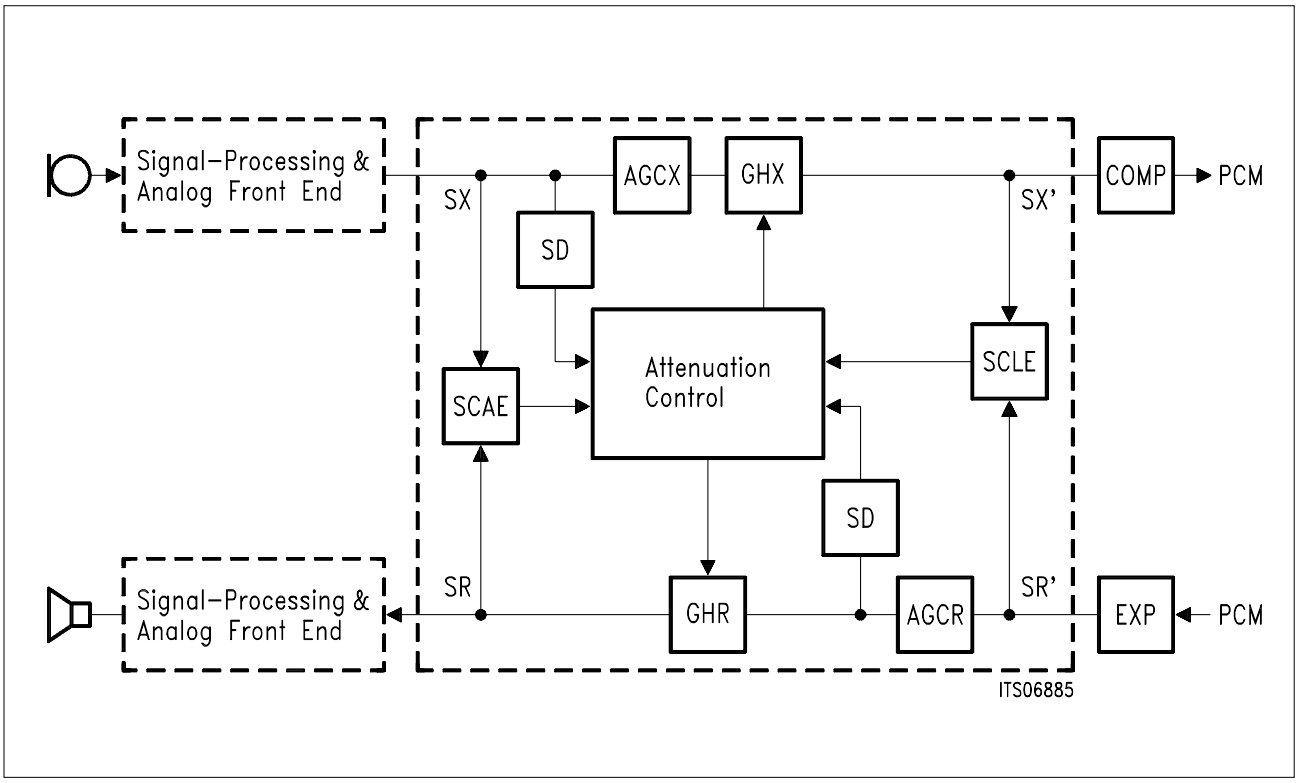

Figure 4
Signal Flow Graph of the Whole Speakerphone Support Block

2.4 Basics about the Speakerphone Algorithm

This chapter explains the interaction of all the blocks seen in **figure 4**, and the three different steady-state modes of the speakerphone. The inside of the speech detectors (SD) and the speech comparators (SCAE, SCLE) including all programmable parameters is explained in the following chapters.

Basically, we have to distinguish three steady-state modes with dynamic transitions between them:

Table 1
Steady-State Modes when the Speakerphone is Active

Mode	Attenuation in GHX-stage	Attenuation in GHR-stage
TRANSMIT	yes, determined by **ATT**	no, 0dB
RECEIVE	no, 0dB	yes, determined by **ATT**
IDLE	yes, **ATT** / 2	yes, **ATT** / 2

The task of the attenuation control unit (see **figure 4**) is to decide which mode should be effective. The information needed for decision is delivered by the two speech detectors SD and the two speech comparators SCAE, SCLE. Assume the automatic gain control stages AGCX and AGCR as switched off.

The speech detectors are able to distinguish between speech signals and any kind of noise and inform the attenuation control unit about the presence or absence of speech in the receive and the transmit path.

Assume the speakerphone is in receive mode, therefore outgoing digital signals are attenuated in the GHX stage, incoming signals from the PCM interface are reproduced by the loudspeaker with no attenuation inserted in the GHR stage. Of course the speech detector in receive direction has recognized speech - otherwise the receive mode would not be active. At the output of the microphone amplifier there is a signal mixture consisting of coupled sound coming from the loudspeaker and from reflections in the room. But also speech activity taking place at the near end in front of the speakerphone will appear in the transmit path (which is still attenuated, if the ARCOFI-SP is in receive mode). The task of the attenuation control unit is now to distinguish between unwanted signals resulting from coupling, echoes etc. and true speech activity. True speech activity has to make the ARCOFI-SP switch into transmit mode. For this purpose, first of all the speech detector in transmit direction must have recognized any speech activity. When both speech detectors have recognized speech activity, a decision must be made, which mode is to use (receive or transmit). This is done by the speech comparators, in this example by the speech comparator for the acoustic echo, SCAE. The speech comparator for the acoustic echo "knows" exactly what signal level SX must be regarded as an echo and which signal level is higher than an echo ever can be. If such a high signal level appears, and this level is a certain (programmable) amount higher than the signal level SR that is actually being received, the speech comparator will change state, therefore indicating this fact to the attenuation control unit. As a result, mode switching from receive mode to transmit mode will happen.

The same explanation applies to the mode switching from transmit mode to receive mode, but in this case not the acoustic echo must be taken into account, but the line echo resulting from delays and reflections in the telephone network is important. This echo is handled by the speech comparator for the line echo, SCLE.

A mode switching can be forced simply by speaking louder than the remote partner. How many "dBs" louder a person has to speak is programmable, but always the speech comparators have to cover the worst case echo. That means for the application, that a speakerphone system with a high acoustical coupling and with strong resonances will show a reduced speakerphone performance, since for winning the channel one always has to be louder than the signal caused by echoes and couplings. But for an appropriate designed telephone plastics (refer to chapter 1.6), a very comfortable behavior regarding mode switching is achieved.

If no speech activity is recognized by the ARCOFI-SP, the speakerphone goes into idle mode. After both speech detectors have indicated "no speech", the ARCOFI-SP remains in the previous mode for the period of time programmed by **TW.** After **TW** has passed, the quantity of switchable attenuation (in dB) is changed to the amount of half the value determined by **ATT** in both branches (see table below) with the speed given by **DS**

(decay speed in ms/dB). Therefore the transition into idle mode is very smooth and hardly noticeable.

Starting from idle mode, depending on the first speech detector recognizing speech, the device switches immediately into transmit or receive mode. The speed for this immediate mode switching is determined by the parameter **SW** (switching time).

Table 2
Parameters for Switchable Attenuation / Speed of Transitions

Parameter	Typical Value	Meaning
ATT	10...40 dB	Amount of switchable attenuation that will always be present in receive and/or transmit path (depending on mode: transmit, receive, idle).
TW	144 ms	Wait time that passes before the transition from receive or transmit mode into idle mode starts.
DS	99 ms/dB	Decay speed that determines how fast the switchable attenuation changes when going into idle mode.
SW	0.6 ms/dB	Switching time for the transition out of idle mode into transmit or receive mode or for the direct transition from receive mode into transmit mode and vice versa.

Note, that the parameters explained above are not responsible for the decision, when to change a mode. Any changes made for **TW**, **DS**, **SW** only affect the speed of the transitions between the modes and are not responsible for example for the capability of recognizing speech and switching the mode. This is handled by the speech detectors and the speech comparators.

2.5 The Speech Detector

Both speech detectors have the same structure. For almost every application the standard parameter set can be used, and there is usually no need for a change except for the parameters described in the paragraph "processing of continuous tones".

Figure 5 shows the block diagram of the speech detector with all programmable parameters. Basically, the speech detector makes use of the burst characteristic of speech, that means, every fast change in signal amplitude compared to the average signal level is recognized as speech. This is done by averaging the input signal with a low pass filter (LP2) and comparing the output signal of this low pass with the input signal itself.

Background Noise Monitor

Background noise monitoring is realized by the low pass LP2. Background noise can be regarded as approximately stationary from its averaged power. Since only a difference

between the average signal level and the instant signal level leads to speech recognition, the influence of noise on the decision is cancelled, even if the noise level exceeds the voice level.

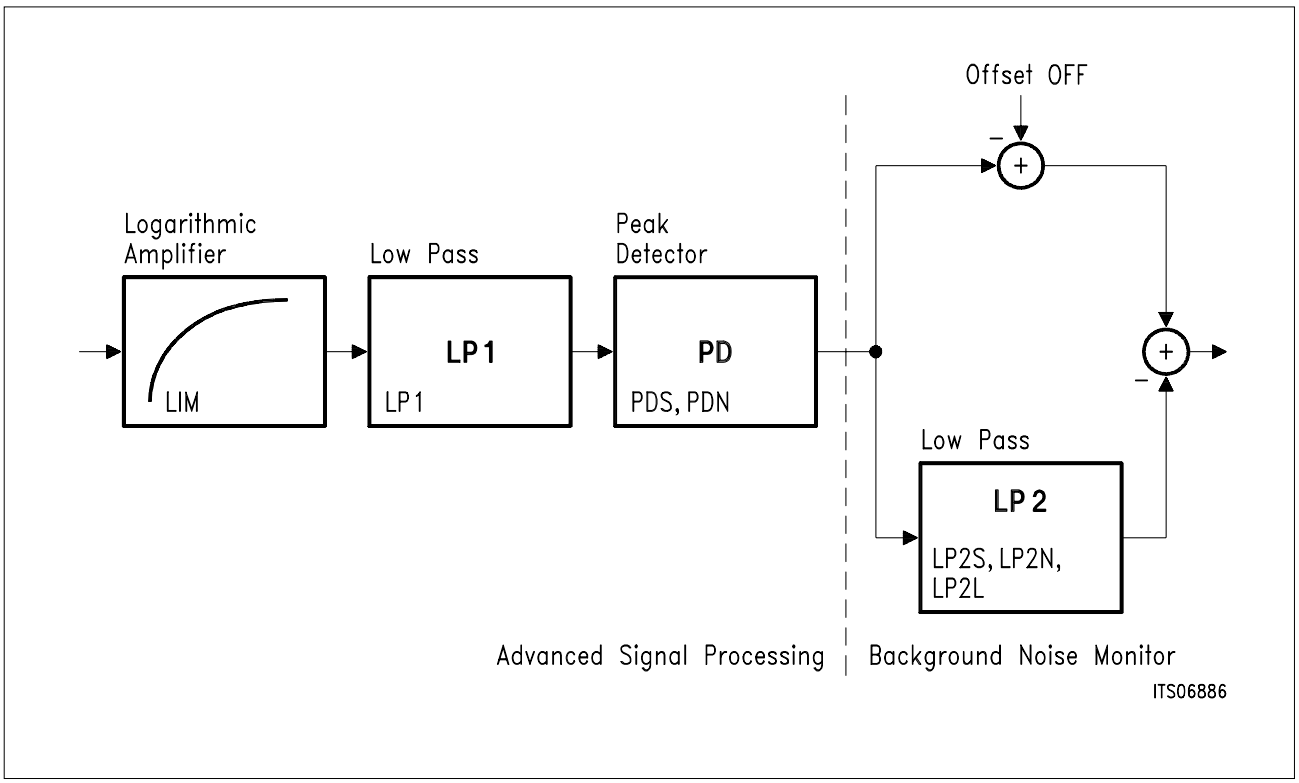

Figure 5
Block Diagram of the Speech Detector

Advanced Signal Processing

Before the signal is applied to the low pass LP2, it is preprocessed by a logarithmic amplifier, a second low pass LP1, and a peak detector.

The logarithmic amplifier compands the signal logarithmically, therefore the speech detector got a high dynamic range. With the parameter **LIM** a threshold is defined. Input signal levels that are below the threshold determined by **LIM** are not processed by the speech detector. Usually **LIM** is programmed for a threshold a few dB above the system's noise floor. Note, that **LIM** is related to the maximum PCM value, causing for example a threshold of -60dBm0 if programmed to **LIM**= – 63.1 dBm0.

The main task of low pass filter LP1 is to filter the incoming signal in a way that main spikes are eliminated. Due to the programmable time constant **LP1** it is possible to defuse as well high-energy syllables as noise edges.

The peak detector bridges the very short speech pauses during a monologue, so this time constant has to be long. Furthermore, the speech bursts are stored, so that a sure speech detection is guaranteed. But if no speech is recognized, the low pass LP2 must be discharged very quickly to the averaged noise level. In addition, the noise edges are

to be smoothed. Therefore two time constants are necessary and have to be separately programmable: **PDS** for speech and **PDN** for background noise signals. Thus "speech mode" may be detected faster and kept longer than "no speech mode" so that smaller breaks may not cause switching.

The low pass filter LP2 provides different time constants for noise (non-detected speech) and speech. It determines the average of the noise reference level. In case of background noise the level at the output of LP2 is approximately the level of the input. Due to the offset **OFF**, the comparator remains in the initial state. In case of speech, the difference of signal level between the offset branch and the LP2 branch at the comparator increases and the comparator changes state. At speech bursts, the digital signals arriving at the comparator via the offset branch change faster than those via the LP2 branch so that the comparator changes its polarity. Hence two logical levels are generated, one for speech and one for noise.

A small fade constant (**LP2N**) enables fast settling down the LP2 to the average noise level after the end of speech recognition. It is recommended to choose a large rising constant (**LP2S**) so that speech itself charges the LP2 very slowly. Generally, it is not recommended to choose an infinite **LP2S** because then approaching the noise level is disabled.

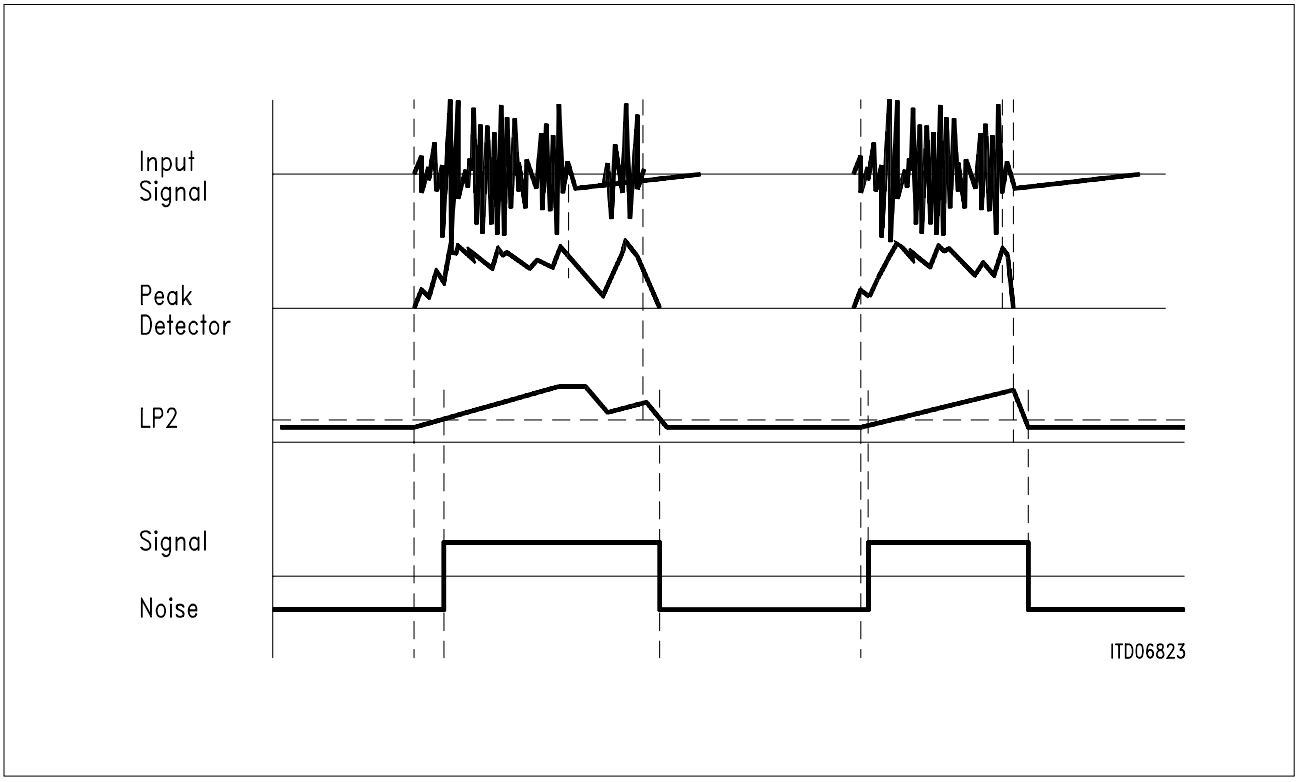

Figure 6
Example Showing the Principle of Speech Detection

The diagrams in **figure 6** graphically describe the inputs and outputs of the speech detector blocks. The result is not completely identical to the implementation in the

ARCOFI-SP, but helps to understand the function of the speech detectors. The first diagram shows the input signal in the analog form because this form is better understood. In the ARCOFI-SP this signal is delivered to the speech detector digitally. The peak detector output is the envelope of the input signal, where short pauses are bridged. The next diagram explains the task of the two branches with the offset **OFF** and LP2, respectively of the background noise monitor. In the last diagram the result of the determination of the complete speech detector can be seen.

Processing of Continuous Tones

Care has to be taken when continuous tones – e.g. signalling tones with a long duration – or "music on hold" are to be processed by the speech detector. Any long lasting signal that does not show the typical burst characteristic like speech will lead to a "no speech" decision of the speech detector after the time constant **LP2S** has passed. This is a necessary function for avoiding background noise to be recognized as speech. With the help of the parameter **LP2L** the charging of the low pass LP2 can be limited to a certain level, therefore a continuous signal that is greater than this limitation plus the offset **OFF** will always be recognized as speech. This feature allows to detect any well leveled signalling tone. **Figure 7** shows the relationship between the input level and the parameters.

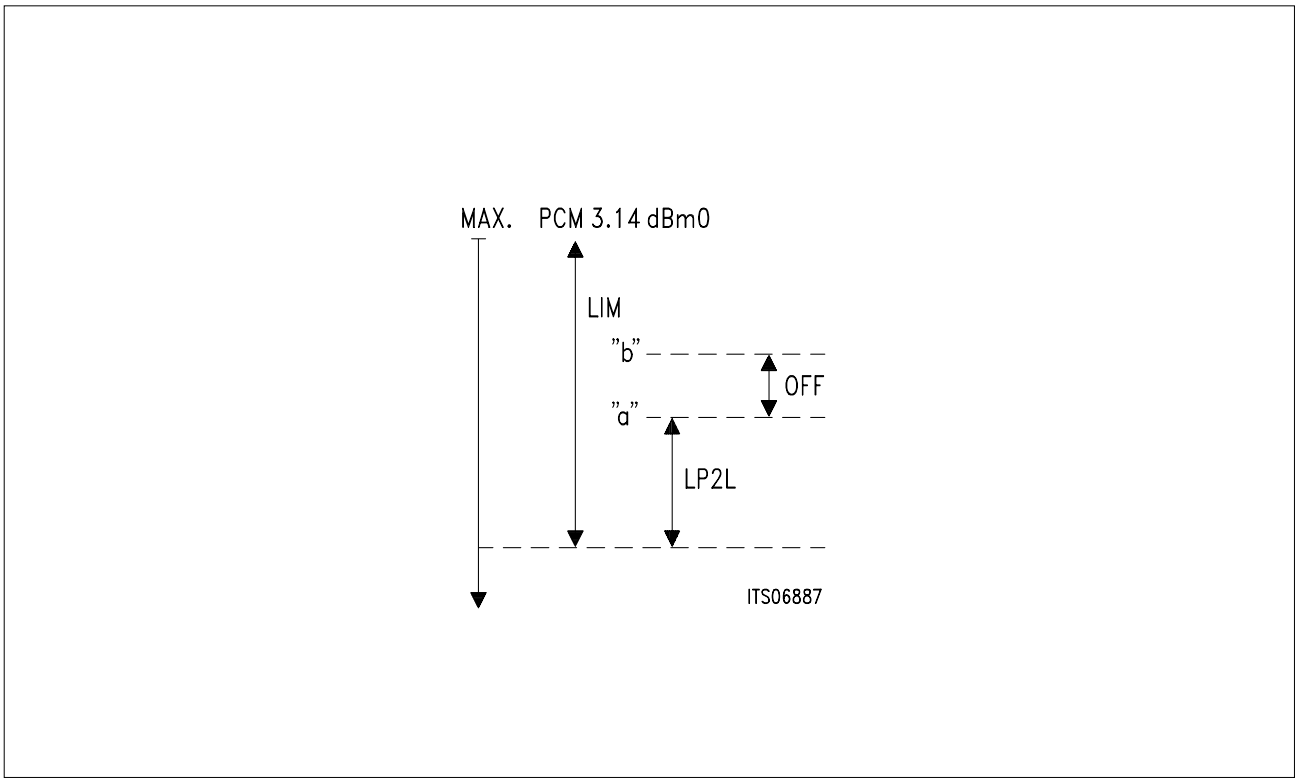

Figure 7
Level Considerations for Processing Continuous Tones

The parameter **LIM** determines an input threshold for the speech detector and is related to the maximum PCM value. The charging of LP2 is limited to a level of **LP2L** dBs above the threshold **LIM**. A continuous input signal that must be recognized as speech has not only to overcome line "a" in **figure 7** but additionally the offset in the second branch of the speech detector. Therefore any signal whose level is above the line "b" is high enough always to be recognized as speech.

With the explanation given above, the required value for **LP2L** can be calculated if the level of the continuous signal is known. Note that because of the averaging in LP2 a calculation with peak values will always lead to a slight mismatch in the range of a few dB.

Table 3
Parameters for the Speech Detectors

Parameter	Typical Value	Comment
LIM	– 54 dB	Threshold, related to max. PCM value of + 3.14 dB; signal values below this threshold are not processed.
LP1	4 ms	Time constant for low pass filter 1; suppression of noise bursts and spikes; **LP1** < **PDN**.
PDS	102 ms	Time constant for peak detector if speech has been recognized; **PDS** > **PDN** for storing speech bursts and bridging breaks during speech.
PDN	32 ms	Time constant for peak detector in case of noise.
LP2S	6.6 s	Time constant for low pass 2 if speech has been recognized; a high value is necessary to avoid a quick charging during speech.
LP2N	30 ms	Time constant for low pass 2 in case of noise; low time constant allows quick adaption to changes of the background noise level.
LP2L	25 dB	Limitation parameter; limits the charging of low pass 2.
OFF	4.5 dB	Offset in one branch of the speech detector; speech bursts must be **OFF** dB above the average signal level to be recognized.

Note that the ARCOFI-SP contains two speech detectors, one for the transmit direction, one for the receive direction. Parameters for the speech detector in transmit direction are usually marked with an additional letter "X", parameters for the speech detector in receive direction are marked with an "R". **Table 3** can be applied for both detectors.

2.6 The Speech Comparator for the Acoustic Echo

The speech comparator for the acoustic echo has the important task to decide, whether a signal actually being received by the microphone is an echo or really a speech activity. This is done by comparing the amplitude of the incoming signal with the amplitude of the outgoing signal (See “Basics about the Speakerphone Algorithm” on page 140). If the transmit signal is stronger than the signal being received at that moment, this will be indicated to the speakerphone control logic which does a mode switching if also the corresponding speech detector has recognized speech.

To understand how the comparator works it is assumed at first order, that mechanical resonances can be neglected compared to the different kinds of acoustic echo. The acoustic echo can be divided into two main parts. The first part of the signal reaches the microphone directly from the loudspeaker, travelling inside or outside the telephone housing (part 1). The second part results from reflections at the walls or boundaries like the desk where the telephone is placed on (part 2). It takes about one millisecond for signal part 1 to travel from loudspeaker to microphone (depending on the geometrical arrangement). Reflected signals are not only weaker than the direct sound, they also arrive with a certain delay. This situation is illustrated in **figure 8**.

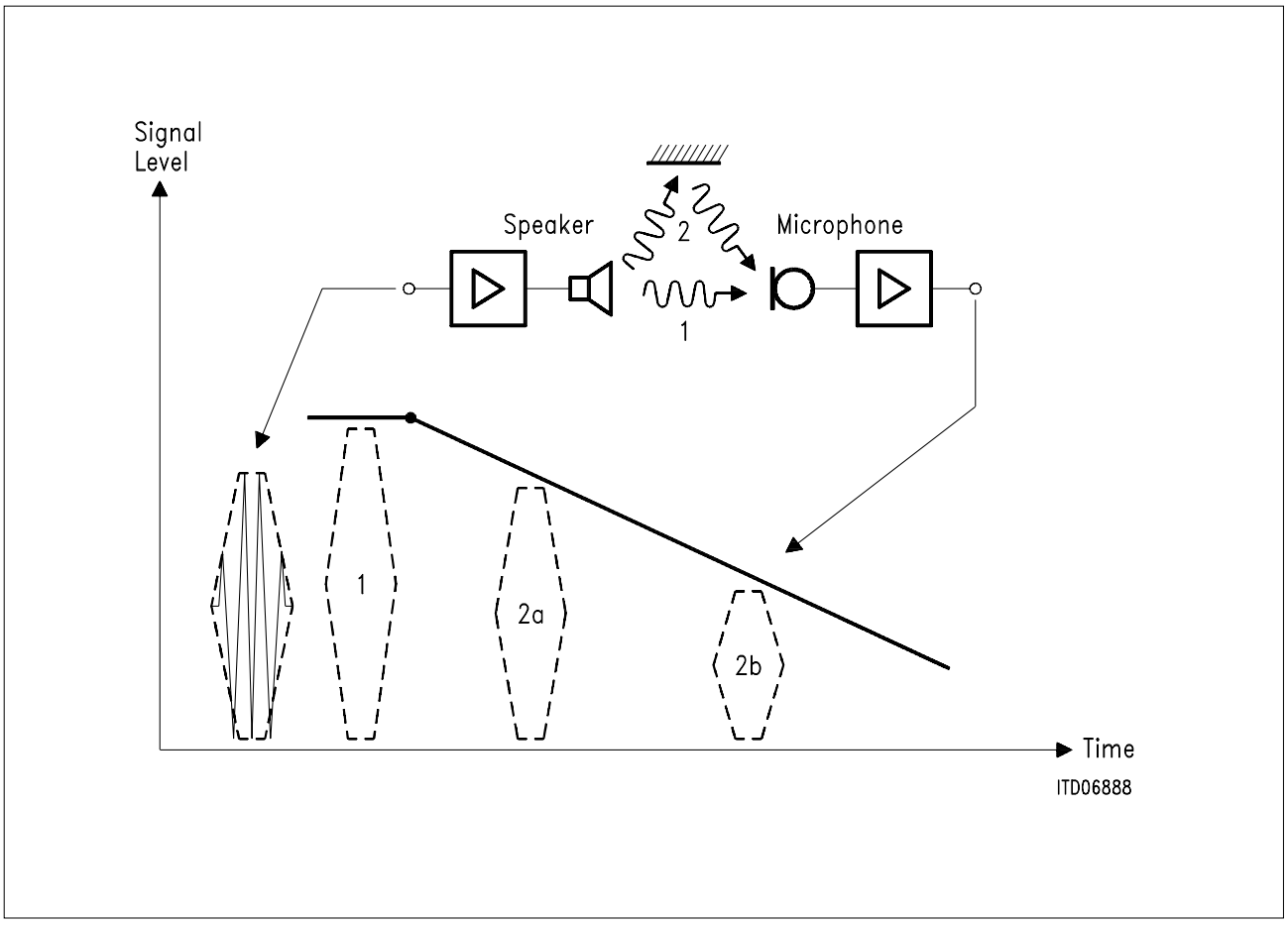

Figure 8
Acoustic Echoes Resulting from Direct Coupling (1) or Reflections (2)

A signal burst fed into the loudspeaker amplifier appears after a short delay at the output of the microphone amplifier (marked with a "1" in **figure 8**). Room echoes (marked with "2") are significantly weaker and arrive later at the microphone. The resulting signal envelope at the output of the microphone amplifier looks somehow like the bold line in **figure 8**.

Therefore in first approximation the characteristic of the acoustical environment can be described by a certain slope for the decrease of intensity of the echoes. But the amplitude of the direct sound (signal part 1) arriving almost instantaneously at the microphone depends on the amplification programmed for the ARCOFI-SP, the kind of microphone and the loudspeaker used. As a consequence, the speech comparator for the acoustic echo inside the ARCOFI-SP offers one parameter to compensate for these amplifications (**GAE**, gain of the acoustic echo) and basically two additional parameters to copy the acoustic properties of the room (**GDAE**, delta gain of the acoustic echo [dB] and **PDAE**, peak decrement of the acoustic echo [dB/ms]). With these three parameters the switching characteristic of the speech comparator is adjusted as shown in **figure 9**. The characteristic is a picture of the acoustical phenomenons allowing a precise differentiation between echo and true speech activity. Every signal whose level is above the bold line in **figure 9** will make the comparator to change state. If the signal level is below the line, it must be regarded as an echo and no switching occurs.

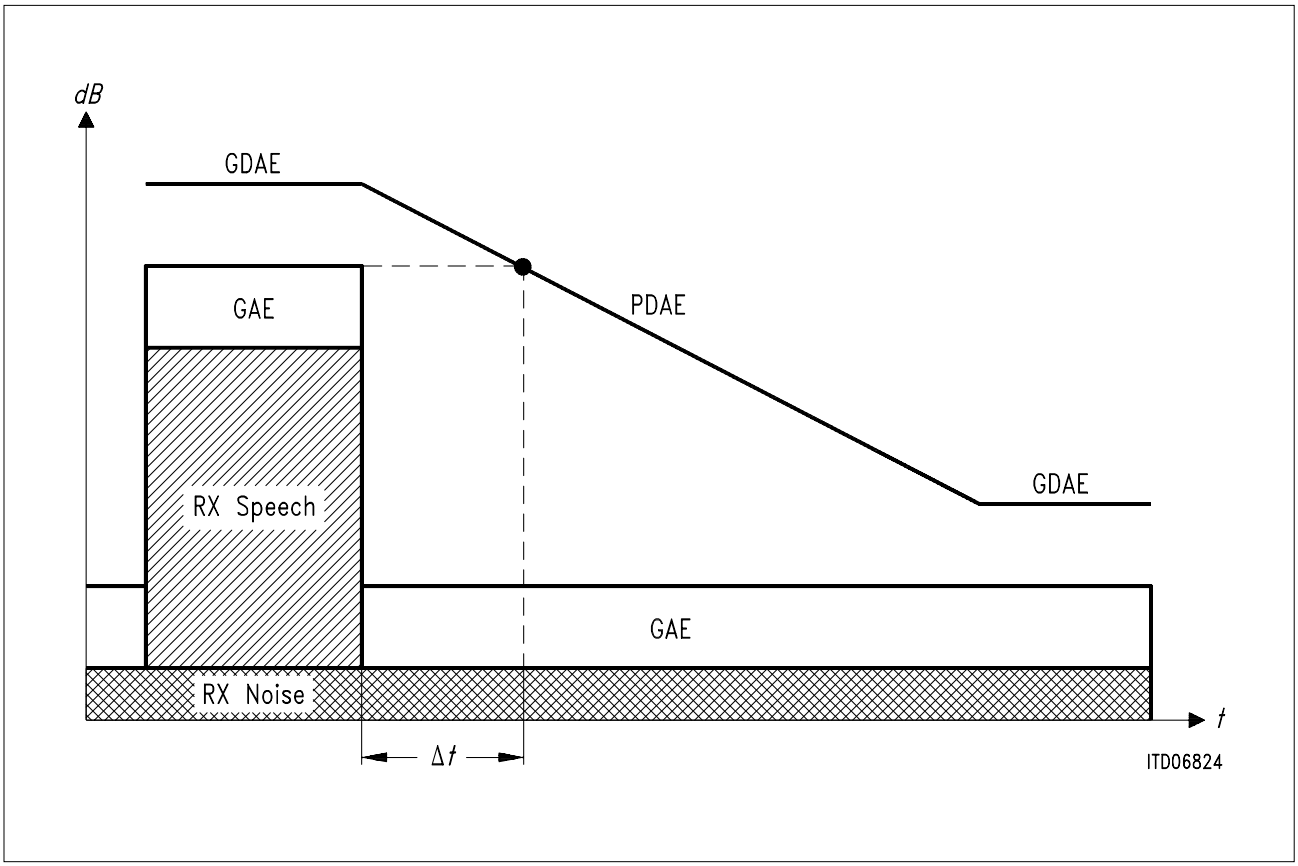

Figure 9
Implementation of the Speech Comparator for the Acoustic Echo

Appropriate Values for the Comparator Parameters

From the explanations given above a set of values for **GAE**, **GDAE**, and **PDAE** can be derived:

- After programming the desired amplifications for receive and transmit path, a measurement of the terminal coupling loss in an anechoic room allows the calculation of the required **GAE** (a detailed explanation follows in chapter 3.4); **GAE** then compensates all amplifications in a way, that in case of direct coupling, the transmitted and received signal shows the same amplitude at the dashed line in **figure 10**.
- The reverberation time of the acoustical environment determines roughly the slope of the comparator characteristic; the reverberation time T_N is defined as the period of time in which the sound pressure level decays for 60 dB after the sound source is switched off. When assuming a reverberation time of about 0.5 seconds, a decrement of **PDAE** = 8.5 ms/dB is necessary (T_N/60 dB = 8.5 ms/dB).
- Now **GDAE** is used to cover the sound that is directly coupled into the microphone, this is the point marked with a black bullet in **figure 9**.

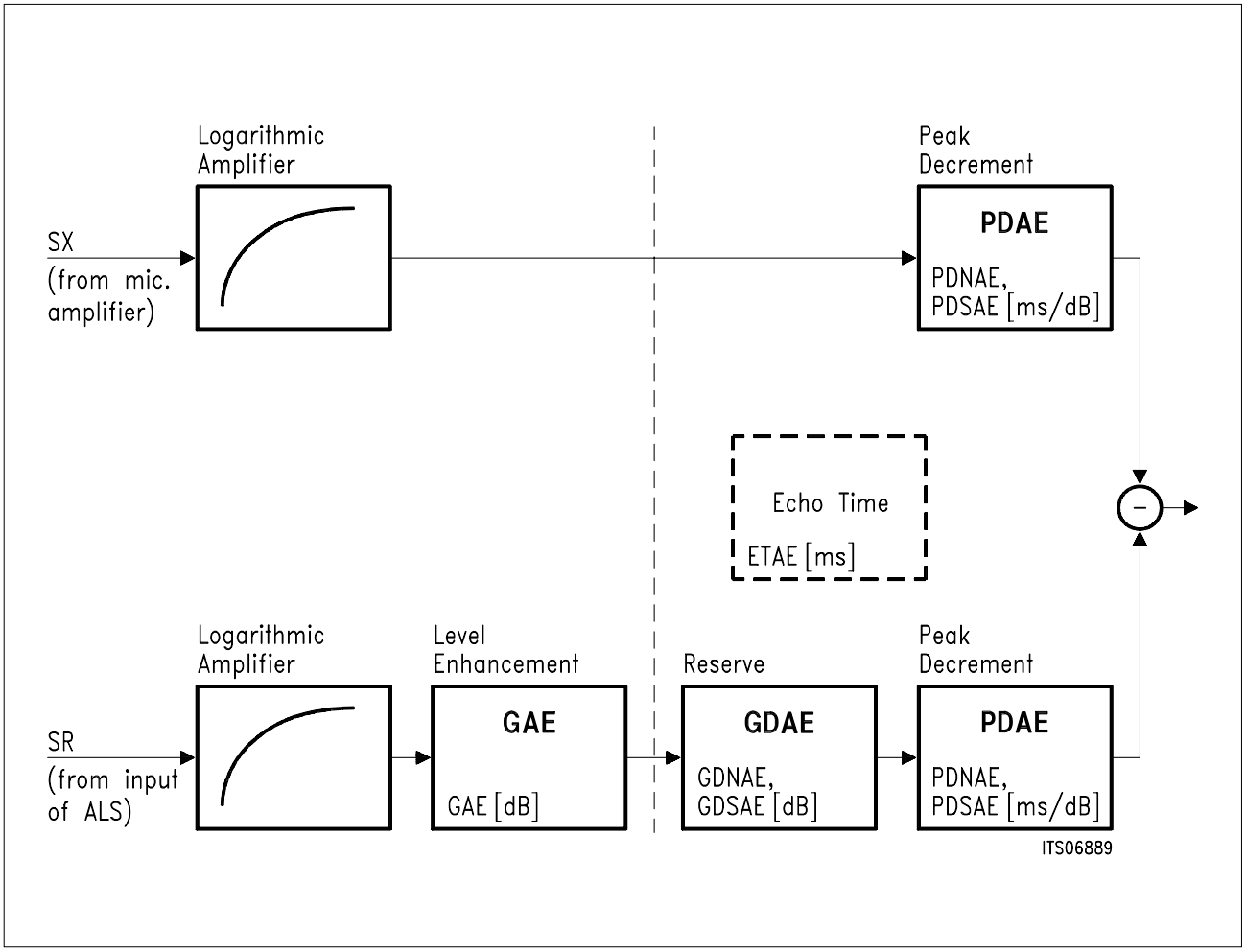

Figure 10
Signal Flow Graph of the Speech Comparator for the Acoustic Echo

It was assumed all the time, that mechanical resonances of the telephone housing can be neglected. If this assumption does not hold, the adjustment of **PDAE** and **GDAE** must be made in a way, that additionally the signal parts resulting from resonances are covered by the comparator characteristic. In this case, other measurements or an empirical approach must be used to find appropriate values. In general, a standard parameter set is sufficient for most of the applications, but it is always advisable to adapt **GAE** to the single telephone housing.

From the signal flow graph in **figure 10** it becomes obvious that in fact there are two programmable parameters each: **GDNAE** and **GDSAE** for the delta gain GDAE, **PDNAE** and **PDSAE** for the peak decrement PDAE. Usually it is not necessary to take care of the presence of two different parameters, and all explanations given in this chapter apply if the same values are used for **GDNAE** and **GDSAE** as well as for **PDNAE** and **PDSAE** the same values are programmed.

Note: To get a comparator characteristic as shown in **figure 9**, set **GDSAE** = **GDNAE** and **PDSAE** = **PDNAE**. Don’t care for **ETAE**.

But of course there are applications where different values make sense, this is always the case if an additional edge should be introduced in the comparator characteristic shown in **figure 9**, for example, if very high mechanical resonances occur with a duration that is short compared to the acoustic echoes. The letter "S" in **GDSAE** and **PDSAE** stands for "speech" and means that these parameters are only effective, as long as speech is recognized. Therefore it is possible to cover e.g. high mechanical resonances with a high **GDSAE** and a relatively slow **PDSAE** but then switch to the other pair of parameters, **GDNAE** and **PDNAE**, to get a fast decay ("N" stands for "noise"). Only in this case with different values the echo time for the acoustic echo **ETAE** becomes important. After the ARCOFI-SP has recognized "no speech" the period of time defined by **ETAE** passes before the parameters for noise (**GDNAE**, **PDNAE**) are used.

Note: To get a comparator characteristic with an additional edge, use **GDSAE**/**PDSAE** for the time during speech is recognized including the time **ETAE** afterwards. Use **GDNAE**/**PDNAE** for the rest of the time where there is noise detected.

For almost every application it is not necessary to work with two sets of parameters, and standard values can be used instead. But the ARCOFI-SP offers the flexibility to handle even difficult coupling problems due to its two switchable coefficient sets for the speech comparators.

Table 4
Parameters for the Speech Comparator for the Acoustic Echo

Parameter	Typical Value	Comment
GAE	– 5 … + 10 dB	Gain of the acoustic echo; used to achieve equal signal levels at the comparator in case of direct coupling sound, therefore representing the acoustic properties of the telephone housing, microphone, and speaker; can be calculated from a TCL measurement.
GDSAE	6 dB	Additional delta gain as reserve for **GAE** and as level shift for the comparator characteristic (in case of speech).
GDNAE	6 dB	Delta gain in case of noise.
PDSAE	8.5 ms/dB	Peak decrement of the acoustic echo in case of speech; slope of the comparator characteristic used to cover all echoes.
PDNAE	8.5 ms/dB	Peak decrement of the acoustic echo in case of noise.
ETAE	don’t care (see comment)	Echo time for the acoustic echo; only effective in case of different parameters for **GDSAE**/**PDSAE** ("S") **GDNAE**/**PDNAE** ("N")**;** determines the period of time the "S" parameters remain active after speech recognition has stopped before the "N" parameters are used.

2.7 The Speech Comparator for the Line Echo

Having understood the task and principle of the comparator for the acoustic echo (SCAE) the understanding of the speech comparator for the line echo (SCLE) is easy. As shown in **figure 2**, the speakerphone has not only to deal with acoustic couplings but also with echoes coming from the network. Basically, the intensity of echoes resulting from reflections somewhere inside the telecommunication network or from the acoustic connected to the far end, decreases exponentially. Therefore a comparator that has to cover the line echo must show a characteristic similar to the one shown in **figure 9** for the acoustic echo.

The implementation of the SCLE is identical to the one of the SCAE and therefore all explanations given in **chapter 2.6** apply also to the comparator for the line echo. The parameters to be used are different and result from the following considerations (compare with the block diagram of the SCLE in **figure 11**).

Experience shows that in worst case the level of the echo coming from the line can be about 10 dB below the sending level. This level difference must be compensated with the gain of the line echo (**GLE**) to get the same input conditions at the dashed line in **figure 11**. Besides, the line echoes can show a significant long delay in the range of some 100 ms depending on the kind of connection used (consider satellite links). By choosing a slow slope for the peak decrement **PDLE** and a high value for the delta gain **GDLE** these echoes can be covered (see typical values in **table 3**).

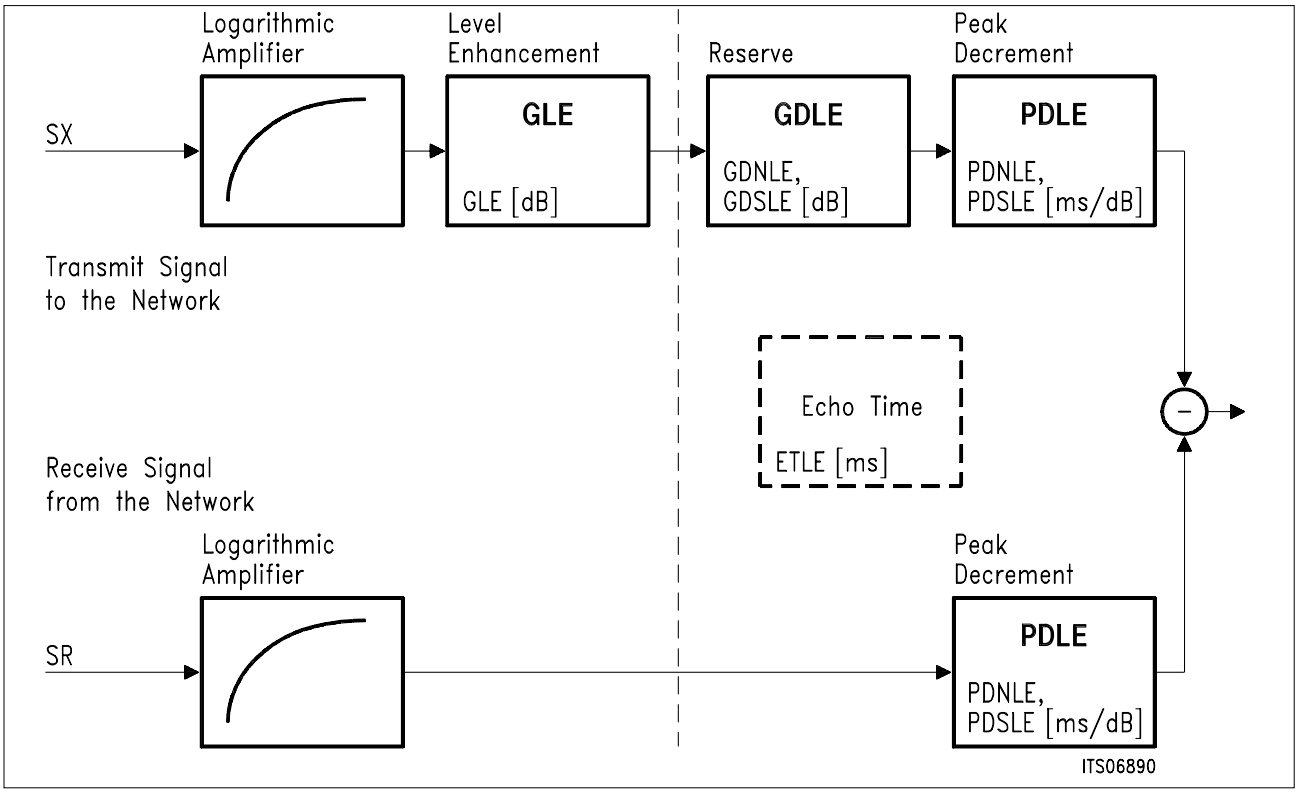

Figure 11
Block Diagram of the Speech Comparator for the Line Echo

Table 5
Parameters for the Speech Comparator for the Line Echo

Parameter	Typical Value	Comment
GLE	– 10 dB	Gain of the line echo; used to achieve equal signal levels at the comparator for covering the first echo; can be measured as the level difference between outgoing and received (echo-)signal at the network interface.
GDSLE	12 dB	Additional delta gain as reserve for **GLE** and as level shift for the comparator characteristic (in case of speech).
GDNLE	12 dB	Additional delta gain in case of noise.
PDSLE	21.3 ms/dB	Peak decrement of the line echo in case of speech; slope of the comparator characteristic used to cover all echoes.
PDNLE	21.3 ms/dB	Peak decrement of the line echo in case of noise
ETLE	don’t care (see comment)	Echo time for the line echo; only effective in case of different parameters for **GDSLE**/**PDSLE** ("S") **GDNLE**/**PDNLE** ("N"); determines the period of time the "S" parameters remain active after speech recognition has stopped before the "N" parameters are used.

3 Programming and Optimizing

3.1 Speakerphone Test Function

At least during the optimization process it is highly recommended to make use of the integrated speakerphone test mode of the ARCOFI-SP. It allows to observe the internal state of the speakerphone control unit by the help of two LEDs connected to the piezo-pins of the ARCOFI-SP (see **figure 12**).

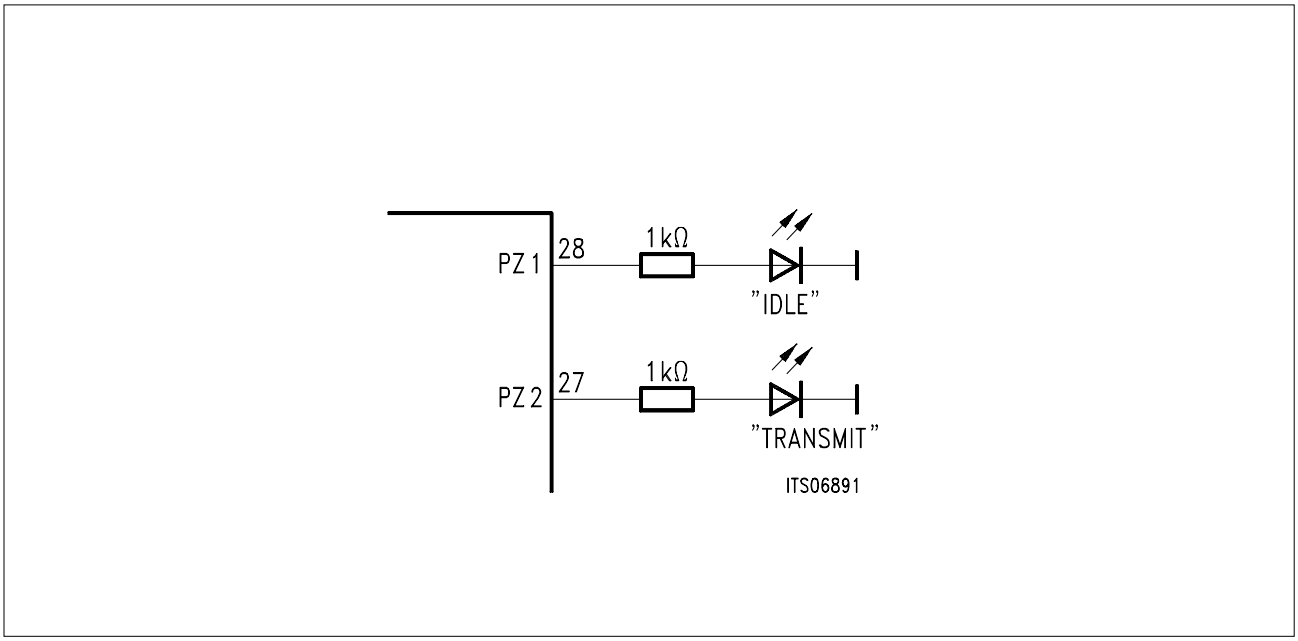

Figure 12
Test LEDs at the PZ-pins

Clipping and transient effects that are almost not audible can easily be detected with the help of these LEDs. To activate the speakerphone test function, the bit **TFCR.EPZST** and the bit **TGSR.PM** must be set. The test function has no influence on the functionality of the ARCOFI-SP.

Table 6
Speakerphone States and Test LEDs

"TRANSMIT" LED	"IDLE" LED	Meaning
OFF	OFF	ARCOFI-SP is in receive mode
OFF	ON	Idle mode is active; it was reached via the receive mode
ON	OFF	ARCOFI-SP is in transmit mode
ON	ON	Idle mode is active; it was reached via the transmit mode

3.2 Programming Hints

COP Sequences

Table 7
COP Sequences and Relation to Speakerphone Parameters (bold)

COP	1. Byte	2. Byte	3. Byte	4. Byte	5. Byte	6. Byte	7. Byte	8. Byte
COP_A	**GAE**	**GLE**	**ATT**	**ETAE**	**ETLE**	**TW**	**DS**	**SW**
COP_B	**GDSAE**	**PDSAE**	**GDNAE**	**PDNAE**	**GDSLE**	**PDSLE**	**GDNLE**	**PDNLE**
COP_C	**LIM**	**OFFX**	**OFFR**	**LP2LX**	**LP2LR**	**LP1X**	**LP1R**	**<xxx>**
COP_D	**PDSX**	**PDNX**	**LP2SX**	**LP2NX**	**PDSR**	**PDNR**	**LP2SR**	**LP2NR**
COP_E	**LGAX**	COMX	AGX	TMHX	TMLX	NOISX	<xxx>	<xxx>
COP_F	**LGAR**	COMR	AAR	AGR	TMHR	TMLR	NOISR	<xxx>

Except the ARCOFI-SP registers and COP_5 for the GX, GR amplification stages, all bold faced parameters in table must be programmed to get the speakerphone work. The corresponding hex values must be taken from the ARCOS-SP software. <XXX> are don't care bytes and should be set to 00_H for future software compatibility.

Aborting COP Sequences

Any COP sequence can be interrupted without losing -with the particular sequence- the already programmed parameters. If for example a COP_A sequence is aborted after the first byte is successfully transmitted, the ARCOFI-SP will use the new value for GAE transmitted within the first byte. This feature allows shortest programming times simply by interrupting the sequence after the desired information has already been transmitted.

High Pass Filter

Especially for speakerphone mode it is necessary that the digital high-pass filters HPX and HPR (compare with **figure 3**) are switched on (**PFCR.DHPR**=0, **PFCR.DHPX**=0), for these digital high-pass filters are to remove the DC portion of the 16-bit word, which e.g. could wrongly be regarded as background noise.

Generally these filters should be always switched on except for the very rare situations when signalling at frequencies below 50 Hz is used.

3.3 Programming Amplifications in Speakerphone Mode

It is important to notice, that as soon as the **GCR.SP** bit is switched on, the gain stages LGAX and LGAR (located inside the automatic gain control stages) are activated automatically. **Figure 13** shows the gain stages responsible for amplification in transmit or receive direction. The GHX and GHR stages for the switchable attenuation are not shown.

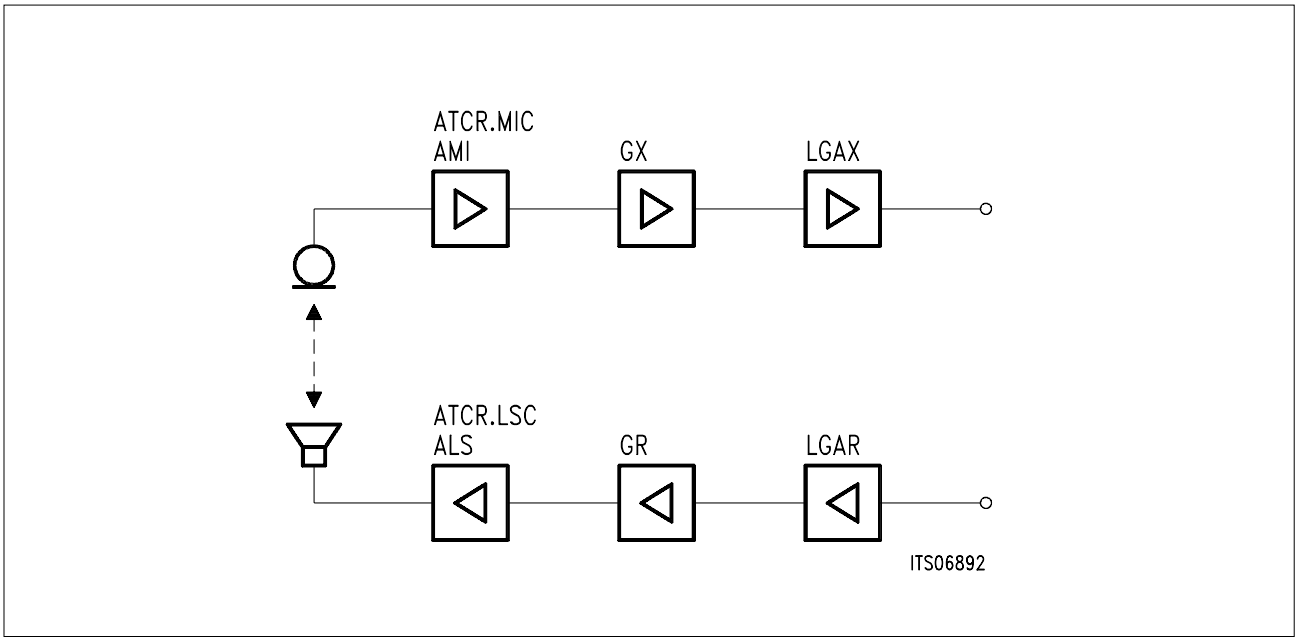

Figure 13
Gain Stages in Speakerphone Mode

For measuring the over-all amplification in speakerphone mode it is necessary to program the switchable attenuation **ATT** to 0 dB (this is done by sending COP_A xx xx 00 xx xx xx xx xx, where "xx" are don't care bytes).

Note: Throughout the ARCOFI-SP user's manual absolute levels are given either in **dBm0** or in **dBm**. Levels given in dBm always refer to a 600 Ω load, therefore 0 dBm is equivalent to 774.6 mVrms. The signal level in the digital domain is usually expressed in dBm0. The maximum PCM signal level defined for A-law coding is 3.14 dBm0 respectively 3.17 dBm0 for μ-law. The signal level in dBm that is delivered from the D/A converter inside the ARCOFI-SP, if a 0 dBm0 PCM signal is applied, is determined by the reference voltage of the converter (1.18 V) causing a level difference of 20 *log* (1.18/0.775) [dBr] = 3.67 dBr.

Level (analog)	Level (digital)
0.0 dBm	– 3.67 dBm0
3.67 dBm	0.0 dBm0

3.4 How to Determine GAE

In the general description of the speech comparator for the acoustic echo the meaning of the gain of the acoustic echo, **GAE** was introduced (see **page 149**). **GAE** should always be adapted to the particular hardware (plastics, microphone, speaker) whereas in first approximation for all the other parameters standard values can be used. This chapter shows a simple measurement procedure to find an appropriate value for **GAE**.

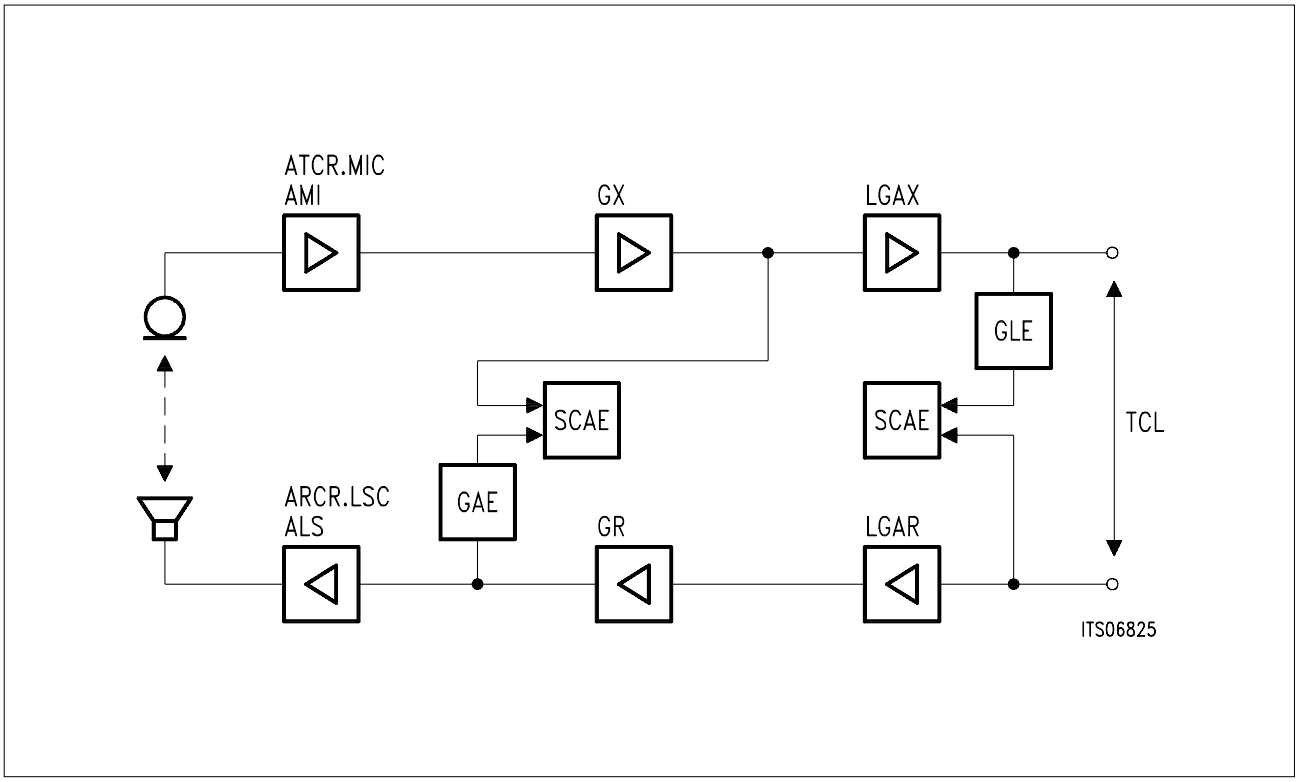

Figure 14
Position of the Speech Comparators SCAE and SCLE

Figure 14 is important as it shows the position of the comparators related to the different amplification stages. It can be seen that the comparator for the acoustic echo, SCAE, senses the receive signal directly in front of the analog loudspeaker amplifier ALS and the transmit signal between the GX and the LGAX stage. As explained in **chapter 2.6** the task of **GAE** is to adjust the signal level in a way, that in case of direct coupling the amplitudes at the input of the SCAE are equal.

Measuring TCL and Calculating GAE

A measurement of the terminal coupling loss TCL[1)] is sufficient to calculate the required value for **GAE**. A typical measurement procedure can be realized as follows:

- Programming of all amplifications (**ATCR.MIC**, **GX**, **LGAX**, **ARCR.LSC**, **GR**, **LGAR**). Note, that for making **LGAR** and **LGAX** effective, the speakerphone must be enabled (**GCR.SP**=1); to suppress any influence of the switchable attenuation **ATT**, set **ATT**=0dB (COP_A xx xx 00 xx xx xx xx xx).
- Measuring the frequency dependent terminal coupling loss. This measurement has to be done in an anechoic environment.
- Calculating **GAE**. Use the following equation with the programmed amplifications and the measured TCL; in general it is sufficient to calculate with the weighted terminal coupling loss TCLw, but if there are strong couplings at discrete frequencies, it can be necessary to use a value between TCLw and the worse TCL values instead. Equation for calculating **GAE:**
  LGAX + TCL + **LGAR** + **GR** + **GAE** = 0 dB.
  Example:
  LGAX = 4.5 dB; **LGAR** = 3.0 dB; **GR** = 0dB; TCL = – 5 dB $\rightarrow$ **GAE**= – 2.5 dB.

Empirical Determination of GAE

If no anechoic room is available or for evaluation purposes also a simple test procedure can lead to an appropriate value for **GAE**. After building up a speakerphone to handset connection with negligeable line delays, **GAE** is varied and the acoustic effects on the handset are evaluated. As a signal source either a human voice or synthetic speech signals can be used (composite source signal, interrupted sinewave sweep, or switched pink noise). If the telephone plastics does not exhibit an "extreme behavior", it should always be possible to find a threshold value for **GAE**. If **GAE** is too low, the speech comparator can not cover the acoustic echo and clipping effects occur. If **GAE** is increased, the comparator will not change state due to echoes (compare with **figure 9**), but the higher **GAE**, the more difficult it is to interrupt the signal from the speakerphone side.

During tests, **GAE** should be changed only in small steps of e.g. 0.5dB because for having the best speakerphone performance it is important to keep the value as low as possible. This optimum value is usually in the range of – 5 dB … + 9 dB. The worse the telephone housing (from the acoustical point of view), the higher the value for **GAE** must be to cover the echo.

---

1 See: ETSI prl-ETS 300 245-3, "Technical characteristics of telephony terminals; Part3: PCM A-law, loudspeaking and handsfree function", 4/93

The task is to find the minimum value for **GAE** for which the speakerphone works properly.

3.5 Basic Rules for Optimizing the Speakerphone

General

- Always make use of the test function described in **chapter 3.1.**
- Start experiments with the standard coefficient set given in chapter 3.8.
- Make sure to have an appropriate value for **GAE**.
- Use a handset to speakerphone connection.
- Be sure to have programmed correct amplifications in the transmit and receive path (see also the paragraph about volume control).
- The transmit and the receive direction can be checked separately, if the microphone inputs or the loudspeaker outputs are disabled (**ATCR.MIC**=00_H or **ARCR.LSC**=00_H)

ATT

- The switchable attenuation **ATT** should be in the range of 20 dB … 30 dB; as mentioned on **page 133**, the smaller **ATT** is, the better is the performance of the half-duplex system.

Speech Detectors

- The standard parameter set is not critical and shows best results under almost every condition.
- With the ARCOFI-SP in receive or transmit mode, the test LED indicating "idle" during a monologue must flash; this behavior is independent of the presence of background noise.
- In case of high background noise which undergoes quick volume changes (e.g. machines that are starting periodically) it could be interesting to allow the low pass LP2 a quicker adaption to the average noise level (decrease **LP2NX**, but always keep **LP2SX** < **LP2NX**); the disadvantage is, that speech detection becomes a bit more insecure.
- If the system noise level – especially in receive direction – is quite high, thinking about increasing the input threshold of the speech detector (**LIMX**) is necessary, but **LIMX** must always be low enough to ensure a secure speech detection for the weakest speech signal to be recognized.

Comparator for the Acoustic Echo, SCAE

- It's most important to have a correct value for **GAE**; read **chapter 3.4** for details
- SCAE is responsible for avoiding clipping effects: a monologue at the handset side should always be transparent at the loudspeaker on the speakerphone side; the "transmit"-LED must remain dark while the "idle"-LED is flashing; after the end of speech at the handset side, the "transmit"-LED has to remain dark, otherwise resonances or room echoes have caused the ARCOFI-SP to switch wrongly into transmit mode
- Consider using a synthetic voice or tone signal (e.g. CSS or SPN from a test CD) since these signals have a constant level
- Once having adjusted the comparator, it should be possible to interrupt a person speaking at the far end simply by speaking loud(er) on the speakerphone side; the lower the value for **GAE** is (respectively the better the telephone acoustics is), the easier it is to interrupt the other side
- In case of clipping problems, it can be helpful to draw the comparator characteristic as shown in **figure 9** in a true scale on a piece of paper and think about possible changes; if the reverberation time of the room is very long, increase **PDAE**; if the telephone plastics shows strong resonances, increase **GDAE;** in worst case, a second edge can be introduced in the comparator characteristic (see **page 149**)

Comparator for the Line Echo, SCLE

- The standard parameters are chosen under the assumption, that the worst case line echo is at least 10 dB below the outgoing signal (**GLE** = – 10 dB) and that the line delay for this high echo is shorter than 0.26 seconds (**GDLE** = 12 dB, **PDLE** = 21.3 ms/dB, delay = **GDLE**×**PDLE**)
- Clipping effects due to a line echo are not to be expected with the parameters given above, but if e.g. tests with a satellite link show unsatisfactory results, an increase of **GLE** from e.g. – 10 dB to – 8 dB gives additional 2 dBs room for higher echoes; longer delays have to be covered with higher **GDLE** and **PDLE**; again, this makes it more difficult to interrupt a person talking at the speakerphone side

Typical Effects and the Corresponding Solutions

(**See "Steady-State Problems and Transient Effects" on page 134**; ↓ means "decreasing the parameter, ↑ stands for "increasing")

Table 8
Typical Effects in Speakerphone Mode

Effect	Solution
Singing	**ATT** ↑
Transmit blocking	**GAE** ↓; **GDSAE** ↓; **GDNAE** ↓
Receive blocking	**GLE** ↓; **GDSLE** ↓; **GDNLE** ↓
Initial clipping	**GDSLE** ↓
Starting echo	**GAE** ↑; **GDSAE** ↑; **GDNAE** ↓
End echo	**GLE** ↑; **GDSLE** ↑; **GDNLE** ↑ ; **PDSLE** ↑; **PDNLE** ↑
Chopping effect	**GAE** ↑

3.6 Controlled Monitoring

"Controlled Monitoring" or "Loudhearing" can be regarded as a special speakerphone mode with the difference, that the telephone user talks into the handset microphone and the receive signal is reproduced by the handset earpiece and the loudspeaker. The handsfree microphone is not active. Volume changes in the earpiece due to switchable attenuation are not allowed.

The ARCOFI-SP supports Controlled Monitoring by using a slightly different attenuation mechanism as in the speakerphone mode. To enable this feature, not only the **GCR.SP** bit has to be set, but also the **ARCR.CME** bit (Controlled Monitoring Enable). The Controlled Monitoring mode can be described as follows (compare the explanation with **figure 15**):

- The speakerphone support is active and works as usual.
- The attenuation stage for receive direction GHR is fixed to a gain of 0 dB (this is in contrast to the normal speakerphone mode and is necessary to have always a constant volume at the handset output).
- The amplification in the analog loudspeaker amplifier ALS is determined by **ARCR.LSC** as usual, but it can be switched to the fixed value of – 9.5 dB regardless of the setting of **ARCR.LSC**.
- ALS is switched to – 9.5 dB automatically as soon as the speakerphone support of the ARCOFI-SP has decided to use attenuation in the receive path; therefore the volume of the signal coming out of the loudspeaker is reduced to a low volume when speech activity takes place in the transmit path ("Controlled" Loudhearing).

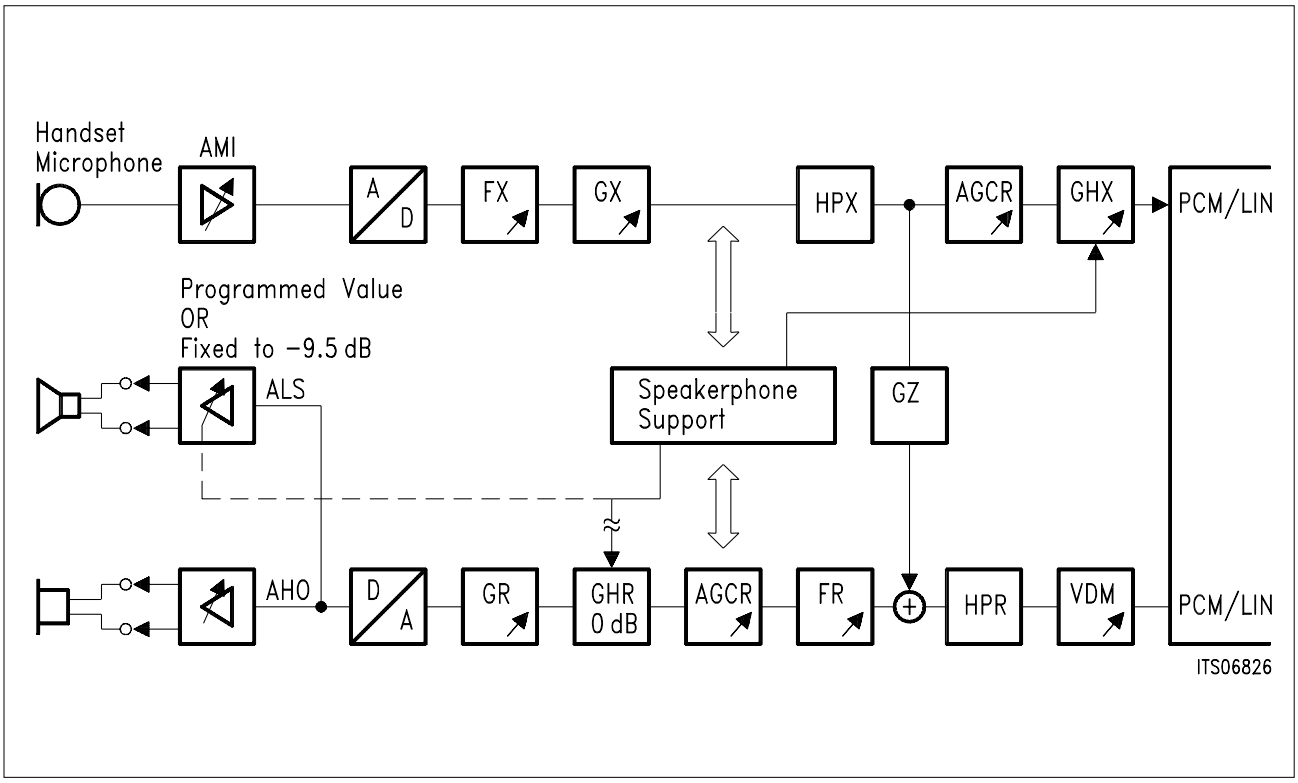

Figure 15
Explanation of the Controlled Monitoring Mode

Hints for Optimizing

Generally, the controlled monitoring feature should be optimized after having found a appropriate set of coefficients for the speakerphone. Then, after enabling the **ARCR.CME** bit, only fine tuning is necessary. The system should be stable even if the handset microphone is placed close to the loudspeaker. Due to the instantaneously switching of the ALS, a reduction of **DS** and **SW** (decay speed, switching time) avoids short-time instabilities. Note, that **GAE** must be adapted, if amplification in the loudspeaker amplifier, the microphone amplifier or the GX stage is reprogrammed (remember **figure 14**).

3.7 Implementing a Volume Control

The telephone user normally has the possibility to choose different volume settings when using the speakerphone. The volume can be adjusted either manually by reprogramming amplifications in the receive path or by means of the automatic gain control stage. Since the automatic gain control stages are described in a separate application note, this chapter deals with the first solution.

Table 9
Example for Eight Volume Steps

Vol. Step	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**
total gain G [dB]	G= 23	G-3= 20	G-6= 17	G-9= 14	G-12= 11	G-15= 8	G-18= 5	G-21= 2
ALS [dB]	11.5	8.5	5.5	2.5	2.5	2.5	2.5	2.5
GR [dB]	3.5	3.5	3.5	3.5	0.5	0	0	-0.5
LGAR [dB]	8	8	8	8	8	5.5	2.5	0
GAE [dB]	Y	Y-3	Y-6	Y-9	Y-9	Y-9	Y-9	Y-9
ATT [dB]	X	X-3	X-6	X-9	X-12	X-15	X-18	X-21

It’s important to keep some items in mind:

- In speakerphone mode, receive amplification can be changed with **LGAR**, **GR**, and **ARCR.LSC**.
- For achieving best signal to noise performance, the maximum signal level should be close to the max. PCM value; clipping must be avoided.
- It’s advisable, not to reduce the loop gain (which includes the switchable attenuation ATT) when reducing the volume[1)]; this can be achieved by reprogramming the parameter ATT; as a consequence, the conversation gets the more transparent, the lower the volume is.
- Every time, either **ARCR.LSC**, **ATCR.MIC**, or **GX** is changed, **GAE** must be adapted too (applies only for speakerphone mode); see also **figure 14**.

Table 9 shows an example for eight volume steps with an over-all amplification in the loudest volume step (step 8) of 23 dB. For each volume step, the amplification is reduced by 3 dB. The value for **GAE** is shown as "Y" and must be reduced every time, the gain in the ALS is reduced. The loop gain remains constant:
LGAR+**GR**+**ARCR.LSC**+**ATCR.MIC**+**GX**+**LGAX**+**ATT** = const.

1 A. Busla: "Fundamental Considerations in the Design of a Voice-Switched Speakerphone", The Bell System Technical Journal; Vol. XXXIX, March 1969, Number 2, page 280

3.8 Example Set of Coefficients

The coefficients shown in **table to** should serve as a basis for every speakerphone application. After starting with these values efforts must be taken to find an appropriate value for **GAE** (see **page 157**). With the hints given in **chapter 3.5** further adaption to the particular requirements can easily be achieved.

Table 10
Standard Parameter Set for the Speech Detectors

Parameter	Value	Meaning	Coefficient
LP1X	4.0 ms	Low-pass 1	COP_C __ __ __ __ __ E1 __ __
PDNX	32.2 ms	Peak detector (noise)	COP_D __ F4 __ __ __ __ __ __
PDSX	102.3 ms	dto. (speech)	COP_D 26 __ __ __ __ __ __ __
LP2LX	24.8 dB	Limitation for LP2	COP_C __ __ __ 42__ __ __ __
LP2NX	30.1 ms	Low pass 2 (noise)	COP_D __ __ __ 44 __ __ __ __
LP2SX	6.6 s	Low pass 2 (speech)	COP_D __ __ 20 __ __ __ __ __
OFFX	4.5 dB	Offset	COP_C __ 0C __ __ __ __ __ __
LIMX	– 54 dB	Limit (threshold)	COP_C 4_ __ __ __ __ __ __ __
LP1R	4.0 ms	Low-pass 1	COP_C __ __ __ __ __ __ E1 __
PDNR	32.2 ms	Peak detector (noise)	COP_D __ __ __ __ __ F4 __ __
PDSR	102.3 ms	dto. (speech)	COP_D __ __ __ __ 26 __ __ __
LP2LR	24.8 dB	Limitation for LP2	COP_C __ __ __ __ 42__ __ __
LP2NR	30.1 ms	Low pass 2 (noise)	COP_D __ __ __ __ __ __ __ 44
LP2SR	6.6 s	Low pass 2 (speech)	COP_D __ __ __ __ __ __ 20 __
OFFR	4.5 dB	Offset	COP_C __ __ 0C __ __ __ __ __
LIMR	– 54 dB	Limit (threshold)	COP_C _4 __ __ __ __ __ __ __

Table 11
Standard Parameter Set for the Comparators

Parameter	Value	Meaning	Coefficient
GAE	5.3 dB	gain of acoustic echo	COP_A 0E __ __ __ __ __ __ __
ETAE	0.0 ms	echo time	COP_A __ __ __ 00 __ __ __ __
GDSAE	6.0 dB	delta gain (speech)	COP_B 20 __ __ __ __ __ __ __
PDSAE	8.5 ms/dB	peak decrement	COP_B __ 05 __ __ __ __ __ __
GDNAE	6.0 dB	delta gain (noise)	COP_B __ __ 20 __ __ __ __ __
PDNAE	8.5 ms/dB	peak dec. (noise)	COP_B __ __ __ 05 __ __ __ __
GLE	– 10.2 dB	gain of line echo	COP_A __ E5 __ __ __ __ __ __
ETLE	0.0 ms	echo time	COP_A __ __ __ __ 00 __ __ __
GDSLE	12.0 dB	delta gain (speech)	COP_B __ __ __ __ 40 __ __ __
PDSLE	21.3 ms/dB	peak decrement	COP_B __ __ __ __ __ 02 __ __
GDNLE	12.0 dB	delta gain (noise)	COP_B __ __ __ __ __ __ 40 __
PDNLE	21.3 ms/dB	peak dec. (noise)	COP_B __ __ __ __ __ __ __ 02

Table 12
Standard Parameter Set - Other Pparameters

Parameter	Value	Meaning	Coefficient
ATT	28.2 dB	attenuation	COP_A __ __ 48 __ __ __ __ __
TW	144.0 ms	wait time	COP_A __ __ __ __ __ 09 __ __
DS	99.0 ms/dB	decay speed	COP_A __ __ __ __ __ __ 25 __
SW	0.6 ms/dB	switching time	COP_A __ __ __ __ __ __ __ 64
LGAX	4.5 dB	gain adjustment	COP_E 13 __ __ __ __ __ __ __
LGAR	5.5 dB	gain adjustment	COP_F 12 __ __ __ __ __ __ __

Table 13
Example Register Setting for Speakerphone Mode

Register	Meaning	Coefficient
TFCR	Test function configuration	SOP_7 40
ARCR	AFE receive configuration	SOP_6 04
ATCR	AFE transmit configuration	SOP_5 70
TGSR	Tone generator switch	SOP_4 00
TGCR	Tone generator configuration	SOP_3 00
PFCR	Programmable filter configuration	SOP_2 00
DFICR	Data format and interface configuration	SOP_1 F1
GCR	General configuration	SOP_0 96
XCR	Extended configuration	SOP_A 00

If the SDI/SCI interface mode is used, in addition to the registers shown in **table** the registers SDICR and TSCR have to be set first. Instead of sending eight particular SOP sequences, a SOP_F can be used: SOP_F 40 04 70 00 00 00 F1 96.

All the bytes given in **table 10 to 13** can be read from the ARCOS-SP Plus software[1)] or from a previously saved file with the extension *.ARC. **Table 14** shows the contents of the ARC-file (not included COP_0 ... COP_9 because they are only necessary for the tone generator and the AGC).

Table 14
Speakerphone Related Sequences to be Found in a ARC-File

```
W 0 COP_A 0E E5 48 00 00 09 25 64
W 0 COP_B 20 05 20 05 40 02 40 02
W 0 COP_C 44 0C 0C 30 30 E1 E1 00
W 0 COP_D 26 F4 20 44 26 F4 20 44
W 0 COP_E 13 84 10 07 13 5F 00 00
W 0 COP_F 12 84 7F 10 07 13 5F 00
W 0 SOP_F 40 04 70 80 00 00 F1 96
```

1 ARCOS-SP software or ARCOS-SP PLUS software for the PSB 2163 (SIPO 2163)

Layout and Wiring Recommendations

Vakat

Table of Contents **Page**

1 Introduction

The ARCOFI-SP PSB 2163 is a high performance codec filter device with a state of the art tone generator and an excellent speakerphone implementation. To obtain the full performance of the device, some care in designing the analog circuitry and the printed circuit board has to be taken. This application note gives some hints and wants to provide understanding of the parameters that influence the performance.

With "performance", especially the following effects are meant:

- Signal to noise ratio, especially in transmit direction (analog to digital)
- Idle channel noise (the noise that is present when there is no signal applied)
- Spurious oscillations
- Sensitivity to any kind of interfering signals (noise on power supply, RF interference, induced voltages etc.)

The ARCOFI-SP contains high performance A/D and D/A converters with more than 16bit resolution in order to allow the different signal processing steps without degradation of the signals themselves. On one silicon the PSB 2163 integrates a high gain, analog preamplifier, the converters as well as an digital signal processor. Besides the ARCOFI-SP is used in an digital environment that typically causes noise on the power supply and produces many kinds of interfering signals. For all these reasons, careful grounding, decoupling, and shielding is the key to get best system performance.

Note: The circuits given in this application note are for general guidance and do not claim to satisfy all user specific requirements. Especially for EMC reasons additional components may be required.

2 Layout Considerations

Since the ARCOFI-SP will be used with different kinds of printed circuit boards in different applications and environments, it is not possible to show the "optimum layout". Instead, this chapter explains the correlations that lead to the optimum layout for a given application.

Power Supply Pins

The PSB 2163 has three ground pins and two pins for connecting the positive supply voltage. Internally all the ground pins and all the power supply pins are connected. From **table 1** it can be seen, what parts of the ARCOFI-SP are supplied from what pins. It is important, that each pair of pins given in one row of **table 1** is decoupled with a pair of capacitors in parallel. One capacitor has to be a 47 nF … 100 nF ceramic one, for the second one a tantalum type with 1 µF … 10 µF is recommended.

Table 1
Power Supply Pins of the PSB 2163

Pin for V_{SS}	Pin for V_{DD} (+ 5 V)	Supply for
1 (V_{SSD})	21 (V_{DD})	Digital signal processor and digital interface
15 (V_{SSP})	13 (V_{DDP})	Analog output amplifier AHO, ALS
20 (V_{SSA})	21 (V_{DD})	Analog preamplifiers and switches

Note, that pin 21 (V_{DD}) is used for both, the supply of the DSP and the supply of the analog part of the ARCOFI-SP except the power amplifiers AHO and ALS.

Ground Plane

A second aspect in designing a perfect PCB layout is a low impedance connection between all points of the circuitry that have to be connected to ground. First of all, this concerns the three ground pins of the ARCOFI-SP (pin 1, 15, 20). These three pins have to be connected to each other directly underneath the IC package. This ensures not only a low impedance ground for the PSB 2163 but also serves as a shield, if the connection between the three ground pins is realized as a ground plane. Shielding is important since it protects the high gain analog amplifiers and the converters against any capacitive coupling. Hence, if multilayer PCBs are used, the ground plane has to be the top layer and not somewhere in between.

Figure 1 shows one possibility to place the decoupling capacitors on a two layer board if no components are allowed on the bottom of the PCB. If mounting on both sides is permitted, one would place the capacitors between pin 1 and 21 on the bottom layer.

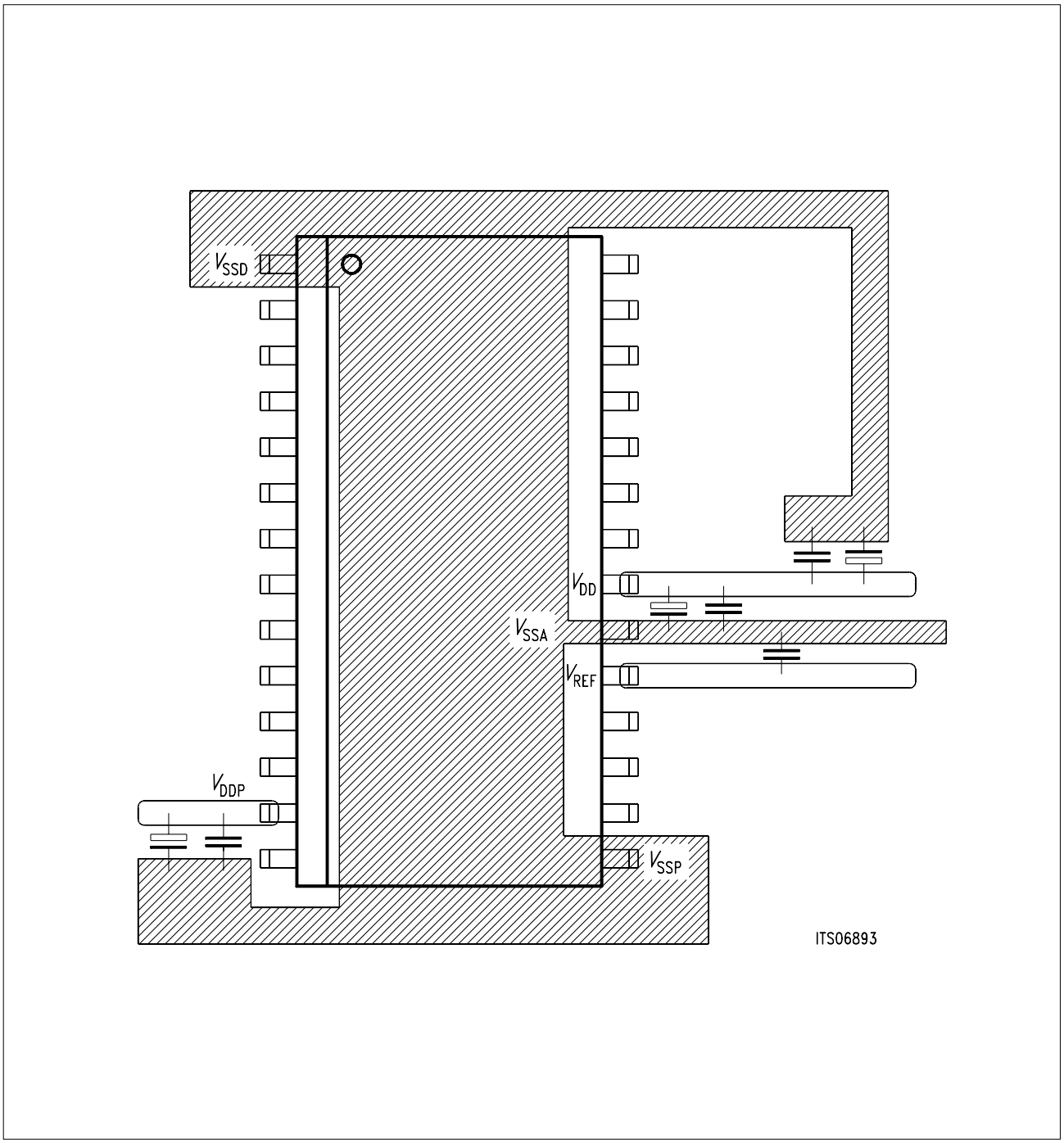

Figure 1
Example Layout with Decoupling Capacitors and Ground Plane

Note the large ground area underneath the chip. It is a good approach to extend this ground area also to the locations of all the passive components required for connecting the acoustical transducers (microphones etc.). But any kind of ground loop must be avoided since this would be an antenna for RF noise. Note also the position of the decoupling capacitor for the reference voltage between pin 19 and 20 in **figure 1**. It should be placed close to pin 19 and 20.

Grounding of Microphones

Some transducers as electret microphones for example, always need a reference to ground and therefore the question arises, which point of the circuit should serve as a microphone ground.

As long as truly differential signal sources are used, this is not a problem. The high common mode rejection ratio of the differential microphone inputs eliminates interfering signals. But if an electret microphone is used, this microphone requires some biasing and will be tied to ground with one pin (see **chapter 3.2** for more examples about connecting microphones). **Figure 2** shows the typical arrangement for connecting electret microphones. The microphone inputs MIN1/MIP1 and MIN2/MIP2 are differential inputs with an input impedance of 15 kΩ or more. No external biasing is required for these inputs. In the unbalanced configuration in **figure 2**, one of the inputs is tied to the reference voltage (V_{REF} pin). The reference voltage is a stable (2.4 V) and very clean DC voltage; a current of up to 1.0 mA can be drawn from V_{REF}. If the V_{REF} pin is used externally, it has to be blocked to the analog ground (V_{SSA}) with a 100 nF capacitor (ceramic). If the V_{REF} pin remains open, no blocking capacitor is required.

From **figure 2** it becomes obvious, that any voltage difference introduced in the circle marked with a dashed line, will be regarded as a wanted signal and therefore will be amplified and converted by the ARCOFI-SP. In a real application, only the voltage originating from the microphone itself has to be amplified. This leads to the requirement, that the microphone ground must be connected directly to the pin V_{SSA} (or to a ground plane which incorporates V_{SSA}).

If on a PCB the microphone is not placed directly next to the ARCOFI-SP, it is a good solution to use a separate ground trace between the microphone and the analog ground of the ARCOFI-SP. If the microphone is connected via a longer cable, the cable should be shielded and again the screen is tied to the analog ground.

Summary

- Good decoupling between the pins given in one row of **table 1**
- Large ground plane underneath the chip connecting all ground pins
- Careful grounding of unsymmetrical signal sources

If these considerations receive attention, the full performance of the PSB 2163 is available even in a very "noisy" environment.

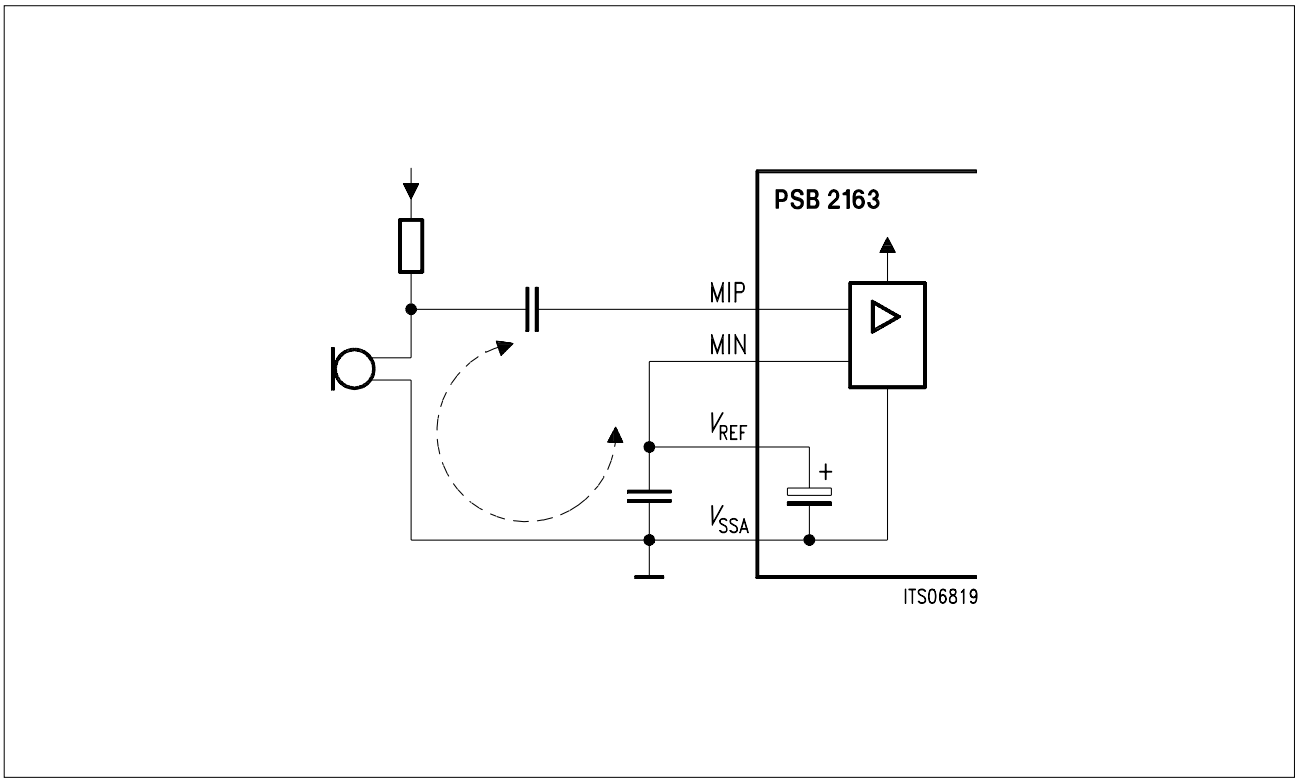

Figure 2
Ground Loop with Single Ended Signal Sources

3 Connecting the Analog Front End

3.1 Outputs for Earpiece and Loudspeaker

The analog handset output amplifier AHO delivers a symmetrical signal at the pins HOP and HON. Any load with an impedance higher than 200 Ω can be connected directly (see **figure 3a**). However, if the load shows a strong capacitive behavior like a piezo-ceramic earpiece, it is better to use series resistors as shown in **figure 3b** to avoid spurious oscillations. This is also an typical example for a circuitry as it is used in a real application. The resistors have to be placed close to the output pins.

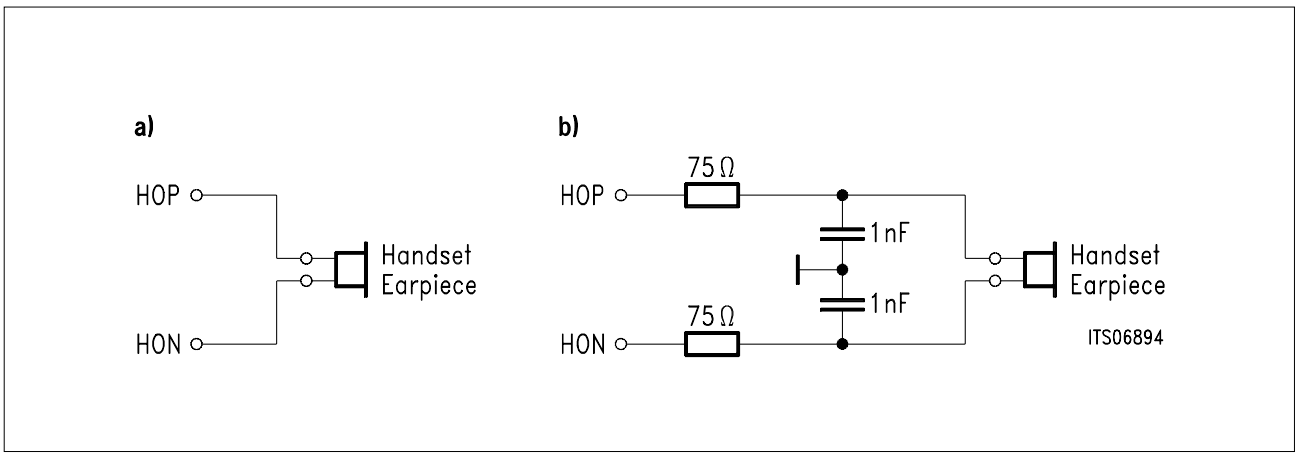

Figure 3
The Analog Handset Output

It is possible to use the outputs HOP and HON as single ended outputs with reference to ground; the load must be greater than 100 Ω and only half of the amplitude swing is available.

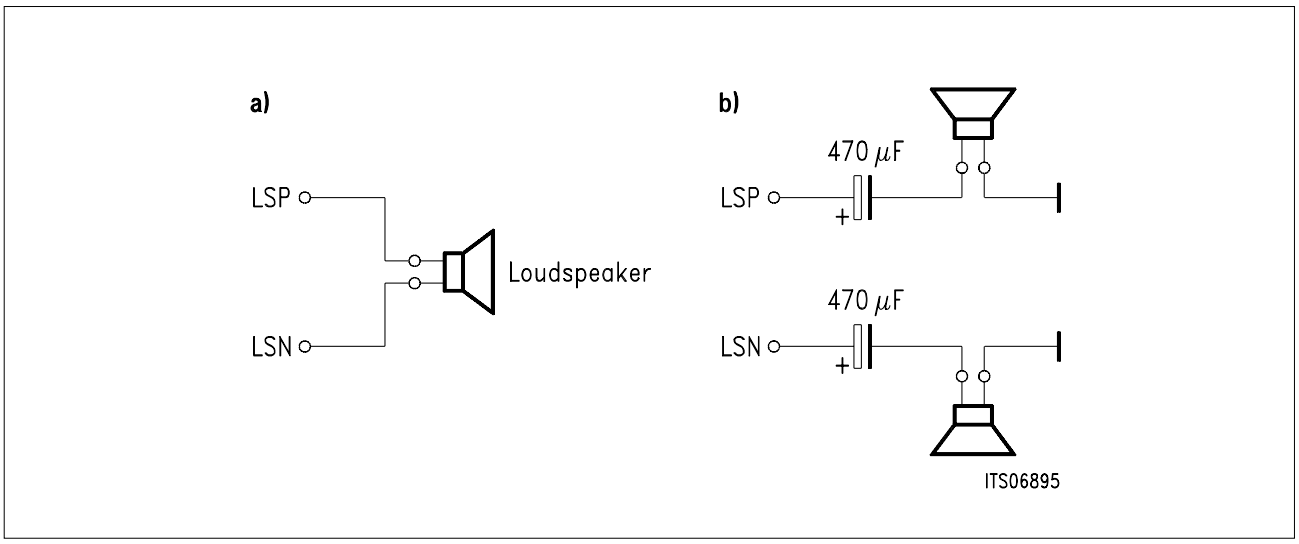

Figure 4
The Analog Loudspeaker Output

The difference between the earpiece output and the loudspeaker output is the driver capability. The load between the pins LSP and LSN may be as low as 50 Ω in order to drive a speaker. A dynamic speaker can be connected directly to these pins (see **figure 4a**). An arrangement for an unsymmetrical connection with two speakers shows **figure 4b**. The load can be 25 Ω but should be decoupled to avoid DC currents through the speakers. With the register bits **XCR.DLSP** and **XCR.DLSN** each output pin can be switched into a high impedance state therefore the speakers can be switched on and off independently. The same applies for the earpiece output with HOP and HON. This feature offers a variety of applications. For example, if one speaker in **figure 4b** is left out, the output pin becomes a switchable line level output. For example, this output could control an external speaker box.

3.2 Differential Microphone Inputs

The ARCOFI-SP offers five pins as microphone inputs. The two differential inputs MIN1/MIP1 and MIN2/MIP2 are equivalent in terms of performance and circuitry. The single ended input MI3 offers a slightly reduced performance due to its unsymmetrical structure. All inputs can be used to interface directly with all kinds of microphones or serve as a high level input.

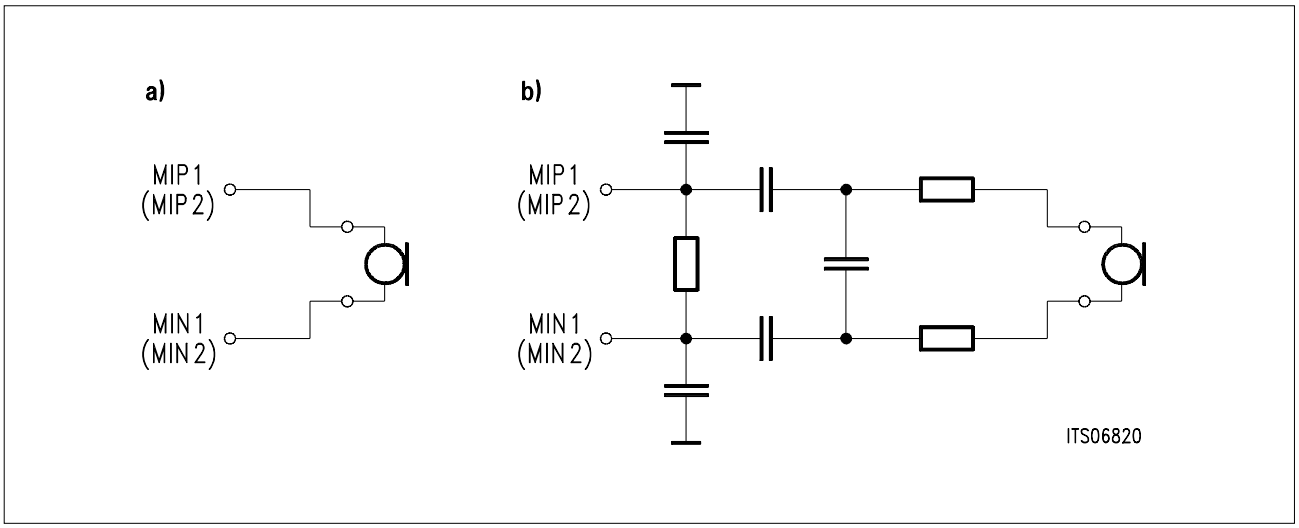

Figure 5
Interfacing Symmetrical Microphones

A symmetric signal source that has no reference to ground can simply be connected to one of the differential inputs. Basically, no additional components are required (**figure 5a**). The microphone can be a dynamic, magnetic, or piezoelectric one. Usually an arrangement similar to the one shown in **figure 5b** will be used in order to get well defined impedances and a certain EMC protection. The component values depend on the type of microphone used.

The microphone inputs are biased internally with V_{REF} and require no external biasing. They can be completely AC coupled. The input impedance is higher than 15 kΩ.

Electret Microphones

Today, electret microphones are widely used in telecommunications devices. These microphones usually contain an active amplifier or a FET to achieve a low output impedance and therefore require some DC biasing.

The DC current to bias the electret microphone can be taken from the positive supply voltage of the ARCOFI-SP (+ 5 V) or the reference voltage V_{REF} can be used for this purpose (2.4 V). The schematic in **figure 6** depicts the first possibility.

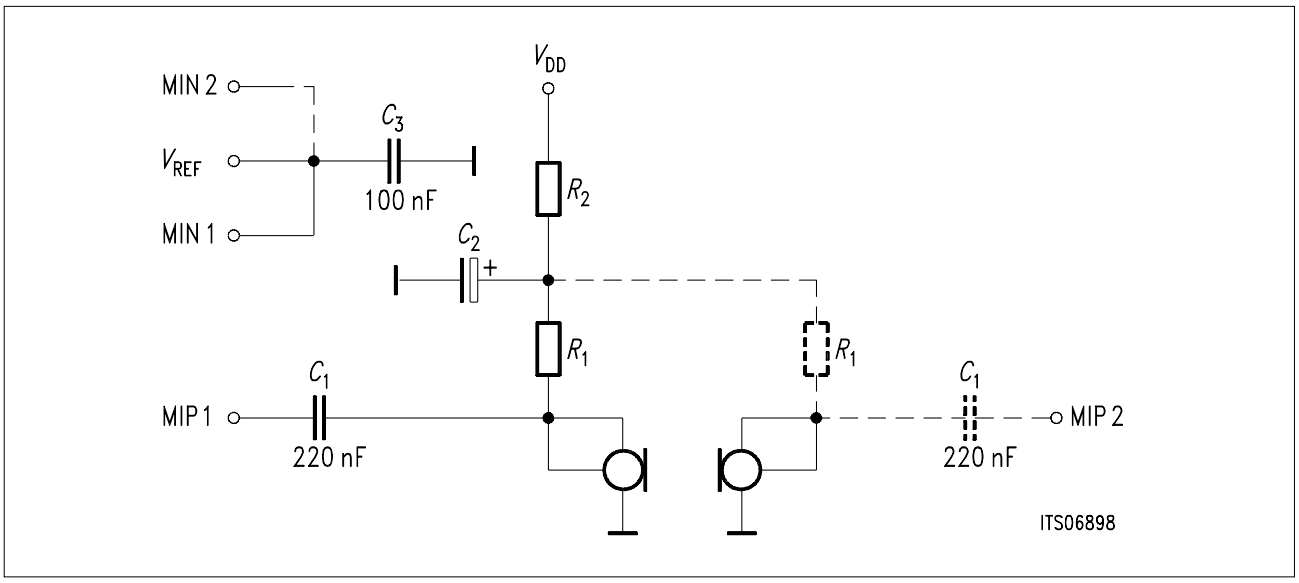

Figure 6
Interfacing Electret Microphones with Bias from V_{DD}

One input pin (MIN1) of the differential input is tied to V_{REF}. This creates a single ended configuration which must be AC coupled with C1 to the signal source, consisting of the electret microphone. R1 and R2 are used to bias the microphone. The RC combination R2/C2 filters out power supply ripple. R1 has the value recommended by the microphone manufacturer and is usually in the range of 1 kΩ … 4 kΩ.

The dashed line in **figure 6** illustrates how to connect a second microphone to the other differential input of the ARCOFI-SP without spending the complete bias network again.

The reference voltage V_{REF} has to be blocked with 100 nF to ground because any noise at the pins MIN1 and MIN2 in the above configuration will be interpreted as a wanted signal.

The second possibility to bias electret microphones is shown in **figure 7**. The DC current is taken directly from the V_{REF} pin of the ARCOFI-SP. No RC network to filter out power noise is necessary because the reference voltage is clean and stable. Only in case of high gains in the analog microphone amplifier (AMI more than 30 dB) the over-all performance can be improved, if the reference voltage is filtered. For this purpose, a R/C combination (1 kΩ/10 µF) between the V_{REF} pin and the resistors R1 in **figure 7** has to be inserted. An application incorporating this RC element shows **figure 8**.

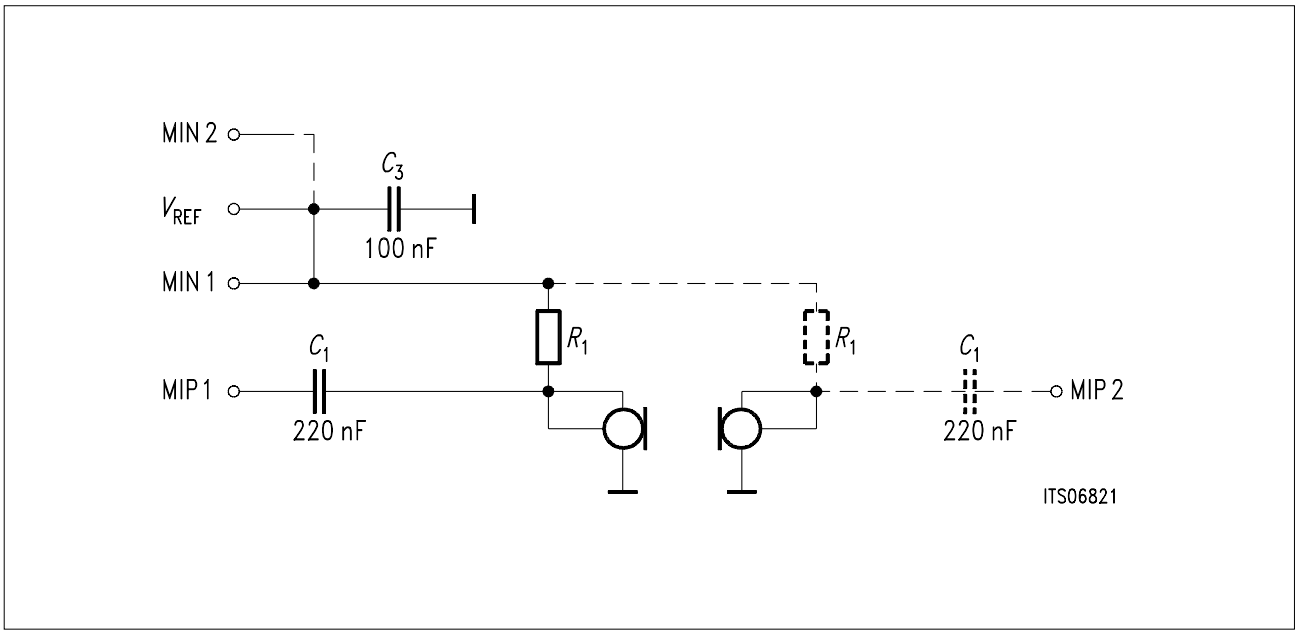

Figure 7
Interfacing Electret Microphones with Bias from V_{REF}

The solutions for connecting microphones shown in **figure 6 and 7** contain a minimum of components to explain the principle. A solution that comes closer to a real application can be seen in **figure 8**. The microphone is biased from the V_{REF} pin.

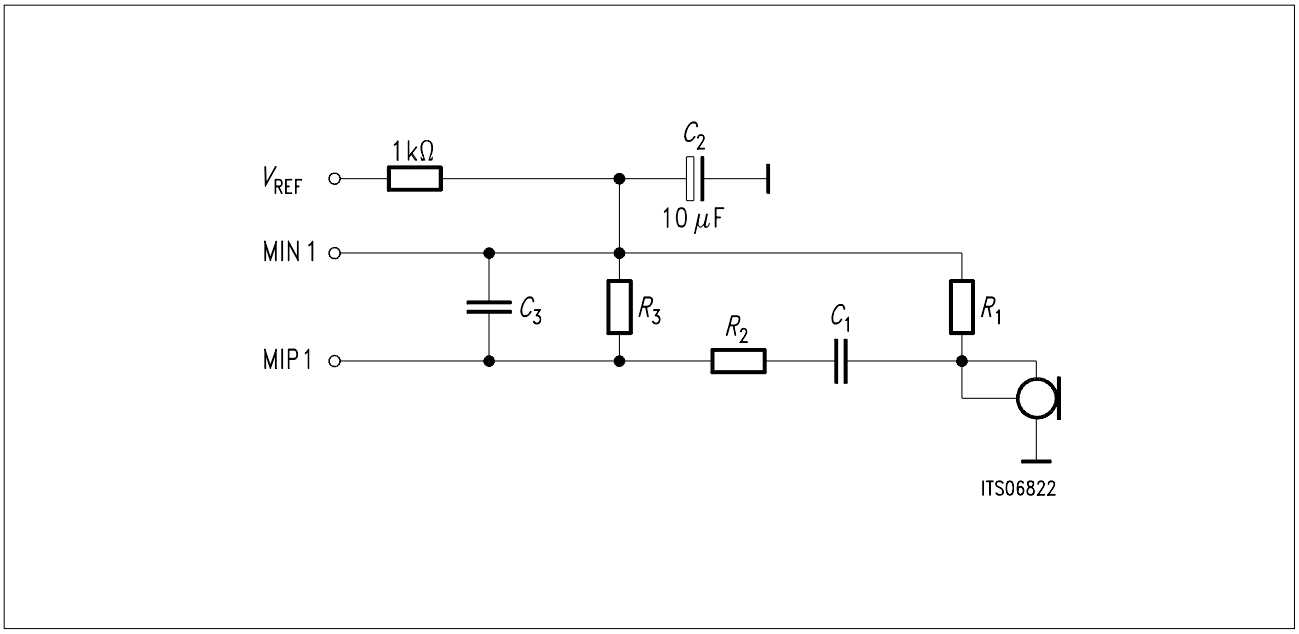

Figure 8
Example for a Real Application

With the help of R3/C3 a well defined input impedance is achieved. If R2 is inserted, a high frequency cut-off can be realized. The 1 k/10 µF combination is used to filter the reference voltage (improved idle channel noise with AMI > 30 dB).

3.3 The Single Ended Input MI3

The single ended input MI3 behaves like one of the differential input pins, in case of one input of the differential inputs is tied to V_{REF}. Therefore the application examples in **figure 9** introduces no new ideas. An electret microphone can be biased from V_{DD} (**figure 9a**) or from the V_{REF} pin (**figure 9b**). Any symmetric signal source with no reference to ground should be connected between the MI3 pin and the V_{REF} pin (**figure 9c**). Often MI3 is used as a additional input e.g. for separate microphones with their own preamplifiers. Such high-level signal sources could be connected to MI3 as shown in **figure 9d**.

In general, if only two inputs are required, it is advisable to use MIN1/MIP1 and MIN2/MIP2 for this purpose. They exhibit a slightly better performance because of their differential nature. Unused inputs can be left open or tied to V_{REF}.

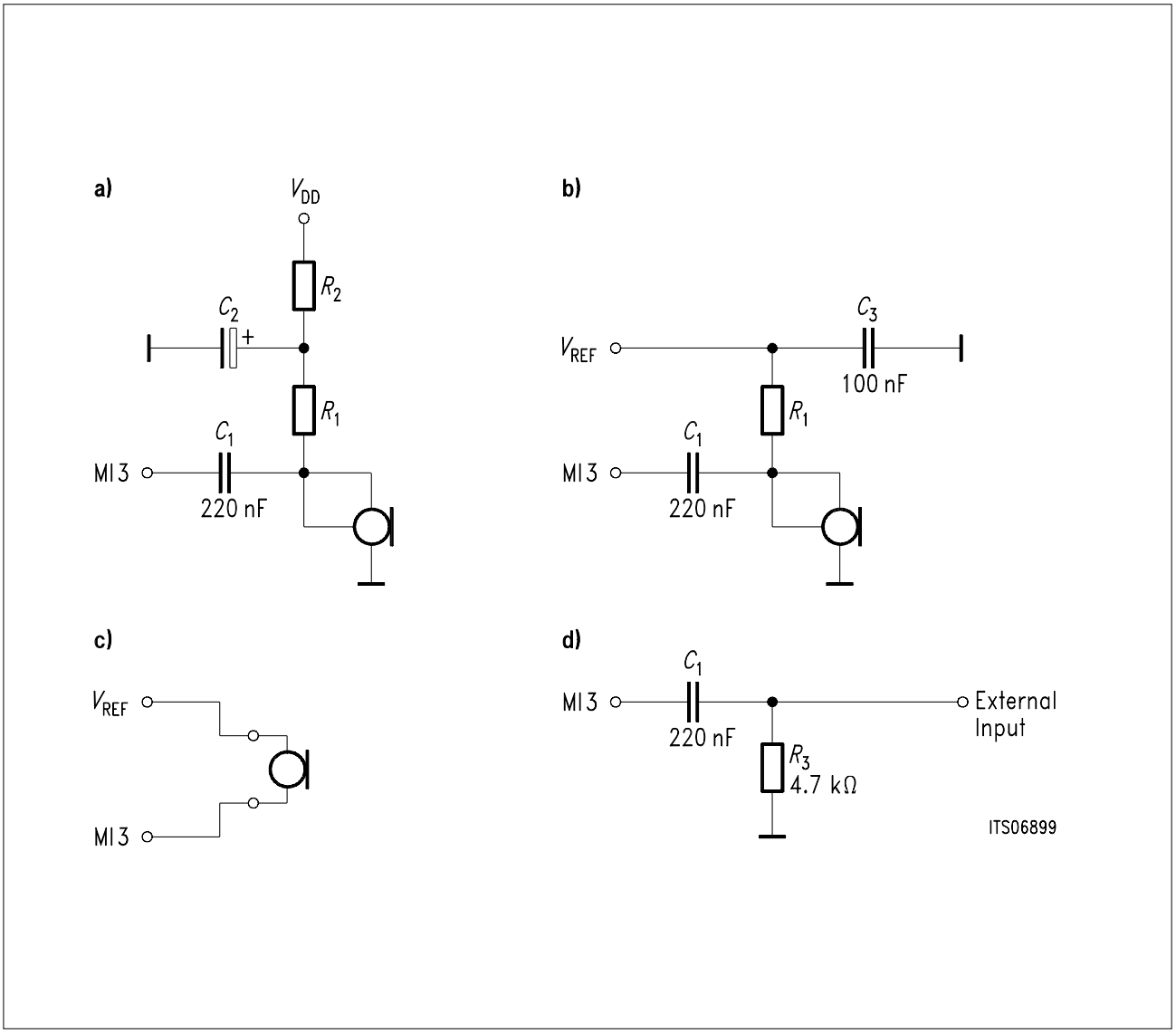

Figure 9
Using the Single Ended Input MI3

Vakat

ARCOFI®-SP Telephone Board V1.0 SIPB 5132-SP

- VAKATSEITE -

ARCOFI®-SP Telephone Board V1.0 SIPB 5132-SP

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1 Introduction

The ARCOFI-SP Telephone Board SIPB 5132-SP V1.0 is part of a demonstration example of the Siemens PC-User Board system SIPB to offer a complete solution for a digital telephone in the ISDN-world of tomorrow. It represents the interface between the audio world – consisting of analog transducers and amplifiers – and the digital world of PCM-coded transmission.

The kernel component of this board, the ARCOFI-SP PSB 2165, realizes all basic features like dialing, ringing and voice transfer. Furthermore, thanks to a strictly applied digital technique, on the same single chip full speakerphone feature without any additional external components are already exhibited; all the required hardware and software has been implemented. Thus besides of working on a single 5-V power supply, using the ARCOFI-SP PSB 2165 considerably eases the realization of modern comfort telephones.

2 Features

- ARCOFI-SP PSB 2165, delivering the following features on-chip:
  - A/D-Conversion and Filtering
  - Programmable Analog Front End
  - Digital Speakerphone Support
  - DTMF-Generator
  - Ringing Generators
  - Comfortable Peripheral Control Interface
- DTMF-generation by the Dual-Tone Multi-Frequency Generator PSB 8593 for scanning the 12 + 1 keys keyboard
- Detection of hook switch changes by Monoflops 74 LS 221 in order to transmit a DTMF-signal that normally starts procedures like activating the line
- IOM-2/SLD-interface to Audio Interface Module V2.0 and up SIPB 5130

3 Use

The ARCOFI-SP Telephone Board was originally conceived to be used at the terminal side of the user board system (TE-configuration). Nevertheless it can also serve as the analogue front end in the NT-S configuration due to the flexible concept of the SIPB-system. Thus the practical use of this ARCOFI-SP Telephone Board SIPB 5132-SP is identical to that of the analogue telephone.

The ARCOFI-SP Telephone Board is always connected to the Audio Interface Module via the IOM-2- or SLD-interface. **Figure 1** shows how and in what combination it is connected via flat cable to the mainboard.

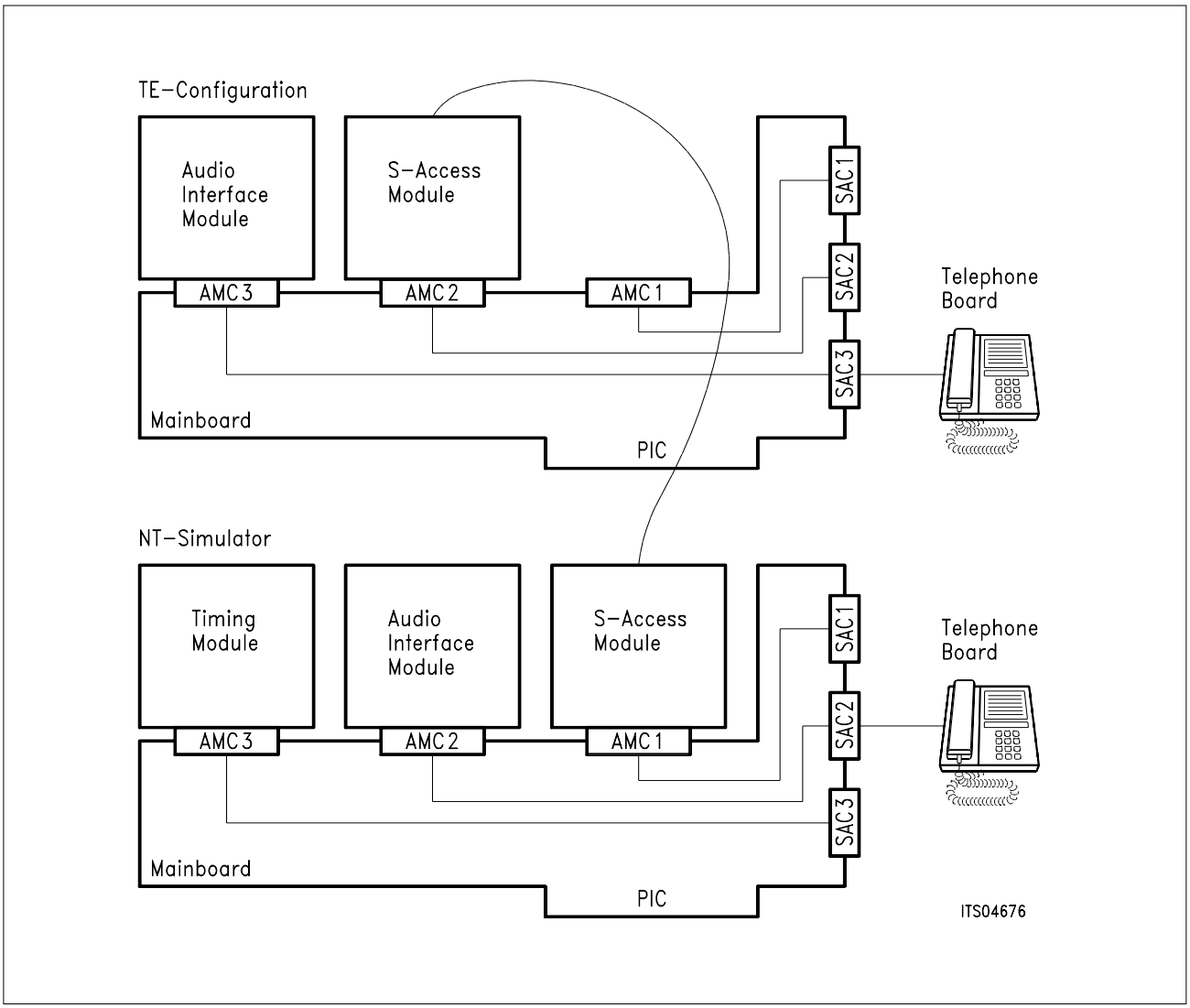

Figure 1
Examples of TE- and NT-S-Configurations in the User Board Concept

4 Circuitry

4.1 Block Diagram

The block diagram of **figure 2** below shows the main components of the ARCOFI-SP Telephone Board. The whole circuitry can be divided into three blocks:

1. Hook Switch Logic
2. Key-Pad and DTMF-Generation
3. ARCOFI SP PSB 2165

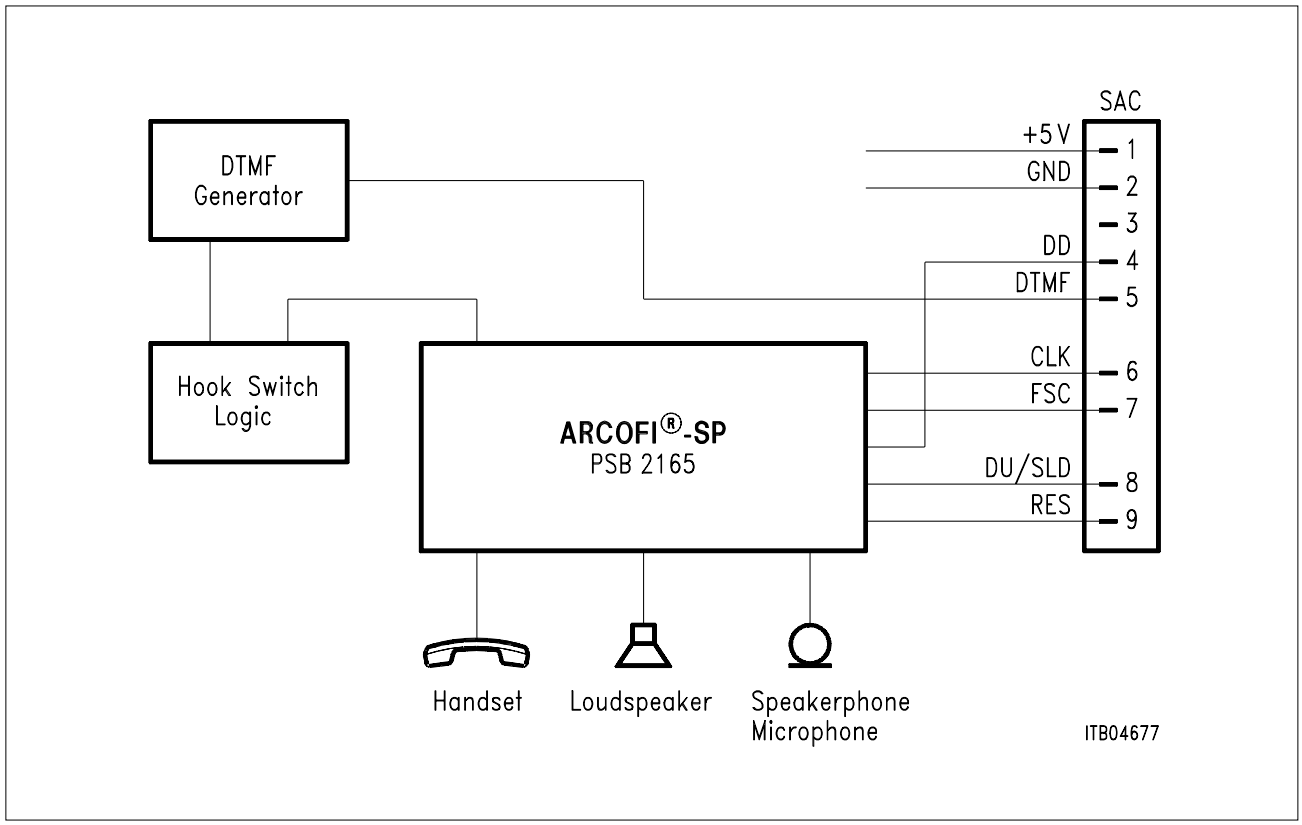

Figure 2
Block Diagram of ARCOFI®-SP Telephone Board

4.1.1 Hook Switch Logic

The hook switch logic provides two features:

- signaling the state of the hook switch via pin 2 (SD) of the ARCOFI-SP and
- signaling a change of the hook switch position.

For a standard terminal application the first information is sufficient because the state is transparent in the registers CIR1 in IOM-2-mode or in SSCR in SLD-mode respectively. In the Siemens ISDN PC-userboard concept, however, the firmware needs an additional information about a change of the hook switch position. This information is gained from a monoflop and an OR-gate. Every change of the hook switch short-circuits a pair of pins of the DTMF-generator, so that a pair of frequencies is transmitted to the DTMF-receiver of the Audio Interface Module SIPB 5130 ("relative detection" of the hook switch) in order to activate/deactivate the line and power-up/power-down the ARCOFI-SP.

4.1.2 DTMF-Generator

According to the key pressed, for each of the 12+1 push buttons on the single-contact keyboard the Dual-Tone Multi-Frequency Generator IC1 (PSB 8593) generates pairs of frequencies. These are specified by CCITT and are derived from a standard TV-crystal (3.58 MHz). The frequencies are sent to the DTMF-receiver of the audio interface module.

4.1.3 ARCOFI®-SP

The Audio Ringing Codec Filter ARCOFI-SP (PSB 2165), the heart of the Telephone Board, provides all necessary functions to convert analog signals into PCM-coded signals and vice versa. In addition the highly sophisticated speakerphone feature is implemented into the same chip. Setting gains and filter coefficients in receive and transmit direction, generating DTMF- and ringing signals, amplifying the analog paths are all done by programming the device. A basic program is shown in section 7. For more details on the ARCOFI-SP circuit and its programming structure refer to the corresponding data sheet and description.

Transmission of PCM-coded signals is done either via lOM-2 bus or SLD-bus:

Using the **IOM-2 bus** two data lines are necessary: DU (Data Upstream) to send data from ARCOFI-SP to layer 1, and DD (Data Downstream) to carry back data from layer 1 to the ARCOFI-SP. While DU is physically equal to the SLD-line (pin 7 of ARCOFI-SP), DD is realized with the line between pin 4 of the SAC-plug and pin 6 of ARCOFI-SP.

Using the **SLD-bus** the digital words are received/transmitted on the bidirectional SLD-line (Serial Line Data) at pin 7 (SIP) of the ARCOFI-SP and led to pin 8 at the SAC-plug of the telephone board.

4.1.4 LEDs

Above the 12+1 keys keyboard of the ARCOFI-SP Telephone Board there are four LEDs to indicate operational states. They are connected to the Peripheral Control Interface (PCI) of the ARCOFI-SP. The left-most of these is to signal the state of the hook switch (SD). It lights up in off-hook position. The remaining ones are for free use (see also **section 5.3**).

4.2 Connector Pin-Outs of the Service Access Connector

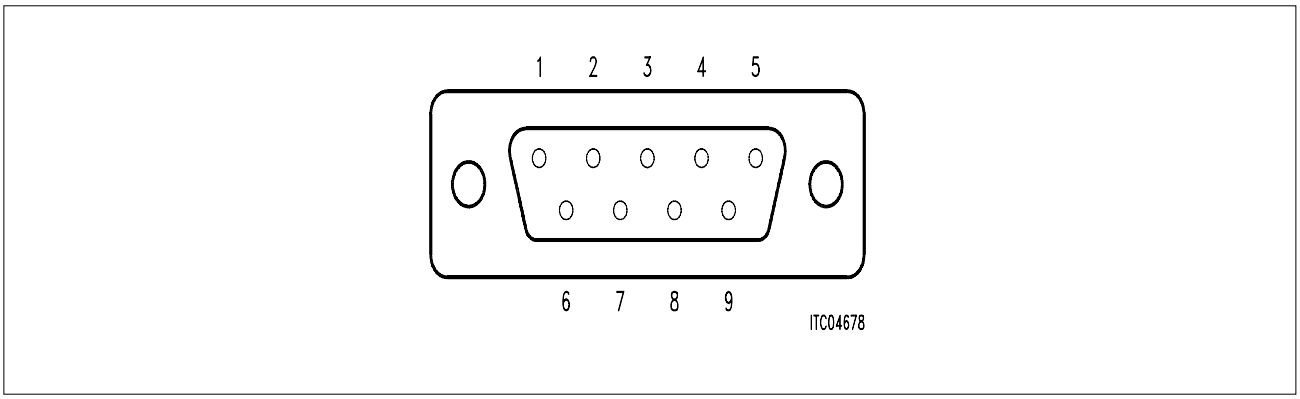

Figure 3
Pin-Outs of the Service Access Connector SAC

Pin	Function
1	Power supply + 5 V
2	Ground GND
3	n. c.
4	DD (Data Downstream)
5	Ringing
6	CLK (512 kHz) /DCL (1.536 MHz)
7	FSC (8 kHz)
8	SIP/DU (Data Upstream)
9	Reset

4.3 Wiring Diagram

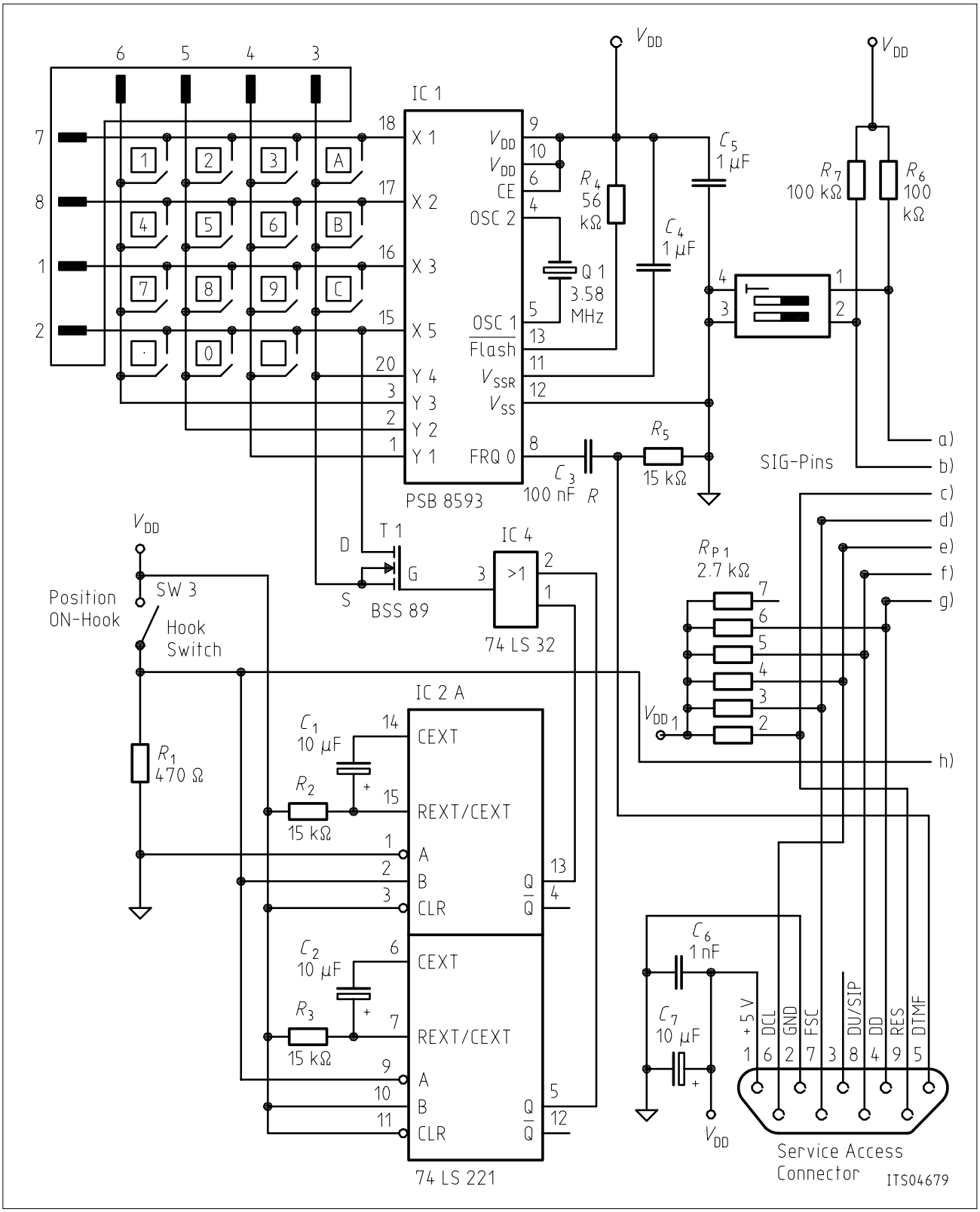

Figure 4a
Wiring Diagram of the ARCOFI®-SP Telephone Board

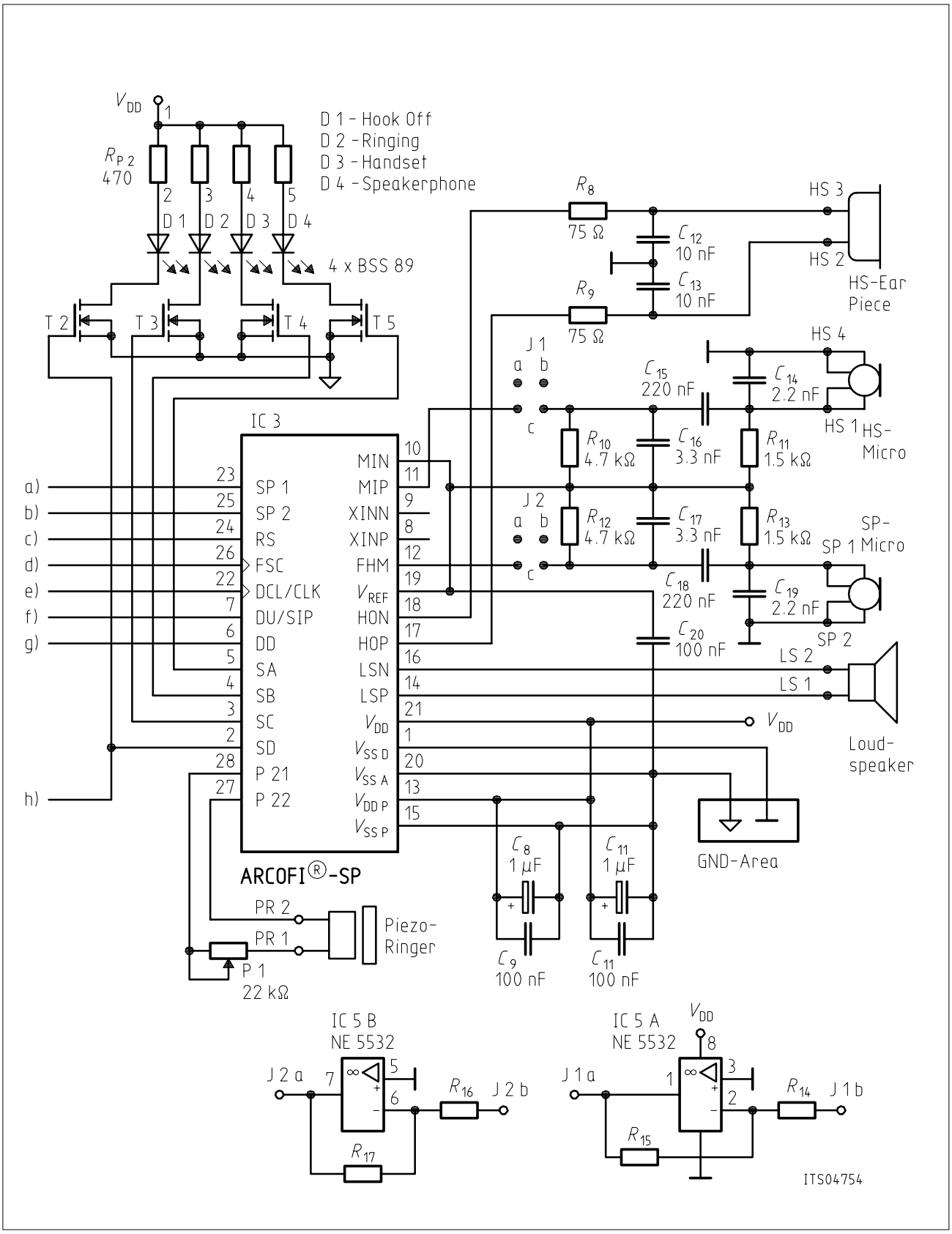

Figure 4b
Wiring Diagram of the ARCOFI®-SP Telephone Board

4.4 List of Replaceable Parts

Component	Outline	Type / Value
IC1	P-DIP-20	PSB 8593
IC2	P-DIP-16	74LS221
IC3	P-DIP-28	PSB2165
IC4	P-DIP-14	74LS32
(IC5	P-DIP-8	NE5532)
T1 … T5	TO92	BSS89
D1 … D4	V300	HLMP1340
Q1	HC18	3.579545 MHz
R_1		470 Ω
R_2, R_3, R_5		15 kΩ
R_4		56 kΩ
R_6, R_7		100 kΩ
R_8, R_9		75 Ω
R_{10}, R_{12}		4.7 kΩ
R_{11}, R_{13}		1.5 kΩ
RP_1		7×2.7 kΩ
RP_2		4×470 Ω
P1	R_{727}	22 kΩ
C_1, C_2		10 µF
C_3		100 µF
C_4, C_5		1 µF
C_6		1 nF
C_7		10 µF
C_8, C_{10}		1 µF
C_9, C_{11}		100 nF
C_{12}, C_{13}		10 nF
C_{14}, C_{19}		2.2 nF
C_{15}, C_{18}		220 nF
C_{16}, C_{17}		3.3 nF
C_{20}		100 nF

4.5 Floor Plan

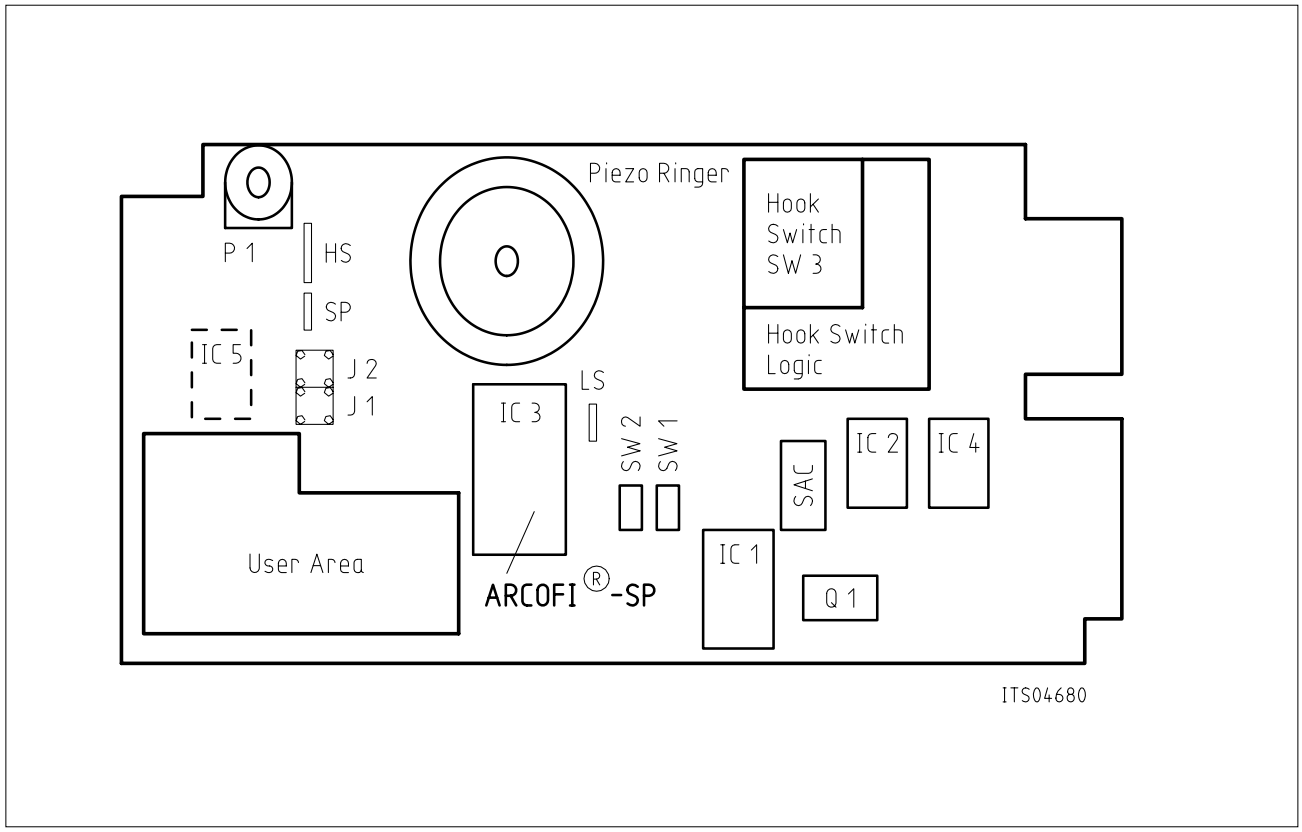

Figure 5
Floor Plan of the ARCOFI®-SP Telephone Board

5 Operational Information

All information about installing the Telephone Board, programming the ARCOFI-SP and the other modules of the set-up in the various configurations is described in this section.

The ARCOFI-SP Telephone Board can be used in two different modes:

- Terminal Equipment TE-Mode
- Network Termination Simulator NT-S-Mode

Configuring the board for a particular mode of operation is done partly by setting switches, and partly by software programming. For the peculiar Menu Software Track Files see section 7.

By setting jumpers accordingly, amplifiers can be inserted in the analog TX-transmission paths.

5.1 Settings of Switches

Two switches are used to configure the ARCOFI-SP Telephone Board for a desired mode of operation. Settings are made before power is applied to the board.

In **figure 6** the positions of switches and their particular functions are depicted.

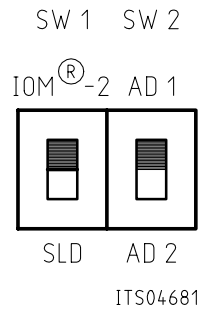

Figure 6
Switches of the ARCOFI®-SP Telephone Board

Switches	Functions
SW1	selects the SLD- or IOM-2(TE)-mode in the ARCOFI-SP
SW2	selects the ARCOFI-SP IOM-2-address, either AD1 or AD2
SW3	Hook Switch

5.2 Settings of Jumpers

Two fields of four jumpers each are provided for inserting an OP-amplifier stage into each of the analog transmit paths if the twin-amplifier IC 5 (NE 5532) is inserted. J1 connects the first amplifier of IC 5 to the handset microphone path while J2 inserts the second one into the speakerphone path.

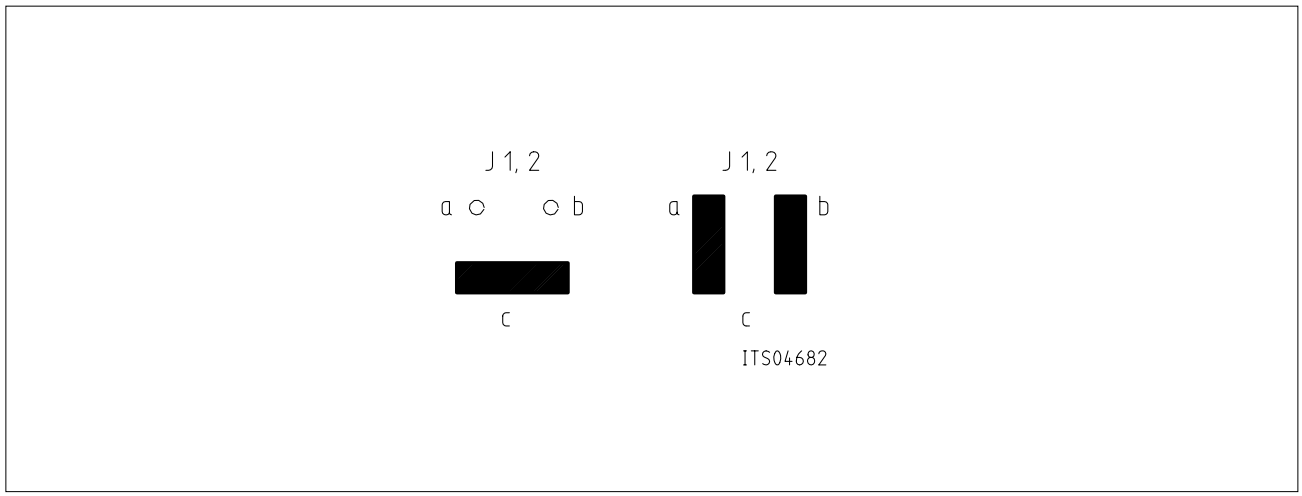

Figure 7
Settings of Jumpers J1 and J2
Left: The OP-Amp is Bypassed.
Right: The OP-Amp is Inserted into the Particular TX-Path.

Attention:

Before starting the initialization procedure with the menu software, please recheck the configuration and switches on the modules to succeed in programming.

Verify that the ARCOFI-SP Telephone Board is always connected to that service access connector that leads to the audio interface module.

5.3 Programming the Peripheral Control Interface (PCI)

According to the hardware configuration of the PCI the configuration register DFICR has to be programmed by

$$DFICR = 8 \times H$$

so that the Hook Switch Detection (SD) is an input while the other three ones (SA, SB, SC) are outputs. The PCI is controlled via CIR1/CIX1 in IOM-2-mode or via SSCR/SSCX in SLD-mode.

5.4 TE-Mode Configuration

In the TE-configuration two serial interface modes – IOM-2 (TE) or SLD – can be used (refer to section 4.1.3).

The configuration described supports both serial interfaces. Just the settings of the DIP-switches select between IOM-2 (TE) – or SLD-mode.

Required hardware:

- a PC-Mainboard SIPB 5000
- an Audio Interface Module V2.0 and up SIPB 5130
  IOM-2: DIP-switches 1 and 2 ON, others OFF
  SLD: DIP-switch 1 ON, others OFF
- any layer-1 and link layer-2 modules
  for example:
  S-Access Module V2.1 SIPB 5100
  IOM-2: DIP-switch 4 ON, others OFF
  SLD: all DIP-switches OFF

For initializing this configuration the track files HS_S02_I.TE (IOM-2-mode) or HS_S02_S.TE (SLD-mode) can be used. These two track files are listed in section 7.

Instead of using the S-Access Module SIPB 5100 any other layer-1 and link layer-2 modules can be used too; if true please verify whether these modules support the serial interface mode.

5.5 NT-S Configuration

In the NT-S configuration only the SLD-mode is defined. The hardware consists of:

- a PC-Mainboard SlPB 5000
- an Audio Interface Module V2.0 and up SIPB 5130
- a Timing Module SIPB 5310
- any layer-1 and link layer-2 modules
  for example:
  S-Access Module V2.1 SIPB 5100
  SLD: DIP-switch 1 ON, others OFF

The track file HS_S0_S.NTS sets up this configuration (see section 7).

Also in this mode, the S-Access Module SIPB 5100 can be replaced by any layer-1 and link layer-2 modules. Please note, that in NT-S-configuration no IOM-2 (TE)-interface mode is defined.

5.6 AC/DC-Characteristics

The complete ARCOFI-SP Telephone Board works on a single + 5 V supply. A few layout hints may be given which are important for a noiseless voice transmission (additional hints may be found in a separate Application Note):

- Provide a large ground (GND) area underneath the ARCOFI-SP PSB 2165 where digital ground V_{SSD} and analog grounds V_{SSA} and V_{SSP} are connected.
- Insert ceramic blocking capacitors at the entry of the Telephone Board and right next to the power pins of the ARCOFI-SP.
- Use sufficient large wire diameters and efficient isolation with the flat cable, which connects the ARCOFI-SP Telephone Board with the Audio Interface Module.
- Separate digital blocks from analog circuitry.

Warning:

CMOS-ICs are very sensitive to electrostatic discharge. Never pull out the SAC-plug at the telephone board before having switched off the power supply.

6 Glossary

ARCOFI-SP	Audio Ringing COdec FIlter with Speakerphone
CCITT	Comité Consultatif International Télégraphe et Téléphone
DC	Direct Current
DD	Data Downstream
DTMF	Dual-Tone Multi-Frequency
DU	Data Upstream
IC	Integrated Circuit
IOM	ISDN-Oriented Modular
ISDN	Integrated Services Digital Network
NT-S	Network Termination Simulator
PC	Personal Computer
PCI	Peripheral Control Interface
PCM	Pulse Code Modulation
PIC	PC-Interface Connector
SAC	Service Access Connector
SIP	Serial Interface Port
SIPB	Siemens ISDN PC-User Board System
SLD	Subscriber Line Digital
TE	Terminal Equipment

7 Menu Software Track Files

7.1 Track File HS_S02_I.TE

```
C ************************************************************************
C ************************************************************************
C *
C * Track File HS_S02_I.TE
C *
C * PROGRAMMING THE ARCOFI-SP VIA IOM2 in HANDSET MODE and additionally
C * ACTIVATING THE S0-INTERFACE
C *
C ************************************************************************
C ------------------------------------------------------------------------
C  ISAC-S in IOM2 mode
C ------------------------------------------------------------------------
W  /S02TE/ISAC_S/SERIAL/ADF2 80
W  /S02TE/ISAC_S/SERIAL/SPCR 80
R  /S02TE/ISAC_S/HDLC/STAR 4A
R  /S02TE/ISAC_S/HDLC/STAR 4A
R  /S02TE/ISAC_S/HDLC/STAR 4A
C ------------------------------------------------------------------------
C  Activation of the S0-Interface
C ------------------------------------------------------------------------
W  /S02TE/ISAC_S/SERIAL/CIX0 60
R  /S02TE/ISAC_S/SERIAL/CIR0 30
R  /S02TE/ISAC_S/SERIAL/CIR0 30
W  /S02TE/ISAC_S/SERIAL/SPCR 05
R  /S02TE/ISAC_S/SERIAL/SPCR 05
C ------------------------------------------------------------------------
C  IOM2-Identification of ARCOFI-SP
C ------------------------------------------------------------------------
W  /S02TE/ISAC_S/SERIAL/MOCR A0
R  /S02TE/ISAC_S/SERIAL/MOSR 00
W  /S02TE/ISAC_S/SERIAL/MOX1 A0
W  /S02TE/ISAC_S/SERIAL/MOCR B0
R  /S02TE/ISAC_S/SERIAL/MOSR 20
W  /S02TE/ISAC_S/SERIAL/MOX1 00
R  /S02TE/ISAC_S/SERIAL/MOSR A0
R  /S02TE/ISAC_S/SERIAL/MOR1 A0
W  /S02TE/ISAC_S/SERIAL/MOCR F0
R  /S02TE/ISAC_S/SERIAL/MOSR 80
R  /S02TE/ISAC_S/SERIAL/MOR1 82
R  /S02TE/ISAC_S/SERIAL/MOSR 40
W  /S02TE/ISAC_S/SERIAL/MOCR A0
R  /S02TE/ISAC_S/SERIAL/MOSR 00
```

```
C ------------------------------------------------------------------------
C  Programming the ARCOFI-SP in HANDSET mode
C ------------------------------------------------------------------------
R  /S02TE/ISAC_S/SERIAL/MOSR 00
W  /S02TE/ISAC_S/SERIAL/MOX1 A1
W  /S02TE/ISAC_S/SERIAL/MOCR B0
R  /S02TE/ISAC_S/SERIAL/MOSR 20
W  /S02TE/ISAC_S/SERIAL/MOX1 1F
R  /S02TE/ISAC_S/SERIAL/MOSR 20
W  /S02TE/ISAC_S/SERIAL/MOX1 00
R  /S02TE/ISAC_S/SERIAL/MOSR 20
W  /S02TE/ISAC_S/SERIAL/MOX1 30
R  /S02TE/ISAC_S/SERIAL/MOSR 20
W  /S02TE/ISAC_S/SERIAL/MOX1 50
R  /S02TE/ISAC_S/SERIAL/MOSR 20
W  /S02TE/ISAC_S/SERIAL/MOX1 00
R  /S02TE/ISAC_S/SERIAL/MOSR 20
W  /S02TE/ISAC_S/SERIAL/MOX1 80

R  /S02TE/ISAC_S/SERIAL/MOSR 20
W  /S02TE/ISAC_S/SERIAL/MOX1 20
R  /S02TE/ISAC_S/SERIAL/MOSR 20
W  /S02TE/ISAC_S/SERIAL/MOX1 82
R  /S02TE/ISAC_S/SERIAL/MOSR 20
W  /S02TE/ISAC_S/SERIAL/MOX1 1B
R  /S02TE/ISAC_S/SERIAL/MOSR 20
C ------------------------------------------------------------------------
C  COP_7: GZL=-00, GZH=-16dB
C ------------------------------------------------------------------------
W  /S02TE/ISAC_S/SERIAL/MOX1 27
R  /S02TE/ISAC_S/SERIAL/MOSR 20
W  /S02TE/ISAC_S/SERIAL/MOX1 97
R  /S02TE/ISAC_S/SERIAL/MOSR 20
W  /S02TE/ISAC_S/SERIAL/MOX1 12
R  /S02TE/ISAC_S/SERIAL/MOSR 20
C ------------------------------------------------------------------------
C  Powering up the ARCOFI-SP
C ------------------------------------------------------------------------
W  /S02TE/ISAC_S/SERIAL/MOX1 10
R  /S02TE/ISAC_S/SERIAL/MOSR 20
W  /S02TE/ISAC_S/SERIAL/MOX1 1E
R  /S02TE/ISAC_S/SERIAL/MOSR 20
W  /S02TE/ISAC_S/SERIAL/MOCR A0
R  /S02TE/ISAC_S/SERIAL/MOSR 00
W  /S02TE/ISAC_S/SERIAL/CIX1 20
```

```
C ------------------------------------------------------------------------
C  Read Out CR: 00, 30, 50, 00
C               80, 20, 82, 1E
C ------------------------------------------------------------------------
W  /S02TE/ISAC_S/SERIAL/MOX1 A1
W  /S02TE/ISAC_S/SERIAL/MOCR B0
R  /S02TE/ISAC_S/SERIAL/MOSR 20
W  /S02TE/ISAC_S/SERIAL/MOX1 9F
R  /S02TE/ISAC_S/SERIAL/MOSR A0
R  /S02TE/ISAC_S/SERIAL/MOR1 A1
W  /S02TE/ISAC_S/SERIAL/MOCR F0
R  /S02TE/ISAC_S/SERIAL/MOSR 80
R  /S02TE/ISAC_S/SERIAL/MOR1 00
R  /S02TE/ISAC_S/SERIAL/MOSR 80
R  /S02TE/ISAC_S/SERIAL/MOR1 30
R  /S02TE/ISAC_S/SERIAL/MOSR 80
R  /S02TE/ISAC_S/SERIAL/MOR1 50
R  /S02TE/ISAC_S/SERIAL/MOSR 80
R  /S02TE/ISAC_S/SERIAL/MOR1 00
R  /S02TE/ISAC_S/SERIAL/MOSR 80
R  /S02TE/ISAC_S/SERIAL/MOR1 80
R  /S02TE/ISAC_S/SERIAL/MOSR 80
R  /S02TE/ISAC_S/SERIAL/MOR1 20
R  /S02TE/ISAC_S/SERIAL/MOSR 80
R  /S02TE/ISAC_S/SERIAL/MOR1 82
R  /S02TE/ISAC_S/SERIAL/MOSR 80
R  /S02TE/ISAC_S/SERIAL/MOR1 1E
R  /S02TE/ISAC_S/SERIAL/MOSR 40
W  /S02TE/ISAC_S/SERIAL/MOCR A0
R  /S02TE/ISAC_S/SERIAL/MOSR 00
C ************************************************************************
C *
C *       End of Track File
C *
C ************************************************************************
C ************************************************************************
```

7.2 Track File HS_S02_S.TE

```
C ************************************************************************
C ************************************************************************
C *
C * Track File HS_S02_S.TE
C *
C * PROGRAMMING THE ARCOFI-SP VIA SLD in HANDSET MODE and
C * additionally ACTIVATING THE S0 - INTERFACE
C *
C ************************************************************************
C ************************************************************************
C
C ------------------------------------------------------------------------
C  Activation of the S0-interface
C ------------------------------------------------------------------------
W  /S02TE/ISAC_S/SERIAL/CIX0 60
R  /S02TE/ISAC_S/SERIAL/CIR0 30
R  /S02TE/ISAC_S/SERIAL/CIR0 30
W  /S02TE/ISAC_S/SERIAL/SPCR 45
R  /S02TE/ISAC_S/SERIAL/SPCR 45
C ------------------------------------------------------------------------
C  Programming the ARCOFI-SP in HANDSET mode
C ------------------------------------------------------------------------
B  1F
B  00
B  30
B  50
B  00
B  80
B  E0
B  82
B  1A
X  /S02TE/ISAC_S/BUS/CONTR
C ------------------------------------------------------------------------
C  COP_5: GX= 00dB
C ------------------------------------------------------------------------
D
B  25
B  A0
B  01
X  /S02TE/ISAC_S/BUS/CONTR
```

```
C-------------------------------------------------------------------------
C  COP_6: GRL= 00dB, GRH= 00dB
C-------------------------------------------------------------------------
D
B  26
B  A0
B  01
B  A0
B  01
X  /S02TE/ISAC_S/BUS/CONTR
C-------------------------------------------------------------------------
C  COP_7: GZL=-54dB, GZH=-16dB
C-------------------------------------------------------------------------
D
B  27
B  97
B  12
X  /S02TE/ISAC_S/BUS/CONTR
C-------------------------------------------------------------------------
C  Powering up the ARCOFI-SP
C-------------------------------------------------------------------------
D
B  10
B  1E
X  /S02TE/ISAC_S/BUS/CONTR
W  /S02TE/ISAC_S/SERIAL/SSCX 20
C-------------------------------------------------------------------------
C  Read Out CR: 00, 30, 50, 00
C               80, E0, 82, 1E
C-------------------------------------------------------------------------
R  /S02TE/ISAC_S/BUS/CONTR 9F 08
A  0030 5000 80E0 821E
C
C*************************************************************************
C*************************************************************************
C*
C*    End of Track File
C*
C*************************************************************************
C*************************************************************************
```

7.3 Track File SP_S02_S.TE

```
C ************************************************************************
C ************************************************************************
C *
C * Track File SP_S02_S.TE
C *
C * PROGRAMMING THE ARCOFI-SP VIA SLD in SPEAKERPHONE MODE and
C * additionally ACTIVATING THE S0 - INTERFACE
C *
C ************************************************************************
C ************************************************************************
C
C ------------------------------------------------------------------------
C  Activation of the S0-interface
C ------------------------------------------------------------------------
W  /S02TE/ISAC_S/SERIAL/CIX0 60
R  /S02TE/ISAC_S/SERIAL/CIR0 30
R  /S02TE/ISAC_S/SERIAL/CIR0 30
W  /S02TE/ISAC_S/SERIAL/SPCR 45
R  /S02TE/ISAC_S/SERIAL/SPCR 45
C ------------------------------------------------------------------------
C  Programming the ARCOFI-SP in SPEAKERPHONE mode
C ------------------------------------------------------------------------
D
B  1F
B  00
B  02
B  62
B  00
B  80
B  00
B  83
B  BA
X  /S02TE/ISAC_S/BUS/CONTR
```

```
C ------------------------------------------------------------------------
C  COP_B: SDX
C ------------------------------------------------------------------------
D
B  2B
B  E1
B  34
B  D3
B  75
B  26
B  F2
B  20
B  44
X  /S02TE/ISAC_S/BUS/CONTR
C ------------------------------------------------------------------------
C  COP_C: SDR
C ------------------------------------------------------------------------
D
B  2C
B  E1
B  34B D3
B  00
B  26
B  F2
B  20
B  44
C ------------------------------------------------------------------------
C  COP_D: ATTENUATION CONTROL
C ------------------------------------------------------------------------
D
B  2D
B  35
B  2B
B  04
B  FF
X  /S02TE/ISAC_S/BUS/CONTR
W  /S02TE/ISAC_S/SERIAL/SSCX 10
C ------------------------------------------------------------------------
C  COP_E: AGCX
C ------------------------------------------------------------------------
D
B  2E
B  14
B  13
B  15
B  80
```

```
C-------------------------------------------------------------------------
C  COP_F: LGA
C-------------------------------------------------------------------------
D
B  2F
B  90
B  00
B  00
B  00
X  /S02TE/ISAC_S/BUS/CONTR
C-------------------------------------------------------------------------
C  Powering up the ARCOFI-SP
C-------------------------------------------------------------------------
D
B  10
B  BE
X  /S02TE/ISAC_S/BUS/CONTR
C-------------------------------------------------------------------------
C  Read Out CR: 00, 02, 62, 00
C               80, 00, 83, BE
C-------------------------------------------------------------------------
R   /S02TE/ISAC_S/BUS/CONTR 9F 08
A  0002 6200 8000 83BE
C
C*************************************************************************
C*************************************************************************
C*
C*     End of Track File
C*
C*************************************************************************
C*************************************************************************
```

7.4 Track File HS_S0_S.NTS

```
C ************************************************************************
C ************************************************************************
C *
C * Track File HS_S0_S.NTS
C *
C * PROGRAMMING THE ARCOFI-SP VIA SLD in HANDSET MODE and
C * additionally ACTIVATING THE S0 - INTERFACE
C *
C ************************************************************************
C ************************************************************************
C
C ------------------------------------------------------------------------
C  Activation of the S0-interface
C ------------------------------------------------------------------------
W  /S02NTS/ISAC_S/SERIAL/CIX0 60
R  /S02NTS/ISAC_S/SERIAL/CIR0 30
R  /S02NTS/ISAC_S/SERIAL/CIR0 30
W  /S02NTS/ISAC_S/SERIAL/SPCR 45
R  /S02NTS/ISAC_S/SERIAL/SPCR 45
C ------------------------------------------------------------------------
C  Programming the ARCOFI-SP in HANDSET mode
C ------------------------------------------------------------------------
D
B  1F
B  00
B  30
B  50
B  00
B  80
B  E0
B  82
B  1A
X  /S02NTS/ISAC_S/BUS/CONTR
C ------------------------------------------------------------------------
C  COP_5: GX= 00dB
C ------------------------------------------------------------------------
B  A0
B  01
X  /S02NTS/ISAC_S/BUS/CONTR
```

```
C-------------------------------------------------------------------------
C  COP_6: GRL= 00dB, GRH= 00dB
C-------------------------------------------------------------------------
D
B  26
B  A0
B  01
B  A0
B  01
X  /S02NTS/ISAC_S/BUS/CONTR
C-------------------------------------------------------------------------
C  COP_7: GZL=-54dB, GZH=-16dB
C-------------------------------------------------------------------------
D
B  27
B  97
B  12
X  /S02NTS/ISAC_S/BUS/CONTR
C-------------------------------------------------------------------------
C  Powering up the ARCOFI-SP
C-------------------------------------------------------------------------
D
B  10
B  1E
B  /S02NTS/ISAC_S/BUS/CONTR
B  /S02TE/ISAC_S/SERIAL/SSCX 20
C-------------------------------------------------------------------------
C  Read Out CR: 00, 30, 50, 00
C               80, E0, 82, 1E
C-------------------------------------------------------------------------
R   /S02NTS/ISAC_S/BUS/CONTR 9F 08
A  0030 5000 80E0 821E
C
C*************************************************************************
C*************************************************************************
C*
C*    End of Track File
C*
C*************************************************************************
C*************************************************************************
```

Using the SIPB 5132-SP Telephone with the PSB 2163

Vakat

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1 Introduction

About this Application Note

The SIPB 5132-SP telephone[1)] is a telephone for evaluation purposes, showing all features of the ARCOFI-SP PSB 2165 and PSB 2163. This telephone is equipped with the ARCOFI-SP PSB 2165 and the explanations given in the documentation of the SIPB 5132-SP telephone are related to the PSB 2165.

With the PSB 2163 a pin compatible device is available, which offers a completely new speakerphone support. The speakerphone implementation of the PSB 2163 has superior performance and enables the telephone user to have very comfortable speakerphone to speakerphone discussions.

The SIPB 5132-SP telephone can be used with both ICs, with the PSB 2165 (with which it comes along) and with the PSB 2163 (which can be build into the telephone).

This document describes how to replace the PSB 2165 with the PSB 2163. This is not an instruction that stipulates each step that must be taken, this is rather an explanation of the things to be taken into account when replacing the PSB 2165 with the PSB 2163.

Differences between PSB 2165 and PSB 2163 Concerning the SIPB 5132-SP Telephone

For a detailed description of the two ICs, please refer to the user's manual of the PSB 2165 and the user's manual of the PSB 2163. This paragraph only gives information about differences that can affect the external hardware circuitry. Basically, both ARCOFI-SPs are fully pin compatible and replacing is possible without any difficulties.

The interface modes that can be used with the PSB 2165 are the IOM-2 TE interface (1.536 MHz), and the SLD interface. Together with the PSB 2163 and the SIPB 5132-SP telephone, the IOM-2 TE interface can be used as well as the IOM-2 NON-TE interface (4.096 MHz).

There is a difference concerning the function of the PCI-interface pins (pin SA, SB, SC, SD) between the two ARCOF-SPs; see **table 1** for details.

1 Ordering Code Q67100-H6299

A slight change concerns the names of the microphone inputs. Although the functionality is the same, the names are different as **table 2** shows.

Table 1
Use of the Pins SA, SB, SC, SD

Device	Interface	Meaning of Pins SA, SB, SC, SD
2165	IOM-2 TE	PCI-interface; SA, SB can also be used to connect test LEDs
2165	SLD	PCI-interface; SA, SB can also be used to connect test LEDs
2163	IOM-2 TE	PCI-interface; (test LEDs can be connected to the PZ1, PZ2 pin)
2163	IOM-2 NON-TE	SB, SC, SD used for slot select; SA unused (V_{SS}); (test LEDs can be connected to the PZ1, PZ2 pin)

Table 2
Microphone Inputs

Pin	PSB 2165	PSB 2163	Used for (SIPB 5132-SP)
8	XINP	MIP1	Not connected
9	XINN	MIN1	Not connected
10	MIN	MIN2	Handset microphone
11	MIP	MIP2	
12	FHM (single-ended)	MI3 (single-ended)	Hands-free microphone

2 Using the SIPB 5132-SP Telephone with the PSB 2163 in IOM-2 TE Mode

The basic steps to be performed are quite simple:

- Open the telephone case
- Replace the PSB 2165 with the PSB 2163
- Switch the DIP-switch according to **table 3**
- Close the telephone case

Normally, the PSB 2163 is not only used in handset mode but also as a speakerphone, therefore the speakerphone test mode is of interest, which indicates the internal status of the speakerphone with the help of two LEDs. As **table 1** shows, with the PSB 2163 this internal status information is outputted at the PZ-pins (pin 27, 28). Inside the SIPB 5132-SP telephone, the piezo-ringer is connected to these pins. With regard to the schematic of the telephone, the following steps have to be performed for a proper connection of the test LEDs:

- Adjust the volume potentiometer for the piezo ringer to the lowest volume or disconnect the piezo ringer (otherwise you hear a "click" each time the LEDs are turned on or off)
- Connect pin 27 (PZ2) with the gate of (e.g.) T4
- Connect pin 28 (PZ1) with the gate of (e.g.) T5 (see schematic)

Now the pins SA, SB (pin 5 and 4), which are normally connected to the gates of T4 and T5, must always be programmed as inputs (default) to avoid a short circuit at the PZ pins. Of course, pin 4 and 5 can also be disconnected. Note, that pin SD is used for hook switch detection and therefore T2/D1 should not be used for the test LEDs.

Table 3
DIP-switch Inside the SIPB 5132-SP Telephone, Equipped with the PSB 2163

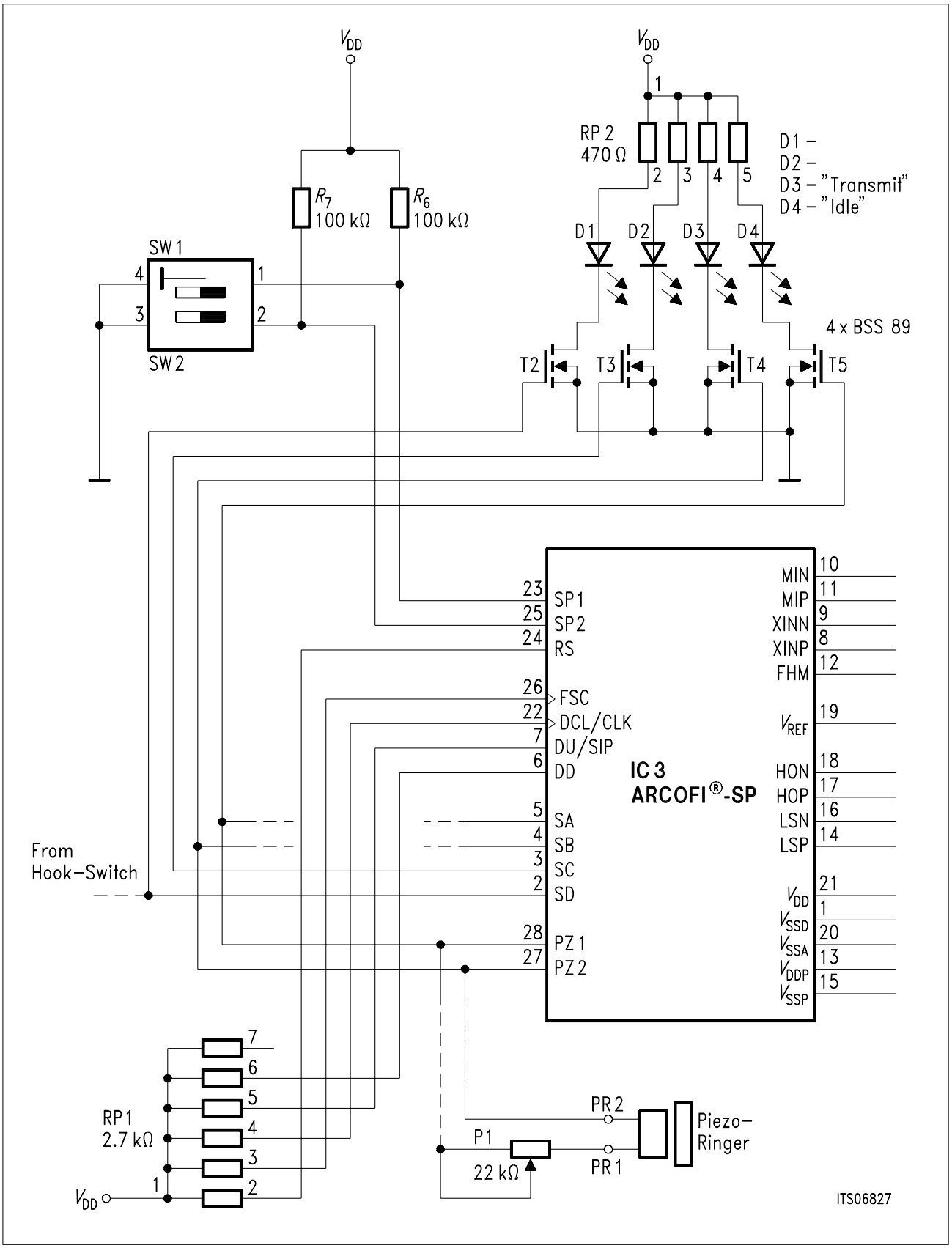
SW1	SW2	Mode
ON	ON	IOM-2 TE, A-Chip
ON	OFF	IOM-2 TE, B-Chip
OFF	ON	IOM-2 NON-TE, A-Chip
OFF	OFF	IOM-2 NON-TE, B-Chip

3 Using the SIPB 5132-SP Telephone with the PSB 2163 in IOM-2 NON-TE Mode

The 4.096 MHz-IOM-2 mode offers the possibility to connect the PSB 2163 directly to a LineCard-Module or for measuring purposes. Since this IOM-2 mode offers eight channels, the pins SB, SC, SD serve as slot-select inputs, as mentioned in **table 1**. A useful solution is to connect all slot-select pins to V_{CC} (+ 5 V), thus making the ARCOFI-SP use channel 7. This is also appropriate for the ARCOS-SP PLUS software.

In addition to the steps explained in **chapter 2**, the best way is to solder pull-up resistors (4k7) at the pins 2, 3, 4 (SB, SC, SD). Note, that when using the IOM-2 NON-TE mode the state of the hook switch can not be transmitted in the C/I-channel. The wire between pin 2 (SD) and the hook switch (SW3) must be disconnected.

Because of the high clock frequency (4 MHz) the flat-band cable between the SIPB 5132-SP telephone and the rest of the test equipment should be as short as possible. Tests have shown that the SIPB 5132-SP with its 1m cable can interface with the SIPB 5130 Audio-Module or the STUT 2000 PERCOFI-Board without any problems. However, in case of troubleshooting, the length is critical and must be taken into account.



Changes for the PSB 2163

Evaluation Board ARCOFI®-SP V1.0 SIPB 5133-SP

- VAKATSEITE -

Evaluation Board ARCOFI®-SP V1.0 SIPB 5133-SP

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1 Introduction

The development of analog front-ends for voice transmission in ISDN-terminals poses enormous efforts to the system houses. The engineers in fulfilling the very strict requirements of the CCITT are to solve these problems partly by experience and partly by following a trial and error procedure.

The Evaluation Board ARCOFI-SP SIPB 5133-SP helps in developing analog front-ends. It offers the possibility to experiment on pure analog transmission parts and to investigate the transmission functions very comfortably in using a PCM4-measuring device by Wandel & Goltermann.

The integration of the Evaluation Board ARCOFI-SP into the SIPB-system with its peculiar software renders developing and adapting a voice transmission part to simplify connecting a module: No protocols need be taken notice of and no specific adapter circuitries for testing the ARCOFI-SP are to be developed any longer.

2 Features

- Comfortable measuring aid for evaluating various transmission functions:
- Transfer Functions
- Gain Tracking
- Signal / Noise Ratio
- Group Delay
- Enables testing the proper adaptation via programmed FX- and FR-filters of the ARCOFI-SP of electro-acoustic transducers
- Programmable via IOM-2 without need for noticing any protocols
- Suitable for IOM-2 TE mode and IOM-2 NON TE mode
- All analog inputs and outputs and the digital signals SA, SB, SC, SD of the ARCOFI-SP connected to the Audio Interface Connector (AIC)
- Power supply (+ 5 V) selectable from the PC or from an external network, programmable via one jumper J1.

3 Use

The use of the Evaluation Board ARCOFI-SP is identical to that of a standard ISDN-Telephone Board. Due to the flexible concept of the user board system it can be employed either as an analog front-end or as a measurement front-end in a terminal equipment (TE) configuration or in a line-card architecture using the IOM-2 NON TE interface.

The Evaluation Board ARCOFI-SP is always connected to the Audio Interface Module via the IOM-interface. **Figure 1** shows, how and in what combination it is connected via a flat cable to the mainboard.

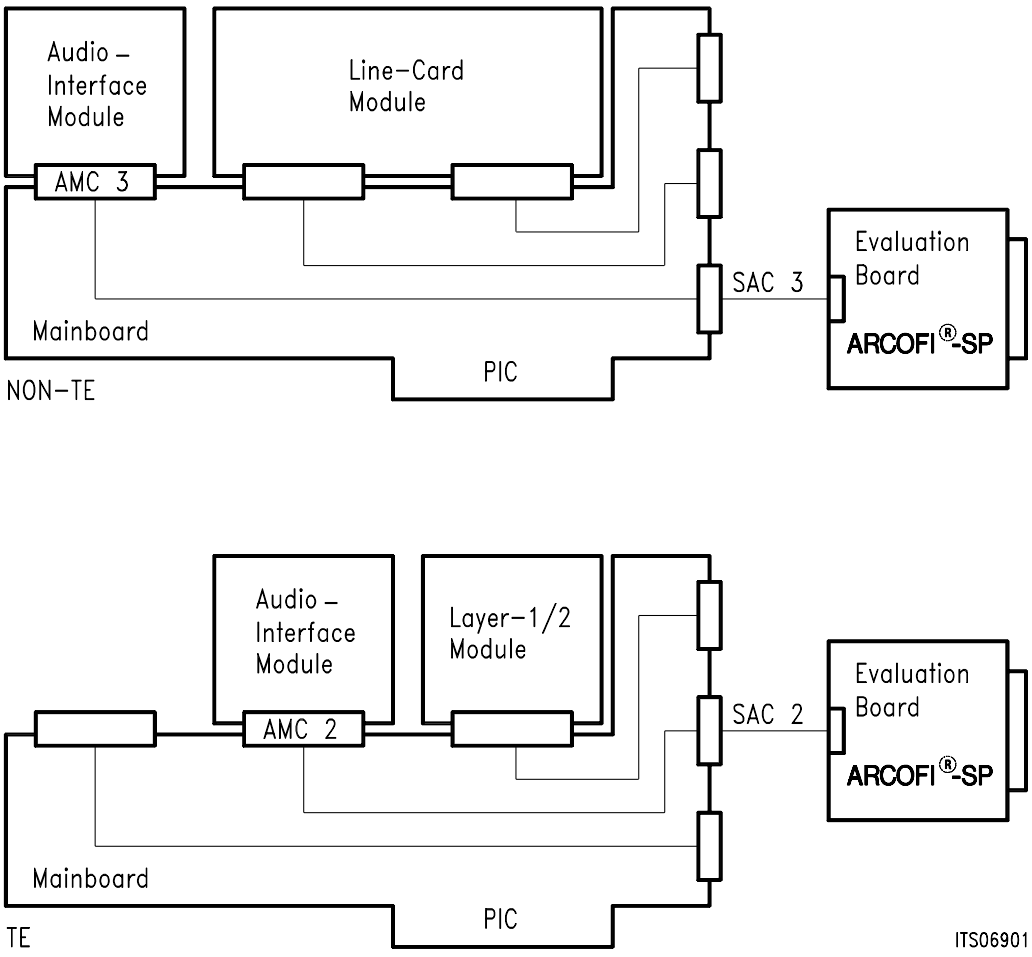

Figure 1
Examples of Two Terminal Configurations in the User Board Concept

4 Circuitry

The circuitry of the Evaluation Board ARCOFI-SP can be divided into a digital and an analog part.

The digital part consists of:

- ARCOFI-SP IC1 (PSB 2163 or PSB 2165)

The analog part is realized in form of an Audio Interface Connector (AIC) where all listed signals are accessible:

- Analog inputs: MIN1, MIP1
  MIN2, MIP2
  MI3
- Analog outputs: HOP, HON
  LSP, LSN
- Reference voltage: V_{REF}
- Digital signals: SA, SB, SC, SD
- Power supply: + 5 V, GND

In addition means for DC blocking is included. By means of the jumper the power supply for the analog front-end can be chosen: + 5 V from the PC or from a separate, external power supply.

The push button switch SW3 resets the whole circuitry by resetting the ARCOFI-SP. The different interface modes and the hardware address can be selected by switches S1 and S2 of SW1 for the ARCOFI-SP.

4.1 Connector Pin-Outs

4.1.1 Service Access Connector SAC

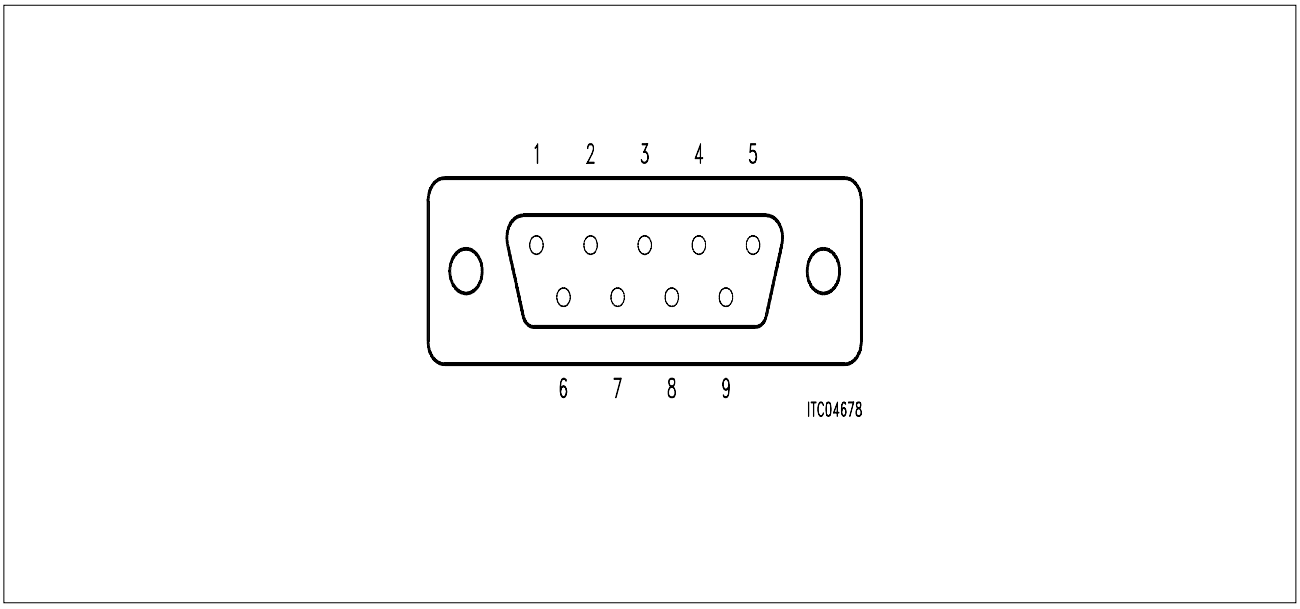

Figure 2
Pin-Outs of the Service Access Connector SAC

Pin	Function
1	Power supply + 5 V
2	GND
3	n.c.
4	DD
5	n.c.
6	DCL (1.536 MHz / 4.096 MHz)
7	FSC (8 kHz)
8	DU
9	Reset

4.1.2 Audio Interface Connector AIC

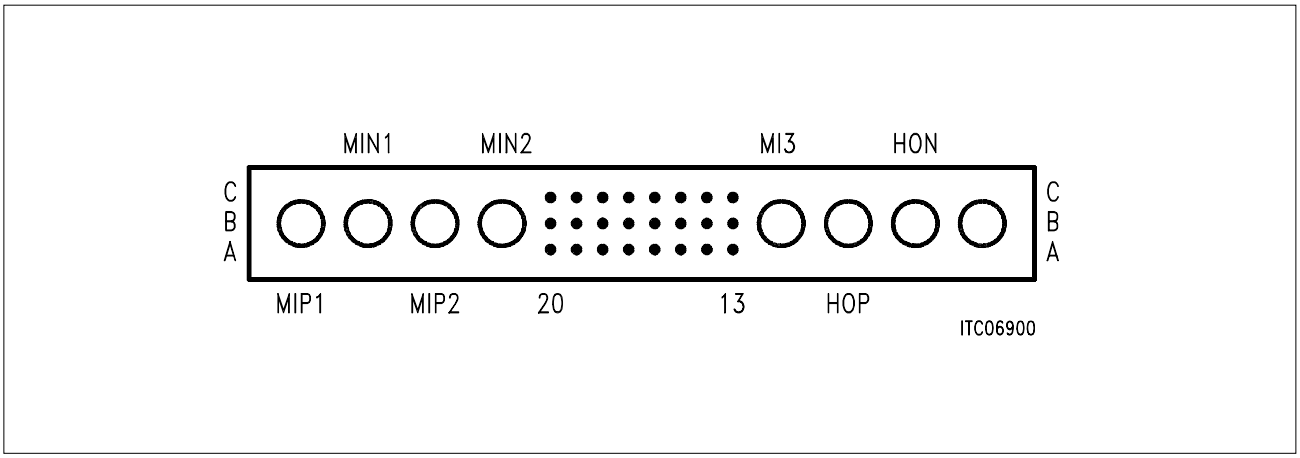

Figure 3
Pin-Outs of the Audio Interface Connector AIC

Pin/Row	A	B	C
13	V_{REF}	V_{REF}	V_{REF}
14	SD	x	x
15	SA	SB	SC
16	+ 5 VA	+ 5 VA	LSP
17	x	x	LSN
18	+ 5 VD	+ 5 VD	x
19	GNDA	GNDA	x
20	x	GNDD	GNDD

x = not connected

4.1.3 External Power Supply Connector EXC

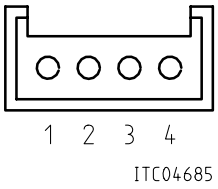

Figure 4
Pin-Outs of the External Power Supply Connector ST1

Pin	Function
1	+ 5 V
2	GND
3	GND
4	X (reserved)

4.1.4 Handset Connector

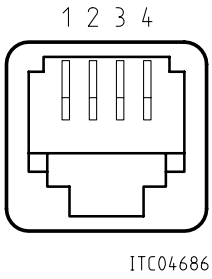

Figure 5
Handset Connector

Pin	Function
1	MIP
2	HOP
3	HON
4	MIN

4.2 Wiring Diagram

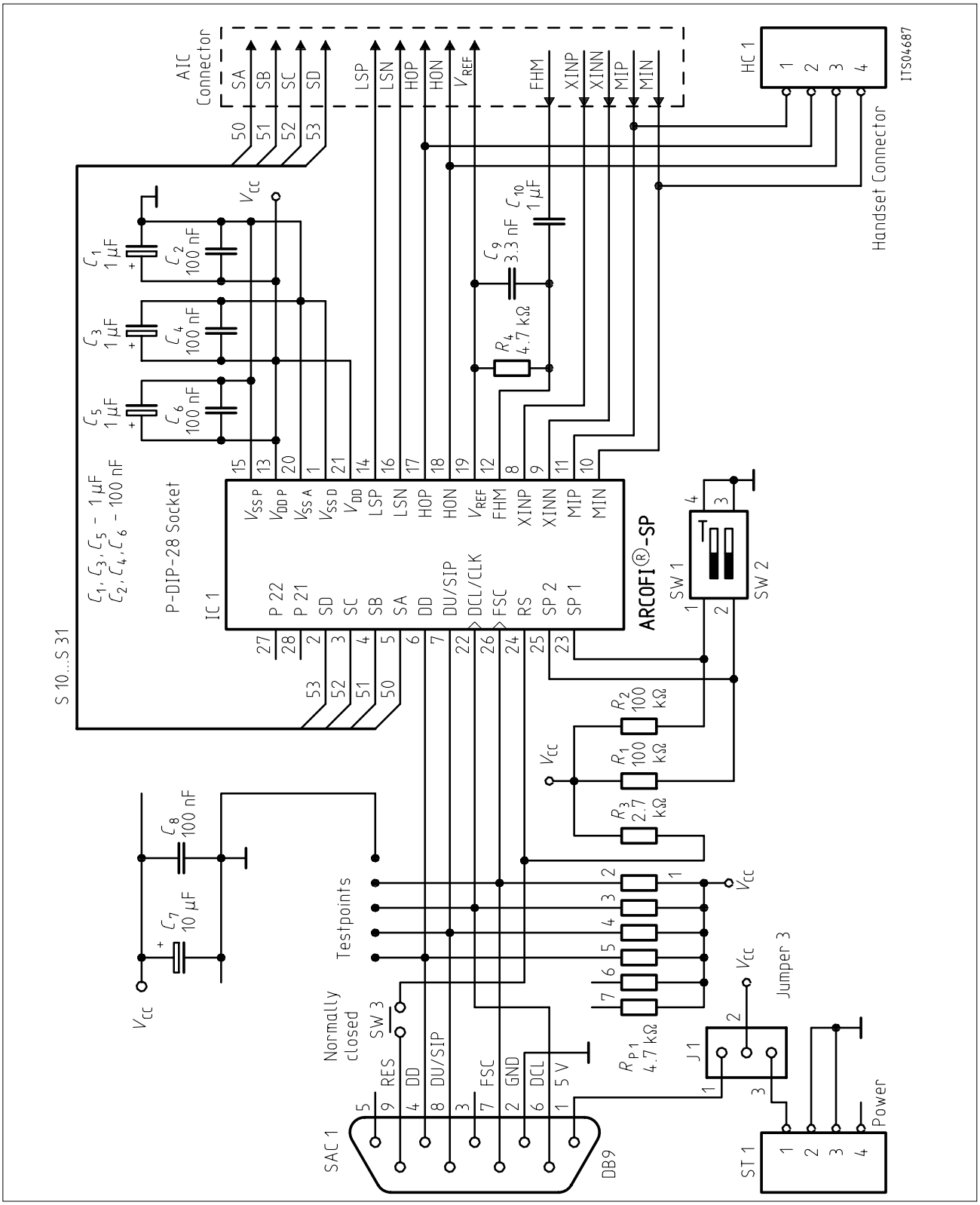

Figure 6
Wiring Diagram of the Evaluation Board ARCOFI®-SP

4.3 List of Replaceable Parts

Component	Outline	Type / Value
IC1	P-DIP-28 F	PSB 2165 (replacable with PSB 2163)
R_1, R_2	RR1	100 kΩ
R_3	RR1	2.7 kΩ
R_4	RR1	4.7 kΩ
R_{P1}	DNET 6	2.7 kΩ
C_1, C_3, C_5, C_7, C_9	XTANT	1 µF/16 V
C_2, C_4, C_6, C_8, C_{10}	CRM 2 + 5	100 nF
C_{11}	X7R	3.3 nF/16 V
C_{12}	MKT	1 µF
C_{13}	XTANT	10 µF
C_{14}	CRM 2 + 5	100 nF
SW1	P-DIP-4	SWITCH
SW3		SWITCH
SAC	CAN9	
ST1		Power Connector

4.4 Floor Plan

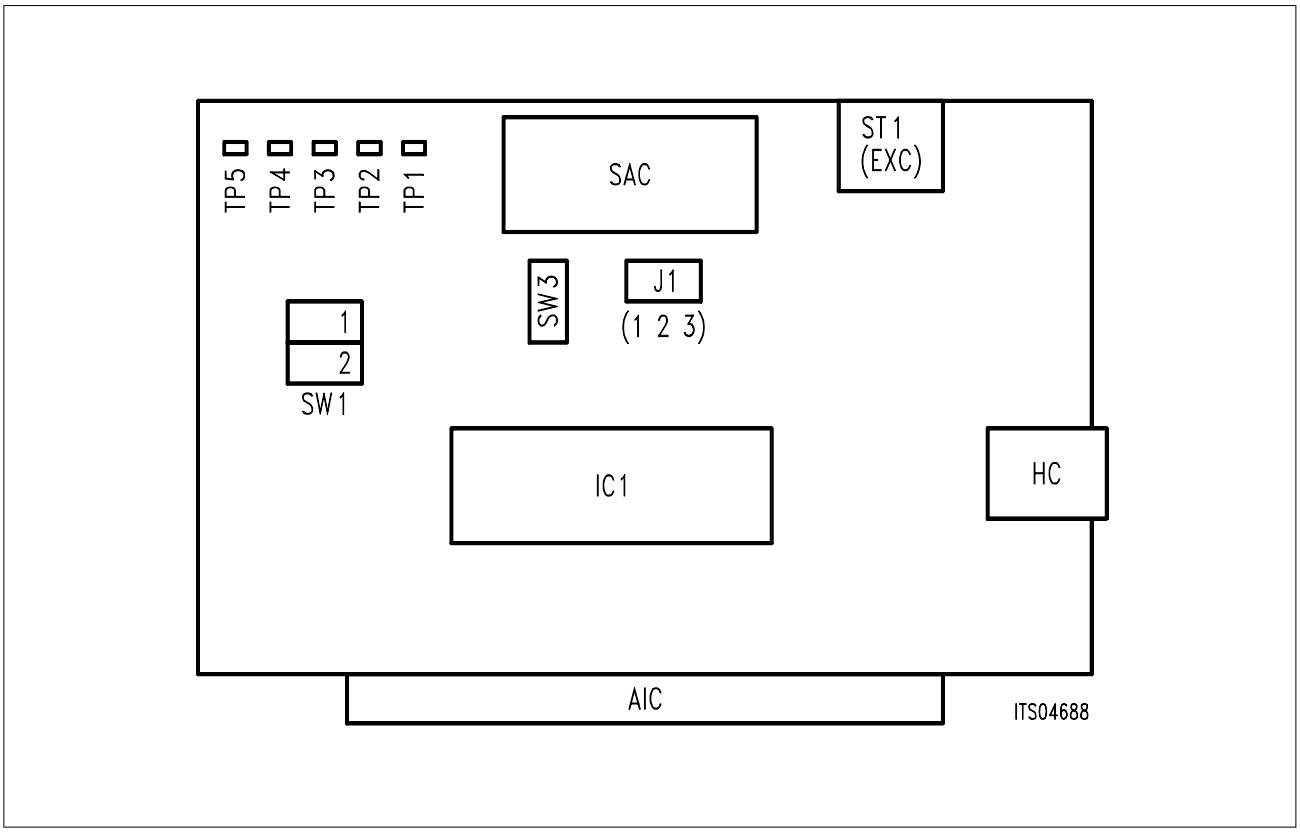

Figure 7
Floor Plan of the Evaluation Board ARCOFI®-SP

5 Operational Information

All information about installing the Evaluation Board ARCOFI-SP, programming the ARCOFI-SP and the other modules of the set-up in various configurations, are described in this chapter.

For programming the set-up using the menu software track files see **chapter 7**. These configurations can also be programmed by the ARCOS-SP Plus software. For more details on ARCOS-SP Plus refer to “ARCOS-SP Plus User Manual V 1.0”.

5.1 Setting Switches

There are three switches at the Evaluation Board ARCOFI-SP. The push button switch SW3 is to reset the whole circuitry by resetting the ARCOFI-SP. Switches S1 and S2 of SW1 select the interface mode (IOM-2 TE or IOM-2 NON TE) and the hardware address (AD0 or AD1) of the ARCOFI-SP respectively. The particular settings are depicted in the table below.

S1	S2	Function
ON	ON	IOM-2 TE mode (A-chip)
ON	OFF	IOM-2 TE mode (B-chip)
OFF	ON	IOM-2 NON TE mode (A-chip)
OFF	OFF	IOM-2 NON TE mode (B-chip)

5.2 Setting Jumper

One jumper J1 is used to select the power supply: If the power is taken from the PC, jumper J1 is set to position 1-2 (towards SW3). If an external power source is connected via the external power supply connector ST1, jumper J1 is set to position 2-3 (towards ST1).

5.3 Configuring the Evaluation Board ARCOFI®-SP

The Evaluation Board ARCOFI-SP can be used in two different interface modes:

- IOM-2 TE; terminal timing (1.536 MHz DCL))
- IOM-2 NON TE; non terminal timing (4.096 MHz DCL)

Attention:

When using the non terminal timing mode (IOM-2 NON TE) the timeslot must be determined by hardwiring the pins SD, SC, SB (pins 2,3,4). By default, these pins are not connected on the SIPB 5133-SP Evaluation Board. Refer to the User’s Manual, **chapter 2.3.2** “IOM-2 Frame Structure and Timing Modes” for more detailed information.

Before starting the initialization procedure using the menu software, please recheck the configuration and the jumpers on the modules to succeed in programming. For IOM-2 NON TE mode, one of the eight timeslot has to be set. Note that the Evaluation Board ARCOFI-SP has always to be connected to that service access connector of the mainboard that leads to the audio interface module (**see also figure 1**).

5.3.1 IOM-2 TE-Mode Configuration

This configuration consists of:

- a **PC-Mainboard** SIPB 5000
- an **Audio Interface Module** SIPB 5130
  DIP-switches S01, S02 set to ON; S03, S04 set to OFF
- a **S-Access Module** SIPB 5100
  DIP-switches S01, S02, S03 set to OFF; S04 set to ON

The whole initialization procedure of this configuration is listed in the track file named "HS_S02_I.TE" in the appendix.

5.3.2 IOM-2 NON-TE-Mode Configuration

This mode needs:

- a **PC-Mainboard** SIPB 5000
- an **Audio Interface Module** SIPB 5130
- a **LineCard Module** SIPB 5121
- a **S-Access Module** SIPB 5100
  DIP-switch S02 is set to ON, others OFF (open);

To set this configuration two track files have to be used. The file “LC_1.IOM” provides a general setup for the EPIC on the LineCard-Module and must be run first. Afterwards either “HS_LC.TRK” can be used to program the handset mode or “LC_PCM4.TRK” to prepare measurements with the PCM4 measurement device from Wandel&Goltermann.

Note, that due to the high transmission frequency on the IOM-2 NON TE bus, the length of the flat band cable between the Audio Interface Module and the Evaluation Board is critical and should not exceed 0.5 meters.

5.4 AC/DC-Characteristics

Important for a noiseless voice transmission and ideal test results are:

- A big ground area underneath the ARCOFI-SP, where digital ground GNDD and analog ground GNDA are connected.
- Blocking capacitors at every IC and at the entry of the evaluation board.
- The flat cable, which connects the ARCOFI-SP Evaluation Board with the audio interface module, has to be of a big cross section and of a good isolation.
- The analog signal lines on the adapter boards should be well screened.

Attention:

CMOS-ICs are very sensible on electrostatic discharge. Never pull out the SAC-plug at the ARCOFI-SP Evaluation Board before switching off the power supply.

5.5 Connectable Adapter Boards

To the Evaluation Board ARCOFI-SP various adapter boards can be connected via the Audio Interface Connector AIC.

- In connection with the Loudhearing Adapter Board SIPB 5133 LH the evaluation board meets all basic functions for voice transmission. On this board there are four pins for connecting a German type handset, and a special connector for joining a US American type handset. In addition the signals LSN and LSP are accessible for connecting a loudspeaker.

6 Glossary

AIC	Audio Interface Connector
ARCOFI	Audio Ringing COdec Filter
DTMF	Dual Tone Multi Frequency
EPIC	Extended PCM Interface Controller PEB 2055
EXC	EXternal power supply Connector
FHM	Free Hand Microphone
FR	Filter in Receive direction
FX	Filter in Transmit direction
GNDA	Ground Analog
GNDD	Ground Digital
GND – 5 VA	Ground for the – 5 V Analog Voltage
GND + 5 VA	Ground for the + 5 V Analog Voltage
HAC	Hands-free Add-on Circuit
HOP, HON	Handset Output Positive / Negative
HS	Handset
IOM	ISDN-Oriented Modular
ISDN	Integrated Services Digital Network
LSP, LSN	Loudspeaker Output Positive / Negative
MIP, MIN	Microphone Input Positive / Negative
PCM4	Measurement Device for PCM channels from Wandel&Goltermann
PIC	PC-Interface Connector
SAC	Service Access Connector
SIPB	Siemens ISDN PC-User Board System
TE	Terminal Equipment
XINP, XINN	Auxiliary Input Positive / Negative
VA	Voltage Analog
VD	Voltage Digital

7 Menu Software Track Files

7.1 Track File HS_S02_I.TE

```
C ************************************************************************
C ************************************************************************
C *
C *  Trackfile  HS_S02_I.TE
C *
C *  Programming the ARCOFI-SP PSB 2163 in HANDSET Mode
C *  and additionally activating the S0 interface
C *
C *  !! COSI /2 MUST BE RUN BEFORE !!
C *
C ************************************************************************
C ************************************************************************
C
C ------------------------------------------------------------------------
C ISAC-S in IOM2 mode
C ------------------------------------------------------------------------
C
W /S02TE/ISAC_S/SERIAL/ADF2 80
W /S02TE/ISAC_S/SERIAL/SPCR 80
R /S02TE/ISAC_S/HDLC/STAR 4A
R /S02TE/ISAC_S/HDLC/STAR 4A
R /S02TE/ISAC_S/HDLC/STAR 4A
C
C ------------------------------------------------------------------------
C Activation of the S0 - interface
C ------------------------------------------------------------------------
C
W /S02TE/ISAC_S/SERIAL/CIX0 60
R /S02TE/ISAC_S/SERIAL/CIR0 30
R /S02TE/ISAC_S/SERIAL/CIR0 30
W /S02TE/ISAC_S/SERIAL/SPCR 05
R /S02TE/ISAC_S/SERIAL/SPCR 05
C
C ------------------------------------------------------------------------
C IOM2 - Identification of ARCOFI-SP
C ------------------------------------------------------------------------
C
R /S02TE/ISAC_S/BUS/MON1 A000 01
A A084
C
C ------------------------------------------------------------------------
C Programming the ARCOFI-SP in HANDSET mode
C ------------------------------------------------------------------------
```

```
D
B A11F
B 0060
B 4100
B 0020
B F112
X /S02TE/ISAC_S/BUS/MON1
C
C ------------------------------------------------------------------------
C COP_6: GZ=-15dB
C ------------------------------------------------------------------------
D
B A126
B 9932
X /S02TE/ISAC_S/BUS/MON1
C
C ------------------------------------------------------------------------
C Powering up the ARCOFI-SP
C ------------------------------------------------------------------------
D
B A131
X /S02TE/ISAC_S/BUS/MON1
W /S02TE/ISAC_S/SERIAL/CIX1 20
C
C ------------------------------------------------------------------------
C Read Out CR: 00, 60, 41, 00
C              00, 20, F1, 16
C ------------------------------------------------------------------------
C
R /S02TE/ISAC_S/BUS/MON1 A19F 05
A A100 6041 0000 20F1 16FF
C
C ************************************************************************
C ************************************************************************
C *
C *         End of Track File
C *
C ************************************************************************
C ************************************************************************
```

7.2 Track File LC_1.IOM

```
C*********************************************************************
C              LC_1.IOM
C*********************************************************************
C
C application: initialization of the line card module
C              for a SICOFI2/ARCOFI-SP measurement
C setup:       line card module SIPB 5121
C
C iom2 channel assignement:
C * ch0: analog subscriber (sicofi2)
C * ch1: analog subscriber (sicofi2)
C * ch2: analog subscriber (sicofi2)
C * ch3: analog subscriber (sicofi2)
C * ch4: analog subscriber (sicofi2)
C * ch5: analog subscriber (sicofi2)
C * ch6: analog subscriber (sicofi2)
C * ch7: analog subscriber (sicofi2)
C
C interface characteristics:
C pcm interface: 2 hws with 32 ts each
C cfi interface: 4 hws with 32 ts each
C                (4 iom2 interfaces)
C
C configuration of the lc module:
C config register bits:
C id,cks/tc2/tc1/tc0/dch/dma/cts/res
C * clock mode 6 (xtal 4096khz)
C * reset of on board devices
W /LINECA/CONFIG/CONFIG/CONFIG 61
W /LINECA/CONFIG/CONFIG/CONFIG 60
C
C configuration of the pcm interface:
C * pcm mode 0
W /LINECA/EPIC/PCMCFI/PMOD 20
W /LINECA/EPIC/PCMCFI/PCSR 11
W /LINECA/EPIC/PCMCFI/POFD F1
W /LINECA/EPIC/PCMCFI/POFU 19
C
C configuration of the cfi interface:
C * cfi mode 0, clock source: pcl/pfs
C * pfs evaluated with falling edge
C * prescaler = 1
W /LINECA/EPIC/PCMCFI/CMD1 20
C * fsc output: fc mode 6
C * dcl output: double rate
```

```
C * xmit rising, rec falling edge
W /LINECA/EPIC/PCMCFI/CMD2 D0
C * cfi bit number is 256
W /LINECA/EPIC/PCMCFI/CBNR FF
C * pfs marks cfi ts31,bit1
W /LINECA/EPIC/PCMCFI/CTAR 02
C * no shift between xmit and rec
W /LINECA/EPIC/PCMCFI/CBSR 00
C * subchannel position:64kbps=bits7.0
C                       32kbps=bits7.4
C                       16kbps=bits7.6
W /LINECA/EPIC/PCMCFI/CSCR 00
C
C initialization of cm ctrl field:
C * cm reset mode
W /LINECA/EPIC/MARSCR/OMDR 00
C * ff is copied to all positions of
C * the cm ctrl field
W /LINECA/EPIC/MARSCR/MADR FF
W /LINECA/EPIC/MARSCR/MACR 70
C
C cfi configuration for iom2:
C * cm init mode
W /LINECA/EPIC/MARSCR/OMDR 80
C
C cfi timeslots  2 and  3 of port 0
C are programmed as monitor and
C signaling channels (analog iom)
C * ts  2 downstream:
W /LINECA/EPIC/MARSCR/MADR FF
W /LINECA/EPIC/MARSCR/MAAR 08
W /LINECA/EPIC/MARSCR/MACR 7A
C * ts  3 downstream:
W /LINECA/EPIC/MARSCR/MAAR 09
W /LINECA/EPIC/MARSCR/MACR 7B
C * ts  2 upstream:
W /LINECA/EPIC/MARSCR/MAAR 88
W /LINECA/EPIC/MARSCR/MACR 7A
C * ts  3 upstream:
W /LINECA/EPIC/MARSCR/MAAR 89
W /LINECA/EPIC/MARSCR/MACR 7A
C
C cfi timeslots  6 and  7 of port 0
C are programmed as monitor and
C signaling channels (analog iom)
C * ts  6 downstream:
W /LINECA/EPIC/MARSCR/MADR FF
```

```
W /LINECA/EPIC/MARSCR/MAAR 18
W /LINECA/EPIC/MARSCR/MACR 7A
C * ts  7 downstream:
W /LINECA/EPIC/MARSCR/MAAR 19
W /LINECA/EPIC/MARSCR/MACR 7B
C * ts  6 upstream:
W /LINECA/EPIC/MARSCR/MAAR 98
W /LINECA/EPIC/MARSCR/MACR 7A
C * ts  7 upstream:
W /LINECA/EPIC/MARSCR/MAAR 99
W /LINECA/EPIC/MARSCR/MACR 7A
C
C cfi timeslots 10 and 11 of port 0
C are programmed as monitor and
C signaling channels (analog iom)
C * ts 10 downstream:
W /LINECA/EPIC/MARSCR/MADR FF
W /LINECA/EPIC/MARSCR/MAAR 28
W /LINECA/EPIC/MARSCR/MACR 7A
C * ts 11 downstream:
W /LINECA/EPIC/MARSCR/MAAR 29
W /LINECA/EPIC/MARSCR/MACR 7B
C * ts 10 upstream:
W /LINECA/EPIC/MARSCR/MAAR A8
W /LINECA/EPIC/MARSCR/MACR 7A
C * ts 11 upstream:
W /LINECA/EPIC/MARSCR/MAAR A9
W /LINECA/EPIC/MARSCR/MACR 7A
C cfi timeslots 14 and 15 of port 0
C are programmed as monitor and
C signaling channels (analog iom)
C * ts 14 downstream:
W /LINECA/EPIC/MARSCR/MADR FF
W /LINECA/EPIC/MARSCR/MAAR 38
W /LINECA/EPIC/MARSCR/MACR 7A
C * ts 15 downstream:
W /LINECA/EPIC/MARSCR/MAAR 39
W /LINECA/EPIC/MARSCR/MACR 7B
C * ts 14 upstream:
W /LINECA/EPIC/MARSCR/MAAR B8
W /LINECA/EPIC/MARSCR/MACR 7A
C * ts 15 upstream:
W /LINECA/EPIC/MARSCR/MAAR B9
W /LINECA/EPIC/MARSCR/MACR 7A
C cfi timeslots 18 and 19 of port 0
C are programmed as monitor and
C signaling channels (analog iom)
```

```
C * ts 18 downstream:
W /LINECA/EPIC/MARSCR/MADR FF
W /LINECA/EPIC/MARSCR/MAAR 48
W /LINECA/EPIC/MARSCR/MACR 7A
C * ts 19 downstream:
W /LINECA/EPIC/MARSCR/MAAR 49
W /LINECA/EPIC/MARSCR/MACR 7B
C * ts 18 upstream:
W /LINECA/EPIC/MARSCR/MAAR C8
W /LINECA/EPIC/MARSCR/MACR 7A
C * ts 19 upstream:
W /LINECA/EPIC/MARSCR/MAAR C9
W /LINECA/EPIC/MARSCR/MACR 7A
C cfi timeslots 22 and 23 of port 0
C are programmed as monitor and
C signaling channels (analog iom)
C * ts 22 downstream:
W /LINECA/EPIC/MARSCR/MADR FF
W /LINECA/EPIC/MARSCR/MAAR 58
W /LINECA/EPIC/MARSCR/MACR 7A
C * ts 23 downstream:
W /LINECA/EPIC/MARSCR/MAAR 59
W /LINECA/EPIC/MARSCR/MACR 7B
C * ts 22 upstream:
W /LINECA/EPIC/MARSCR/MAAR D8
W /LINECA/EPIC/MARSCR/MACR 7A
C * ts 23 upstream:
W /LINECA/EPIC/MARSCR/MAAR D9
W /LINECA/EPIC/MARSCR/MACR 7A
C cfi timeslots 26 and 27 of port 0
C are programmed as monitor and
C signaling channels (analog iom)
C * ts 26 downstream:
W /LINECA/EPIC/MARSCR/MADR FF
W /LINECA/EPIC/MARSCR/MAAR 68
W /LINECA/EPIC/MARSCR/MACR 7A
C * ts 27 downstream:
W /LINECA/EPIC/MARSCR/MAAR 69
W /LINECA/EPIC/MARSCR/MACR 7B
C * ts 26 upstream:
W /LINECA/EPIC/MARSCR/MAAR E8
W /LINECA/EPIC/MARSCR/MACR 7A
C * ts 27 upstream:
W /LINECA/EPIC/MARSCR/MAAR E9
W /LINECA/EPIC/MARSCR/MACR 7A
C cfi timeslots 30 and 31 of port 0
C are programmed as monitor and
```

```
C signaling channels (analog iom)
C * ts 30 downstream:
W /LINECA/EPIC/MARSCR/MADR FF
W /LINECA/EPIC/MARSCR/MAAR 78
W /LINECA/EPIC/MARSCR/MACR 7A
C * ts 31 downstream:
W /LINECA/EPIC/MARSCR/MAAR 79
W /LINECA/EPIC/MARSCR/MACR 7B
C * ts 30 upstream:
W /LINECA/EPIC/MARSCR/MAAR F8
W /LINECA/EPIC/MARSCR/MACR 7A
C * ts 31 upstream:
W /LINECA/EPIC/MARSCR/MAAR F9
W /LINECA/EPIC/MARSCR/MACR 7A
C * pcm status is
R /LINECA/EPIC/MARSCR/STAR 05
C * not synchronized (pss=0)
C
C setting epic to normal mode
W /LINECA/EPIC/MARSCR/OMDR C0
R /LINECA/EPIC/MARSCR/ISTA 08
R /LINECA/EPIC/MARSCR/STAR 25
C pcm status: synchronized (pss=1)
C
C initialization of the pcm tristate
C field, all ch. to high impedance
W /LINECA/EPIC/MARSCR/MADR 00
W /LINECA/EPIC/MARSCR/MACR 68
C
C activation epic:
C * normal mode, pcm and cfi active
C * cfi output drivers push-pull
C * mf ch. handshake protocol enabled
W /LINECA/EPIC/MARSCR/OMDR E6
C
C reset cififo:
W /LINECA/EPIC/MARSCR/CMDR 10
C ***************************************************************
C
C the line card is now ready for use with the SICOFI2 or the ARCOFI-SP
C
C Now you can run your trackfile with the filter coefficients or
C program the ARCOFI-SP
C
C ***************************************************************
C end of trackfile
C ***************************************************************
```

7.3 Track File HS_LC.TRK

```
C*************************************************************************
C*************************************************************************
C
C  Track File HS_LC.TRK
C
C  Programming the ARCOFI-SP PSB 2163
C  via IOM-2 NON-TE in Handset Mode
C
C  !! Trackfile LC_1.IOM has to be run before !!
C
C  Configuration:
C  -------------
C  LineCard     SIPB 5121
C  Audio Module SIPB 5130
C               DIP-Switch 1 ON
C                          2 ON
C                          3 OFF
C                          4 ON
C
C*************************************************************************
C*************************************************************************
C
C-------------------------------------------------------------------
C Connecting the LineCard to the Audio Interface Module
C-------------------------------------------------------------------
C
W /LINECA/CONFIG/CONFIG/CONFIG E0
C
C-------------------------------------------------------------------
C Selecting the timeslot
C (depends on the pins SB,SC,SD)
C Here: slot 7 (all pins to VCC)
C
C MFSAR = 04  => slot 0
C MFSAR = 0C  => slot 1
C MFSAR = 14  => slot 2
C MFSAR = 1C  => slot 3
C MFSAR = 24  => slot 4
C MFSAR = 2C  => slot 5
C MFSAR = 34  => slot 6
C MFSAR = 3C  => slot 7
C-------------------------------------------------------------------
C
W /LINECA/EPIC/MCHSTR/MFSAR 3C
C
```

```
C-------------------------------------------------------------------
C ARCOFI-SP Identification
C-------------------------------------------------------------------
W /LINECA/EPIC/MCHSTR/CMDR 01
W /LINECA/EPIC/MCHSTR/MFFIFO A0
W /LINECA/EPIC/MCHSTR/MFFIFO 00
W /LINECA/EPIC/MCHSTR/CMDR 08
R /LINECA/EPIC/MCHSTR/ISTA 20
R /LINECA/EPIC/MCHSTR/STAR 26
R /LINECA/EPIC/MCHSTR/MFFIFO A0
R /LINECA/EPIC/MCHSTR/STAR 26
R /LINECA/EPIC/MCHSTR/MFFIFO 84
W /LINECA/EPIC/MCHSTR/CMDR 01
C
C-------------------------------------------------------------------
C COP_6: GZ=-15dB
C-------------------------------------------------------------------
W /LINECA/EPIC/MCHSTR/MFFIFO A1
W /LINECA/EPIC/MCHSTR/MFFIFO 26
W /LINECA/EPIC/MCHSTR/MFFIFO 99
W /LINECA/EPIC/MCHSTR/MFFIFO 32
W /LINECA/EPIC/MCHSTR/MFFIFO 00
W /LINECA/EPIC/MCHSTR/MFFIFO 00
W /LINECA/EPIC/MCHSTR/CMDR 04
W /LINECA/EPIC/MCHSTR/CMDR 01
C
C-------------------------------------------------------------------
C SOP_F: Handset Mode
C-------------------------------------------------------------------
W /LINECA/EPIC/MCHSTR/MFFIFO A1
W /LINECA/EPIC/MCHSTR/MFFIFO 1F
W /LINECA/EPIC/MCHSTR/MFFIFO 00
W /LINECA/EPIC/MCHSTR/MFFIFO 60
W /LINECA/EPIC/MCHSTR/MFFIFO 41
W /LINECA/EPIC/MCHSTR/MFFIFO 00
W /LINECA/EPIC/MCHSTR/MFFIFO 00
W /LINECA/EPIC/MCHSTR/MFFIFO 20
W /LINECA/EPIC/MCHSTR/MFFIFO F1
W /LINECA/EPIC/MCHSTR/MFFIFO 16
W /LINECA/EPIC/MCHSTR/CMDR 04
W /LINECA/EPIC/MCHSTR/CMDR 01
C
C*******************************************************************
C*
C* End of Track File
C*
C*******************************************************************
```

7.4 Track File LC_PCM4.TRK

```
C*********************************************************************
C
C  Track File LC_PCM4.TRK
C
C  Preparing the ARCOFI-SP PSB 2163 for PCM4 measurements
C
C  Trackfile LC_1.IOM has to
C  be run before !
C
C  Configuration:
C  -------------
C  LineCard     SIPB 5121
C  Audio Module SIPB 5130
C               DIP-Switch 1 ON
C                          2 ON
C                          3 OFF
C                          4 ON
C  PCM4 Adapter SIPB 5311
C               Jumper open
C
C*********************************************************************
C
C---------------------------------------------------------------------
C Connecting the LineCard to the Audio Interface Module
C---------------------------------------------------------------------
C
W /LINECA/CONFIG/CONFIG/CONFIG E0
C
C---------------------------------------------------------------------
C Selecting the timeslot (depends on the pins SB,SC,SD)
C Here: slot 7 (all pins to VCC)
C---------------------------------------------------------------------
C
W /LINECA/EPIC/MCHSTR/MFSAR 3C
C
C---------------------------------------------------------------------
C B-channel switching for the PCM4 Adaptor
C B1 -> TS1
C B2 -> TS2
C---------------------------------------------------------------------
C
W /LINECA/EPIC/MARSCR/MADR 0F
W /LINECA/EPIC/MARSCR/MAAR 81
W /LINECA/EPIC/MARSCR/MACR 60
C
```

```
W /LINECA/EPIC/MARSCR/MADR 0F
W /LINECA/EPIC/MARSCR/MAAR 88
W /LINECA/EPIC/MARSCR/MACR 60
C
W /LINECA/EPIC/MARSCR/MADR 81
W /LINECA/EPIC/MARSCR/MAAR F0
W /LINECA/EPIC/MARSCR/MACR 71
C
W /LINECA/EPIC/MARSCR/MADR 01
W /LINECA/EPIC/MARSCR/MAAR 70
W /LINECA/EPIC/MARSCR/MACR 71
C
W /LINECA/EPIC/MARSCR/MADR 88
W /LINECA/EPIC/MARSCR/MAAR F1
W /LINECA/EPIC/MARSCR/MACR 71
C
W /LINECA/EPIC/MARSCR/MADR 08
W /LINECA/EPIC/MARSCR/MAAR 71
W /LINECA/EPIC/MARSCR/MACR 71
C
C-----------------------------------------------------------------------
C ARCOFI-SP Identification
C-----------------------------------------------------------------------
C
W /LINECA/EPIC/MCHSTR/CMDR 01
W /LINECA/EPIC/MCHSTR/MFFIFO A0
W /LINECA/EPIC/MCHSTR/MFFIFO 00
W /LINECA/EPIC/MCHSTR/CMDR 08
R /LINECA/EPIC/MCHSTR/ISTA 20
R /LINECA/EPIC/MCHSTR/STAR 26
R /LINECA/EPIC/MCHSTR/MFFIFO A0
R /LINECA/EPIC/MCHSTR/STAR 26
R /LINECA/EPIC/MCHSTR/MFFIFO 84
W /LINECA/EPIC/MCHSTR/CMDR 01
C
C-----------------------------------------------------------------------
C Insert now the desired programming sequence for the PSB 2163
C-----------------------------------------------------------------------
C
C***********************************************************************
C***********************************************************************
C*
C* End of Track File
C*
C***********************************************************************
C***********************************************************************
```

ARCOFI®-SP Coefficients Software ARCOS-SP and ARCOS-SP PLUS SIPO 2163 V1.0

Table of Contents **Page**

1 Introduction

1.1 The ARCOFI®-SP PSB 2163

The PSB 2163 provides the subscriber with an optimized Audio, Ringing, Codec, Filter processor solution for a digital telephone. The ARCOFI-SP fulfils all the necessary requirements for a full-featured digital telephone including handsfree operation. The ARCOFI-SP performs all coding, decoding and filtering according to CCITT and ETSI standards. The outstanding advantage of the PSB 2163 is the high performance speakerphone implementation with the "stronger-wins algorithm" that allows almost a full duplex conversation.

Due to the completely digital concept of the circuit no external components are required. The various filters and processing steps of the voice channel including the speakerphone, the signalling, and the tone generation can be adapted to meet the different operating conditions by means of software. Also adapting different acoustical transducers to the ARCOFI-SP is accomplished simply by programming registers and coefficients.

Therefore evaluating the features and the high performance of the PSB 2163 is an easy thing if some software is available to program the chip. An important task of the ARCOS-SP PLUS software is to offer an quick and easy way for evaluation.

1.2 The ARCOS-SP PLUS Software

The ARCOS-SP PLUS program has been designed to generate all the required coefficients and to program the ARCOFI-SP in a real environment. Besides the software offers an easy way to get familiar with the internal structure of the ARCOFI-SP because all functional blocks are displayed in a graphic form with many possibilities of interaction (switches, parameters, registers that can be clicked upon).

Note: The ARCOS-SP PLUS software is also available as a demonstration software. The demo-version is called ARCOS-SP (instead of ARCOS-SP PLUS). This user’s manual describes ARCOS-SP PLUS but is also used as a manual for ARCOS-SP. However, certain commands are not possible with the demo-version and cause an error message ("ARCOS-SP does not support this command...").

The demonstration software ARCOS-SP does not support any kind of hardware access. That means, it is neither possible to load or save files nor to access the ARCOFI-SP with the help of the SIPB userboards or any other hardware. Because this restriction is easily understood, there will be no further hints throughout this manual that describe, what things can not be done with the demo-version. The calculation of all the coefficients is possible with ARCOS-SP since this requires no hardware access.

Features of the ARCOS-SP PLUS Software

ARCOS-SP PLUS supports the calculation and programming of

- Coefficients for the ARCOFI-SP digital speakerphone
- Coefficients for the three ARCOFI-SP tone generation registers
- Coefficients for the ARCOFI-SP DTMF tone generator registers
- Coefficients for both ARCOFI-SP programmable gain registers GX and GR
- Coefficients for the GZ side tone gain register
- Coefficients for the FX and FR correction filter registers;
  adaptive software calculates coefficients to fit a target frequency response

ARCOS-SP PLUS supports also the configuration registers and offers an user-friendly dialogue mode allowing full programming of the ARCOFI-SP configuration registers and the coefficient RAM (CRAM).

Other features simplify working with the ARCOFI-SP:

- Access to different kinds of hardware (see **chapter 4** for details)
- NOTE and EXECUTE (a kind of keyboard macro)
- READ ARCOFI and WRITE ARCOFI
- Support of transmission measurements using the Wandel&Goltermann PCM4 measuring instrument

It is highly recommended to have an PSB 2163 User's Manual at hand when working with the ARCOS-SP PLUS software. It is recommended to use the manual as a reference when working with ARCOS-SP or ARCOS-SP PLUS software. On the other hand, not all coefficients are documented in detail in the User's Manual of the PSB 2163 and the ARCOS-SP PLUS or the ARCOS-SP software allow easy determination of all coefficients.

1.3 System Requirements

An IBM or compatible Personal Computer (AT or better) is required. The computer should have at least 400 kByte of free conventional DOS memory. DOS version 3.2 or newer is required. The usage of a mouse as an input device is recommended and offers access to all features of the user area. A mouse driver must be installed before calling the ARCOS-SP PLUS software.

For hardware access the SIEMENS ISDN PC Board (SIPB) system is required. The SIPB family consists of a mainboard (SIPB 5000) and a wide variety of modules to realize different applications. The following equipment is needed:

- A Mainboard SIPB 5000
- Any Layer-1 module SIPB 511x
- Any Layer-2 module SIPB 512x
- An Audio Interface Module SIPB 5130, EPROM version 2.0 or newer
- As well as one of the following modules containing the ARCOFI-SP:
- An ARCOFI-SP Telephone SIPB 5132-SP[1)]
- An ARCOFI-SP Evaluation Board SIPB 5133-SP

The SIPB 5133-SP is an ARCOFI-SP Evaluation Board used for measurement purposes. The SIPB 5132-SP is an ARCOFI-SP Telephone used for demonstration and teaching purposes.

The ARCOS-SP PLUS software not only supports the SIPB 5000 system, but also some evaluation boards that have serial interfaces. These are:

- SIPB 8051 ISDN Telephone and Terminal Adapter Development Board,
- SISI 2197 SmartLink Board,
- STUT 2000 PERCOFI-Board.

The setups for the different kinds of hardware are described in **chapter 4**.

1.4 Installation and Activation of ARCOS-SP PLUS

Installation

The following simple procedure is recommended for the installation of ARCOS-SP PLUS on a hard-disc:

Create ARCOS-SP directory: `md c:\ARCOS-SP`

Change to ARCOS-SP directory: `cd ARCOS-SP`

Copy ARCOS-SP files: `copy a:*.* c:\ARCOS-SP\*.*`

At least the following files should have been copied:

- ARC63.EXE, the main program (ARC63D.EXE for the ARCOS-SP software)
- ARC63.TAB, data file (ARC63D.TAB for the ARCOS-SP software)
- RS232.INI, initialization file for the serial interface
- MSHERC.COM (hercules driver; only necessary if the system is equipped with a Hercules monochrome graphics card)

The program MSHERC.COM loads a Hercules driver resident in the RAM. When using a Hercules graphics card, this program must be called before starting ARCOS-SP PLUS.

The file ARC63.INI (ARC63D.INI) is generated by ARCOS-SP itself, it is not delivered with the program.

[1] These telephones are equipped with an PSB 2165 which can be replaced with an PSB 2163 (refer to the App. Note "Using the SIPB 5132-SP Telephone with the PSB 2163")

Starting ARCOS-SP PLUS

Enter the following DOS command to start ARCOS-SP:

`ARC63 [File[.xxx]]`

`[File[.xxx]]` is an optional initialization file. The initialization file contains information about the last hardware settings and the options chosen (see **chapter 4**). As default, the file `ARC63.INI` is used as initialization file.

Please note, that the ARCOS-SP PLUS software must be started with a special option when using external hardware which is controlled via the serial interface (command line switch /V; this is described in **chapter 4.3**).

After having started ARCOS-SP PLUS the following is carried out:

- Loading the initialization file,
- Loading the coefficient file,
- Showing the ARCOS-SP PLUS main menu and the SIEMENS label (once a day),
- After a mouse click or carriage return the SIEMENS label will disappear.

The next step to be done is either to disable any hardware access or to initialize the hardware.

2 Using ARCOS-SP PLUS

2.1 Introduction

When working with ARCOS-SP PLUS the screen is divided into four main areas (please compare with **figure 1**):

- Row 1 is reserved for the menu line
- Rows 2 to 23 are for the User Area
- Row 24 contains the command line
- Row 25 is the status line.

All items that can be activated via the menu line are described in **chapter 2.2**. The user area is controlled with a mouse and allows to program the whole ARCOFI-SP (**chapter 2.3**). Everything that can be done with the mouse in the user area can also be done via the command line using the keyboard. The syntax for the command line can be found in **chapter 2.4**.

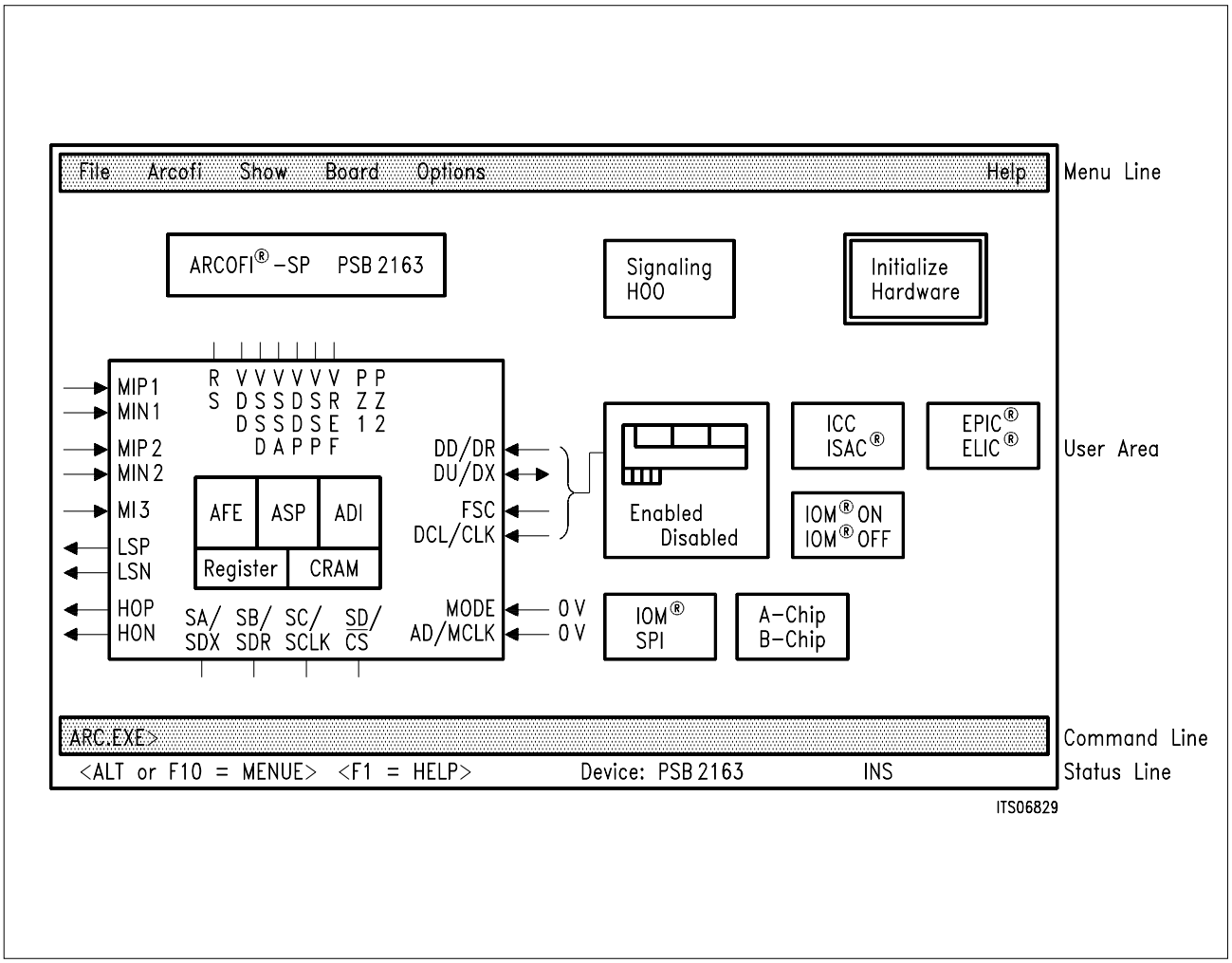

Figure 1
ARCOS-SP PLUS Screen

2.2 The Menu Line

2.2.1 Using the Menu Line

The menu items can always be activated by pressing either the F10-key or the ALT-key in combination with the highlightened letter of the menu item (e.g. "ALT+O" for the options menu). Of course, clicking with the left mouse button is also possible. The subsequent paragraphs describe each menu item.

2.2.2 Pull-Down Menu "File"

"Load"

The name of the file to be loaded has to be entered in the input field or can be selected in the file list. The command to load a file will be aborted if an incorrect, non-existent file name is entered. Both kinds of files: *.ARC and *.ARB are loadable (refer to the next paragraph). This menu item is used to restore a previously saved set of coefficients.

The load command can also be activated by pressing "Ctrl+L".

"Save"

The complete programming of the ARCOFI-SP as well as the state of the ARCOS-SP PLUS software can be saved in a file.

When saving, a file name and format is asked for. There are two different formats supported by ARCOS-SP PLUS. They are an ARCOS-SP PLUS specific binary file format and a text format. If no extension is given, the entered name will automatically receive the following one:

- Sequence of commands: *.ARC (text format)
- State of ARCOS-SP PLUS: *.ARB (binary format)

Afterwards the filename is checked for validity. If the file name is not correct, an error message appears and the save command is aborted.

The binary format is used to store the device status. Since the format is device specific it is not readable by the user. Being in binary format, the information exchange between the hard-disc and the ARCOS-SP PLUS software is speeded up.

The text format takes more time to program a sequence since this format has to be translated to the binary format via the ARCOS command interpreter before it is sent to the ARCOFI-SP. The user, however, can read this format, which facilitates programming the ARCOFI-SP. For documentation purposes the contents of an *.ARC file can be used in standard word-processing software. It can even be altered with an ASCII-Editor and then again be loaded with the LOAD command.

The save command can also be activated by pressing "Ctrl+S".

"Execute"

A file name is asked for and then checked for validity. Any file which was previously recorded with the "Note" function, may be read and executed. If the file name is invalid or non-existent, an error message is shown and the execute command is aborted.

"Note"

It is possible to record all activities between the ARCOFI-SP and ARCOS-SP PLUS. The feature "Note" can be turned on or off to record all actions in a pre-named file.

To implement "Note" the user has to activate the pull-down menu. When "Note" is active, the menu command will have a check mark to the left of it. Once active, one has to name the file and give an appropriate extension to it. The file extension depends on what one wants to record, either a sequence of commands or just a line input.

- Extension `*.ARC` : ARCOFI-SP sequence of commands: only ARCOFI-SP programming
- Extension `*.ARS` : ARCOS-SP PLUS commands; a record of every key stroke or mouse activity

The `*.ARS` file consists of a list of all commands that the user has entered via the ARCOS-SP PLUS dialogue mode to program the ARCOFI-SP. It is possible to read the `*.ARC` file and review what was programmed. The `*.ARS` commands, however, are written in an ARCOS-SP PLUS specific program language to program the ARCOFI-SP. This feature allows to run a test pattern several times without looking at the file, thereby saving time.

"DOS Shell"

"DOS Shell" is provided for calling the operating system. It is possible to toggle back and forth between ARCOS-SP PLUS and the DOS command level. The following actions are carried out:

- The screen in ARCOS-SP PLUS is completely stored as it is,
- The DOS operating system is called,
- When returning to ARCOS-SP PLUS, the screen reappears just the way it was left before.

"Exit"

To leave the ARCOS-SP PLUS program, use the "Exit" command or just type a "Q" in the command line.

2.2.3 Pull-Down Menu "ARCOFI"

"READ ARCOFI"

The command READ ARCOFI reads the complete device. If the coefficients of the ARCOS-SP PLUS software are not identical to the coefficients in the ARCOFI-SP, the current window as well as the status line are corrected.

This command can also be activated by pressing "Ctrl+R".

"WRITE ARCOFI"

With the WRITE ARCOFI function the ARCOS-SP PLUS software coefficients which are displayed on the screen are written to the ARCOFI-SP. In general, this is always done automatically by the software, but the WRITE ARCOFI command allows to write all coefficients at once a second time.

This command can also be activated by pressing "Ctrl+W".

2.2.4 Pull-Down Menu "Show"

This feature enables the user to switch between various windows in the user area to show the device parameters that are read from the chip and to manipulate them. The following windows can be displayed (refer to **chapter 2.3**):

- CRAM (Coefficient RAM)
- Register
- ARCOFI
  - AFE (Analog Front End)
  - ADI (ARCOFI Digital Interface)
  - ASP (ARCOFI Signal Processor)
    - Tone-Generator
    - DTMF-Generator
    - Speakerphone
      - SD-Transmit (Speech Detector)
      - SD-Receive (Speech Detector)
      - SC-Acoustic (Speech Comparator for the acoustic echo)
      - SC-Line (Speech Comparator for the line echo)

2.2.5 Pull-Down Menu "Board"

This menu serves for changing the configuration of the Mainboard, setting the signalling channel and choosing the ARCOFI-SP device (interface mode and chip address).

"A-Chip/B-Chip"

These two menu items can only be selected when the IOM-2 mode is activated. In this case switching between two devices via software is possible. If the serial interface mode was selected (SPI Serial Programming Interface; SCI/SDI) this feature is not available.

"Signalling"

This menu listing allows to set the bits in the C/I channel 1. Please note, that this menu item is only available in the IOM-2 TE mode of the ARCOFI-SP. The setting of the bit CAM in the GCR-register influences the bit positions in the signalling window (refer to the ARCOFI-SP User's Manual, **chapter 3.4.3**).

2.2.6 Pull-Down Menu "Options"

A variety of options exists with the ARCOS-SP PLUS software. It is possible to set the colors, the sensitivity of the mouse, the beeper (ON/OFF), the tone frequency of the error beep, the double borders for the menu (ON/OFF) and the shadow effect (for the windows).

2.3 The User Area

Working with the User Area

The user area is the portion of the screen between row 2 and 23 (see **figure 2.2**). In this area different background items can be displayed and manipulated with the mouse. The screen contents of the user area can be chosen either with the menu item "Show" from the main menu or simply by clicking at different boxes inside the user area with the left mouse button.

Being in the user area of ARCOS-SP PLUS, only a click with the left button of the mouse will activate the different fields.

A field can have three different states:

- ON: the border and contents of the field are highlighted
- OFF: the border and contents of the field are dimly displayed
- ERROR: the border and contents of the field are displayed in red

The left and right mouse buttons have different meanings. The **left mouse button** is used to program a field or used to zoom into another window. A double click with the left button turns a field ON/OFF and at the same time programs the corresponding bit in the configuration register. The **right mouse button** is used to read a field and to show the coefficients in hexadecimal code, i.e. as they have to be written into the ARCOFI-SP.

Initializing the Hardware

Before it is possible to work with the user area either the external hardware must be initialized (click at the field "Initialize Hardware", compare with **figure 2.2**) or it must be disabled (field "Disabled"). With a disabled hardware the ARCOS-SP PLUS software can be used to evaluate ARCOFI-SP coefficients without influencing any external hardware containing the ARCOFI-SP. If the hardware is successfully initialized, any programming action will also concern the ARCOFI-SP.

The hardware is initialized as soon as the initialization field in the ARCOFI-SP window is clicked upon or when the ARCOFI-SP is accessed. Access takes place either with a "Read" command or with a "Load" command. In this case the hardware will be programmed completely with the ARCOS-SP PLUS conditions displayed on the screen.

In **chapter 4** a description of the different setups depending on the external hardware can be found.

Changing Registers and Coefficients in the User Area

Functions or switches can be activated simply by clicking upon the desired, double framed fields. This is equivalent to the bit combinations in the registers as they can be found in the register window. For example the sidetone gain stage GZ can be activated by setting the GZ bit in the register window or simply with a double click at the GZ box in the user area. Another example is the DTMF bit. This bit can be activated with a single click on the DTMF switch in the user area.

A coefficient like the sidetone gain coefficient required for GZ can be programmed with a single click at the GZ box in the user area. As a result, a pop-up window appears which offers all possible values. Should the desired value not be shown, one can scroll through the list by clicking upon the small up and down arrows located at the top of the frame surrounding the coefficient values. It is also possible to type in the desired value. The program automatically chooses the closest value available. If the value of the coefficient is unknown, then two question marks will be shown. The entered coefficient must carry the same unit as the main header of the window.

These explanations apply to all bits and coefficients. In general, the user area is self-explanatory and can also be used to become familiar with the architecture of the ARCOFI-SP. However, the generation of coefficients for the FX- and FR-filters is a bit more difficult to understand and will be explained separately in **chapter 3**.

The Register Window and the CRAM Window

For experienced users, the two windows "Register" and "CRAM" offer the possibility to change almost every bit or coefficient of the ARCOFI-SP with the help of only two different screen masks. Everything that can be done in the other windows of the user area can be done with the register and CRAM window instead. Using the right mouse button in the register and CRAM window shows the complete programming sequence that is required for the actual setting of the ARCOFI-SP.

Clicking upon register bits makes them toggle or a pop-up window appears. CRAM coefficients can also be altered by clicking upon them. A double click at one of the coefficients causes ARCOS-SP PLUS to switch to the corresponding window in the user area. For example a double click at the parameter ATT in the CRAM window activates the speakerphone window.

2.4 The Command Line

Introduction

It is highly recommended to use a mouse to work with the ARCOS-SP PLUS software, but it is also possible to enter all inputs via the keyboard. All commands have to be entered in the command line (see **figure 12.2**).

This chapter gives a complete description of all inputs that can be done in the command line. The command line is not case sensitive. The F3 key can be used to recall the last command.

ARCOS-SP PLUS Commands

Show	**ASP** | **Reg**[ister] | **ARCOFI** | **AFE** | **ADI** | **CRAM** | **Tone**[generator]| **DTMF**[generator] | **Spe**[akerphone] | **SDT**[ransmit] | **SDR**[eceive]
W[rite]	**ARCOFI**
R[ead]	**ARCOFI**
Board	{ **A**[-][Chip] | **B**[-][Chip]} | {**B1** | **B2**} | **Sig**[nalling] [<Hex><Hex>] | **En**[abled] | **Dis**[abled] | **Init**[ialise]}
Load	<Filename>
Save	<Filename>
Note	<Filename>
Exec[ute]	<Filename>
Delay	<Time>
DOS	
Exit	
Q[uit]	

Commands for Setting Coefficients

<Command>	**<Coefficient>**	**[<Coefficients Set>]**
DTMF	<Float><Float>[<Float><Float>]	F3, G3, [FD, GD3]
F[T]	<Float> <Float>[<Float>]	F1, F2, [F3]
FS	<Float> <Float>[<Float>]	F1S, F2S, [F3S]
G	<Float> <Float>[<Float>]	G1, G2, [G3]
GD	<Float> <Float>[<Float>]	GD1, GD2, [GD3]
T	<Float> <Float>[<Float>]	T1, T2, [T3]
FX	<**OptimMode**> <Files> <**OptimSpeed**>	
FR	<**OptimMode**> <Files> <**OptimSpeed**>	

Coefficients

GX	**GR**	**GZ**			
TOn	**TOff**				
F1[T]	**F2[T]**	**F3[T]**			
F1S	**F2S**	**F3S**	**FD**		
G1	**G2**	**G3**			
GD1	**GD2**	**GD3**			
T1	**T2**	**T3**			
A1	**A2**	**K**	**GE**		
GAE	**GLE**	**ATT**	**ETAE**	**ETLE**	
TW	**DS**	**SW**			
GDSAE	**PDSAE**	**GDNAE**	**PDNAE**		
GDSLE	**PDSLE**	**GDNLE**	**PDNLE**		
LIM	**OFFX**	**OFFR**			
LP2LX	**LP2LR**	**LP1X**	**LP1R**		
PDSX	**PDNX**	**PDSR**	**PDNR**		
LP2SX	**LP2NX**	**LP2SR**	**LP2NR**		
LGAX	**LGAR**				
COMX	**AGX**	**TMHX**	**TMLX**	**NOISX**	
COMR	**AGR**	**TMHR**	**TMLR**	**NOISR**	**AAR**

Extended Commands

Po[wer] Down

Po[wer] Up

Re[set]

Configuration Setting Commands

S[et] <CRBit> [0 | 1 | I | II | ALw | uLw | in | out | SQ | TR]

C[lr] <CRBit>

S[et] VDM <Hex>

C[lr] VDM

S[et] **MIC|AMI** [down | by [-pass]| 0 | 6 | 12 | 18 | 24 | 30 | 36 | 42]

C[lr] **MIC|AMI**

S[et] **AIMX|AIN**[-MUX] [MIP1[|MIN1]|MIP2[|MIN2]|MI3]

C[lr] **AIMX|AIN**[-MUX]

S[et] **HOC|AHO** [down | by [-pass] | 2.5 | -3.5 | -9.5 | -15.5 | -21.5]

C[lr] **HOC|AHO**

S[et] **LSC|ALS** [down | by [-pass] | 11.5 | 8.5 | 5.5 | 2.5 | -0.5 | -3.5 | -6.5 | -9.5 | -12.5 | -12.5 | -15.5 | -18.5 | -21.5]

C[lr] **LSC|ALS**

S[et] **DLTF** [NOT | IDR | DLP | DLS | DLN]

C[lr] **DLTF**

S[et] **Tone**[generator]

C[lr] **Tone**[generator]

S[et] **Spe**[akerphone]

C[lr] **Spe**[akerphone]

S[et] **AGCX**

C[lr] **AGCX**

S[et] **AGCR**

C[lr] **AGCR**

S[et] **Comp|Exp|VDM**

C[lr] **Comp|Exp|VDM**

S[et] **{ GCR | DFICR | PFCR | TGCR | TGSR | ATCR | ARCR | TFCR | SDICR | XCR } <Hex><Hex>**

C[lr] **GCR | DFICR | PFCR | TGCR | TGSR | ATCR | ARCR | TFCR | SDICR | XCR**

Low-Level Setting Commands

W[rite] [**0|1**] <WCommands>

R[ead] <RWCommands>

Print Commands

P[rint] DTMF | CRAM | AFE | ADI |Tone[generator]|
Spe[akerphone]| AG[CX] | AG[CR] | Reg[ister] |
GX | GR | GZ | Exp[&VDM] | Comp

P[rint]**FX** Freq[uency]|Res[ult]|<OptimMode> <Files> <OptimSpeed>

Command Parameters

<**CRBit**> SP | AGCX | AGCR | EVX | SLOT | PU | CAM | ESIG |
LAW | SD | SC | SB | SA | VDM3 | VDM2 | VDM1 | VDM0 |
GX | GR | GZ | FX | FR |DHPR | DHPX | TG | DT | ETF |
CG | BT | BM | SM | SQTR | PM | TRL | TRR | DTMF |
TRX | MIC3 | MIC2 | MIC1 | MIC0 | EVREF | AIMX1 |
AIMX0 | HOC2 | HOC1 HOC0 | CME | LSC3 | LSC2 | LSC1 |
LSC0 | DHS | EPZST | ALTF2 | ALTF1 | ALTF0 | DLTF2 |
DLTF1 | DLTF0 | EPP | DCE | MCLKR2 | MCLKR1 | MCLKR0 |
PGCR | PGCX | RAAR | OBS | DHOP | DHON | DLSP | DLSN

<**RWCommands**> SOP_0 | SOP_1 | SOP_2 | SOP_3 |
SOP_4 | SOP_5 | SOP_6 | SOP_7 |
SOP_8 | SOP_A | SOP_D | SOP_F |
COP_0 | COP_1 | COP_2 | COP_3 |
COP_4 | COP_5 | COP_6 | COP_7 |
COP_8 | COP_9 | COP_A | COP_B |
COP_C | COP_D | COP_E | COP_F

<**WCommands**> XOP_0 | XOP_1 | XOP_D |
XOP_E | XOP_F

<**Files**> <Filename> [<Filename> [<Filename>
[<Filename>]]]

<**Filename**> Filename with extension

<**OptimMode**> F[lat] | T[arget] | L[imited]

<**OptimSpeed**> /F[ast]| /M[iddle]| /B[est]

<**Float**> Standard Real Number

<**Time**> <Float>

<**Hex**> 0 ... F

3 Generating the Correction Filter Coefficients

3.1 Filter Implementation and Theory of Calculation

Two high performance frequency correction filters FX and FR are implemented in the ARCOFI-SP, allowing an optimum adaption to different types of transducers or compensating the frequency response of the telephone plastics itself. Specifications of different countries can be fulfilled by means of a simple software change.

One filter consists of two equalizers with variable gain, factor of quality, and center frequency followed by a high-/low-pass filter. The filters can only attenuate the signal, they behave like passive filters. The FX or FR filter is adjusted with the help of twelve coefficients which are calculated by the ARCOS-SP PLUS software.

It is obvious, that there are different ways to configure the two equalizers and the high-/ low-pass filter to achieve one and the same frequency response. Therefore always more than one coefficient set is capable of fulfilling the desired response.

The basic idea for calculating the coefficients is, that two frequency responses are given. One represents the desired over-all frequency response (target function), the other one is the frequency response, that the hardware actually offers (input function). While the first one is usually a flat frequency response, the latter one can be measured or estimated. ARCOS-SP PLUS then calculates the filter coefficients (filter function) in a way, that the filter function plus the input function results in the target function. If for example the hardware transmits high frequencies only attenuated, it exhibits a kind of low-pass function (input function). If a flat frequency response is desired (target function) ARCOS-SP PLUS would calculate the coefficients in a way, that the FX or FR filter shows a high-pass behavior in order to compensate the input function.

Furthermore, it is not only possible to give a desired target function but also an upper and lower limit for the target function can be given.

The algorithm used for generating the filter coefficients is based on a stochastic method, similar to the law of cooling: i.e. at the beginning of the process, the parameters (here the filter coefficients) may be within a large range. This range progressively is reduced such that the parameters converge. Up to and including the 8th calculation step the quality of the approximation is defined by the mean square of the difference between the target function and the addition of the filter functions of FX or FR and the input function. Thus the discrepancy between the two curves is calculated for each sampling frequency, then it is squared, added and finally divided by the number of the sampling frequency points.

From the 9th calculation step the quality of the approximation is defined by the greatest absolute difference. The algorithm shows the value of the absolute minimum and the quality of the coefficient set which is presently considered as the best solution.

In order to calculate the discrepancy properly, each amplitude curve is normalized. Before the algorithm starts, each amplitude curve is shifted such that it has an amplitude

value of 0 dB at one sampling frequency point. The reference frequency is the sampling frequency which is equal to or closest to 1000 Hz.

Note: Because the algorithm is based on a random process, different runs of the program, starting from the same input function, can give different results. It is recommended to make several runs and to take the best result (see also **page 262**).

3.2 Calculation of Coefficients

The coefficients for the FX transmit and FR receive path correction filters can be calculated either with the ARCOS-SP PLUS or with the ARCOS-SP program. Both programs generate filter coefficients and graphically display the filter transfer functions (amplitude transfer function in dB, group delay response in µs). The graphic output is only possible if the system is equipped with an EGA, VGA, CGA, or a Hercules graphics card. The transfer function can also be stored in tabular form in two separate files, one for the amplitude response (`*.AMP`) and one for the group delay response (`*.GDY`).

After clicking at the FX or FR filter box in the ASP window (ARCOFI-SP signal processor) an dialogue box appears that offers the choice between three basic optimization modes. For each mode the optimization speed must be chosen as either "fast", "middle" or "best". Once the optimization mode, the selected speed of optimization and the required file names have been entered, the calculation starts.

Optimization Speed

The optimization process might require long computing time in some difficult cases, in particular a "best" fit with over 100 frequency points might take hours to be completed when using a slow PC without co-processor. It has been found that between 20 to 30 sampling points usually give a satisfactory result while keeping the calculation time reasonably short.

Optimization Mode "flat target function"

For a flat frequency response, the algorithm approximates the inverted function of the input function. The input function must be declared in an input file. The file has to be entered with the filename and the extension. An example for an input file shows **table 1**.

For the FR filter a second input function can be entered (e.g. one for the handset earpiece, the second for the loudspeaker). The calculation points of this second input function are interpolated and subsequently averaged. Hereby ARCOS-SP PLUS will eliminate automatically the frequency areas which are not common in both input functions (ranges at lower and upper frequencies).

When the coefficients have been calculated, the inverse curve of the input function is displayed if a graphics screen is available. On the same graph the filter functions of FX

or FR are displayed. Both curves are shifted such that they have the same amplitude value at the reference frequency.

After having quit (using pressing carriage return or the key "Q") the discrepancy between the two curves is displayed. The graphics mode can be left by quitting a second time.

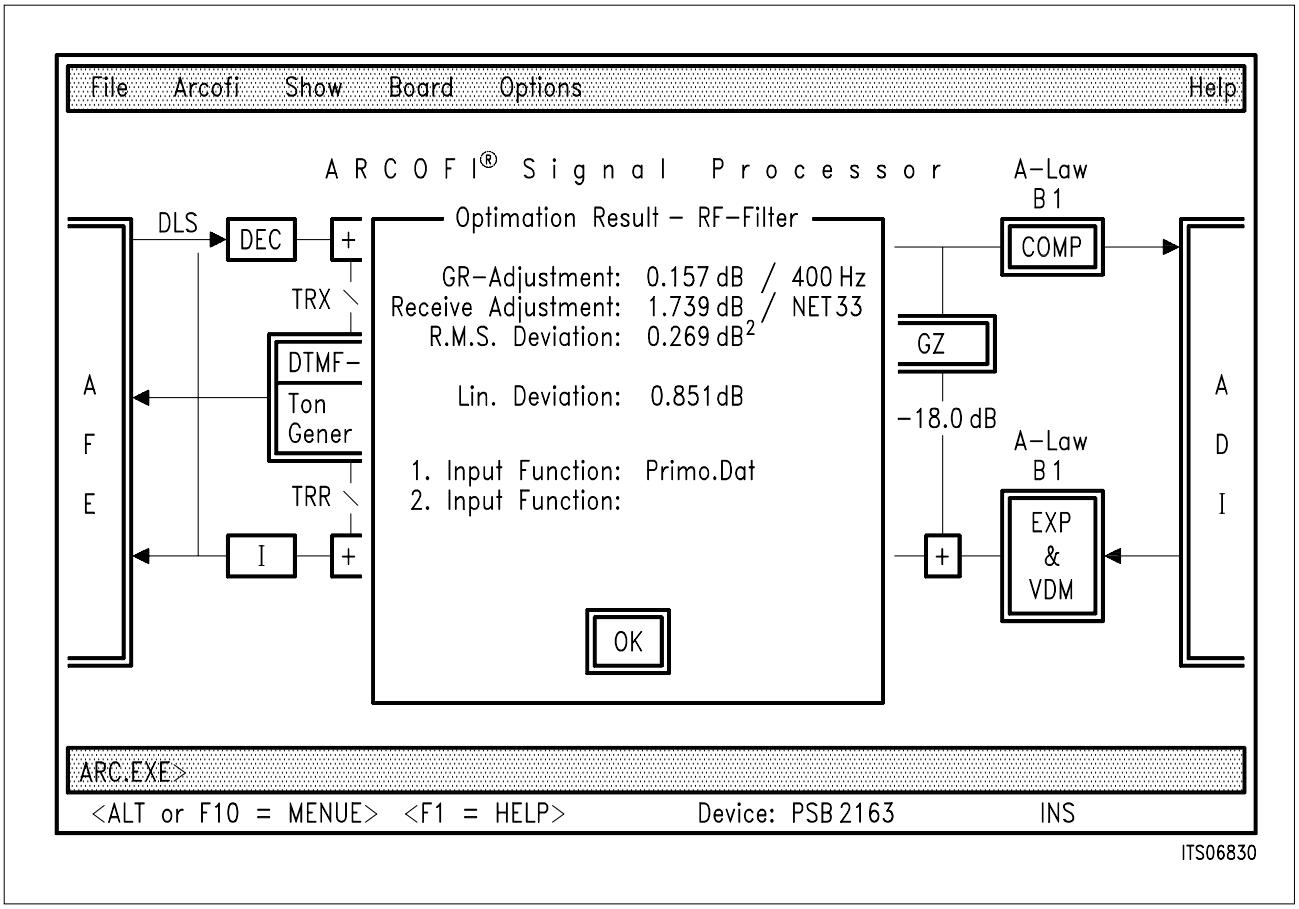

Figure 2
Screen after Calculating Filter Coefficients

The optimization result is displayed in a separate window after successful completion (see **figure 2** for an example). Here the values GR- or GX-Adjustment, r.m.s. deviation and linear deviation are displayed as well as the relevant input files. Because the FX/FR filters can be regarded as passive filters, the additional loss caused by the filter must be compensated. ARCOS-SP PLUS displays different values that represent this additional loss and are also a measure for the quality of the optimization:

- "lin. deviation" is the minimum filter loss
- "Receive Adjustment" ("Transmit Adjustment") is the filter loss weighted according to CCITT and ETSI NET33
- "GR-Adjustment" ("GX-Adjustment") is the weighted filter loss over the complete frequency range of 4 kHz
- "r.m.s. deviation" is the mean square of the difference between the filter function and the desired response

Figure 3 illustrates the meaning of these values.

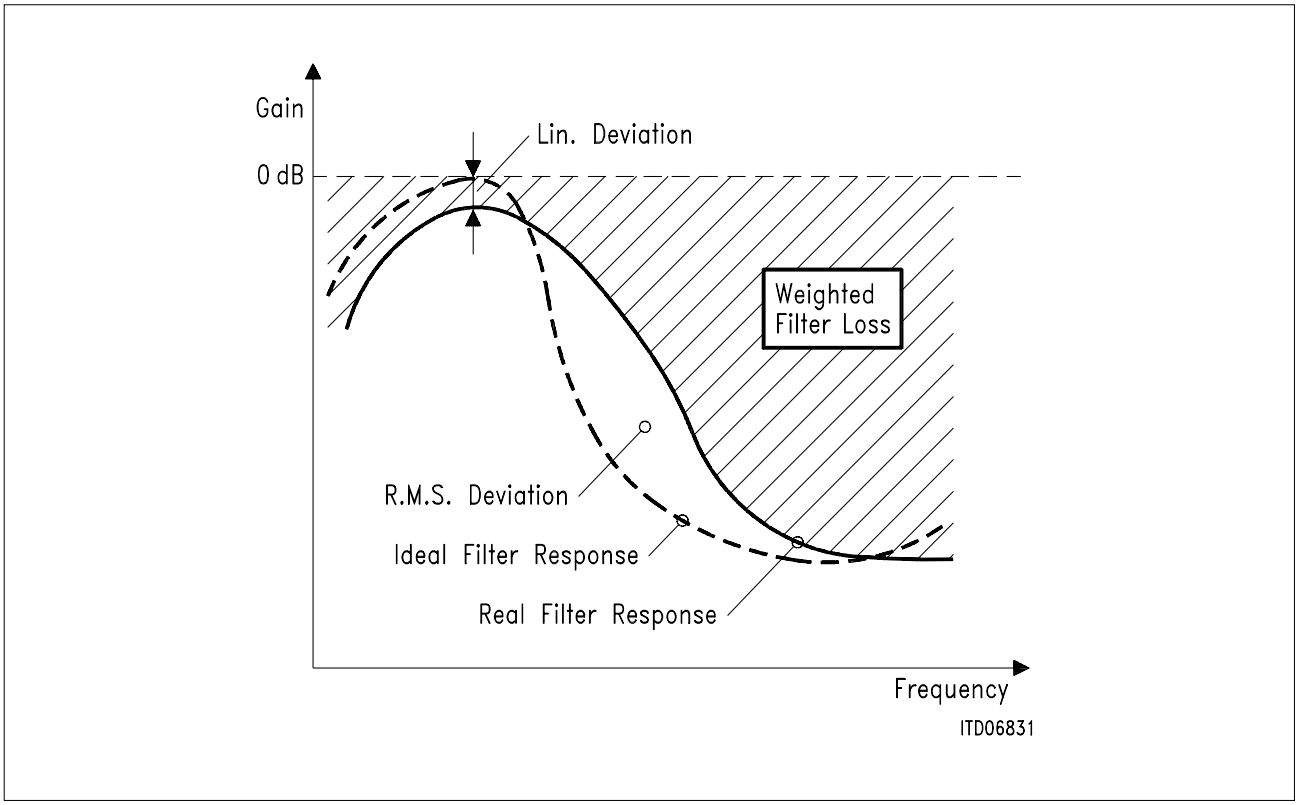

Figure 3
Illustration of Filter Loss and Deviation

Especially the "linear deviation" is a measure for the quality of the coefficient set. The lower this value, the better the approximation is. Several runs of the program can result in different values for the linear deviation because of the random starting parameters the algorithm uses. In general, it should be possible to reach a value of less than 3 dB for the "lin. deviation".

Optimization Mode "target function"

The algorithm tries to compensate the input function in such a way that the addition of this input function and of the filter functions of FX or FR is as close as possible to the target function. The target function must be given in a file.

Before starting the algorithm, the sampling frequency points of the target function are adjusted to the sampling frequency points of the input function. ARCOS-SP PLUS checks if each sampling frequency point of the input function has a corresponding sampling frequency point in the target file. If a sampling frequency point is not found in the file, then the amplitude value of this sampling frequency point is interpolated by making a linear approximation from the two points closest to the desired sampling frequency point. Thus the algorithm can work with two curves not having the same sampling frequency points.

If a sampling frequency point is higher than the highest point or lower than the lowest point of the target function then the algorithm considers that the frequency response can have any value at this point. These calculation sampling points are not recognized and therefore do not influence the calculation.

After the calculation of the coefficients the input functions and filter functions of FX or FR are added and the result is graphically displayed. In the same graph the target function is also shown. Both curves are shifted such that they have the same amplitude value at the reference frequency.

After quitting the discrepancy, i.e. the difference between the two curves, is graphically shown. When quitting again one leaves the graphics mode. Finally the results as described for the "flat frequency response" are displayed.

Optimization Mode "limited by an upper and lower curve"

The algorithm tries to compensate the input function such that the addition of this input function and of the filter functions of FX or FR is as close as possible to the middle of the upper and the lower limiting curves (which is then the target function). Before starting the algorithm, the target function as well as the weighting factors are calculated.

First, the sampling frequency points of the upper limit and lower limit are adjusted to the ones of the input function. Then the algorithm checks whether each sampling frequency point of the input function has a corresponding sampling frequency point in the upper and lower function. If a sampling frequency point is not found in the upper and lower curves, then the amplitude value for this sampling frequency point is interpolated by making a linear approximation from the two points closest to the desired sampling frequency point. Finally for each frequency point the mean of the upper and the lower limit is calculated. These mean values describe the target function.

If a sampling frequency point is higher than the highest point or lower than the lowest point of the upper and lower limiting curve, then the algorithm considers that the frequency response can have any value at this point. These calculation samples would not be recognized.

The ratio of the longest and shortest distance between the upper and the lower limiting curves (for one frequency) defines the size of a weighting factor. The shorter the distance between the limiting curves, the better the correction, the larger the weighting factor. The weighting factor is taken into consideration when calculating the greatest absolute difference as well as the mean of the square of the difference.

After the calculation of the coefficients, the input function and the filter functions of FX or FR are added and the result is graphically displayed. In the same graph the upper and lower limits are also shown. The curves are shifted in such a way, that the input function and the target function have the same amplitude value at the reference frequency.

Finally the mean square of the difference and the other values described above, are displayed.

File Format

A maximum of up to 100 frequency/amplitude points can be used by the approximation algorithm. The frequency points must be in progressing order between 1 Hz and 3999 Hz. The amplitude values should be limited to a maximum of |20| dB although this is not required for the fitting algorithm.

The software expects one pair of values (frequency and level) in one line, both values separated by one or more blanks and/or tab-stops. The first value must be the frequency, the second one the level. Units are Hz and dB; they are not part of the file. Numbers can be integer or real (e.g. 3 or - 3.1 are allowed). **Table 1** shows an example for an input file.

Table 1
Example for an Input File

Frequency (Hz)	Level (dB)
300	– 1
700	– 1
800	– 0.5
1000	0
1050	0.1
1200	0.5
1250	0.75
1300	1
1350	1.25
1400	1.5
1450	1.75
1500	2
1700	3.75
1750	4.25
1900	5.5
2250	6.9
2550	7.45
3000	8
3250	6.75
3350	6.25

3.3 Reading the FX- and FR-Filters

A click with the right mouse button (or the input `Print FX` or `Print FR`) at the command line) invokes the read window for the filters. This window is a blend between an input and an output window. There are three fields which can be clicked upon and one entry field to enter a file name. If one clicks upon the field "Frequency Response", then the frequency and phase response of the filter are shown in a graphical format. If one chooses the field "Optimization", the three values of the last calculation and the file name are shown (optimization result window). With a click on the "Check Optimization" field, the same window is displayed that appears after programming the filters (see **figure 2**), but the coefficients are not recalculated, instead the result of the optimization is taken. If it is desired that the frequency response is saved in a separate file, the file name has to be entered in this window.

3.4 Examples for the Usage of the FX/FR Filters

3.4.1 Adapting the FX Filters to a Target Frequency Response

The use of the FX filter to match a required mask template will be highlighted in the following example.

According to the European Telecommunications Standards Institute (ETSI) standard, the sending sensitivity and frequency response from the mouth reference point (MRP) to the digital interface shall be within a mask template given in **table 2**.

Table 2
Mask Template According to ETSI

Frequency (Hz)	Upper Limit (dB)	Lower Limit (dB)
100	– 12	
200	0	
300	0	– 12
1000	0	– 6
2000	4	– 6
3000	4	– 6
3400	4	– 9
3999	0	

The sampling points (in units of Hz and dB) of the upper and the lower limits are written into a text file with the help of an editor. The first column contains the frequency values in Hz, the second column contains amplitude values in dB (refer also to **table 1**). The units themselves are not inputs, they are generated by ARCOS-SP PLUS.

The names chosen for the files in this example are `UPPER.LIM` and `LOWER.LIM`.

Table 3
Listing of Boundary Curves (in Hz and dB)

Upper Curve		**Lower Curve**	
		300	– 12
1000	0	1000	– 6
2000	4	3000	– 6
3400	4	3400	– 9

The frequency response of the microphone can be measured. The sampling points are also input into a text file. For example it is assumed, that the appropriate file is `PRIMO.DAT` as shown in **table 1**. Because frequencies under 300 Hz and above 3400 Hz are blocked by the ARCOFI-SP filters, only the sampling points in the range 300 Hz - 3400 Hz should be entered in the file. In order to obtain a good approximation, at least 20 points between 300 Hz and 3400 Hz should be selected. However, not more than 100 points should be entered.

After having entered the measurement points, the program ARCOS-SP PLUS is called. When in the ASP-Window, a click with the left mouse button upon the FX field opens a display where the input files, the optimization mode and the optimization speed have to be selected. For this example the optimization mode "limited by an upper and a lower curve" must be chosen. The input function is the file called `PRIMO.DAT`, the upper and lower curves are given with the files `UPPER.DAT` and `LOWER.DAT`. A click upon the "OK" field starts the calculation.

At the end of the approximation process the frequency response of the microphone (input function) and that of the FX correction filter (filter function) are added and the sum is displayed together with the two limiting curves. Notice that the curves are shifted. The value of the amplitude at the reference frequency (1000 Hz in the example) is 0 dB. The two limiting curves are shifted such that the mean value of the limiting curves at the reference frequency is 0 dB.

As already described, the linear deviation of the filter function is a indication of the quality of the coefficient set. The calculation in this example should be done several times until a set of coefficients is found, that results in a deviation of less than 2 dB.

3.4.2 Using the "Execute" Feature to Calculate Coefficients

The process of starting the filter calculation several times and checking the results after each calculation can be eased by using the "Execute" function of ARCOS-SP PLUS. With the help of an appropriate *.ARS file, the software calculates as many sets of coefficients as desired and allows to check the optimization result afterwards.

To understand the contents of the *.ARS file it is necessary to remember the command line syntax of ARCOS-SP PLUS, as far as it is required for the FX/FR filters:

```
FX <OptimMode> <Files> <OptimSpeed>
FR <OptimMode> <Files> <OptimSpeed>
<OptimMode>          :          F[lat]  | T[arget]  | L[imited]
<OptimSpeed>         :          /F[ast] | /M[iddle] | /B[est]
<Files>    : <DATFile> [ <DATFile>  [ <LIMFile> [  <LIMFile> ]]]
<DATFile>  : Filename containing an input function
<LIMFile>  : Filename containing an upper/lower limit
```

A simple example illustrates the use of the "Execute" function. It is assumed that the FX filter should compensate the frequency response given with a file called PRIMO.DAT. The desired response is "flat" and the optimization mode is "best". The following steps have to be performed:

- With the help of an ASCII editor a file with the extension *.ARS has to be prepared, that contains two lines of text for each set of coefficients to be calculated; one line tells the ARCOS-SP PLUS software to do the calculation, the second line is used to save the result in an *.ARC file; **figure 4** shows the contents of such an *.ARS file, it is called CALC.ARS; the combination of "FX...SAVE" must be repeated as many times as sets of coefficients are to be calculated.
- In a second step an *.ARS file has to be prepared to check the previously stored *.ARC files; see **figure 5** for an example, here the file is called CHECK.ARS
- Now the ARCOS-SP PLUS software is started and the menu item FILE, EXECUTE is chosen; the name of the first *.ARS file is given (e.g. CALC.ARS) and the calculation starts; depending on the optimization speed and the number of coefficient sets, this can take quite a long time but the calculation is performed automatically and needs no interaction from the keyboard.

- When the calculation is completed, the previously saved *.ARC files can be loaded separately by using the "Load" command, or the second *.ARS file (CHECK.ARS) is used to load all the files one after the other and to inspect especially the "lin. deviation"; the best approximation is taken as a final result then.

```
FX      Flat primo.dat /B
SAVE    result01.ARC
FX      Flat primo.dat /B
SAVE    result02.ARC
FX      Flat primo.dat /B
SAVE    result03.ARC
```

Figure 4
Contents of the File CALC.ARS (calculation for 3 sets of coefficients shown)

```
LOAD result01.ARC
Print FX Result
LOAD result02.ARC
Print FX Result
LOAD result03.ARC
Print FX Result
```

Figure 5
Contents of the File CHECK.ARS

4 Hardware Setup for Use with ARCOS-SP PLUS

4.1 Introduction

The ARCOFI-SP PSB 2163 is able to work in three different interface modes:

- IOM-2 TE interface (1.536 MHz)
- IOM-2 NON-TE interface (4.096 MHz)
- Serial control / serial data interface (SCI/SDI)

The ARCOS-SP PLUS supports each of these three interface modes in conjunction with appropriate hardware. This chapter describes the different hardware setups. First the ARCOFI-SP has to be connected to the particular hardware which must be configured correctly. Then the ARCOS-SP PLUS software is called and informed about the hardware configuration. With a click at the "Initialize Hardware" box the hardware is checked and initialized for the use with ARCOS-SP PLUS. The ARCOFI-SP itself can be located either on the SIPB 5133-SP evaluation board, inside a SIPB 5132-SP telephone, or on a dedicated board like the SIPB 8051 telephone board. Also custom specific boards with an IOM-2 interface are suitable.

In the "Show ARCOFI" window in the user area of ARCOS-SP PLUS, the following modes can be set if the hardware support is enabled (compare with **figure 1**):

- Either the **ICC/ISAC** as a layer 1/2 device, or the **EPIC/ELIC**
- Either **IOM** interface mode, or **SPI** interface mode (SCI/SDI interface)
- Either **A**-Chip or **B**-Chip (only possible in IOM-2 interface mode)

These settings must correspond to the hardware that is connected to the PC on which the ARCOS-SP PLUS software runs.

4.2 Using the SIPB 5000 System

The ARCOS-SP PLUS software requires a specific SIPB 5000 hardware environment. The firmware EPROM version 1.1 or newer must be installed on the SIPB 5000 mainboard. Three standard configurations are described in the next paragraphs. More detailed information can be found in the technical description of the SIPB 5000 system.

Please note, that if the ICC-B is used as a layer-2 device, EPROM version 2.2 or newer is required for the SIPB 5000 mainboard.

IOM-2 TE Interface with an ISAC-X

A common setup uses the SIPB 5100 (ISAC-S Module) or the SIPB 5103 (ISAC-P Module) as layer 1/2 module. The ARCOFI-SP is connected via a SIPB 5130 (Audio Module). **Figure 6** shows the general setup either with an ISAC-S or with an ISAC-P Module. The ARCOFI-SP is located inside a SIPB 5132-SP telephone, but instead of the telephone any hardware which offers an IOM-2 interface can be connected.

For the use with ARCOS-SP PLUS the fields **ICC/ISAC** as well as **IOM** must be activated.

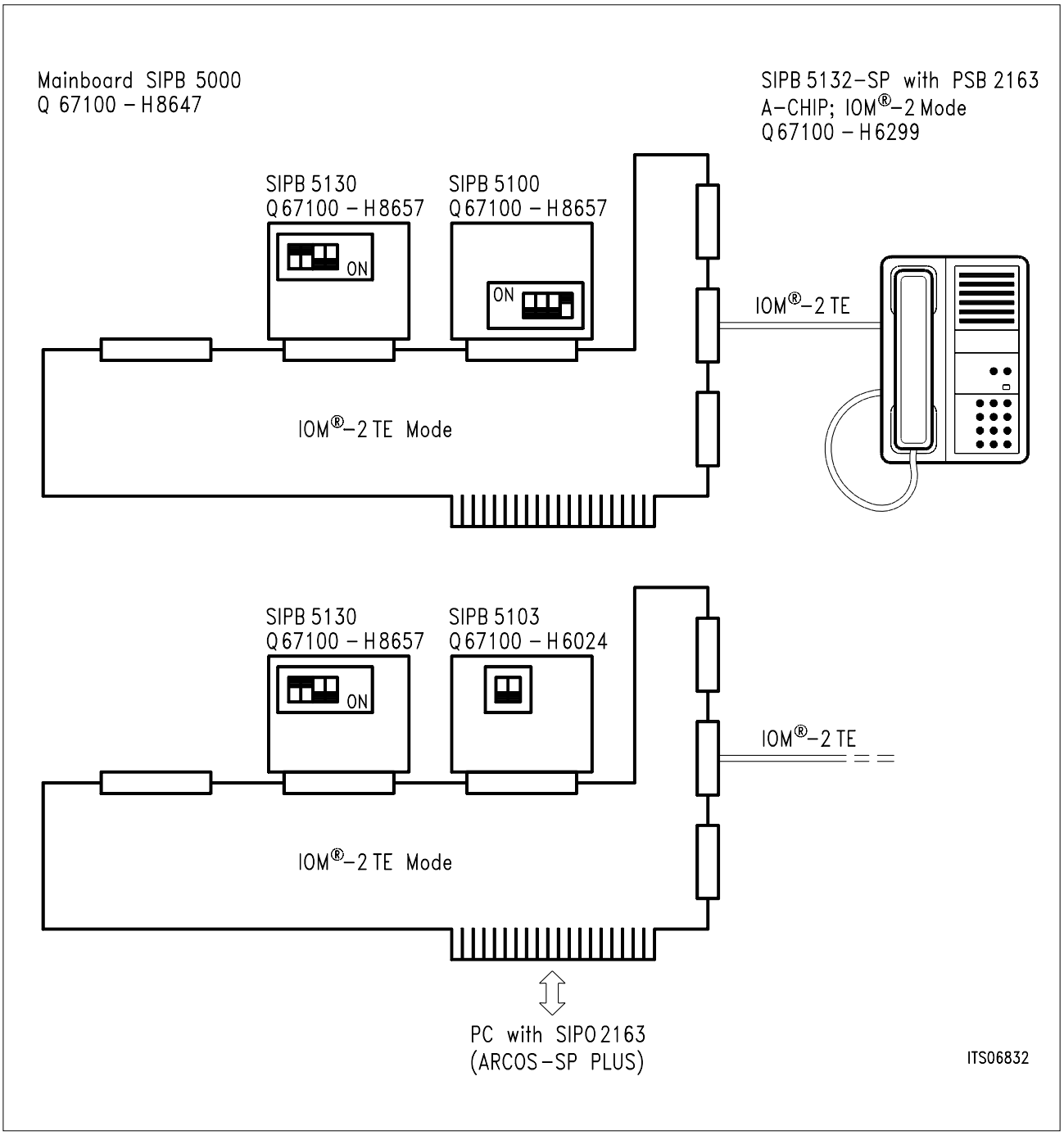

Figure 6
Setup for IOM-2 TE Mode with the ISAC-X in TE-Mode

The ISAC-X runs in TE-mode and the B channels are switched to the S_0 bus or the U_{P0} bus respectively. Therefore the setup in **figure 6** can be connected to an NT simulator consisting of another SIPB 5000 mainboard with another ISAC-X in LT-S mode and a voice connection can be established.

IOM-2 NON-TE Interface with an EPIC/ELIC

The 4.096 MHz IOM-2 NON-TE interface can also be used if a Linecard-Module SIPB 5121 is connected to the SIPB 5000 mainboard. Optionally, this configuration offers the possibility to do measurements with the PCM4 measuring instrument from Wandel&Goltermann which has to be connected with the help of an PCM4 adapter SIPB 5311. **Figure 7** shows the setup with the ARCOFI-SP placed on the SIPB 5133-SP ARCOFI-SP evaluation board. Due to the relatively high clock frequencies it is necessary to keep the cable length between the mainboard and the evaluation board (or any other hardware platform containing the ARCOFI-SP) as short as possible. This also applies to the cable between mainboard and PCM4 adapter.

Table 4
Timeslot Assignment for Measurements with the PCM4

Timeslot PCM4	IOM-2 Channel
TS1	B1
TS2	B2

Since the IOM-2 NON-TE interface offers eight channels, it is important to know that the ARCOS-SP PLUS software supports channel 7 (the last one) and therefore the ARCOFI-SP must be pin-strapped to this channels. This can easily be done by connecting[1)] pull-up resistors to the pins used for timeslot select (SB, SC, SD). For measurements with the PCM4 measurement device the B1 and B2 channel are switched to timeslot 1 and 2 (**table 4**).

[1] The resistors must be soldered manually; refer also to the App. Note "Using the SIPB 5132-SP telephone with the PSB 2163"

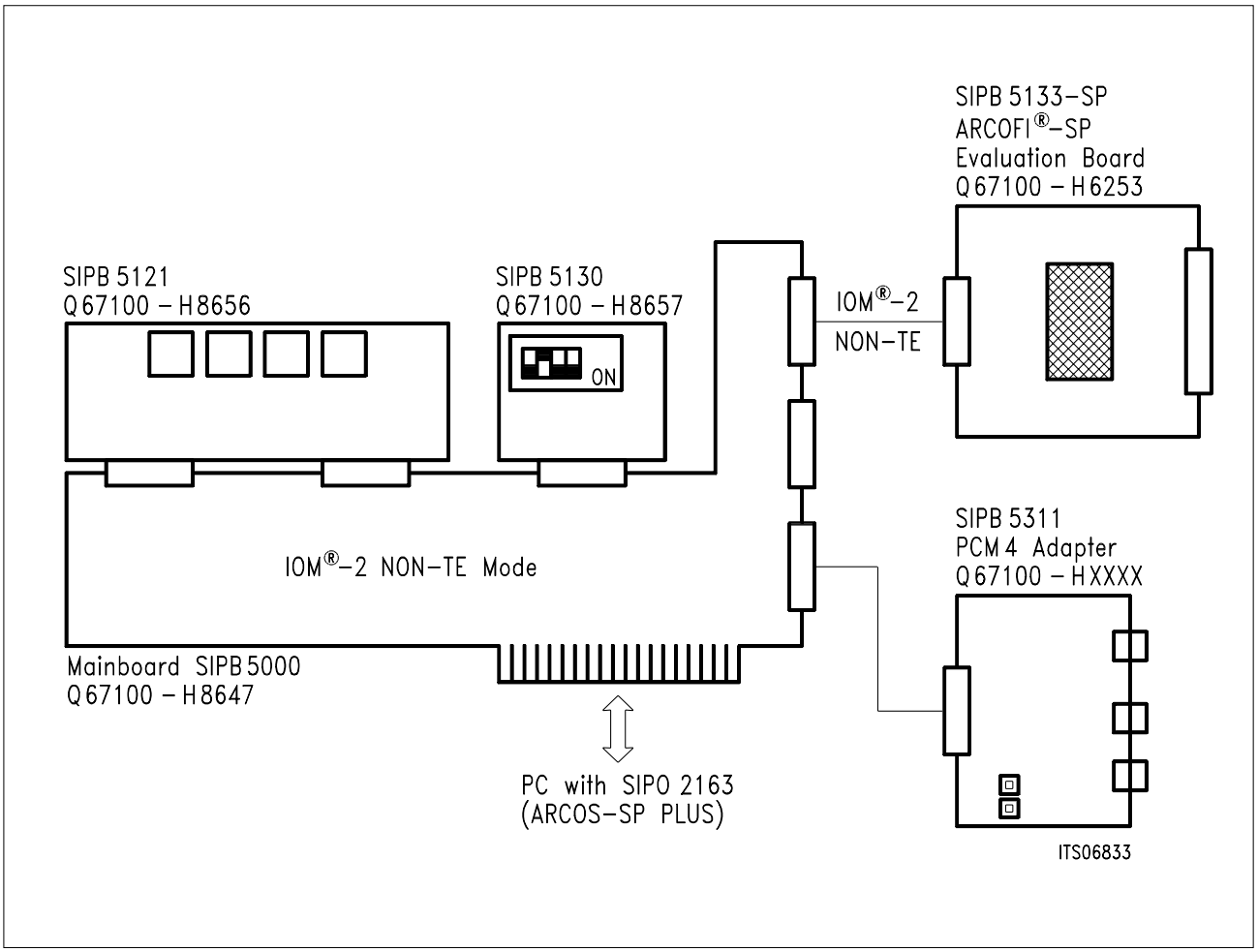

Figure 7
Setup for IOM-2 NON-TE Mode with the Linecard Module

4.3 Other Hardware Tools

The ARCOS-SP PLUS software is able to communicate with different evaluation boards via the serial interface port of the PC. The following boards are supported:

- PERCOFI-Board STUT 2000; the ARCOFI-SP is programmed with the help of an EPIC in IOM-2 TE mode
- Smart Link Kit SISI1097; the SCI/SDI interface of the ARCOFI-SP is used
- ISDN Telephone Board SIPB 8051; the ARCOFI-SP is programmed by an ISAC-X in IOM-2 TE mode

In order to enable the software to communicate with the boards, a special firmware version is required for the evaluation boards. This firmware must be loaded to the target hardware before the ARCOS-SP PLUS software is started. **Table 5** shows the names of the HEX-files with the special firmware versions and the names of the batch files used to download the HEX-files. The download itself is performed by the utility `SIMPLV24.EXE` which is called from the batch files.

Table 5
Hardware to be Connected to the Serial Interface

Hardware Platform	Required Firmware	Batch File for Download	Required RS232 Cable
PERCOFI-Board STUT 2000	PERCOFI.HEX	LPERCOFI.BAT	Null-modem
Smart Link Kit SISI1097	SMART.HEX	LSMART.BAT	Serial 1:1
ISDN Telephone Board SIPB 8051	SIPB51.HEX	LSIPB.BAT	Null-modem

Table 6
Configuration to be made in the User Area of ARCOS-SP PLUS

Hardware Platform	Hardware Switches in the User Area	
PERCOFI-Board STUT 2000	EPIC/ELIC	IOM
Smart Link Kit SISI1097		SPI
ISDN Telephone Board SIPB 8051	ICC/ISAC	IOM

Therefore the procedure for starting ARCOS-SP PLUS for the use with one of the hardware platforms given in **table 5** is the following:

- Connect the hardware with an appropriate cable to the PC (the cable is delivered together with the hardware).
- Make sure that the correct serial port is chosen (default: COM1, see paragraph "choosing the COM port" for more information).
- Make sure that the hardware is in "loader mode" (see board documentation; switching between "loader mode" and "program" is performed with the reset button on the board).
- Download the firmware (batch file according to **table 5**).
- Make sure, that the board is switched to "program mode"; this is done automatically after the download, except for the Smart Link Kit where the reset button must be pressed once (the loader LED on the SmartLink board has to be inactive then).
- Start ARCOS-SP PLUS in the serial interface mode; this is done by adding the switch /V to the command line input; the syntax is:
  `ARC [IniFile[.xxx]] /V`
  When started with this option, the ARCOS-SP PLUS software ignores any SIPB 5000 based hardware and scans the serial port for the presence of one of the boards from **table 5** instead.
- After quitting the hardware message ("board xxx found at the serial port") the usual window appears in the user area; in this window the hardware switches must be set according to **table 5** before the "initialize hardware" field has to be activated.

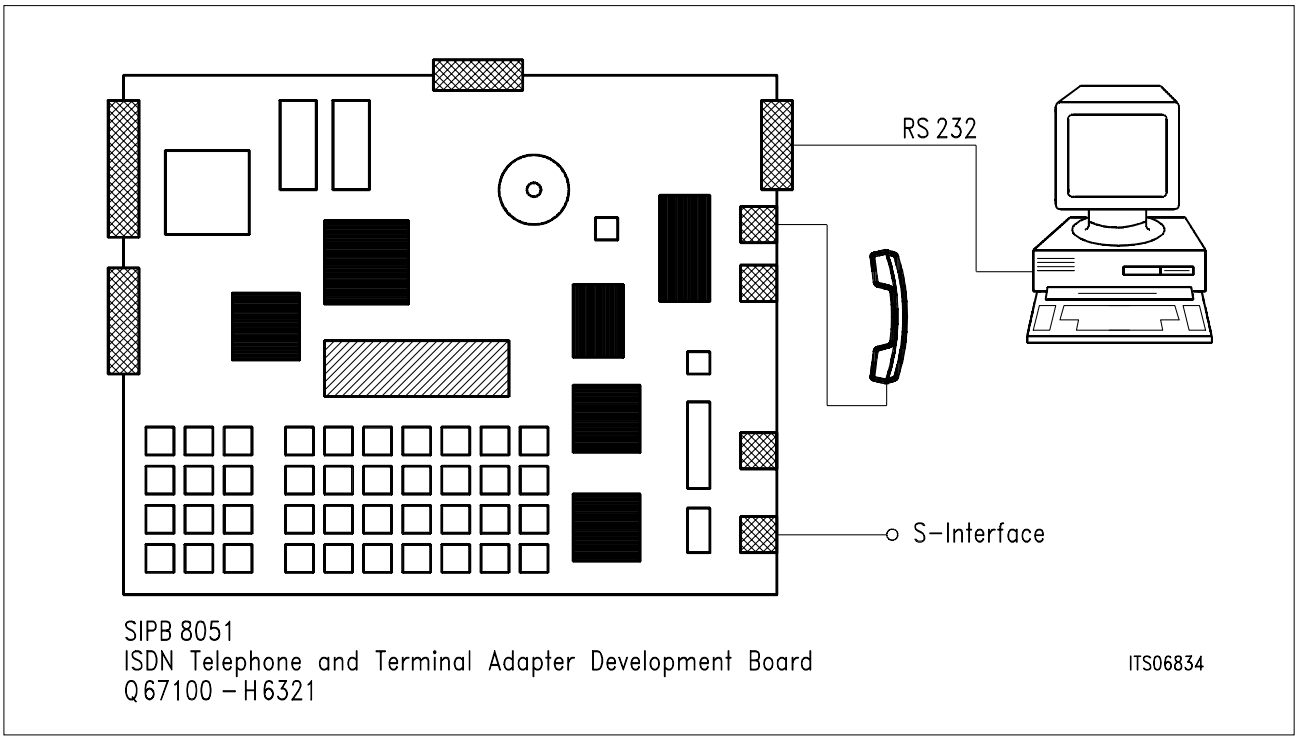

Figure 8
Setup for the SIPB 8051 Telephone Board

The **figures 8, 9, and 10** show the setup for the different kinds of hardware. With the SIPB 8051 Board the B channels are switched to the S interface as well as with the Smart Link Kit the B channels are transferred over the U interface. Therefore in conjunction with an NT-simulator, a voice connection can be established.

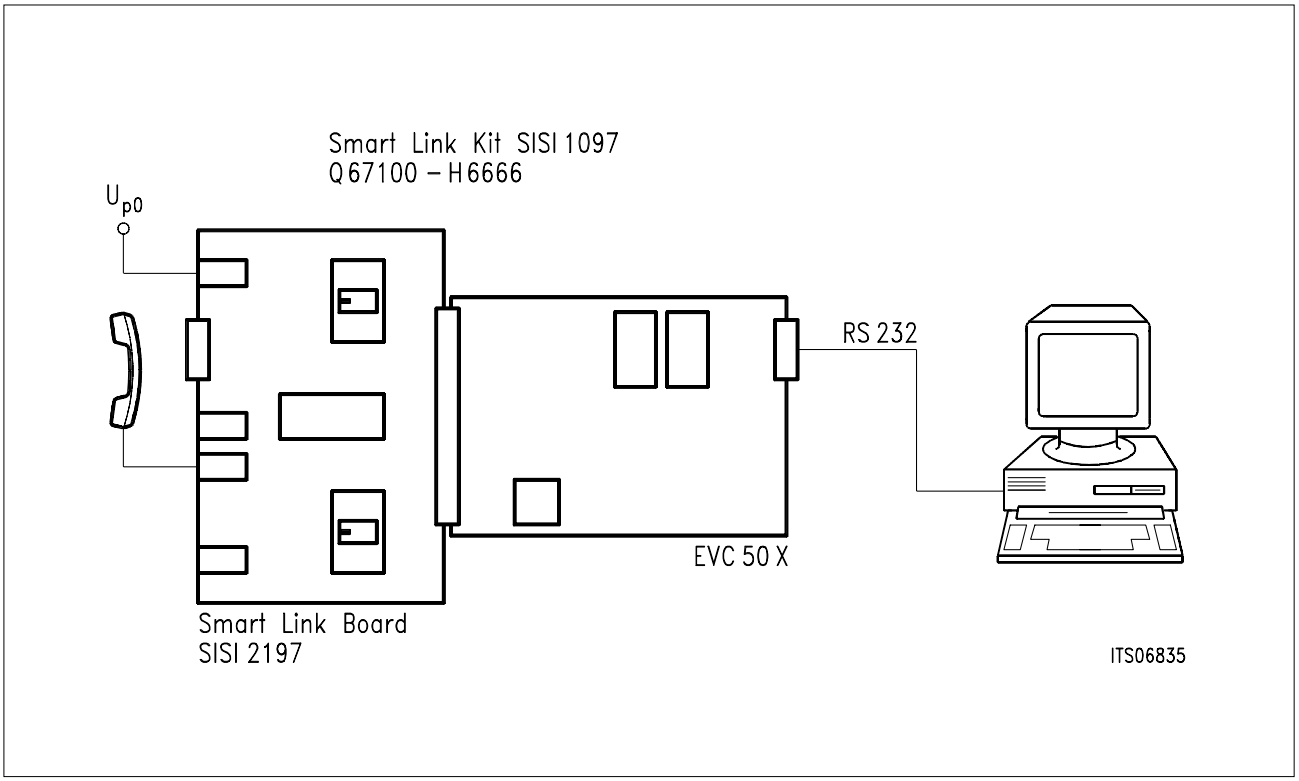

Figure 9
Setup for the Smart Link Kit

The STUT 2000 PERCOFI Board is mainly intended for measuring purposes and can directly be connected to the PCM4 measurement device from Wandel&Goltermann, but nevertheless it can be used to provide an IOM-2 interface for the SIPB 5132-SP telephones equipped with the PSB 2163. The timeslot assignment for measurements with the PCM4 measurement device is given in **table 7**.

Please note, that especially together with the STUT 2000 board, the programming of all the coefficients over the serial interface takes significantly longer than with the SIPB 5000 system. When the ARCOS-SP PLUS software accesses the serial port, the message "RS232 active" appears in the status line.

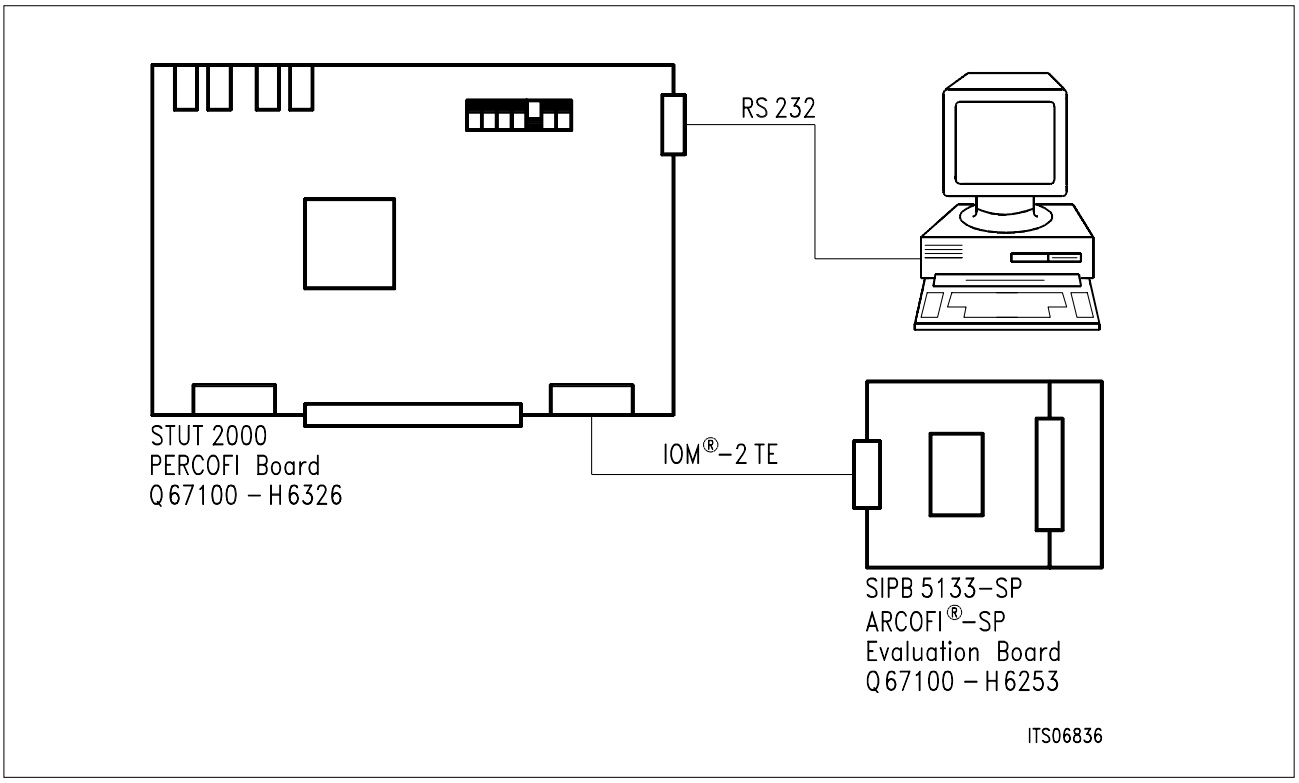

Figure 10
Setup for the STUT 2000 PERCOFI Board

Table 7
Timeslot Assignment for Measurements with the STUT 2000 Board and the PCM4

Timeslot PCM4	IOM-2 Channel
TS1	B1
TS2	B2
TS3	IC1
TS4	IC2

Choosing the COM Port

There are two different programs that have to access the serial port. First of all the ARCOS-SP PLUS software itself, but also the `SIMPLV24.EXE` utility for downloading the firmware.

The serial port number for ARCOS-SP PLUS is defined in the `RS232.INI` file. This file can be altered with the help of an ASCII editor (default is COM1).

The serial port number for the download of the firmware is given as a command line argument for `SIMPLV24.EXE`. If no option for the COM port is given, the utility uses COM1, otherwise the option `/P<n>` must be added, where <n> is the number of the COM port. For this purpose it is convenient to edit the corresponding batch file (see **table 5**) and to add e.g. the option `/P2` for COM2.

5 Error Messages and Troubleshooting

This chapter does not offer an complete overview of all error messages since most of them are self explanatory. Instead, it gives some hints to locate the problems that are most likely to occur.

5.1 Hardware Related Problems

Message: "Configuration of the Mainboard not supported"

ARCOS-SP PLUS has tried to initialize the hardware but is not able to recognize the hardware configuration that is currently set with the switches in the user area and/or with the /V switch in the command line.

Check the configuration of the external hardware (including DIP-switches and jumpers); does the setting in the user area match with the hardware configuration?; reset the hardware (reset button), terminate ARCOS-SP PLUS and try it again.

Message: "No ARCOFI found"

The hardware is successfully initialized but it is not possible to establish a connection with the ARCOFI-SP.

Check the connection between hardware and ARCOFI-SP (e.g. the IOM-2 cable between the SIPB 5000 mainboard and the SIPB 5133-SP Evaluation Board). Is the ARCOFI-SP in the correct interface mode (DIP-switches on the SIPB 5133-SP Evaluation Board)? Is the IOM-2 cable defect or too long? Again a good idea is to reset the hardware, terminate the software and to try it a second time.

Message: "No A-Chip found"

ARCOS-SP PLUS expects to work with an ARCOFI-SP whose address is $A1_H$ (A-Chip) but does not get a response from an A-Chip.

Check the DIP switch on the hardware determining the chip address (SW 1: ON on the SIPB 5133-SP Evaluation Board) or measure the logic level at pin 25 (AD-pin), it must be low.

Message: "No B-Chip found"

ARCOS-SP PLUS expects to work with an ARCOFI-SP whose address is $B1_H$ (B-Chip) but does not get a response from an B-Chip.

Check the DIP switch on the hardware determining the chip address (SW 1: OFF on the SIPB 5133-SP Evaluation Board) or measure the logic level at pin 25 (AD-pin), it must be high.

Message: "This version of the A-Chip is not supported" or
"This version of the B-Chip is not supported"
"This version of the ARCOFI is not supported"

ARCOS-SP PLUS has detected an PSB 2160, or PSB 2165, or an other device, but not the PSB 2163.

Message: "No ICC/ISAC found"

The field "ICC/ISAC" is activated but ARCOS-SP PLUS cannot find an ICC or an ISAC-S or an ISAC-P on the external hardware.

Check the configuration of the external hardware (including DIP-switches and jumpers); does the setting in the user area match with the hardware configuration?

Message: "No EPIC/ELIC found"

The field "EPIC/ELIC" is activated but ARCOS-SP PLUS cannot find an EPIC or an ELIC on the external hardware.

The EPIC/ELIC is part of the STUT 2000 PERCOFI Board and of the LineCard Module. Check the configuration of the external hardware; does the setting in the user area match with the hardware configuration?

Message: "Serial I/F Init failed at COM port"

ARCOS-SP PLUS was started with the option `/V` and has tried to detect one of the hardware platforms from **table 5** without success.

This message can have many reasons:

- None of the boards from **table 5** is connected to the COM port
- The wrong cable is used (see **table 5**)
- The wrong port number is given in the `RS232.INI` file
- The firmware for the external hardware was not loaded before
- The external hardware is not in program mode (but in loader mode instead)
- The external hardware has no power supply

Message: "Unable to write the ARCOFI"

The communication with the ARCOFI-SP is disturbed.

Has anything changed that concerns the interface mode, the chip address or the hardware configuration? Is any cable removed or loose? Does the software try to execute a file that was created by the ARCOS-SP PLUS program for the PSB 2165? A good idea is to quit the ARCOS-SP software and to start again with the initialization of the hardware.

Message: "Unable to read the ARCOFI"

The communication with the ARCOFI-SP is disturbed (see above)

5.2 Other Problems

Message: "Opening Coefficient-file failed"

ARCOS-SP PLUS was not able to open the file ARC63.TAB (ARC63D.TAB). Make sure that this file is in the same directory as ARC63.EXE (ARC63D.EXE) itself.

Message: "Syntax Error or command not allowed"

An input in the command line does not match the syntax given in **chapter 2.4**.

Message: "Interpreter Error! File loading stopped"

A file that should be executed contains an unknown command. Probably it is not a file that was created with ARCOS-SP PLUS for the PSB 2163.

Message: "ARCOS-SP program does not support this command"

You are using the ARCOS-SP software which is a demo-version that does not support hardware access in any way. Only the ARCOS-SP PLUS software is able to execute the desired command.

Message: "ARCOS-SP program does not support this window"

You are using the ARCOS-SP software which is a demo-version that does not support hardware access in any way.

Message: "Not enough memory" or "Unable to allocate enough memory..."

The ARCOS-SP PLUS software requires at least 400 kB free conventional DOS memory. Remove any other memory resident programs that are not necessary for running a DOS application to get enough memory space.